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Design and Fabrication of a Multi-Functional Programmable Thermal Test Chip

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Abstract—This paper focuses on the design and fabrication of a new programmable thermal test chip as a flexible and cost-effective solution for simplification of characterization/prototyping of new packages. The cell-based design format makes the chip fit into any modular array configuration. One unit cell is as small as 4x4 mm2, including 6 individually programmable micro-heaters and 3 resistance temperature detectors (RTDs). All micro-heaters and sensors have 4-point Kelvin connections for improved measurement accuracy. The chip contains 2 metal layers: 100 nm thin-film Titanium to create micro-heaters and RTDs, and 2 µm Aluminum to add single bump measurement units and daisy chain connections. These structures facilitate bump reliability investigations during thermal/power cycling tests in flip-chip assembly technology. The calibration curves of RTDs show a sensitivity of 12 Ω/K which is improved by 50 percent compared to the state-of-the-art TTC. The proposed design provides higher spatial resolution in thermal mapping by accommodating 3 RTDs per cell. The dense configuration of micro-heaters increases the uniformity of the power dissipation, which enhances the accuracy of thermal interface material (TIM) characterizations. The steady-state infra-red (IR) thermography of a 20x20 mm2 TTC, including 150 active micro-heaters, verifies the promising uniformity of the heat profile over the chip surface.

Keywords—thermal test chip (TTC), characterization, resistance temperature detector (RTD), micro-heater, 4-point Kelvin connection, thin-film, daisy chain connection, reliability, thermal/power cycling test, flip-chip assembly technology, sensitivity, infra-red (IR) thermography

I. Introduction

The rapid shrinking of semiconductor devices and increasing power densities have created challenging circumstances in semiconductor packages. This challenge pushes scientists and engineers to focus on developing novel materials, designs, and processes to improve the reliability of advanced electronic devices. As a result, ever-improving packages and reliability investigations play an essential role in modern applications.

There is often a link between the lifetime of electronic devices and their power density. Increasing power densities necessitates in-situ reliability investigation of electronic packages to identify relevant destructive causes of package failure and guarantee the required lifetime of an electronic device. Applications like self-driving cars demand a high amount of power and complexity. Besides, they must be entirely reliable as the failure of such technologies could be catastrophic and fatal. With this in mind, it is of high significance to understand the critical reasons that cause package failure.

These failures could originate from high power densities and high frequency on/off cycling which induce a severe amount of interfacial stress inside a package due to different coefficients of thermal expansions (CTE). Accordingly, this thermal-induced stress triggers "health-related" issues and package failure during the device performance.

To address thermal reliability issues in ever-changing packages, thermal test chips (TTC) or thermal mock-up chips have been presented recently [1-7]. They include microheaters to mimic the device power mapping, and sensors for tracking the junction temperature. The micro-heaters can be realized using large transistors as unit power cells. However, they can adversely affect the uniformity of the power distribution. Moreover, RTDs as the temperature sensors show higher sensitivity than Si diodes in calibration [1].

This paper demonstrates the design and fabrication of a new thin-film thermal test chip. Our modular design is based on a 4x4 mm2 unit cell, which is suitable for any desired array configuration. The chip comprises 6 electrically isolated micro-heaters per cell to generate programmable power mapping, i.e., uniform, non-uniform, or hot-spot profiles. In addition, 3 RTDs are designed to measure the junction temperature. 4-point Kelvin connections are provided for the micro-heaters and RTDs to improve measurement accuracy. In the following sections, the design and fabrication of the chip, the characterization and measurement results, and the IR thermography images are discussed in detail.

II. Design and fabrication

A. TTC Design

The chip contains 2 metallization layers: first, 100 nm thin-film Titanium used to create arrays of micro-heaters and RTDs. Second, 2 µm Aluminum sputtered and patterned to add interconnects and bump measurement units.

As shown in Fig. 1, the first metallization layer contains 6 equally distant micro-heaters, which provides more than 82% heating source area coverage despite accommodating 3 RTDs per cell. This will make the power distribution uniform enough and highly reliable for active power cycling tests. Since micro-

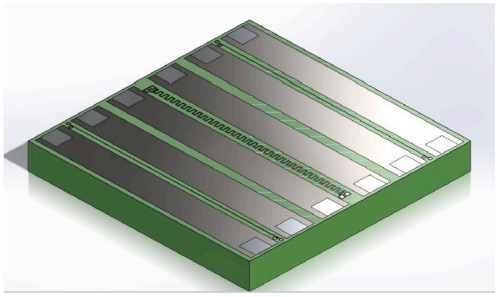


Fig. 1. Unit cell design in SolidWorks.

heaters are electrically isolated, uniform and non-uniform power mappings could be supported in high spatial resolution. The heating lines are designed in a rectangular shape with two pads on each side. The current pads of the micro-heaters are designed large enough to handle the current needed for 100 W/cm2 uniform power density and above. Considering all heaters in parallel, 16 W power can be achieved per cell using a low voltage of 12 V. Therefore, a 20x20 mm2 die, in particular, can yield 400 W. The current density to gain this power is 0.4×10^6 A/cm2 which is far below the critical value of 10×10^6 A/cm2.

The wafer mapping is shown in Fig. 2(a). The wafer includes 12 20x20 mm2 dies. Each die contains an array of 5x5 cells with the size of 4x4 mm2. The TTC unit cell design is depicted in Fig. 2(b).

In our design, we proposed using two types of RTDs in one single cell for performance comparison. The first type (RTD2) is a spiral temperature sensor with 15 µm track width. The second type, RTD1 and RTD3, are linear metal tracks that are 5 µm wide. This structure will allow us to implement a higher resistance value while using the same area, resulting in better sensitivity of Titanium RTDs compared to the state-of-the-art TTC. The wider metal track of spiral RTD causes less sensor sensitivity but more uniformity over the wafer due to less process variation dependency. As shown in Fig. 2(b), the RTDs are optimally placed where they can accurately measure maximum chip temperature and provide a high-resolution thermal mapping.

The second metallization layer accommodates single bump measurement units in 4 corners per cell and daisy chain connections, described in Fig. 3. The bump measurement units are added to support solder bump's reliability investigations

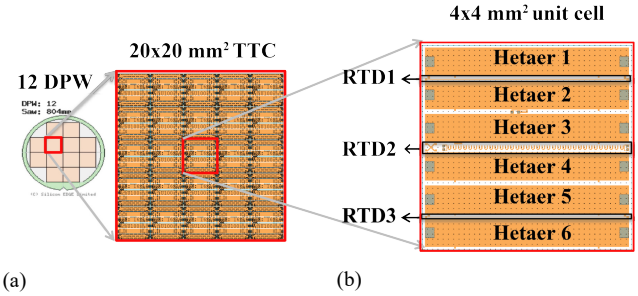


Fig. 2. (a) Wafer layout design including 12 20x20 mm2 dies *(arrays of 5x5 cells)* (b) TTC unit cell design.

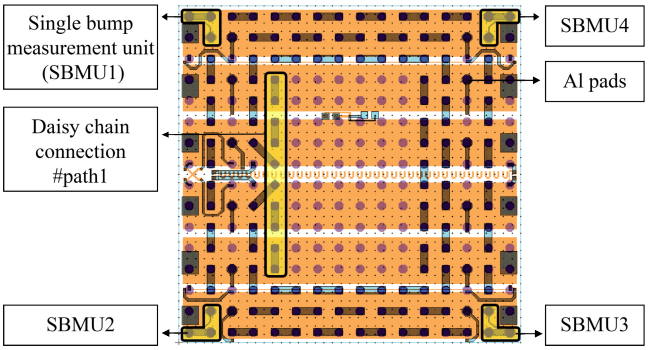


Fig. 3. Second metallization layer including single bump measurement units (SBMU), daisy chain connections, and Aluminum pads.

during thermal/power cycling tests in flip-chip assembly technology.

The chip is flexible to be assembled via flip-chip or wire-bonding technology. In case of flip-chipping, the bump pads designed in octagonal shape with 100 µm diameter and 250 µm pitch can be used. The optical imaging of a processed unit cell is shown in Fig. 4 using Keyence 3D laser scanning microscope.

B. TTC Fabrication

To process the wafers, the layout design of a unit cell is transferred to a set of 5 lithography photomasks. These images were employed to pattern each layer of the TTC using ASML wafer Stepper. 12 20x20 mm2 dies per wafer (DPW) are considered in the wafer mapping as in Fig. 5.

The device is fabricated on 4-inch p-type silicon wafers with 525 µm thickness. The first metallization layer is 100 nm thick Titanium sputtered by Trikon Sigma 204 Dealer. The wafers were coated by photoresist as the masking layer to be prepared for the photolithography process. This photoresist was exposed using ASML wafer stepper. To etch the Titanium layer, plasma enhanced reactive ion etching (RIE) was employed. In this step, two types of resistive temperature detectors and an array of micro-heaters were created. Following the process, the first metal contacts were etched by RIE, and the redistribution layer (RDL) was sputtered via a second metallization step. The layer was patterned by the photolithography process followed by plasma-enhanced RIE. In this step, the interconnects and daisy

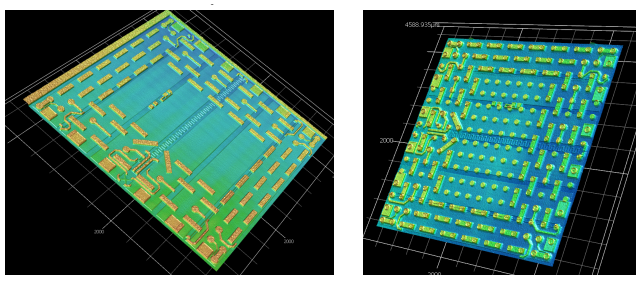
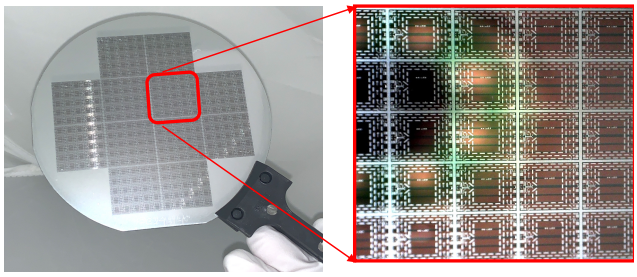


Fig. 4. 3D optical microscope imaging of a unit cell during fabrication process (a) After first and second metallizations (b) After top pad metallization.



(a) (b)

Fig. 5. (a) 4-inch processed wafer (b) Zoomed image of a signle die.

chain connections were formed. Eventually, the deposition of the passivation layer, contact openings, and final top-level bonding pad metallization were implemented.

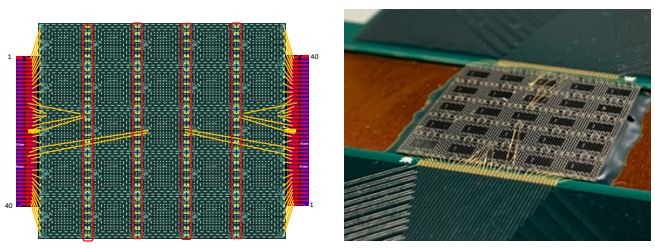
III. Assembly and Measurement Setup

In this section, the implementation of the measurement setup is presented. This setup is used for infra-red (IR) thermography and power mapping investigation. The setup consists of a 20x20 mm2 mock-up chip that is wire bonded to the pads on printed circuit board (PCB) for connections.

Bonding to the inner cells becomes increasingly more difficult as the array of cells expands in size. The TTC contains an array of 5x5 cells, i.e., 25 unit cells. With that in mind, to access all 150 micro-heaters, a particular bonding diagram has to be utilized. To alleviate the difficulty, 5 micro-heaters in each row are serialized, and in total 30 heating rows are accessible on the board. In addition, one central spiral temperature sensor and two linear RTDs are bonded to the PCB. The bonding diagram and the assembled TTC are shown in Fig. 6(a) and 6(b), respectively.

To create a promising thermal path, a copper lid and a closed-loop water cooling block are employed. The copper lid is glued to the water-cooling plate using thermal interface material (TIM) to fill the air gaps. The thermal chip is attached to the copper lid using die-attach material available at TUD MEMS lab. The SolidWorks model of the setup and the implemented setup are shown in Fig. 7(a) and Fig. 7(b), respectively.

Two separate PCBs are glued to the copper lid that supports both the chip and PCBs. Besides, the measurement setup is flexible in using any desired chip size. Additionally, the copper lid improves the uniformity of the heat flow to the cooling plate. We used 0.5 mm thick PCBs to keep the chip and the board



(a) (b)

Fig. 6. (a) The bonding dragram (b) The assembled TTC.

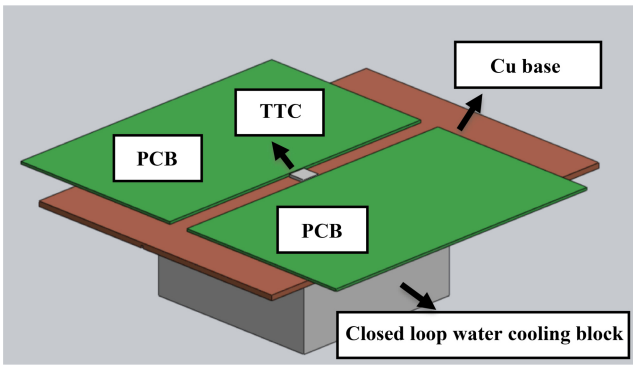
connections at the same level. Additionally, the backside of the chip is coated with Ti/Au stack of metals for compatibility with die-attach materials.

IV. Results and Discussion

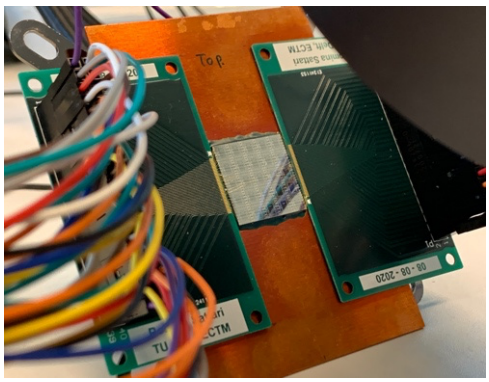
One of the main goals of thermal test chips is to provide precise and stable thermal measurements for in-situ reliability experiments. Therefore, the stability and accuracy of temperature sensors and micro-heaters have to be analyzed. In the following sections, the characterization of micro-heaters and RTDs are presented. In addition, the measurement results of the IR thermography of an assembled 20x20 mm2 TTC are reported.

A. Temperature Sensors and Micro-heaters

In this section, I-V measurement results of micro-heaters and RTDs are discussed. The measurements were done on 14 processed wafers to confirm the reproducibility of the device. To this end, the semi-automatic wafer probe station and ICCAP measurement software were employed as described in Fig. 8. The semi-automatic measurement capability allowed us to investigate 12 20x20 mm2 dies on 14 wafers. The central cell of each die represents the die performance. Moreover, the cell-by-cell measurement results of the die (0,0) are reported to verify the uniformity of the performance. The index (x,y) refers to a specific die, which relates to the die coordinates described in Fig. 10(a). This figure is exported using a data visualization tool

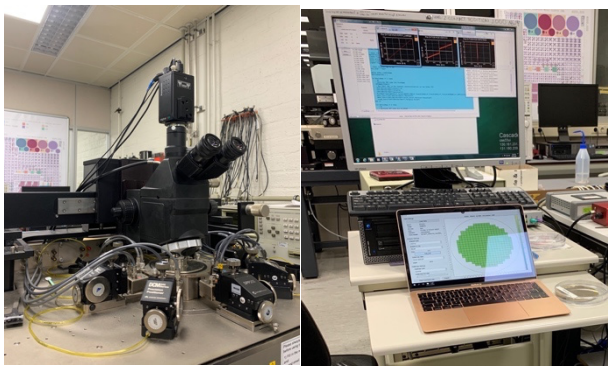


(a)



(b)

Fig. 7. (a) The SolidWorks model (b) The measurement setup including an assembled TTC.



(a) (b)

Fig. 8. (a) The semi-automatic wafer probe station (b) ICCAP I-V measurement software and Matlab DVT.

(DVT) in MATLAB for each wafer. The order of numbering cells per die is specified in Fig. 9(a) as well.

Micro-heaters resistance distribution at room temperature (RT) is shown in Fig. 11. The standard deviation, which relates to the process variation, indicates an acceptable uniformity in resistance values, allowing us to do one-time calibration and connect microheaters in parallel to inject the current. Moreover, it enhances the uniformity of power distribution over the die, resulting in higher accuracy for in-situ thermal reliability experiments.

The spiral and linear RTD characterization results are plotted in Fig. 12. During characterization, the temperature sensors' output signal was measured in the temperature range of -20 ℃ to 120 ℃. The results verify the stability and linearity of RTDs and the improved sensitivity of linear RTD (12 Ω/℃) compared to the state-of-the-art TTC [3].

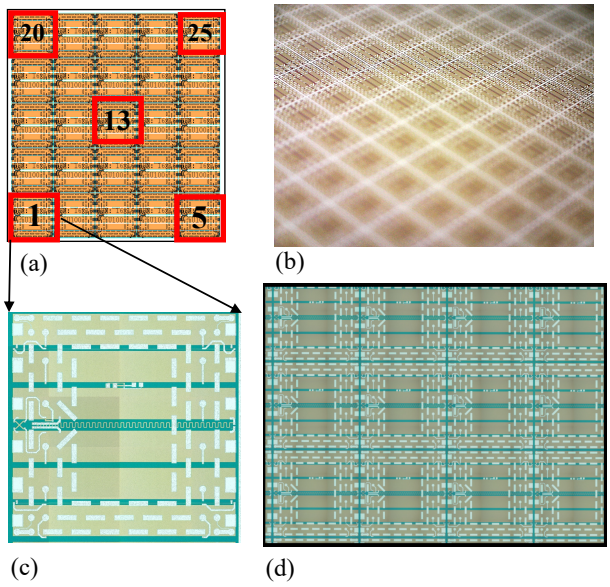


Fig. 9. (a) The measured cells per die (b) The device under test (DUT) (c) 4x4 mm2 unit cell (d) 3D optical microscopy before top bad metallization.

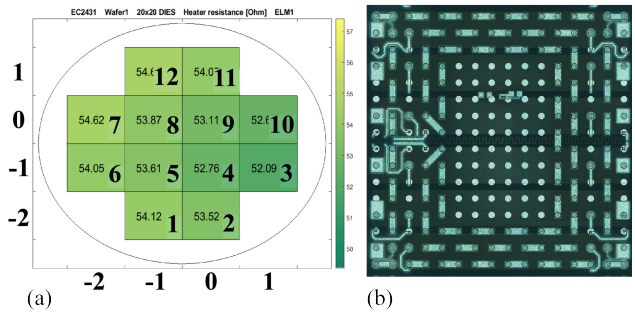


Fig. 10. (a) Die coordinates and numbering (b) Optical image of a unit cell.

It can be seen that the spiral RTD (SRTD) in comparison to linear RTD (LRTD) shows more uniformity over the die while having less sensitivity (9 Ω/℃). The reason is related to the sensor geometry where we used three times wider metal track for SRTD. It positively affects the process variations as the higher linewidth results in less mismatch in the process. On the other hand, it reduces the initial resistance value and therefore degrades the sensor sensitivity. More detailed results can be found in Fig. 13 and Fig. 14. Table I summarizes the specifications of the proposed TTC and compares its performance with state-of-the-art TTCs.

B. TTC Characterization and IR Thermography

The homogeneity of the heat profile is an essential property of a TTC. A uniform heat flux over the contact surface of the sample increases the accuracy of package thermal reliability investigations, particularly TIM characterization. A unit cell

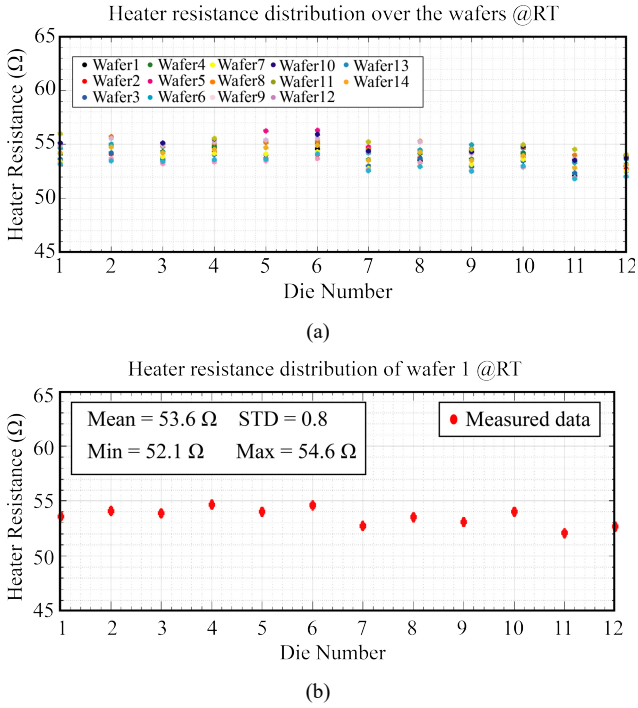
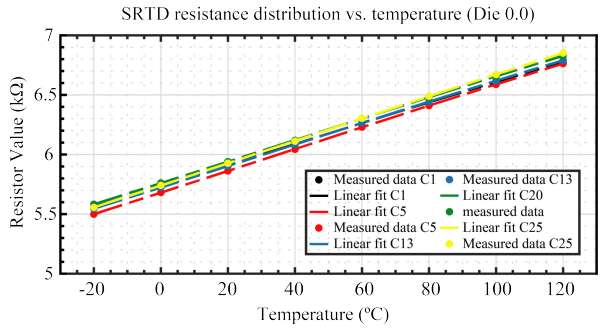
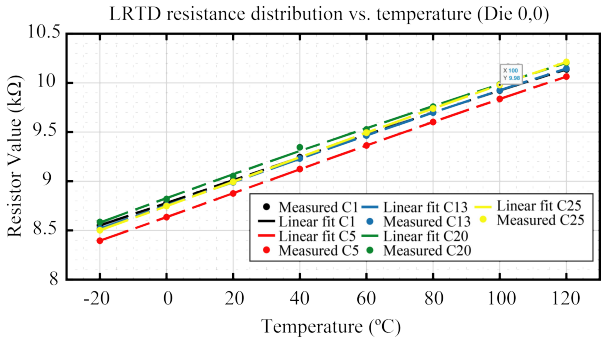


Fig. 11. (a) Micro-heaters characterization results at RT for (a) 14 wafers (b) Wafer 1.



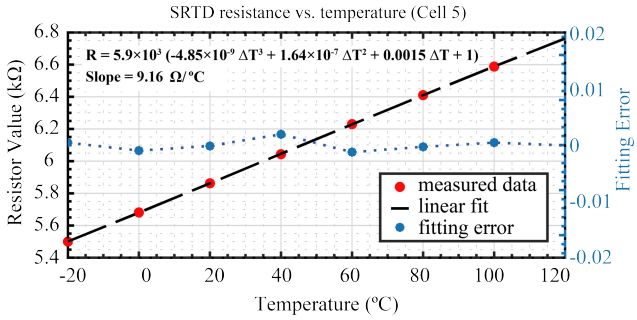
(a)



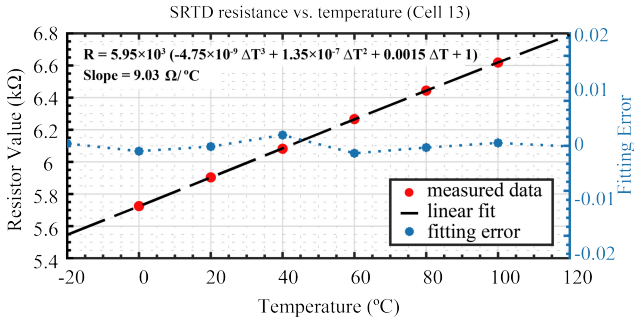
(b)

Fig. 12. Characterization results of RTD in 5 cells (a) SRTD (b) LRTD.

model is defined and simulated in COMSOL Multiphysics software to investigate the TTC power distribution. In this simulation, Titanium is modeled as a thin film structure, and the relevant boundary conditions are set to obtain 100 W/cm2 power

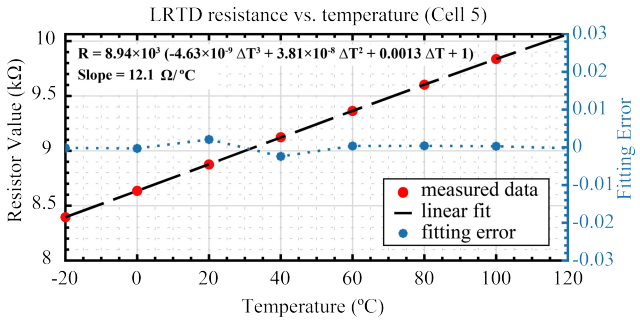


(a)

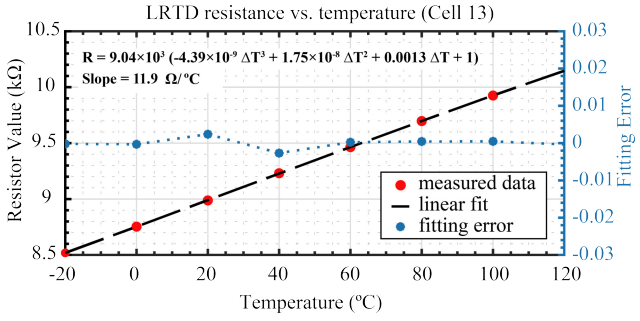


(b)

Fig. 13. Characterization results of SRTD (a) Cell 5 (b) Cell 13.



(a)



(b)

Fig. 14. Characterization results of LRTD (a) Cell 5 (b) Cell 13.

density. The current that flows into each microheater is 220 mA. The model, the meshing grids, and the simulation result are shown in Fig. 15.

The heat flux distribution of an assembled 20x20 mm2 TTC was measured using a non-contact thermal measurement method, IR thermography. The measurement setup, including a closed-loop water cooling block and an IR camera, is described in Fig. 16. The device under test (DUT) is wire-bonded as demonstrated in Fig. 6(b). As discussed in section III, The DUT

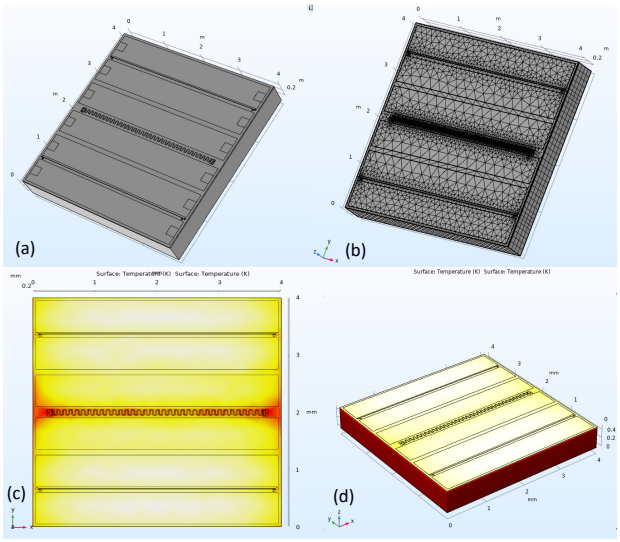


Fig. 15. COMSOL heat profile simulation (a) The 3D model of a unit cell (b) The meshing grids (c) 2D heat profile (d) 3D heat profile.

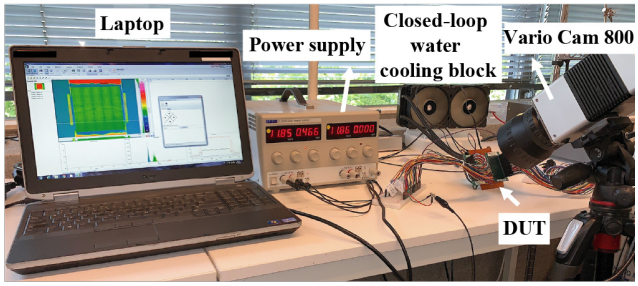


Fig. 16. IR thermography measurement setup.

is attached to the cooling plate while the chip surface is exposed to air. Due to the voltage limitation of the power supply, the total maximum current applied in this measurement is 1.8 Amps.

The thermal imaging results at different current levels ranging from 0.3 Amps to 1.8 Amps are plotted in Fig. 17. The results comprise both 2D and 3D thermal images. It can be seen that at higher flowing currents, the maximum temperature is increasing. In addition, at higher power dissipations, a stronger concentration of the heat profile was observed at the central parts of the chip with a higher temperature gradient.

V. Conclusion

In this paper, we presented a programmable and multi-functional thermal test chip (TTC). The design and fabrication process in thin-film technology were discussed. The design comprises two metallization layers and supports both wire-bonding and flip-chipping assembly technologies. Daisy chain connections on the second metallization layer support solder bump reliability experiments in power/thermal cycling tests. The characterization results of Titanium micro-heaters and RTDs were covered in this paper. To verify the reproducibility of the design, 14 wafers were processed and measured. The TTC

TABLE I. Performance Comparison

TTC	Our work	NT16-3K [2]	NT20-3k [3]	[1]
Sensor Type	RTD	RTD	RTD	Diode
Heater Type	Resistor	Resistor	Resistor	Resistor
Cell Size (mm2)	4x4	3.2x3.2	2.5x2.5	2.5x2.5
Sensitivity (Ω/K)	12	8	8	2
Cell Power at 12 V (W)	16	9	17	26 [a.]
Max Power per Cell (W)	360 [b.]	250 [b.]	70	22
Resistance per Heater (Ω)	54	160	17	11
Heaters per Cell	6	10	2	2
Sensors per Cell	3	1	1	4
Active Heater Area	82.5 %	62 %	82 %	85 %

[a.] Exceeds the maximum current handling of the heater.
[b.] Could be achieved only by applying proper cooling.

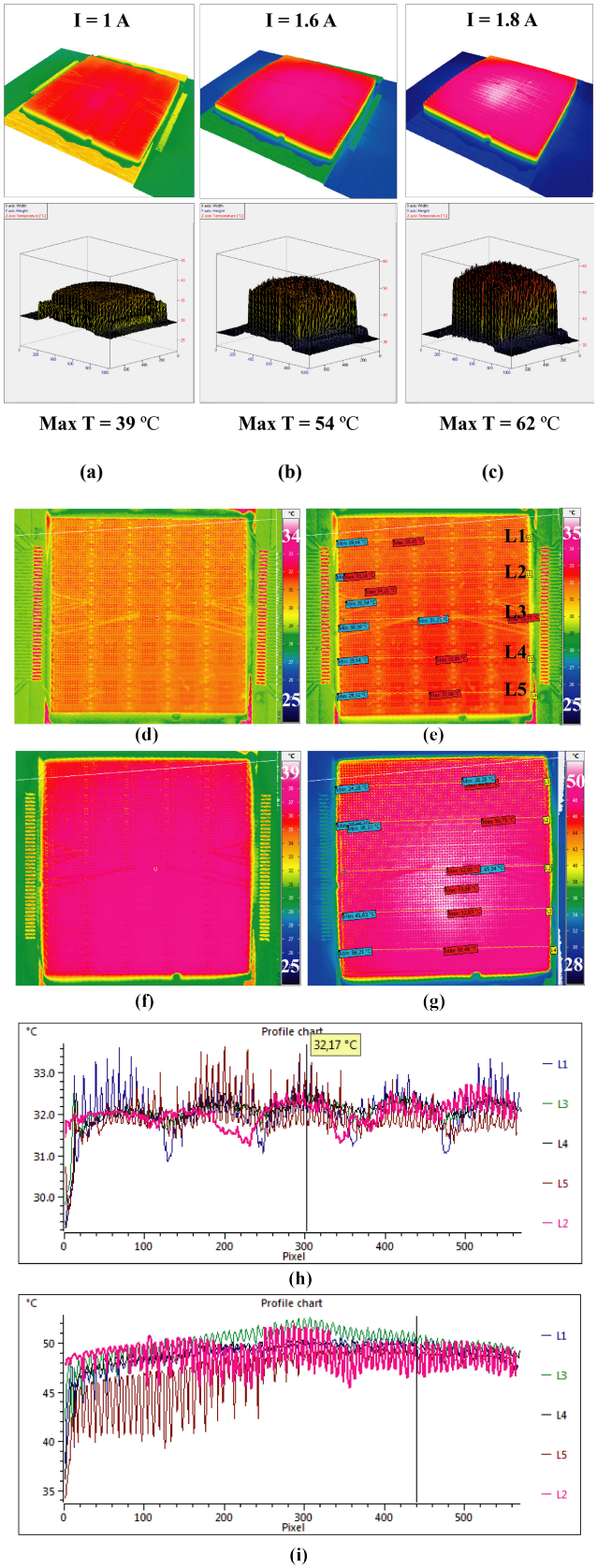


Fig. 17. 3D and 2D steady-state IR thermography measurement results (a) 1 A (b) 1.6 A (c) 1.8 A (d) 0.3 A (e) 0.5 A (f) 1 A (g) 1.6 A (h) Temperature profile chart at 0.3 A (i) Temperature profile chart at 1.6 A.

presented shows promising performance in terms of stability and linearity of RTD sensors for temperature mapping as well as uniformity of micro-heaters resistance for power homogeneity. The design supports modularity in power mapping and chip size. Moreover, the infra-red thermography result of a 20x20 mm2 TTC, including an array of 150 active micro-heaters, was reported. The results confirm that the proposed TTC could serve as a flexible and cost-effective platform for thermal reliability experiments and the qualification of materials and semiconductor packages.

ACKNOWLEDGMENT

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