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# Analysis, Design and Implementation of Power-Efficient DC-DC Converters for Biomedical and IoT Applications

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# Analysis, Design and Implementation of Power-Efficient DC-DC Converters for Biomedical and IoT Applications

Alessandro Urso

# Analysis, Design and Implementation of Power-Efficient DC-DC Converters for Biomedical and IoT Applications

Dissertation

For the purpose of obtaining the degree of doctor
at Delft University of Technology,
by the authority of the Rector Magnificus prof. dr. ir T.H.J.J. van der Hagen,
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*"Opportunities are usually disguised as hard work, so most people don't recognize them."*

Ann Landers

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Chapter

# 1

# Introduction

DC-DC converters, and more in general voltage regulators, are essential blocks of the power management unit (PMU) in electronic systems. In particular a PMU takes an unregulated voltage as input, and by implementing one or more step-down/-up conversions, it can potentially generate any desired regulated output voltage.

To highlight the importance of DC-DC converters let's consider today's smartphones. Inside a smartphone, many integrated circuits (ICs) are mounted on a Printed Circuit Board (PCB), each of them requiring a dedicated supply while implementing determined functions. In this scenario, the task of the PMU, starting from the single and unregulated voltage provided by the battery, is to generate all the required voltage levels to properly power each of the ICs. Moreover, internally, each of the ICs is made of several smaller circuits which, depending on the supply requirements (e.g., voltage amplitude, noise level, leakage current), are often assigned to a particular voltage domain. A voltage domain can be seen as an island containing circuits with the same supply requirements. Hence, internally in such an IC, another PMU is required which takes the single voltage provided by the PCB-level PMU and generates all the required supplies to power up each of the voltage domains.

To better picture the role of the PMU we can refer to Fig. 1.1. On the left-hand side, we have the unregulated voltage provided by the storage element (e.g., a supercapacitor or a (rechargeable or non-rechargeable) battery) (0.9-4.2 V), whereas on the right-hand side there is the load that requires several regulated voltages to supply both low-voltage (0.6-3.3 V), and high-voltage (∼20 V) circuits. To bridge the voltage gap, the PMU generates the required voltages while meeting the supply requirements of each of the powered circuits.

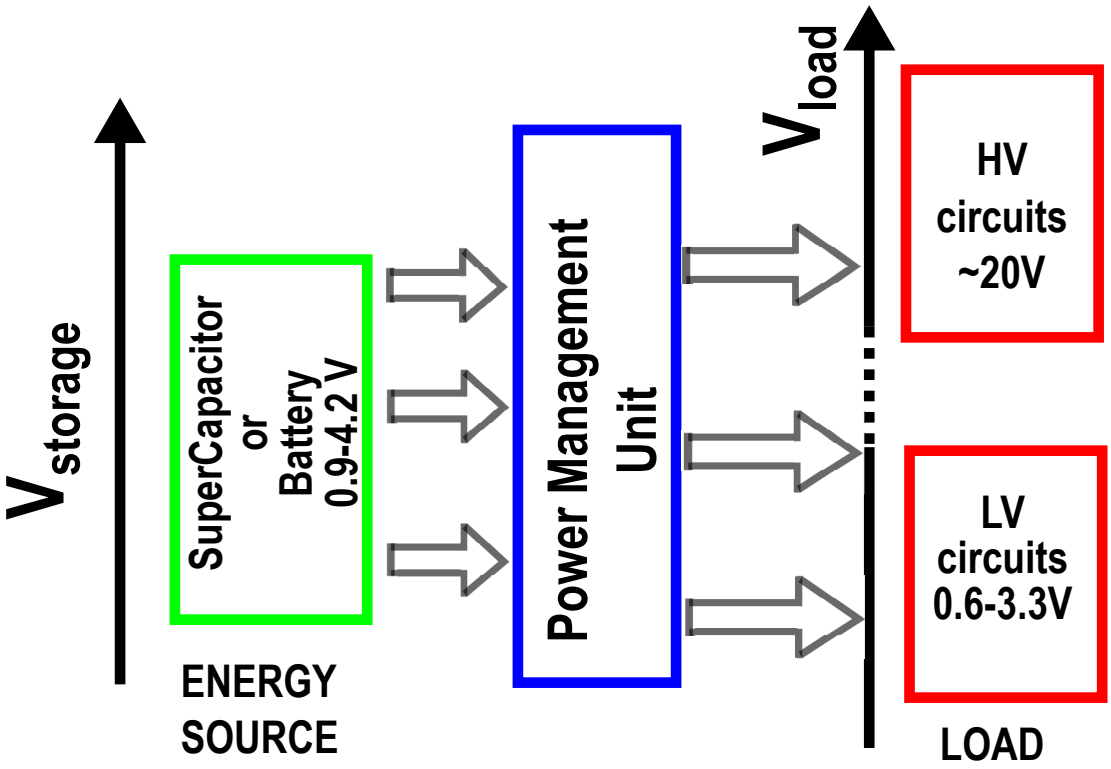


Figure 1.1: The power management unit used as a bridge to interface the output voltage of the storage element with the required supply voltage of the load.

The primary constraint of the structure shown in Fig. 1.1 is the energy efficiency of the PMU, as this limits the discharge-cycle of the energy source.

A popular approach to extend the discharge-cycle of the storage element, or in some cases even avoid its replacement, is to bring additional external energy into the device. Two examples of such an approach are by means of:

- an *Energy Harvesting*, which aims to collect, convert and store energy already available in the environment. However, the harvested energy heavily depends on the type of harvester used. Generally speaking, the output power of the energy harvester is well below the power required by the electronics [1]. Hence, this approach requires a storage element, a duty-cycled load and a PMU with a power efficiency as high as possible.
- *Wireless power transfer* [2, 3], which aims, by means of an inductive, capacitive or optical link, to wirelessly transfer power to the device without having physical contact with it. The major drawback of this approach is the power efficiency of the link. It depends, among all, upon the misalignment, the distance and the size difference between the coupling elements at the transmitting and receiving sides and their power losses.

This suggests there is an inherent voltage- and current-levels mismatch over time between the source and the load. Hence, to bridge this energy gap, a PMU with a storage element and a power efficiency as high as possible is required.

## 1.1 Target Applications

This thesis aims to introduce novel circuit techniques to improve the power efficiency of DC-DC converters for two different applications, namely implantable neural stimulators and devices for the Internet of Things (IoT).

### 1.1.1 Implantable Neural Stimulators

An implantable neural stimulator is a device that generates electrical impulses, which are used to treat neural disorders, restore lost senses, such as hearing, vision, sense of balance, or pain relief. Stimulators are typically implanted into the human body, which, although physically close, are very difficult to access. Therefore, any operation that requires physical access to the device can become very challenging. For example, the simple operation of replacing the battery would mean that the patient needs a surgical operation which comes with its own side effects. Moreover, the size of the whole implant is another big burden as it causes complications and increases the risk of infection. Since the battery is a bulky component, reducing its physical size would also drastically reduce the overall size of the stimulator. However, a smaller battery is typically associated with lower available energy which in turns reduces the lifespan of the neurostimulator.

With this respect, this thesis aims to increase the life-span of the battery without increasing its physical size (i.e., boosting the power-efficiency of implantable neural stimulators).

### 1.1.2 IoT Sensor Nodes

With the increasing demand for (inter-connected) IoT devices, transceiver architectures, of which RF oscillators are essential blocks, are becoming widely used. A relevant parameter to asses the performance of RF oscillators is its phase noise, as it can corrupt both the transmitted and received signals. Due to the stringent regulation's requirements on the spectrum of the oscillator, a lot of effort has been put in reducing its phase noise (PN) and improve its related Figure-of-Merit (FOM) [4–6]. To preserve the oscillator spectral purity, typically a low-noise low-dropout regulator (LDO) is used in the PMU, which however drastically reduces the system power efficiency. In this thesis, the use of the LDO in the PMU is avoided while a fully-reconfigurable and power-efficient switched-capacitor DC-DC converter is used to directly supply the RF oscillator.

## 1.2 Objectives and Thesis Organization

This thesis is composed of two parts. The first part tackles the challenge of improving the power efficiency of implantable neurostimulators. To this end, the design of a power-efficient, multichannel neural stimulator is presented. The second part tackles the challenge of designing fully-integrated and power-efficient voltage regulators suitable for powering up supply-sensitive blocks (e.g., RF oscillators).

The first part of this thesis starts in **Chapter 2** with an introduction to electrical stimulation. The goal of this chapter is to make the reader familiar with electrical stimulation as well as the circuit-level challenges in the design of safe, power-efficient and multichannel neural stimulators.

**Chapter 3** presents the design of a 8-channel current-controlled neurostimulator with a particular attention to its power efficiency. The core of the neurostimulator is an inductor-based DC-DC converter that is used to generate the current pulses required for the stimulation. The fully reconfigurable 16-electrode stimulator shows a peak power efficiency of 68%, while only one external component is used. The circuit techniques introduced here allow to improve the power efficiency up to a factor of 3x when compared to prior art.

The second part of this thesis starts in **Chapter 4** with an analysis of the power supply requirements of an LC oscillator such that its inherent spectral purity is preserved. A design guideline for an analog LDO to meet these supply requirements is presented, while the system power-efficiency degradation is quantified.

Given the poor LDO efficiency performance, **Chapter 5** investigates the use of switched-capacitor (SC) DC-DC converters as supply blocks for LC oscillators. In particular, a power efficiency and noise analysis of a reconfigurable 2:1 and 3:2 SC DC-DC converter is presented. A closed-form equation to estimate the output noise of the SC DC-DC converter is derived, merely based on its equivalent resistance and capacitance. The insights of this analysis are then used to design a SC DC-DC converter that meets the requirements discussed in Chapter 4. Based on this analysis, a new scheme in which a DC-DC converter directly powers up an LC oscillator is presented. The $4.9 - 5.6\,\text{GHz}$ digitally-controlled oscillator embeds in its biasing network a spur reduction block to mitigate the effects of the ripple generated by the DC-DC converter. Measurement results show a DC-DC converter peak efficiency of 83% with an output noise $<0.9\,\text{nV}/\sqrt{\text{Hz}}$ at 1 MHz which is low enough to preserve the oscillator spectral purity.

In order to provide a constant supply voltage for the oscillator, the 2:1 or 3:2 SC DC-DC converter requires to be operated from a fixed supply. Hence, to regulate the output voltage of the storage element, while directly supplying the oscillator, a fully-integrated recursive switched-capacitor (RSC) DC-DC converter is presented in **Chapter 6**. A Finite-State-Machine (FSM)-based digital control method is introduced which, among all, allows for a predictable spectrum of the output voltage. A gate-driver circuit is introduced that guarantees minimum switch on-resistance across PVT variations. The converter is designed to meet the requirements discussed in Chapter 4, and is therefore suitable to directly power up the same LC oscillator. Measurement results show a converter peak power efficiency of 87% with an output noise of $<1.5\,\text{nV}/\sqrt{\text{Hz}}$ which does not degrade the oscillator phase noise performance, while the level of the ripple-induced spurs is <-65 dBc.

**Chapter 7** concludes this thesis and provides recommendations for future work.

# Part I

# Design and Implementation of a Power-Efficient, Multichannel Neural Stimulator System

Chapter

# 2

# An Introduction to Electrical Stimulation

The goal of electrical stimulation for activation of excitable cells, such as cardiac, muscle and neuronal cells, is to deliver a well-defined amount of charge to the tissue to build up a specific electric field distribution in the tissue such that an action potential is generated (anodic phase), and subsequently remove the charge (cathodic phase). This stimulation sequence is called a biphasic pulse. Strictly speaking, stimulation can also be done by means of monophasic stimulation. However, this is never used in implantable devices as it requires non-polarizable electrodes, which are not used in the body. Though electrical stimulation can be accomplished by means of voltage, current and charge [8–10], most stimulators use current sources to build up and remove the charge from the tissue. A generic biphasic, constant-current, stimulation (CCS) setup is shown in Fig. 2.1 (a). Generally, two electrodes ($el_1$, $el_2$) are required for (bipolar) stimulation, although multi-polar stimulation by means of multiple electrodes is sometimes also used to generate a specific electric field pattern in the tissue. The electrode-tissue interface (ETI), to a first approximation, can be modelled as a resistance $R_{\text{load}}$ with a series capacitor $C_{\text{load}}$.

During the chatodic phase (highlighted in red in Fig. 2.1 (a)), there is a constant voltage drop $R_{\text{load}}I_{\text{stim}}$ across $R_{\text{load}}$, while capacitor $C_{\text{load}}$ is being charged with a constant current $I_{\text{stim}}$, leading to a linearly increasing voltage $V_{\text{load}}$ across the electrode-tissue interface. During the anodic phase (highlighted in blue in Fig. 2.1 (a)), the current is reversed and $C_{\text{load}}$ can be discharged with the same current $I_{\text{stim}}$. Fig. 2.1 (b) sketches the resulting voltage across the ETI ($V_{\text{load}}$) when a current $I_{\text{stim}}$ is used for stimulation. In order to have a more localized stimulation, there is the need to have

This chapter is based on the article published in the Journal IEEE Solid-State Circuits Magazine [7].

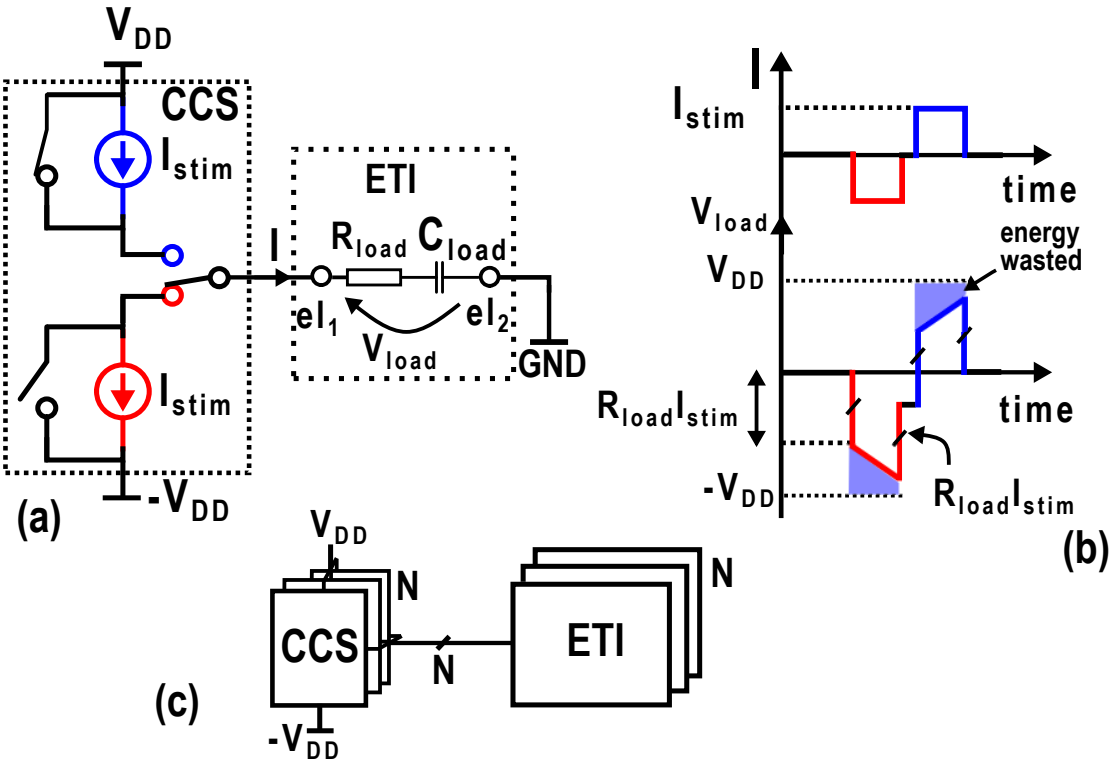


Figure 2.1: (a) Biphasic constant-current stimulator (CCS), along with the equivalent model of the electrode-tissue interface (ETI); (b) sketch of the stimulation current and resulting voltage across the electrode-tissue interface and (c) representation of a possible configuration of a multichannel neural stimulator.

several independent stimulation sites. A possible setup of a multichannel neural stimulator is shown in Fig. 2.1 (c), in which each ETI is connected to its current driver. Although the drivers share the same compliance voltage ($V_{\mathrm{DD}}$), they can be programmed to deliver different currents.

## 2.1 Power Efficiency of Constant-Current Stimulators

Constant-current stimulators exploit a voltage drop across the current driver to keep the stimulation current constant. This leads to an inherently inefficient system (see Fig. 2.1 (b)). A popular way to reduce the energy wasted, and therefore increase the power efficiency, is to continuously adapt the voltage supply of the neurostimulator to the voltage across the electrodes [11–13]. For instance, in [11], four different voltage supplies, both positive and negative, are generated from the main power supply. During each of the biphasic pulses, the stimulator voltage supply tracks the ramping electrode voltage such that the supply voltage is kept relatively close to the voltage required at the stimulator output. Despite that this seems a neat solution, the power efficiency improvement is not so significant due to the additional inefficiencies introduced by generating all the voltage supplies and due to the large amount of additional switches deployed. In a similar concept [8, 14], a compliance monitor is used to continuously adjust the stimulation

supply voltage. For all the adaptive supply stimulators, however, during multichannel operation, the supply voltage has to accommodate the channel with the highest required output voltage. Hence, the voltage of the compliance monitor is still over-designed for the rest of the stimulating channels. This problem is even more significant in retinal implants where electrode arrays with hundreds of electrodes, hence larger numbers of independent channels, are used [13]. Moreover, the driver circuits of these electrodes, traditionally, are operated from a single high-voltage supply [8, 15], degrading the overall power efficiency as not all electrodes develop the same voltage and, as a consequence, a lot of voltage headroom is being wasted. The best power efficiency of multi-channel stimulator circuits, therefore, can be achieved by not driving every electrode from its own (current or voltage) driver circuit, but by using an Ultra High-Frequency (UHF) pulse-based technique that builds up the right amount of charge at every electrode by means of rapid (e.g., 1 micro-second duration) current pulses. The concept of the UHF neural stimulator will be further discussed in the next chapter.

## 2.2 Safety Aspect

An important safety aspect for all neural stimulators is the excess of charge accumulation at the electrode-tissue interface of neural stimulators. At the end of a biphasic pulse, there will still be residual charge at the electrode-tissue interface, e.g. due to device or circuit mismatch, but most often as a result of the inherent non-linearity of the tissue itself. This residual charge must be avoided as it leads to electrolysis and thereby to tissue damage. To this end, typically a medical-grade, external capacitor is placed between the output of the stimulator and the electrodes such that it ensures that the average voltage over the electrode-tissue interface is zero. Moreover, even in case of device failure, it prevents any DC current to reach the ETI. However, it has been proven that this coupling capacitor introduces an offset voltage over the electrode-tissue interface, which depends on the electrode type and the intensity of the stimulation [16]. This offset voltage should not exceed the safety boundaries as this leads to irreversible electrochemical reactions. Moreover, medical-grade DC-blocking capacitors, being bulky external components, significantly contribute to the overall size of the implant and reduce the reliability of the whole stimulator. An alternative and safer approach to reach charge balance is to briefly monitor, and eventually actively correct, the electrode voltage after each biphasic pulse, either by means of a pulse-insertion technique [17] or by means of adjusting the duty-cycle of the biphasic stimulation pulse [18].

## 2.3 Conclusions

In this chapter, two important aspects of circuits for electrical stimulation have been discussed, namely power efficiency and safety. The setup of a constant-current, biphasic stimulation pulse was shown along with a possible implementation in a multichannel operation. The power-efficiency degradation due to the voltage drop across the current drivers was discussed. The safety aspects due to the excess of charge accumulation at the electrode-tissue interface were discussed. In the next chapter a stimulator architecture which overcomes the above-mentioned problems is presented.

Chapter

# 3

# An Ultra-High-Frequency 8-Channel Neurostimulator Circuit Achieving 68% Peak Power Efficiency

This chapter presents the design and and measurement results of a power-efficient, current-controlled, multi-channel, ultra-high-frequency (UHF) neural stimulator[1]. The core of the neurostimulator is based on an inductor-based buck-boost DC-DC converter without the external output capacitor. The ultimate goal is to increase the power efficiency of the UHF stimulator for multiple-channel operation, while keeping the number of external components minimal. To this end a novel zero-current detection scheme is introduced. It allows to remove the freewheel diode typically used in DC-DC converters to prevent current to flow back from the load to the inductor. Furthermore, a gate-driver circuit is implemented that allows the use of thin gate-oxide transistors as high-voltage switches. By doing so, the need for a high-voltage supply is eliminated and the stimulator is powered up from a 3.5 V input voltage.

Both the current-detection technique and the gate-driving circuit allow to boost the power efficiency by $3X$ when compared to previous UHF stimulator works. A peak power efficiency of 68 % is achieved, while 8 independent channels with 16 fully configurable electrodes are used. The circuit has been implemented in a 0.18 $\mu m$ HV process, and the total chip area is 3.65 $mm^2$.

[1]This chapter has been published in the IEEE Transactions on Biomedical Circuits and Systems [9].

## 3.1 Introduction

Over the past few decades, many implantable neurostimulators have been developed in order to treat various neural and brain disorders. Typical applications of such stimulators are retinal implants [11], deep-brain stimulation (DBS) and spinal-cord stimulation [19–21]. The biggest challenge that such devices have in common is their limited battery life. Most batteries for neurostimulators last three to five years, and in case of extensive use the battery has to be replaced or recharged yearly [22]. In order to cope with this problem, the battery size is increased at the expense of post-surgery trauma and risk of infection. If the stimulator, together with the battery, is small enough, it can be implanted by means of a percutaneous injection. These devices are known as *Injectable Neurostimulators* [23]. In this scenario, a surgical operation is avoided, and so are its complications. Furthermore, in the emerging field of Bioelectronic Medicine, neural implants need to be miniaturized to a level which allows for a direct interface with tiny nerves. In this scenario, a battery-less solution might be necessary, in which all available power would have to be harvested or transferred from outside the body [24]. Hence, the need for an increased power efficiency is more relevant than ever. At the same time, current trends indicate the need for an increasing number of independent stimulating channels to accommodate a large number of stimulation sites. In applications like retinal implants, several hundreds or even a thousand stimulation channels are implemented [15]. Due to the high number of stimulation channels, the overall size of the stimulator increases at the expense of its safety (post-surgery trauma, risk of infection, charge accumulation). These two requirements, namely power efficiency and multi-channel operation, are not trivial to accomplish simultaneously. In this chapter we present an 8-channel UHF neurostimulator circuit that embeds a new zero-current detection scheme and a gate-driver circuit to boost the power efficiency even when the channels are operated simultaneously.

The rest of the chapter is organized as follows. In Section 3.2, the concept of UHF stimulation is presented. Section 3.3 describes the overall architecture of the stimulator and elaborates on the circuit details. Section 3.4 reports the measurement results of a prototype IC realization as well as a comparison with the state of the art. Finally, in Section 3.6, conclusions are drawn.

## 3.2 Principle of UHF Stimulation

The concept of UHF dynamic stimulation was introduced for the first time in [25]. By means of a stimulator circuit made of discrete components, it was shown that UHF stimulation depolarizes the cell membrane in a similar way as constant-current stimulation does. *In vitro* experiments using Purkinje cells proved that this new way of stimulating the tissue also induces neural recruitment in the targeted area. It uses a different way of stimulating the neural tissue compared to constant-current stimulation. Each stimulation phase, i.e. the anodic and the cathodic phase, is made of a sequence of current pulses injected into the tissue at a high rate. In Fig. 3.1 (a), an example of such a biphasic pulse is shown and it is compared with a classical constant-current biphasic pulse.

In Fig. 3.1 (b), a system-level architecture that implements the concept of UHF stimulation is shown. It consists of an inductor-based buck-boost DC-DC converter without the external capacitor,

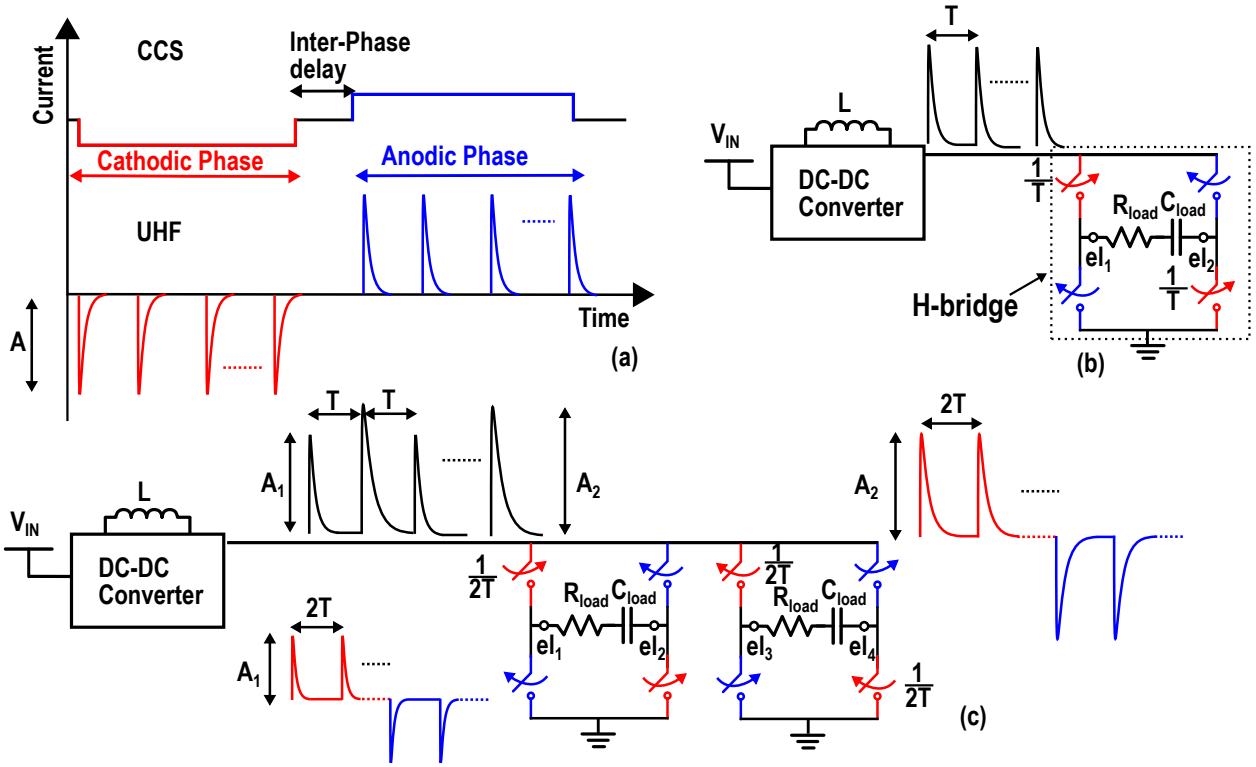


Figure 3.1: (a) Sketch of a biphasic pulse, produced by constant-current stimulation (CCS) and by UHF stimulation; (b) high-level architecture of an UHF neural stimulator with a sketch of the current profile for a single channel and the H-bridge to reverse the current; (c) example of 2-channel operation.

in which a duty-cycle signal is used to modulate the amplitude of the stimulation (A in Fig. 3.1 (a)). The current pulses are not directly drawn from the main power supply. In fact, the inductor is first charged from the power supply, and then it is discharged into the tissue. The discharging process of the inductor into the tissue generates the current pulses. Hence, this implementation of UHF neural stimulator provides a current-controlled stimulation. Please note that during the discharging process, L is connected in series with $R_{load}$ and $C_{load}$, thereby generating the exponentially decaying pulses.

In case more channels are operated concurrently, the pulses generated by the only inductor are sent to all the activated channels in an interleaved fashion (see Fig. 3.1 (c)). Assuming that the DC-DC converter generates the pulses at a rate $\frac{1}{T}$, each channel receives its own pulse at a rate of $\frac{1}{NT}$, where N is the number of channels being operated simultaneously. Moreover, by adjusting the duty-cycle of each pulse, the channels can be stimulated with different intensities (e.g. $A_1$ and $A_2$ in Fig. 3.1 (c)).

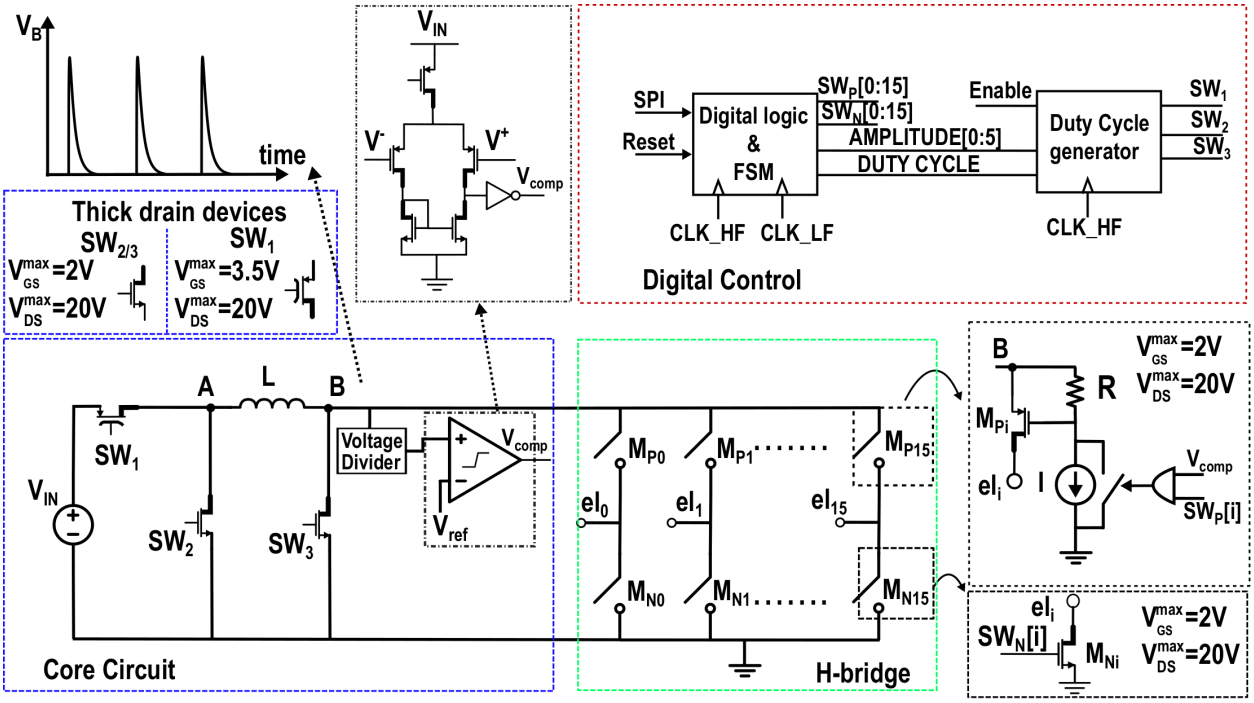


Figure 3.2: System architecture showing the three subsystems of the implemented neural stimulator: the core circuit that generates the high-frequency pulses, the H-bridge that, by means of thin-oxide switches, is capable of implementing a biphasic pulses and the digital control that generates all the signals needed by the core circuit and the H-bridge.

## 3.3 System-Level Design

The circuit diagram of the proposed UHF neural stimulator is shown in Fig. 3.2. It is made of the following subsystems:

- *Core Circuit*, which is a power-efficient buck-boost DC-DC converter without the external capacitor. Hence, a train of current pulses is generated from the main power supply at a frequency equal to the switching frequency of the DC-DC converter. The most important requirement of this block is its power efficiency.
- *H-bridge*, which is a particular configuration of switches that allows for the selection of the desired channel and, by reversing the direction of the current flowing into the tissue, implements the biphasic stimulation. Since the H-bridge is directly connected to the output of the Core Circuit, the parasitic capacitance introduced by those switches has to be kept minimal. By doing so, the power efficiency can be further increased.
- *Digital Control Module*, which is able to generate and to store the stimulation patterns based on a serial bit stream loaded via a Serial Peripheral Interface (SPI).

The detailed operation and the structure of the subsystems are discussed in the following subsections.

### 3.3.1 Core Circuit with Zero-Current Detection Scheme

In Fig. 3.3, a detailed representation of the core circuit is given along with a sketch of its most relevant waveforms. It is a forward buck-boost DC-DC converter without the external filtering capacitor. The forward topology allows the output voltage to be of the same polarity as the input voltage.

During $\Phi_1$, only Switches $SW_1$ and $SW_3$ are closed, hence the input source ($V_{IN}$) is in parallel with the inductor and provides energy to it. The voltage across the inductor, $v_L(t)$, can be written as

$$v_L(t) = V_{IN} = L\frac{di_L(t)}{dt}. \tag{3.1}$$

$V_{IN}$ is constant, hence during $\Phi_1$, $i_L(t)$ has a positive constant slope which can be seen in Fig. 3.3 (b).

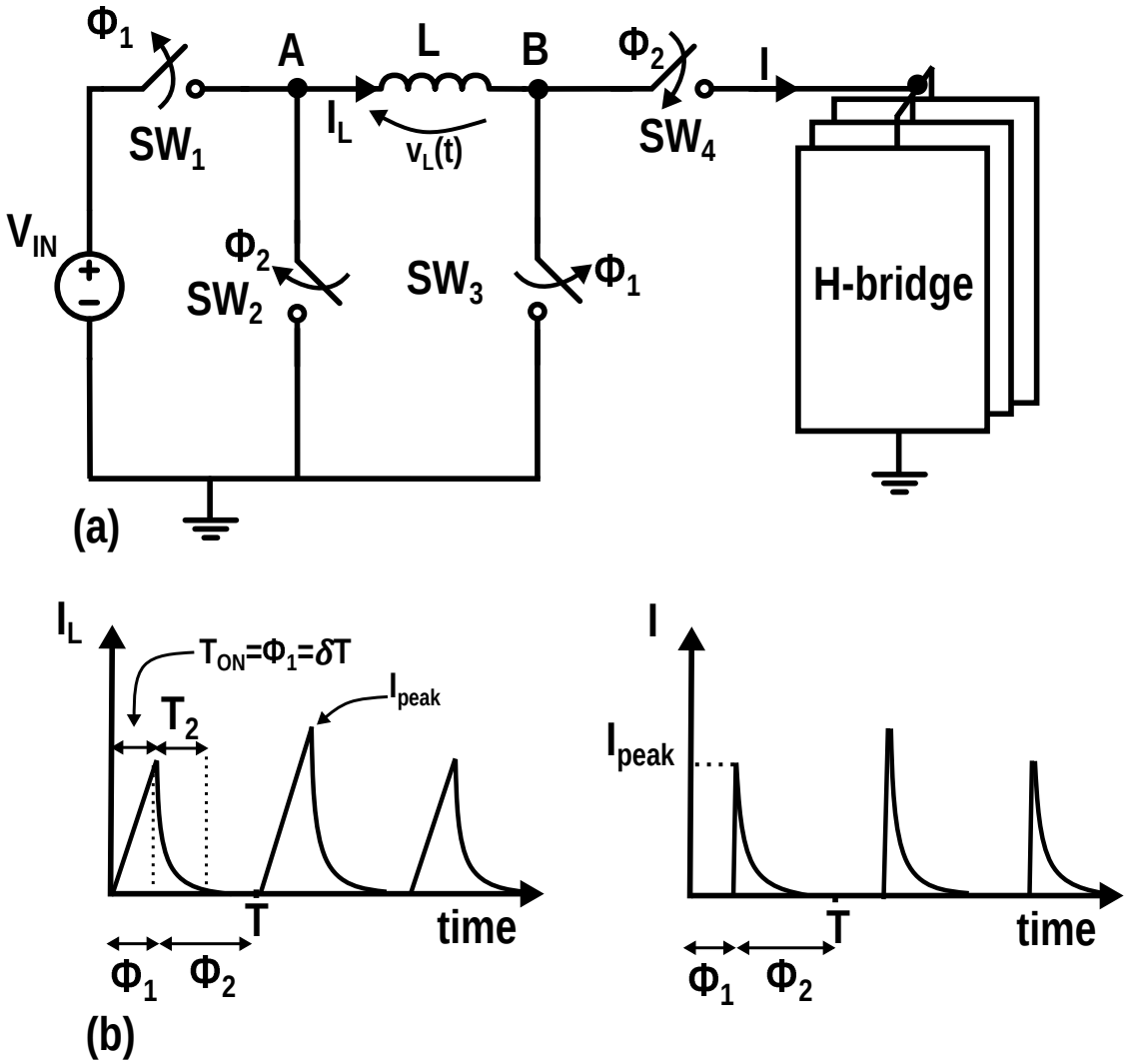


Figure 3.3: (a) Schematic of the inductor-based buck-boost converter; (b) sketch of the current waveforms during $\Phi_1$ and $\Phi_2$.

At time $t = T_{\mathrm{ON}}$, the inductor current reaches its peak value, which can be expressed as

$$I_{\mathrm{peak}} = \frac{V_{\mathrm{IN}}}{L} T_{\mathrm{ON}}. \tag{3.2}$$

During $\Phi_2$, only Switches $\mathrm{SW}_2$ and $\mathrm{SW}_4$ are closed. Hence, through the H-bridge, the inductor supplies its current to the load. The amount of energy transferred from the battery to the inductor during $\Phi_1$ is proportional to the *duty-cycle* $\delta = \frac{T_{\mathrm{ON}}}{T}$. The converter works in discontinuous conduction mode, which means that, during $\Phi_2$, the inductor current reaches zero before the next phase starts. In order to prevent the current flowing from the load back to the inductor, i.e. $I_L < 0$, a freewheel diode (i.e., $\mathrm{SW}_4$) is usually placed between Node B and the H-bridge [26]. The voltage drop across the diode has a big impact on the power efficiency, especially for low-intensity stimulation. In this work, the diode is avoided and the switches on the top side of the H-bridge are controlled by a zero-current detection scheme implemented by means of a comparator.

The core circuit together with the additional circuits required to implement the zero-current detection technique is shown in Fig. 3.2. During $\Phi_2$, as soon as the inductor current becomes 0 and stays 0, the voltage across the inductor becomes 0. Since the voltage at Node A during $\Phi_2$ is 0 as well, we only need to detect when the voltage at Node B becomes 0. As the inductor and the parasitic capacitance of Switch $\mathrm{SW}_3$ introduce a resonance, the voltage at Node B rings around zero. Therefore, a reference voltage, $V_{\mathrm{ref}}$ that is slightly greater than 0 V is used [27]. Voltage $V_{\mathrm{ref}}$ is generated on chip and its value is much smaller than the voltage at the ETI, therefore it does not affect the accuracy of the zero-current detection technique. The output voltage is not filtered, hence the voltage at Node B, depending on the duty-cycle value, can be as high as 20 V. Exceeding this voltage would mean that some transistors would work out of their safe operating region.

A comparator with the input pair made of thin-oxide transistors is needed to reduce the parasitic capacitance at Node B. In order not to violate the maximum voltage compliance of the thin-oxide device, the voltage is first scaled down by means of a capacitive voltage divider and then compared to $V_{\mathrm{ref}}$. The size of each capacitor used in the capacitor divider is 350 fF. The total parasitic capacitance at Node B of Fig. 3.2 is dominated by the gate-to-source capacitance of the 16 $\mathrm{M_P}$ switches. From circuit simulations, the gate-to-source capacitance of each $\mathrm{M_P}$ transistor is 2.5 pF which leads to a total parasitic capacitance at Node B of $16 * 2.5\,\mathrm{pF} = 40\,\mathrm{pF}$. As a consequence, the additional capacitance introduced by the voltage divider is negligible when compared to the total capacitance at Node B and therefore does not affect the power efficiency.

During $\Phi_1$ the total charge taken from the battery can be written as:

$$Q_{\mathrm{BAT}} = I_{L_{\Phi_1}} T_{\mathrm{ON}} = \frac{V_{\mathrm{IN}} T_{\mathrm{ON}}}{2L} T_{\mathrm{ON}}, \tag{3.3}$$

where $I_{L_{\Phi_1}}$ is the average inductor current during $\Phi_1$. From Eq. (3.3), we can see that, by means of the duty cycle, the energy transferred from the battery to the inductor, and hence from the inductor to the load, can be controlled. Since the inductor directly powers the load, the stimulation is current-steered. Therefore, by controlling the current flowing into the tissue, the charge transferred to the tissue can be easily controlled irrespective of the value of the load. This allows the stimulator

to work with many different electrode types, and across a wide range of load impedances.

### 3.3.2 H-Bridge

The H-bridge has a double purpose. It allows for the selection of the desired active electrodes (one electrode acts as anode while another acts as cathode), but it also allows for the implementation of biphasic stimulation pulses, as discussed in the previous section. A principle diagram of the H-bridge suitable for multi-channel operation is depicted in Fig. 3.2. Assuming that N is the number of channels that can be stimulated simultaneously, in this work, as well as in [26], the H-bridge has $2 \cdot \mathrm{N}$ electrodes and $4 \cdot \mathrm{N}$ switches.

With respect to the H-bridge representation of Fig. 3.2, since the output voltages (up to 20 V) can exceed the supply voltage by a large amount ($V_{IN} = 3.5\,\mathrm{V}$), the switches on the bottom side can be implemented using NMOS transistors with thick drains and thin gate oxides. Their source terminals are always connected to ground, hence it is relatively easy to turn the switch on and off. For the switches on the top side of the H-bridge, a similar configuration would require that the gates of the PMOS transistors are driven with a voltage directly, which would need to be as high as the voltage at Node B, in this case up to 20 V. Hence, transistors with thick gate oxide are to be used [26]. In the IC technology used, the minimum channel length of thick-oxide devices is 600 nm which leads to a significantly higher gate-to-source parasitic capacitance. Since all the switches on the top side of the H-bridge have their source terminals connected together, the parasitic capacitance at Node B would be large. This has a big impact on the power efficiency because the parasitic capacitance at Node B is charged and discharged at every converter switching cycle (i.e., 1 MHz).

To reduce the parasitic capacitance at Node B, we have implemented a different approach in this work. For the switches on the top side of the H-bridge, PMOS transistors with thin gates and thick drains ($\mathrm{M_P}$ in Fig. 3.2) are used with resistors placed between their source and gate terminals. The current source provides a constant current, I, flowing through R such that the source-to-gate voltage of Transistor $M_P$ can be controlled. Therefore, $\mathrm{M_P}$ can be turned on and off by turning on and off the current source, respectively. Current source I is controlled by the comparator such that Transistor $\mathrm{M_P}$ is turned off as soon as the current flowing through the inductor reaches zero, as described in the zero-current detection scheme presented in the previous subsection. Using this approach makes it possible to use thin-gate-oxide devices for the PMOS transistors as well. By doing so, the external HV supply usually used in neural stimulators is also avoided. The value of I equals 1 mA, hence with a resistance $R = 1.75\,\mathrm{k\Omega}$, a constant source-to-gate voltage $V_{\mathrm{SG}}$ of 1.75 V is ensured. If a smaller value of current is used, then the value of the resistance needs to increase proportionally. Hence, the time constant associated with the charging and discharging of the parasitic gate-to-source capacitance of Transistor $\mathrm{M_P}$ also increases proportionally. This makes Switch $\mathrm{M_P}$ slower to be turned on and off, which directly impacts the efficiency and the functionality.

Current I flows through the resistor only during $\Phi_2$. Under the assumption that the load is purely resistive, the time constant associated with the discharging process of the inductor into the

load is $\tau = \frac{L}{R_{\text{load}}}$. After a time $t = 3\tau$, 95% of the current is discharged and the switch can be turned off. Hence, the charge dissipated in the resistor can be written as

$$Q_{\text{res}} = IT_2 = I\frac{3L}{R_{\text{load}}}. \tag{3.4}$$

The ratio of the charge taken from the battery and the charge dissipated in the resistor can be written as

$$\frac{Q_{\text{BAT}}}{Q_{\text{res}}} = \frac{V_{\text{IN}}T_{\text{ON}}^2 R_{\text{load}}}{6L^2 I}. \tag{3.5}$$

Assuming $L = 22\,\mu H$, $I = 1\,\text{mA}$, $V_{\text{IN}} = 3.5\,\text{V}$, $R_{\text{load}} = 500\,\Omega$ and $T_{\text{ON}} = 150\,\text{ns}$ (15% of the duty-cycle), the charge dissipated by the resistor is ∼14 times smaller than the charge delivered to the tissue. Eq. (3.5) shows that the higher the duty cycle value, the lower is the impact of the gate-driving technique on the power efficiency of the whole system. On the other hand, at the lowest duty-cycle value ($T_{\text{ON}} = 50\,\text{ns}$), the charge dissipated in the resistor is only ∼2× smaller than that delivered to the load. Hence, as will be discussed in Section 3.4, this is the main limitation to the power efficiency for the lowest duty cycle values.

The overdrive voltage of the PMOS switches ($\text{M}_\text{P}$) on the top side of the H-bridge may vary due to process variations. This directly affects its on-resistance and therefore the power efficiency of the whole neural stimulator. To further investigate this, a Monte Carlo simulation with 100 data points has been performed. Fig. 3.5 (b), shows that the average source-to-gate voltage of Switch $M_P$ is 1.72 V with a standard deviation $\sigma$ of only 99 mV. Fig. 3.5 (a), shows how the total power efficiency is affected by process variations and mismatch. With the ETI modelled as $R_{\text{load}} = 500\,\Omega$ with a series $C_{\text{load}} = 1\,\mu F$, the average efficiency is 67.7% with a standard deviation $\sigma = 0.9\%$.

Fig. 3.4 shows a cross-section view of the PMOS thick-drain transistor used in this design. Its rating voltages are $V_{\text{SGMAX}} = 2\,\text{V}$, $V_{\text{SDMAX}} = 20\,\text{V}$. The parasitic diode highlighted in green is of particular relevance to the designer. The diode always needs to be reversed biased. Since the source terminal is usually connected to the bulk terminal, the source-to-drain voltage always needs to be positive. This makes the device shown in Fig. 3.4 non-symmetrical with respect to its source and drain terminals. In literature, such a device is often called a Lateral Double-Diffused MOSFET (LDMOSFET).

### 3.3.3 Digital Control Module

The Digital Control Module has a similar architecture as the one presented in [26]. It generates all the required control signals to make the neurostimulator work. This block is powered from a 1.8 V supply, and from circuit simulations, its power consumption is approximately $100\,\mu W$. For each stimulation cycle, the pair of electrodes to be used, the amplitude and the pulse width can be set independently via an SPI. The stimulation pattern of each channel is stored in the memory and it can be edited whenever needed. The commands used as input, and loaded into the control module via the SPI are: 1) edit a channel, 2) start the stimulation of a single channel, 3) stop the stimulation of a single channel, 4) start the stimulation of all the channels loaded in the memory

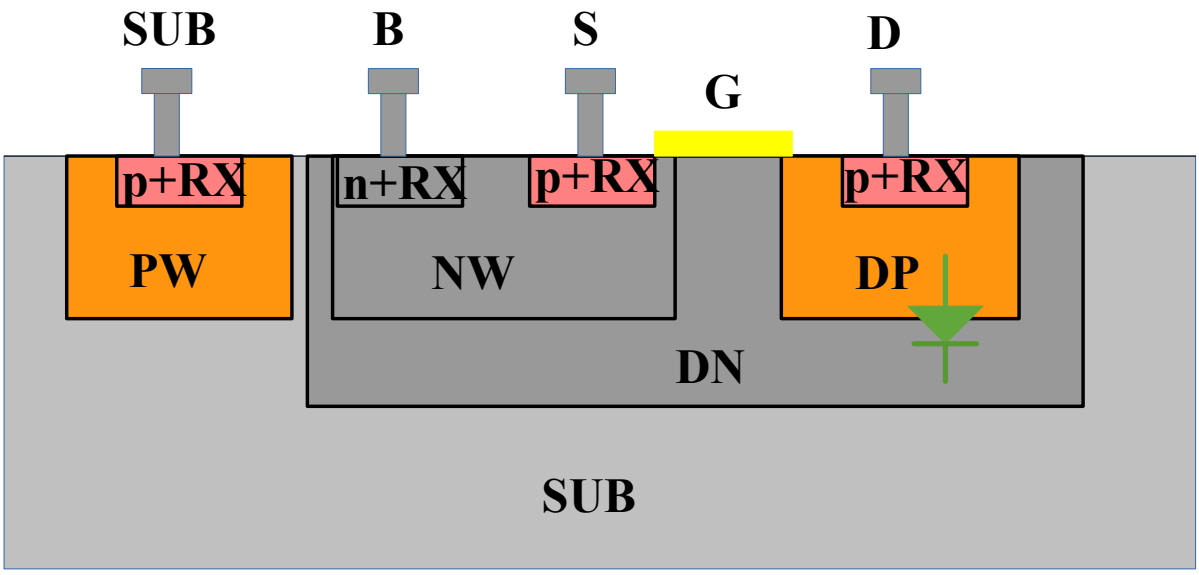


Figure 3.4: Cross section view of a thick-drain PMOS transistor operated as high-voltage switch.

(maximum of 8), 5) stop all the active channels. The digital control module runs with two different clocks: a low-frequency clock CLK_LF, at $f_{\mathrm{clk_{LF}}} = 1\,\mathrm{kHz}$ and a high-frequency clock, CLK_HF at $f_{\mathrm{clk_{HF}}} = 1\,\mathrm{MHz}$. The signal CLK_LF is used to trigger the commands sent by the user. Therefore it is always active. The signal CLK_HF controls the Core Circuit and it is used to generate the DUTY_CYCLE signal used to control switches $\mathrm{SW}_1$, $\mathrm{SW}_2$ and $\mathrm{SW}_3$ of the Core Circuit. The value of the duty cycle for each channel is stored in the memory and it is set in accordance with the bits loaded via the SPI interface.

The basic functionality of the digital control module for implementing a biphasic stimulation pulse is illustrated in Fig. 3.6. The finite state machine (FSM) starts from the IDLE state. As soon as a Trigger command is received, the first phase starts. Depending on the setup stored in the memory for that channel, the first phase can either be an anodic or a cathodic stimulation phase. The duration of this phase is set by counting the number of CLK_HF periods and it ends when it equals the value stored in the memory for that particular channel. Also the number of pulses in between the two phases, *INTERPHASE DELAY (IPD)* in Fig. 3.6, is counted and compared to its reference value stored in the memory. To depolarize the cell membrane, the second phase starts. Just as for the first phase, its duration is determined by counting the number of CLK_HF periods and comparing its value to the one stored in the memory. At the end of a biphasic pulse, active charge balancing is implemented. To do so, the residual charge at the tissue-electrode interface is sensed [17]. Based on the sign of the residual charge, a pulse with the opposite sign of the residual charge and the same amplitude is injected into the tissue. Then the residual charge is sensed again and if its sign is the same as before another pulse of the same sign is injected. This sense-inject procedure is repeated until the residual charge changes sign. As a result, the residual charge after charge balancing is always lower than the charge transferred by each single high-frequency pulse.

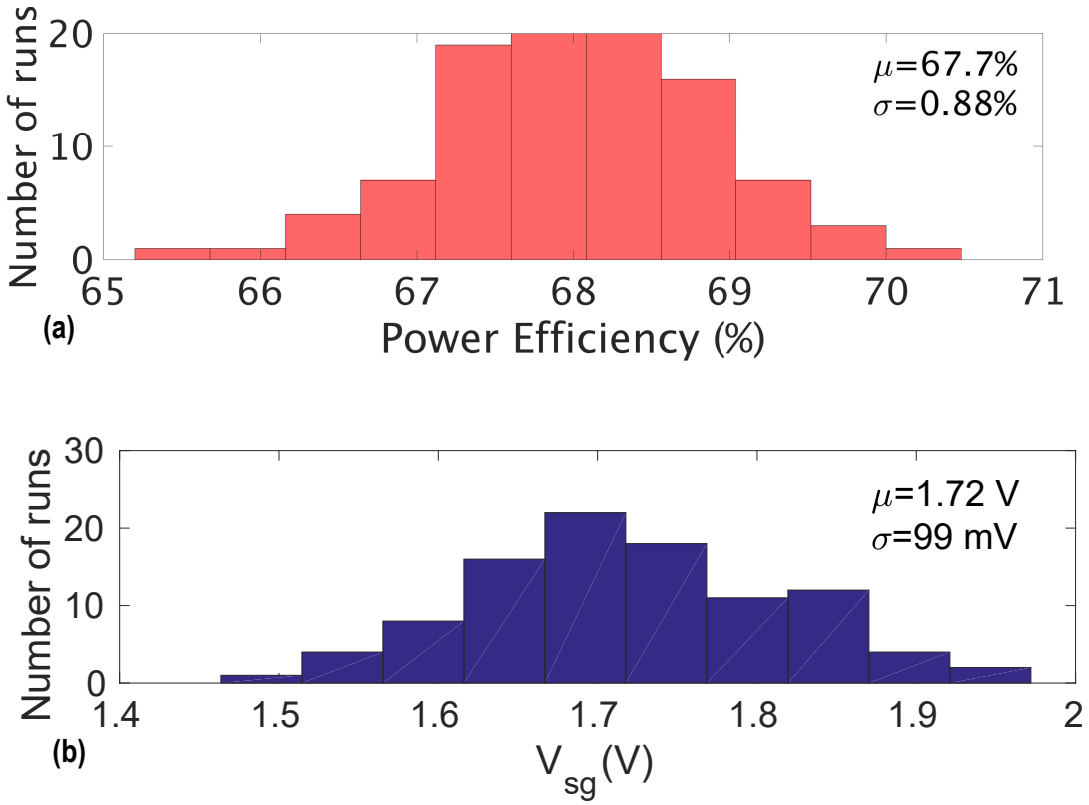


Figure 3.5: Monte-Carlo simulations showing (a) the power efficiency of the stimulator circuit for $R_{\text{load}} = 500\,\Omega$, $C_{\text{load}} = 1\,\mu F$ and duty-cycle = 24 %; (b) the gate-to-source voltage of the PMOS switches on the top side of the H-bridge.

The number of biphasic pulses for each channel is also stored in the memory. Therefore, after charge balancing, the *Digital Control Module* can decide whether another biphasic pulse is due.

When more channels are used at the same time, the core circuit keeps running at the frequency of 1 MHz, while the digital logic drives the switches of the H-bridge in such a way that all pulses generated by the core circuit are sequentially injected in the activated channels in accordance to the stimulation patterns stored in the memory for each channel. Therefore, when the system operates in multi-channel mode, each channel receives its own pulse at a frequency 1 MHz/N, where N is the number of channels simultaneously active. This does not affect the efficacy of the stimulation, as shown in [25].

## 3.4 Measurement Results

This section presents the measurements results of the UHF neural stimulator previously discussed. The circuit was implemented in a standard 0.18 $\mu m$ high-voltage CMOS process. The chip micrograph is shown in Fig. 3.7, while the total silicon area, including bondpads, is 3.65 $\text{mm}^2$.

The system works with two voltage domains: 1.8 V and 3.5 V. The 1.8 V voltage domain is used in the digital control module and in the H-bridge. Switches $SW_2$, $SW_3$ and $M_N$ of Fig. 3.2 are

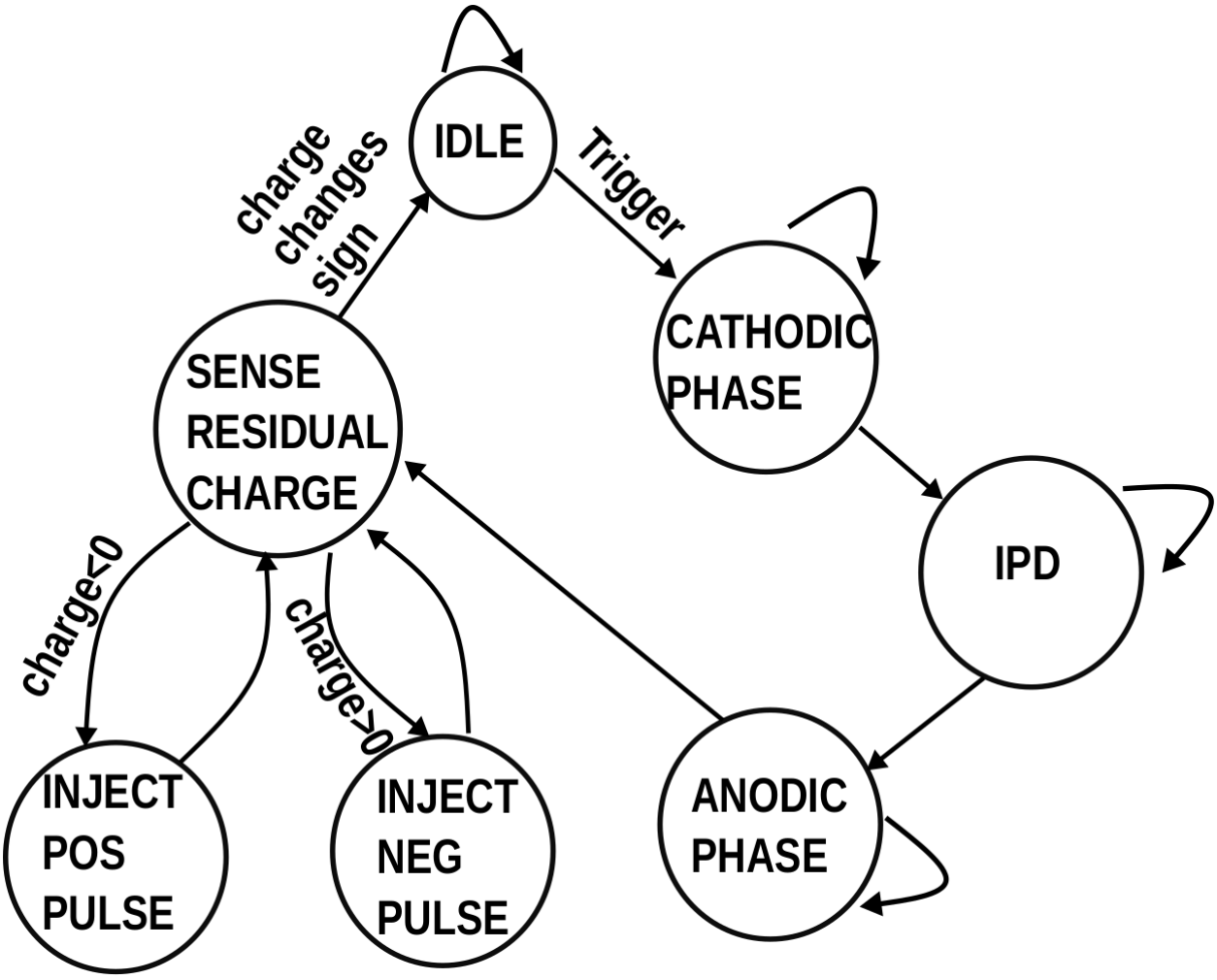


Figure 3.6: Finite-state-machine (FSM) representation of a biphasic pulse and charge-balancing procedure. The FSM moves through the phases of a classical biphasic pulse. Based on the sign of the residual charge, the stimulator senses and injects additional pulses until the residual charge changes sign.

operated from the 1.8 V voltage domain. Switch $SW_1$ and the core circuit are operated from a 3.5 V voltage domain. An external inductor $L = 22\,\mu H$ is used in the core.

The voltage waveforms have been acquired by means of an oscilloscope (Tektronics TDS2014C), and plotted with MATLAB software. The average currents needed to compute the power efficiency have been measured with a Keithley 6430 sourcemeter.

### 3.4.1 Power Efficiency

In Fig. 3.8, the measurement results of the power efficiency versus the duty cycle and for different load values are shown. Higher values of $R_{\text{load}}$ lead to a higher peak value of the output voltage. The peak value of the output voltage is determined by the values of $R_{\text{load}}$ and $\delta$, and it can exceed the maximum rating voltages of the devices. Therefore, in Fig. 3.8, the measurements were stopped

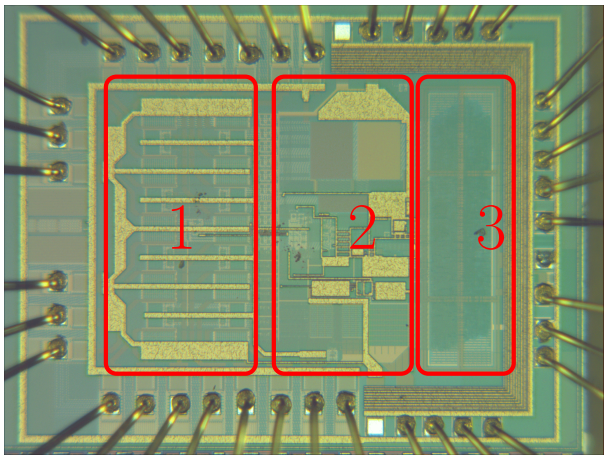


Figure 3.7: Photomicrograph of the UHF neural stimulator: (1) H-Bridge, (2) Core Circuit and (3) Digital Control Logic.

when the peak voltage across the load was 20 V. Exceeding this voltage would mean that some transistors would work outside of their safe operating region.

The lowest value of the duty cycle (i.e. $\delta = 4\%$) for $R_{\text{load}} = 200\,\Omega$ corresponds to the lowest ETI voltage ($< 2\,\text{V}$). With such a low output voltage, the losses are dominated by the on-resistance of the high-voltage switches involved in the conversion (i.e., conduction losses) and by the energy dissipated in the gate-driver circuit. As the duty-cycle increases, the voltage across the ETI increases and the impact of the conduction losses on the power efficiency becomes less important. Moreover, the ratio $Q_{\text{BAT}}$ over $Q_{\text{res}}$ is proportional to $T_{\text{ON}}^2$ (see Eq. 3.5), thereby leading to an increase of the power efficiency. By implementing the gate-driver technique, the source-to-gate voltage of each switch, and thereby the losses due to the dynamic operation of the switches, are kept constant with respect to the duty cycle. For high duty-cycle values, the switching losses dominate, resulting in a relatively constant power efficiency.

The authors have not noticed any significant reduction in power efficiency when more channels are used at the same time. Therefore, the power-efficiency measurements shown in Fig. 3.8 are valid even when 8 channels are operated simultaneously.

### 3.4.2 Biphasic Pulse and Multi-channel Operation

In Fig. 3.9 (a), a single-channel biphasic stimulation is shown. The DC-DC converter is operated with a constant frequency of 1 MHz and the number of pulses injected into the ETI equals 100. Since it is the only channel being stimulated, the duration of the cathodic phase is $t_{\text{cathodic}} = 100\,\mu s$. After the biphasic pulse, the charge balance ensure the removal of the residual charge from the ETI. A zoom during the cathodic phase in Fig. 3.9 (b) shows the pulses injected in the ETI at a rate of 1 MHz.

In Fig. 3.10, the multi-channel operation is illustrated by operating two channels simultaneously. The 1 MHz pulses generated by the inductor are delivered to the two activated channels in an interleaved fashion, as sketched in Fig. 3.1 (c). Hence, as discussed in Section 3.3, each channel

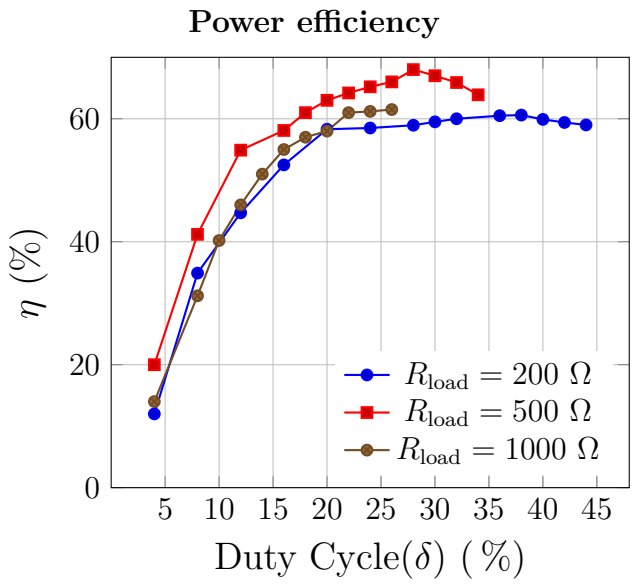


Figure 3.8: Measured power efficiency versus duty cycle for different load values.

receives its own pulses every $2\,\mu s$. In particular, the anodic phase of Channel 2 is performed while Channel 1 is being stimulated. This means that each channel receives its own pulses every $2\,\mu s$. Part of the cathodic phase of Channel 2 is performed while Channel 1 is not operated. During this time, Channel 2 is the only channel being stimulated, hence it receives its own pulses at a rate of 1 MHz. As a consequence, for Channel 2, the duration of the anodic and the cathodic phases are different.

### 3.4.3 Measurements in Saline Solution

The proposed stimulator has been tested using real electrodes immersed in a phosphate-buffered saline (PBS) solution bath. The 8-contact electrodes are commercially used for spinal-cord stimulation. For a complete characterization of the electrodes in a PBS solution, electrochemical impedance spectroscopy (EIS) experiments were carried out. Between two electrodes, a 50 mV RMS sinusoidal signal was applied and the impedance was measured using a frequency response analyzer (FRA). The impedance measured between the two electrodes over a $1\,\text{Hz} - 100\,\text{kHz}$ frequency range is shown in Fig. 3.11 (a), while Fig. 3.11 (b) shows the measurement setup in detail. The electrode-tissue interface is characterized by two main contributions: a resistive and a capacitive. At a sufficiently high frequency (e.g. $f > 10^3\,\text{Hz}$) the resistive part of the electrode-tissue interface dominates. Hence, from Fig. 3.11 (a), we can conclude that $R_{\text{tissue}} \sim 154\,\Omega$. At low frequencies (e.g. $f < 10\,\text{Hz}$), the impedance of the electrode-tissue interface is dominated by the capacitive contribution. By using a curve-fitting technique, the FRA found the capacitive contribution to be $C_{\text{tissue}} \sim 13\,\mu F$. Fig. 3.11 (c) shows a biphasic stimulation pulse when the electrodes are immersed in a PBS solution, while Fig. 3.11 (d) shows a zoom-in view around the inter-phase delay. For this stimulation, the settings are $T_{\text{cathode}} = 200\,\mu s$ and $duty\ cycle = 44\%$, leading to a peak stimulating voltage of approximately 11 V.

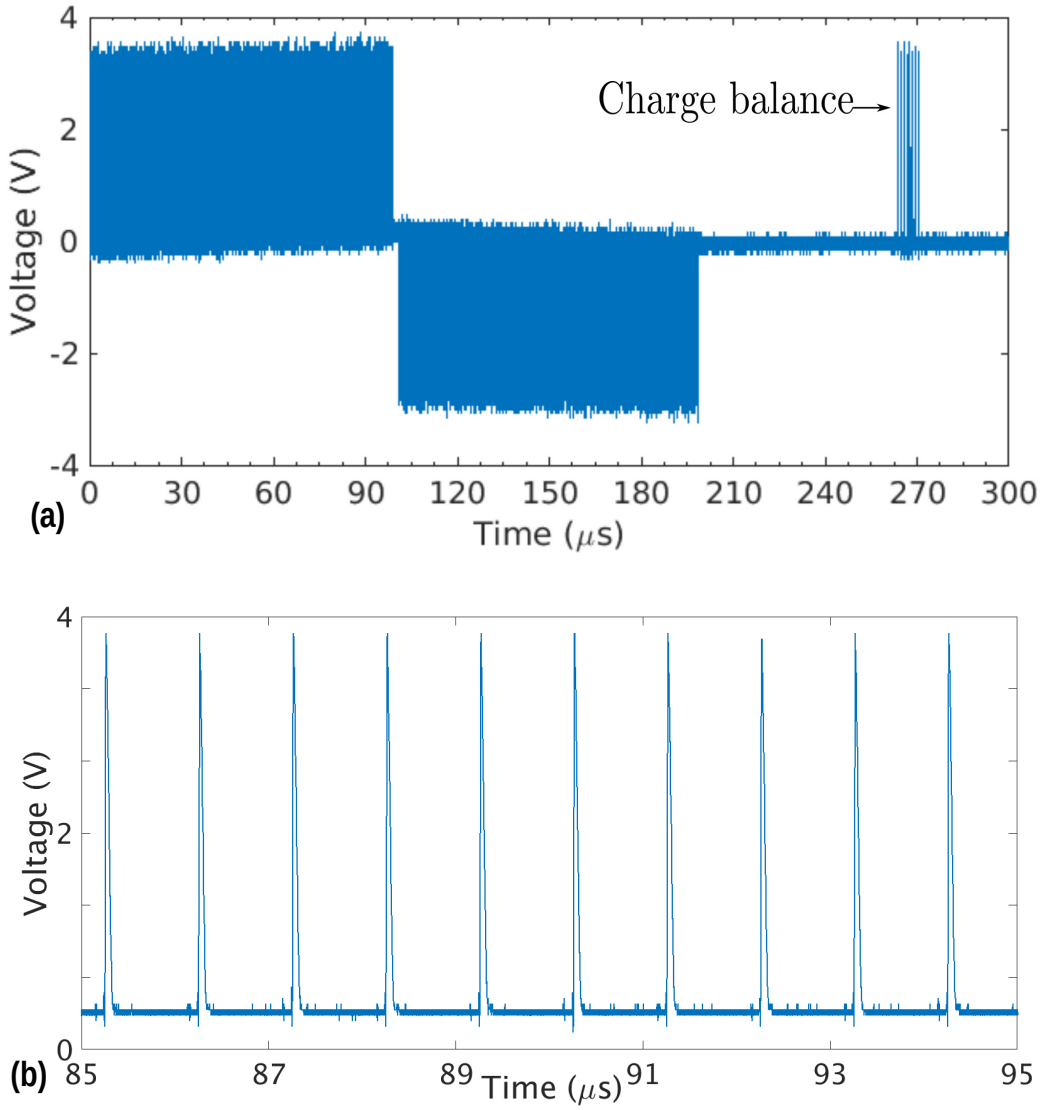


Figure 3.9: (a) Single-channel biphasic pulse with $t_{\text{cathod}} = 100\,\mu s$, $R_{\text{load}} = 200\,\Omega$, $C_{\text{load}} = 500\,\text{nF}$ and *duty cycle* = 15%. (b) zoom showing the high-frequency pulses injected into the ETI.

## 3.5 Comparison with the State of the Art and Discussions

Many different implementations of neural stimulators can be found in literature. The specifications and constraints of these stimulators heavily depend on their applications. One can think of retinal implants and deep-brain stimulators. The former tend to have a larger number of electrodes (up to thousands). The latter, however, often deliver more power to the excitable tissue. As a result, evaluating circuits with different specifications and constraints can lead to a meaningless comparison.

In order to have a quantitative evaluation of the performances of various stimulator circuits, a Figure of Merit (FOM) was introduced in [28]. Given a stimulator system with $N$ channels, its

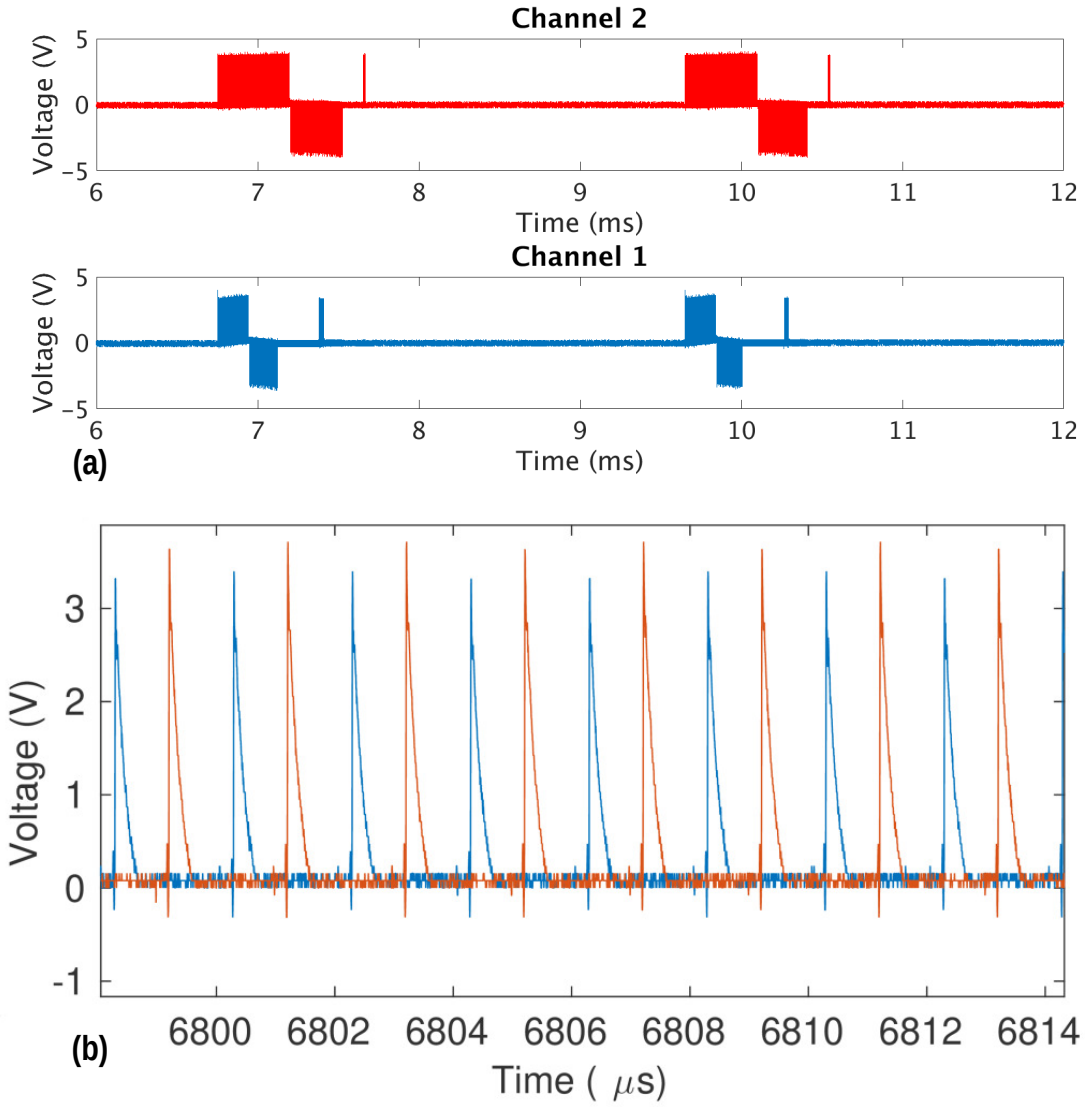


Figure 3.10: (a) Multi-channel operation when two independent channels are stimulated. For Channel 1: $R_{\text{load}} = 500\,\Omega$, $C_{\text{load}} = 100\,\text{nF}$, duty-cycle = 8% and for Channel 2: $R_{\text{load}} = 200\,\Omega$, $C_{\text{load}} = 500\,\text{nF}$, duty-cycle = 15% . (b) Zoom of two independent channels operated simultaneously

FOM is defined as:

$$FOM = \frac{I_{\text{dc}} P_{\text{system}}}{2N\Delta V_{\text{supply}} (I_{\text{cath}} T_{\text{cath}} f_{\text{stim}})^2}, \tag{3.6}$$

where $I_{\text{dc}}$ is the residual DC current after charge balancing, $P_{\text{system}}$ is the total power consumption, $\Delta V_{\text{supply}}$ is the maximal compliance of the stimulator, $I_{\text{cath}}$ is the average current during the cathodic phase, $T_{\text{cath}}$ is the duration of the cathodic phase and $f_{stim}$ is the stimulation rate. The FOM is dimensionless and an ideal neural stimulator has a FOM=0. The FOM values of the most recent neural stimulators along with their performance are reported in Table 3.1. The FOM, as defined in [28] is only applicable to current-mode stimulation (CMS) and voltage-mode stimulation (VMS). Hence, Eq. (3.6) does not hold for [29] and [10], as they present a switched-capacitor-based stimulator

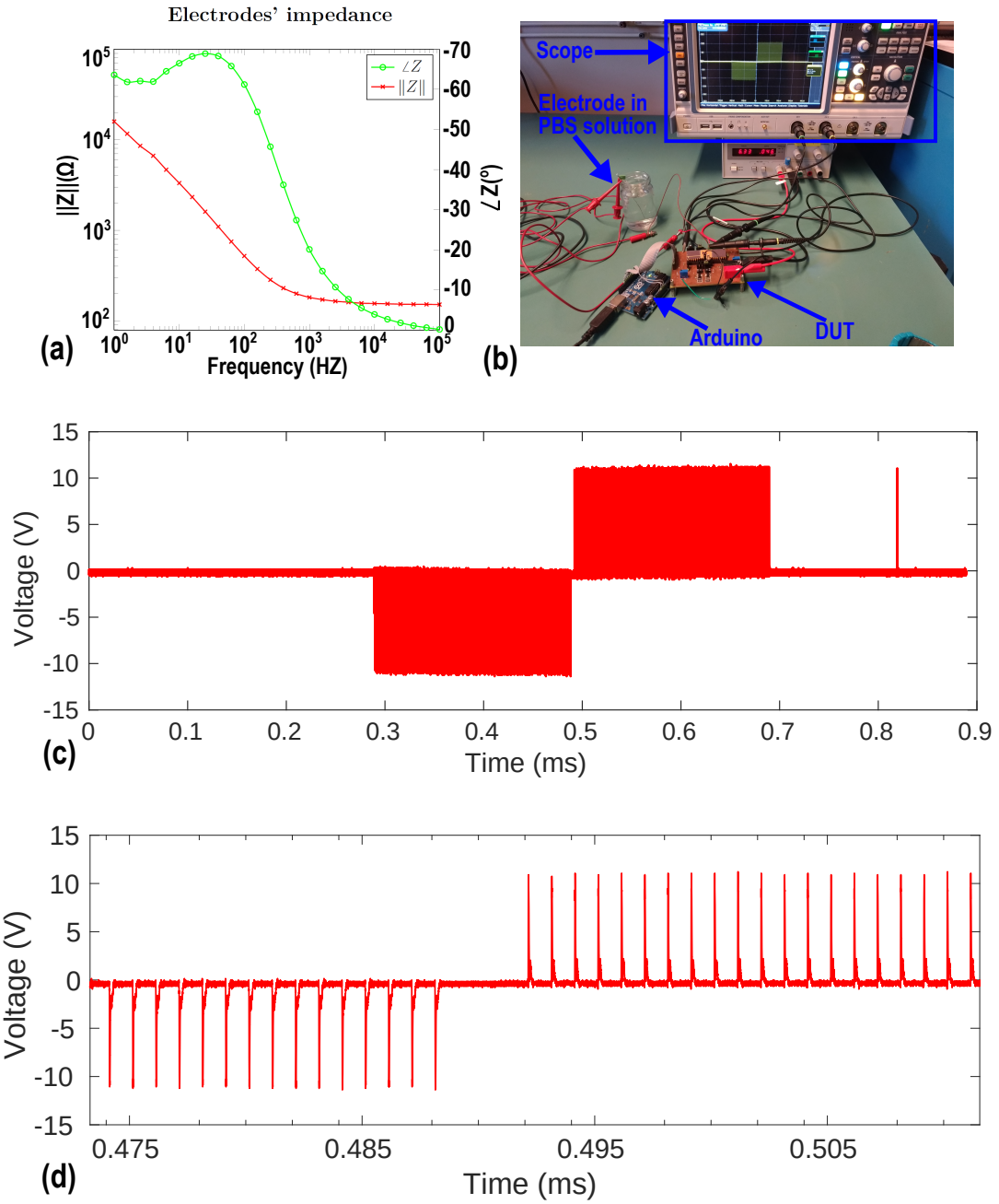


Figure 3.11: (a) Module and phase of the electrodes' impedance immersed in the PBS solution bath and (b) detailed measurement setup in which an Arduino Uno is used to program the stimulator via an SPI interface, the 8-contact electrode array immersed in a PBS solution bath and a Rohde & Schwarz oscilloscope used to capture the waveform. (c) Measured biphasic stimulation pulse with $t_{\text{cathod}} = 200\,\mu s$ and duty-cycle = 44% and (d) zoom of the biphasic pulse showing the inter-pulse delay.

(referred as SCS in Table 3.1).

The stimulator presented in [10] has the highest peak power efficiency (80.4%). However, it requires 2 external capacitors per channel, bringing the total number of external components to 8.

Table 3.1: COMPARISON OF PERFORMANCE

| | **This work** | [11] | [26] | [30] | [29] | [31] | [32] | [10] |
|---|---|---|---|---|---|---|---|---|
| **Application** | **Gen. Purpose** | Retinal | Gen. Purpose | Gen. Purpose | Gen. Purpose | Neuroprostheses | DBS | DBS |
| **Process** | **0.18 $\mu m$** | 1.5 $\mu m$ | 0.18 $\mu m$ | 0.35 $\mu m$ | 0.18 $\mu m$ | 0.6 $\mu m$ | 0.18 $\mu m$ | 0.35 $\mu m$ |
| **Operating voltage** | **3.5 V** | ±1.75 V | 3.5 V | 3.3 V | 5 V | 5 V | 3.3 V | ±2.1 V |
| **Channels** | **8** | 1 | 8 | 1 | 1 | 1 | 1 | 4 |
| **Electrodes** | **16 (fully arbitrary)** | 15 (monopolar) | 16 (fully arbitrary) | 2 | 2 | 2 | 2 | 8 |
| **HV Generation** | **Not needed** | Inductive link | External 20 $V$ | N.A. | Integrated Charge pump | On-Chip | External 12 $V$ | - |
| **Stimulator peak Efficiency** | **68 %** | 39% | 57% | 35 – 50% | 49% | – | 56% | 80.4% |
| **Stimulation type** | **CMS** | CMS | CMS | CMS | SCS | CMS | CMS | SCS |
| **FOM ($*10^3$)** | **0.0075** | 0.4 | 0.009 | – | *N.A.* | 1.15 | 0.67 | *N.A.* |
| **Stimulation Current (mA)** | **< 10** | 0.4 | < 10 | < 0.45 | - | ≤ 1 | 0.2 – 3 | ≤ 4 |
| **Load Impedance** | **100 Ω – 1 $k\Omega$** | 1.15 $k\Omega$ | 100 Ω – 1 $k\Omega$ | 500 Ω – 2 $k\Omega$ | 1.79$k$ Ω – 4.8 $k\Omega$ | - | 4 kΩ | 0.5 kΩ |
| **Multi-channel Efficiency** | **Yes** | No | No | Yes | No | Yes | No | No |
| **# of external components** | **1** | N.A. | 1 | 3 | 0 | 0 | 0 | 8 |

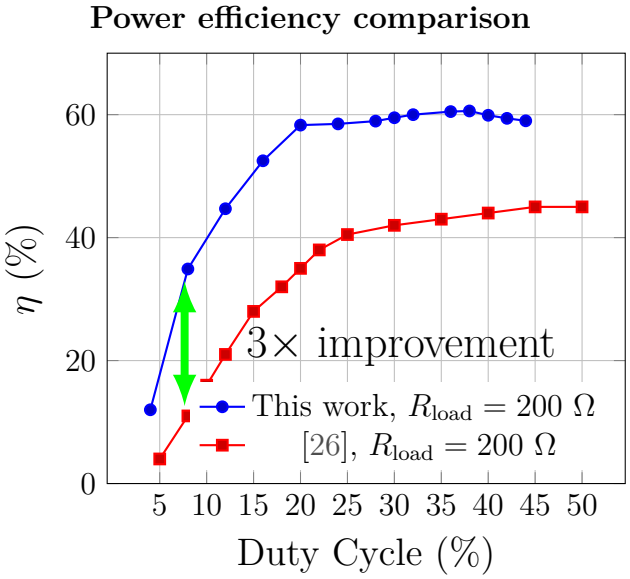


Figure 3.12: Power-efficiency comparison when the ETI is modelled as $R_{\text{load}} = 200\,\Omega$, $C_{\text{load}} = 500\,\text{nF}$.

Moreover, the 4 channels can be operated neither simultaneously nor independently. Hence, the system presented in [10] does not scale well in applications in which hundreds of channels need to be operated. Likewise in switched-capacitor stimulators (SCS), the system in [10] also suffers from power-efficiency degradation when the charge delivered to the tissue needs to be regulated.

The proposed design offers a peak power efficiency of 68% with 8 independent channels and only one external component, the inductor, shared among all the channels. Moreover, the need for an external high-voltage power supply is avoided.

In Fig. 3.12, the power efficiency of the proposed UHF stimulator is compared with [26], which

uses a diode to implement the Switch $SW_4$ of Fig. 3.3. For low duty-cycle values, conduction losses dominate. The output peak voltage is in the order of a few volts and the voltage drop across the diode, which typically is around $V_{DROP} = 0.6\,\mathrm{V}$, is comparable to the output voltage. Hence, by avoiding the use of the diode, the power efficiency can be boosted up to three times. For low duty-cycle values, the power efficiency is now limited by the power dissipated in the resistor $R$, as predicted by Eq. (3.5). Implementing an even more efficient gate-driving technique would allow, for low duty-cycle values, to boost the power efficiency even further.

The main limitation to increase the number of electrodes even further is the gate-to-source parasitic capacitance of all the $M_P$ switches connected at Node B (Fig. 3.2). This limitation can be easily overcome in applications in which the stimulating current is in the order of $\mu A$. This allows to reduce the size, and therefore the parasitic gate-to-source capacitance, of the $M_P$ switches. If we reduce the current delivered to the tissue by 10 times, the size of each $M_P$ transistor can be reduced by the same amount. This would allow, given the same parasitic capacitance at Node B, to have 10 times more electrodes, bringing the total number of electrodes to 160. Another approach to increase the number of electrodes without increasing the capacitance at Node B would be to arrange the H-bridge in several blocks. Each block is made of a fixed number of electrodes (e.g. 16) and one additional switch that connects the block to Node B. Every time a pulse is generated by the core circuit, the digital control module decides which block is used and within the block which pair of electrodes receives the pulse. A combination of the two mentioned approaches could scale the number of electrodes up to several hundreds.

## 3.6 Conclusion

This chapter presents the design and the measurement results of an 8-channel current-mode neural stimulator. A novel zero-current detection scheme has been discussed which allows to remove the freewheel diode usually used in DC-DC converters. A gate-driver circuit allows the use of thin-oxide transistors as high-voltage switches, eliminating the need to control the switches from an external high-voltage supply. A prototype IC was fabricated in a standard CMOS process. Measurements results show a peak power efficiency of 68% with the best FOM with respect to the state of the art.

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# Part II

# Analysis Design and Implementation of Energy-Efficient Power Supply Circuits for RF Oscillators

Chapter

# 4

# Power Supply Requirements of LC Oscillators

## 4.1 Introduction

The Internet-of-Things (IoT) is constantly spanning new applications [1]. IoT devices are mostly powered from energy stored in supercapacitors or batteries. However, their output voltage fluctuates due to the availability of energy sources. Consequently, a DC-DC buck converter cascaded with a linear low drop-out (LDO) regulator is customarily used to generate a 'clean' and stable nominal supply voltage of $\sim$1 V $V_{\mathrm{DD}}$ to supply nanoscale CMOS circuits and systems, as shown in Fig. 4.1 [2–5].

However, the input-referred noise of the LDO's voltage reference, error amplifier and feedback resistors appears at its output multiplied by the feedback factor, potentially degrading the performance of the supplied circuitry (e.g., the phase noise of an oscillator). Low-noise LDOs can be implemented at the cost of an additional quiescent current [2, 6–8], which, however, impacts the system power efficiency significantly.

For example, in [2], an inductor-based buck-boost DC-DC converter is used to regulate the voltage coming from the storage element. Several LDOs are then employed to provide a clean voltage for various supply-sensitive blocks of a transceiver architecture. Each LDO has a minimum dropout voltage of 200 mV, which, together with its quiescent current, makes the whole system power inefficient. On the other hand, a co-design of a class-D oscillator and an LDO is presented in [6]. The co-design relies on the fact that the error amplifier (EA) of the LDO regulates the gate voltage of the tail transistor directly, which is then used to provide the bias current to an LC oscillator. To avoid limiting the oscillator phase noise (PN) performance, the EA operates from a

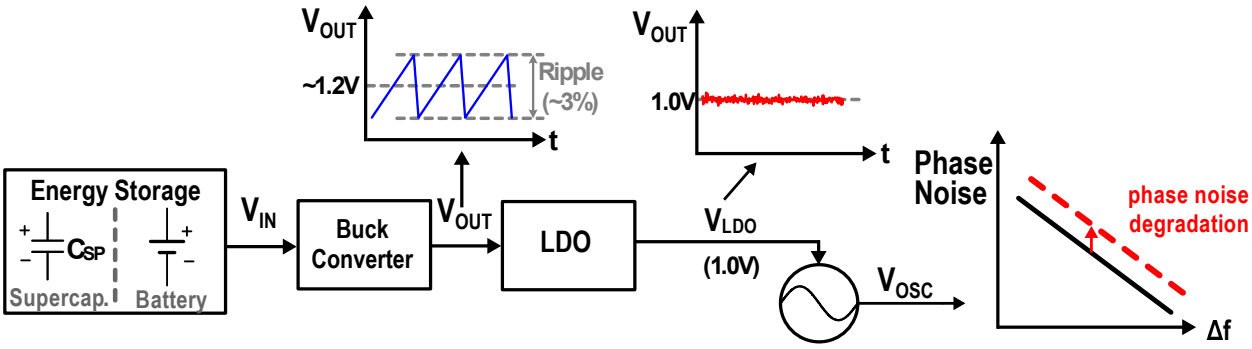



Figure 4.1: System diagram of a conventional cascade of a buck converter with an LDO to power up an oscillator.

separate supply of 1.2 V and consumes 0.5 mA of quiescent current, meaning that more than 40% of the power consumption is wasted in the LDO itself.

The primary focus of this chapter is to derive the requirements of supply blocks of LC oscillators. A design guideline for an analog LDO that meets those requirements is also provided[1]. The rest of this chapter is organized as follows: in Section 4.2, the ripple amplitude and the noise level required by the power supply of an LC oscillator not to affect its inherent spectral purity are derived. In Section 4.3, a design guideline for an analog LDO to meet these supply requirements is presented. As a result, the derived closed-form equations relate the system requirements to the LDO's maximum power efficiency and its component parameters. In Section 4.4, two system-level power management solutions to supply several supply-sensitive blocks comprising a complex RF System-on-Chip (SoC) are analysed and discussed. Finally, conclusions are drawn in Section 4.5.

## 4.2 Supply Requirements of an LC Oscillator

The voltage ripple and noise on the power supply can significantly degrade the oscillator's spectral purity. In this section, the requirements on the power supply noise and ripple are calculated such that the oscillator phase noise and spurious tones are not limited by the supply.

### 4.2.1 Power-Supply-Rejection Requirement

The level of the spurious tones around the carrier, induced by a sinusoidal supply ripple with an amplitude of $V_m$ and a frequency of $f_m$ can be calculated by

$$S_{\text{spur}} = 10\log_{10}\left(\frac{K_{\text{V}}V_{\text{m}}}{2f_{\text{m}}}\right)^2 \text{dBc}, \tag{4.1}$$

[1]This chapter has been published in IEEE Transactions on Circuits and Systems I: Regular Papers [9].

where $K_{\mathrm{V}}$ is the supply pushing factor of the oscillator expressed in Hz/V [10]. Given the desired spur level, the maximum supply ripple amplitude tolerated by the oscillator can be calculated by

$$V_{\mathrm{m}} < \frac{2 * f_{\mathrm{m}}}{K_{\mathrm{V}}} 10^{(S_{\mathrm{spur}})/20}. \tag{4.2}$$

For powering up the oscillator, a cascade connection of a switched-capacitor DC-DC converter and an LDO is usually used to simultaneously achieve a high power efficiency and a large power supply rejection. The switched-capacitor DC-DC converter generates a sawtooth-shaped supply voltage with a peak-to-peak ripple amplitude

$$V_{\mathrm{ripple}} = \frac{I_{\mathrm{L}}}{C_{\mathrm{fly}} f_{\mathrm{CLK}}}, \tag{4.3}$$

where $I_{\mathrm{L}}$ is the current drawn by the oscillator. $f_{\mathrm{CLK}}$ and $C_{\mathrm{fly}}$ are the converter switching frequency and flying capacitance, respectively. Considering the sawtooth shape of the DC-DC converter output voltage, the magnitude of the fundamental component of the ripple is $V_{\mathrm{ripple}}/\pi$. As a result, the required power supply rejection (PSR) of the LDO can be estimated by

$$PSR = \frac{\pi \cdot V_{\mathrm{m}}}{V_{\mathrm{ripple}}} = \frac{2\pi C_{\mathrm{fly}} f_{\mathrm{CLK}}^2 10^{(S_{\mathrm{spur}}/20)}}{I_{\mathrm{L}} K_{\mathrm{V}}}. \tag{4.4}$$

Note that there is a quadratic relation between the PSR and $f_{\mathrm{CLK}}$, since both the ripple of the DC-DC converter and the filtering capability of the oscillator simultaneously improve by increasing $f_{\mathrm{CLK}}$. It, however, comes at a price of a higher dynamic power consumption to drive the switches of the DC-DC converter, potentially degrading the system efficiency.

### 4.2.2 Noise Requirement

The PN performance of an oscillator is determined by the device excess noise factor and its tank quality factor, and can be calculated by

$$\mathcal{L}(\Delta f) = 10 \log_{10} \left[ \frac{10^{\frac{-\mathrm{FOM}}{10}} 1\mathrm{mW}}{P_{\mathrm{DC}}} \left( \frac{f_0}{\Delta f} \right)^2 \right], \tag{4.5}$$

where $P_{\mathrm{DC}}$ is the oscillator power consumption, and FOM[1] is its Figure-of-Merit with a typical value of 190-195 dBc/Hz [11, 12]. $f_0$ and $\Delta f$ are the carrier frequency and the offset frequency with respect to the main tone, respectively. Note that Eq. (4.5) is only valid in the thermal noise (20 dB/dec) region of the oscillator PN. Since the FOM is a general performance metric for LC oscillators and the variation of its typical value is not large [12], its use in Eq. (4.5) allows to reach more general conclusions in the following sections, which are independent of the oscillator topology and parameters.

[1] FOM= $\mathcal{L}(\Delta f) + 20 \log_{10} \left( \frac{f_0}{\Delta f} \right) - 10 \log_{10} \left( \frac{P_{\mathrm{DC}}}{1\mathrm{mW}} \right)$

On the other hand, the PN induced by the noise on the oscillator supply can be estimated to be

$$\mathcal{L}_{\text{sup}}(\Delta f) = 10\log_{10}\Big(\frac{K_{\text{V}}^2}{\Delta f^2}V_{\text{n,supply}}^2(\Delta f)\Big) \tag{4.6}$$

where $V_{\text{n,supply}}^2(\Delta\text{f})$ is the PSD of the supply noise [11]. To preserve the inherent phase noise of the oscillator, it is required that

$$\mathcal{L}_{\text{sup}}(\Delta f) \ll \mathcal{L}(\Delta f), \tag{4.7}$$

leading to

$$V_{\text{n,supply}}^2 < \frac{10^{\frac{-\text{FOM}}{10}}1\text{mW}}{P_{\text{DC}}}\Big(\frac{\text{f}_0}{K_{\text{V}}}\Big)^2. \tag{4.8}$$

Superficially, Eq. (4.8) indicates that a larger supply noise can be tolerated at higher oscillation frequencies. However, the total tank capacitance ($C_{\text{tot}}$) is composed of a variable capacitor used to tune $f_0$ and a voltage-dependent parasitic capacitance of the oscillator core transistors ($C_{\text{par}}$). Hence, the effective value of $C_{\text{par}}$ is modulated by the supply voltage. As $f_0$ increases, the variable capacitance is reduced, and $C_{\text{par}}$ becomes a bigger portion of $C_{\text{tot}}$, thereby increasing $K_{\text{V}}$. Consequently, $f_0/K_{\text{V}}$ and the noise requirement remain almost constant over the operating frequency range. The variation of the equivalent value of $C_{\text{par}}$ comes from the fact that the time interval during which the transistors stay in various operating regions is altered when the oscillation amplitude varies due to supply ripple. When the ripple frequency increases, the time that the transistor stays in each region becomes shorter. However, its ratio to the period of the supply ripple remains relatively constant, leading to a similar equivalent value of $C_{\text{par}}$. Therefore, $K_{\text{V}}$ is weakly related to the ripple frequency.

## 4.3 LDO Design Guidelines as a Voltage Supply of LC Oscillators

Several LDOs are reported in the literature with a power efficiency higher than 95% [13–15], which, however, do not meet the requirements discussed in the previous section. The goal of this section is to quantify the efficiency degradation of an analog LDO while meeting the requirements discussed in the previous section.

The LDO shown in Fig. 4.2 consists of an Error Amplifier (EA), a feedback network ($R_{\text{F1}}$ and $R_{\text{F2}}$), an accurate voltage reference ($V_{\text{ref}}$), and a pass transistor ($\text{M}_{\text{P}}$). The feedback network provides a scaled version of the output voltage, $V_{\text{FB}}$. The EA compares $V_{\text{ref}}$ with $V_{\text{FB}}$ and generates an error signal $V_{\text{G}}$ that modulates the gate terminal of the pass transistor such that the output voltage $V_{\text{OUT}}$ is kept constant. In steady state, the output voltage can be expressed as

$$V_{\text{out}} = (1+\frac{R_{\text{F1}}}{R_{\text{F2}}})V_{\text{ref}} = \frac{V_{\text{ref}}}{\beta}, \tag{4.9}$$

where $\beta = \dfrac{R_{\text{F2}}}{R_{\text{F1}}+R_{\text{F2}}}$ is the reciprocal of the closed-loop gain of the LDO. The power efficiency

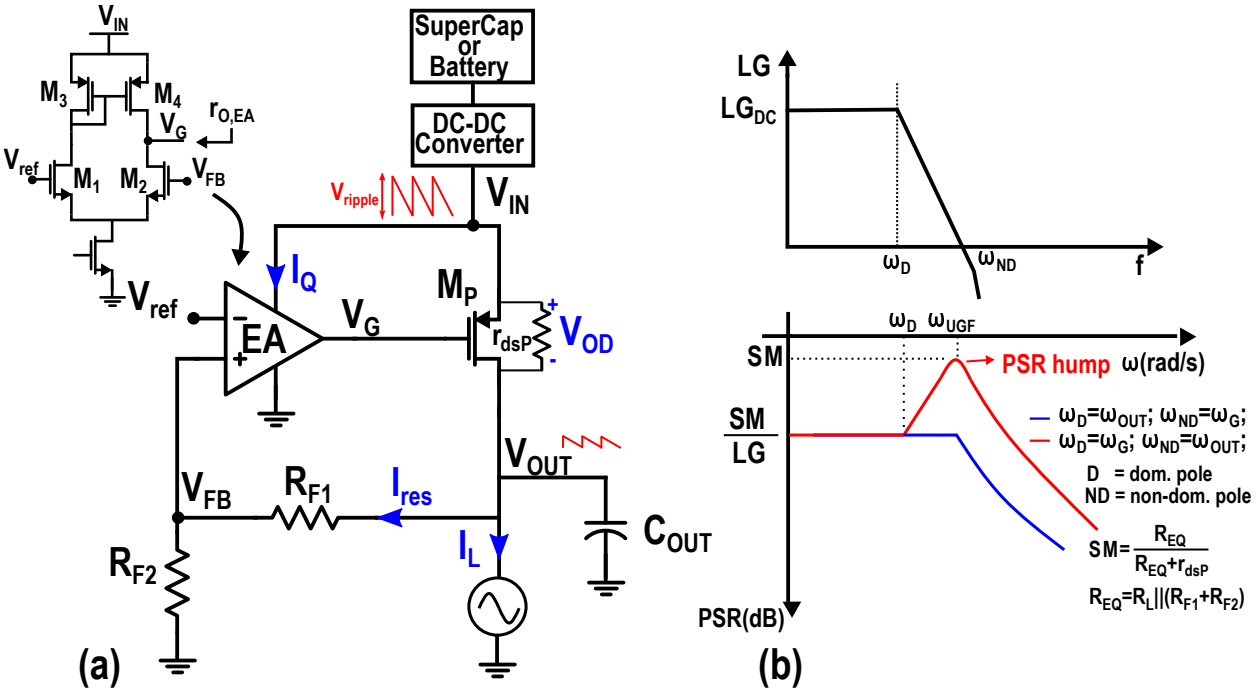



Figure 4.2: (a) Block diagram of a typical LDO topology; (b) its Loop Gain (LG) (top) and PSR (bottom) with (blue line) and without (red line) the use of an external capacitor.

can be written as

$$\eta = \left(\frac{V_{\mathrm{IN}} - V_{\mathrm{OD}}}{V_{\mathrm{IN}}}\right)\left(\frac{I_{\mathrm{L}}}{I_L + I_{\mathrm{res}} + I_{\mathrm{Q}}}\right)$$
$$\eta = \left(\frac{V_{\mathrm{IN}} - V_{\mathrm{OD}}}{V_{\mathrm{IN}}}\right)\left(\frac{I_{\mathrm{L}}}{I_{\mathrm{L}} + \frac{V_{\mathrm{OUT}}}{R_{\mathrm{F1}}+R_{\mathrm{F2}}} + I_{\mathrm{Q}}}\right) \tag{4.10}$$

where $V_{\mathrm{OD}}$ is the overdrive voltage of transistor $\mathrm{M_P}$, $I_{\mathrm{L}}$ are the currents drawn by the oscillator, $I_{\mathrm{res}}$ and $I_{\mathrm{Q}}$ is the current that flow through the resistors and the quiescent current, respectively. $V_{\mathrm{OD}}$, $I_{\mathrm{res}}$ and $I_{\mathrm{Q}}$ affect the power efficiency. Hence, in this section, their minimum value is calculated such that the oscillator's requirements are met.

### 4.3.1 Calculation of $I_{\mathrm{res}}$ Based on Noise Requirements

A bandgap voltage reference is usually used to generate $V_{\mathrm{ref}}$. Its noise is filtered out either by placing a big external capacitor, or by implementing an $RC$ filter with a big on-chip resistor and a capacitor [16]. Consequently, it is neglected in the following analysis.

Resistors $R_{\mathrm{F1}}$ and $R_{\mathrm{F2}}$ generate an input-referred noise voltage with a power spectral density (PSD), in $\mathrm{V^2/Hz}$, of $4kT(R_{\mathrm{F1}}||R_{\mathrm{F2}})$, where $k$ is Boltzmann's constant and $T$ is the absolute temperature expressed in kelvin. Their noise contribution directly appears at the output and it is filtered only at frequencies above the non-dominant (ND) pole of the LDO. For this reason, one would choose $R_{\mathrm{F1}}$ and $R_{\mathrm{F2}}$ as small as possible while keeping the ratio constant. However, the lower the value of the resistors, the higher the current ($I_{\mathrm{res}}$) flowing through them, thus degrading the

power efficiency of the LDO (Eq. (4.10)). The PSD of the feedback resistors noise is multiplied by $\frac{1}{\beta^2}$ and appears at the output of the LDO, resulting in $S_{\mathrm{V,OUT,R}} = (\frac{R_{\mathrm{F1}}}{R_{\mathrm{F2}}})4kT(R_{\mathrm{F1}} + R_{\mathrm{F2}})$.

To not affect the inherent PN of the oscillator, the PN induced by the feedback resistors must be significantly smaller (e.g., $\sim 10$ times smaller) than the inherent PN of the oscillator. By using Eq. (4.7) and Eq. (4.8), we have

$$\Big(\frac{R_{\mathrm{F1}}}{R_{\mathrm{F2}}}\Big)4kT(R_{\mathrm{F1}} + R_{\mathrm{F2}}) < \frac{1}{10}\frac{10^{\frac{-FOM}{10}}1\mathrm{mW}}{P_{\mathrm{DC}}}\Big(\frac{f_0}{K_{\mathrm{V}}}\Big)^2. \tag{4.11}$$

Given that $P_{\mathrm{DC}} = \frac{V_{\mathrm{OUT}}^2}{R_{\mathrm{L}}}$ and $V_{\mathrm{OUT}} = V_{\mathrm{ref}}\Big(1 + \frac{R_{\mathrm{F1}}}{R_{\mathrm{F2}}}\Big)$, Eq. (4.11) can be rewritten as

$$\Big(\frac{I_{\mathrm{res}}}{I_{\mathrm{L}}}\Big) > 10\frac{4kT(\frac{1}{\beta} - 1)(V_{\mathrm{OUT}})^2}{10^{\frac{-FOM}{10}}1\mathrm{mW}\Big(\frac{\mathrm{f_0}}{\mathrm{K_V}}\Big)^2}. \tag{4.12}$$

Eq. (4.12) allows to quantify the efficiency degradation due to the current, $I_{\mathrm{res}}$, flowing through the feedback resistors.

Assuming $P_{\mathrm{DC}} = 1\,\mathrm{mW}$, $V_{\mathrm{OUT}} = 1\,\mathrm{V}$, $K_{\mathrm{V}} = 40\,\mathrm{MHz/V}$ and $FOM = 190\,\mathrm{dBc/Hz}$, from Eq. (4.8) the maximum supply noise is $V_{\mathrm{n,supply}} = 38\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. Furthermore, by using Eq. (4.12), the two feedback resistors are found to be $R_{\mathrm{F1}} = 5.3\mathrm{k}\,\Omega$ and $R_{\mathrm{F2}} = 7\,\mathrm{k}\Omega$. As a result, $I_{\mathrm{res}} \sim 80\,\mu A$, which results in a current efficiency of 92%. Note that high-performance oscillators have a higher FOM, posing even more stringent requirements on the supply noise and the size of the feedback resistors (e.g., an FOM of $196\,\mathrm{dBc/Hz}$ leads to $V_{\mathrm{n,supply}} < 19\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, $R_{\mathrm{F1}} = 1.8\,\mathrm{k}\Omega$, $R_{\mathrm{F2}} = 7\,\mathrm{k}\Omega$ and $I_{\mathrm{res}} \sim 130\,\mu A$).

It is worth pointing out that the efficiency degradation due to $I_{\mathrm{res}}$ does not change with $P_{\mathrm{DC}}$ or $I_{\mathrm{L}}$ for a constant $V_{\mathrm{OUT}}$. When $I_{\mathrm{L}}$ increases, the noise power tolerated by the oscillator decreases with the same ratio. Hence, $I_{\mathrm{res}}$ should proportionally increase to reduce the noise contribution from the feedback resistors, leading to a constant $\frac{I_{\mathrm{res}}}{I_{\mathrm{L}}}$. Therefore, the efficiency degradation due to $I_{\mathrm{res}}$ also remains constant.

### 4.3.2 Calculation of $I_{\mathrm{Q}}$ Based on Noise Requirements

The input-referred noise of the EA can be written as [17]

$$S_{V,IN,EA} = 2S_{\mathrm{V,M_1}} + 2\Big(\frac{g_{\mathrm{m3}}}{g_{\mathrm{m1}}}\Big)^2 S_{\mathrm{V,M_3}}, \tag{4.13}$$

where $S_{\mathrm{V,M_1}}$ and $S_{\mathrm{V,M_3}}$ are the power spectral density of the noise (voltage) generated by $\mathrm{M_1}$ and $\mathrm{M_3}$, respectively. Each of the PSD is made of thermal and flicker noise components. Given that at higher frequencies the thermal component is dominant, in this analysis, the flicker noise component is neglected. Hence,

$$S_{\mathrm{V,M_i}} = \frac{4kT\gamma}{g_{\mathrm{mi}}} \tag{4.14}$$

where $\gamma$ is the excess noise factor and it is equal to $\frac{2}{3}$ in strong inversion saturation. By substituting Eq. (4.14) into Eq. (4.13), and assuming $M_{1-4}$ of the same size, the total noise at the input of the EA can now be expressed as

$$S_{\mathrm{V,IN,EA}} = \frac{16\gamma kT}{g_{\mathrm{m}}}. \tag{4.15}$$

The total output-referred noise of the EA can be written as

$$S_{\mathrm{V,OUT}} = \frac{S_{V,IN,EA}}{\beta^2}. \tag{4.16}$$

It is worth mentioning that, due to the gain of the error amplifier, the noise of the pass transistor $M_P$ has a negligible contribution compared to the error amplifier noise when referred to the LDO input.

Similarly to the noise of the feedback resistors, it can be assumed that the PN induced by the EA should be $\sim 10$ times smaller than the inherent PN of the oscillator (Eqs. (4.7, 4.8)). Hence,

$$g_m > 10 \cdot \frac{16\gamma kTP_{\mathrm{DC}}}{10^{\frac{-FOM}{10}} 1\mathrm{mW}\beta^2\left(\frac{f_0}{K_{\mathrm{V}}}\right)^2}. \tag{4.17}$$

By multiplying both sides of Eq. (4.17) by $I_{\mathrm{Q}}$, the quiescent current can be expressed as

$$I_Q > 10 \cdot \frac{\frac{32}{3}kTP_{\mathrm{DC}}}{10^{\frac{-FOM}{10}} 1\mathrm{mW}\left(\frac{f_0}{K_{\mathrm{V}}}\right)^2\beta^2\left(\frac{g_{\mathrm{m}}}{2I_{\mathrm{D}}}\right)}, \tag{4.18}$$

where $I_D = \frac{I_Q}{2}$ is the drain current of $M_{1:4}$. Assuming $g_{\mathrm{m}}/I_{\mathrm{d}} = 12S/A$ and $\gamma = \frac{2}{3}$, $I_{\mathrm{Q}}$ must be $> 145\,\mu A$, further degrading the power efficiency by a factor of 1/0.87.

To avoid degrading the oscillator phase noise, Eq. (4.18) suggests that $I_{\mathrm{Q}}$ should be increased proportionally to $P_{\mathrm{DC}}$ for the same $V_{OUT}$ and $g_m/I_D$. As a result, $\frac{I_{\mathrm{Q}}}{I_{\mathrm{L}}}$, and therefore, the power efficiency degradation due to the error amplifier is constant with respect to $P_{\mathrm{DC}}$.

### 4.3.3 Calculation of $V_{\mathrm{OD}}$ Based on PSR Requirement

The two poles of the LDO topology shown in Fig. 4.2 are located at the gate of $M_P$ ($\omega = \omega_{\mathrm{G}}$) and at the output node $V_{\mathrm{OUT}}$ ($\omega = \omega_{\mathrm{OUT}}$) [18–20], and can be calculated by

$$\begin{aligned} \omega_{\mathrm{G}} &= \frac{1}{r_{\mathrm{O,EA}}(C_{\mathrm{gsP}} + (1 + g_{\mathrm{mP}}R_{\mathrm{OUT}})C_{\mathrm{gdP}})} \\ \omega_{\mathrm{OUT}} &= \frac{1}{R_{\mathrm{OUT}}C_{\mathrm{OUT}}} \end{aligned} \tag{4.19}$$

where $r_{\mathrm{O,EA}}$ is the output impedance of the error amplifier, $R_{\mathrm{OUT}} = R_{\mathrm{L}}||(R_{\mathrm{F1}} + R_{\mathrm{F2}})||r_{\mathrm{DS,P}}$, $r_{\mathrm{DS,P}}$ is the output resistance of $M_P$, $C_{\mathrm{gdP}}$ and $C_{\mathrm{gsP}}$ are the gate-to-drain and gate-to-source capacitances of $M_P$, respectively. Based on the location of the dominant pole ($\omega_{\mathrm{D}}$), the LDO topologies can be

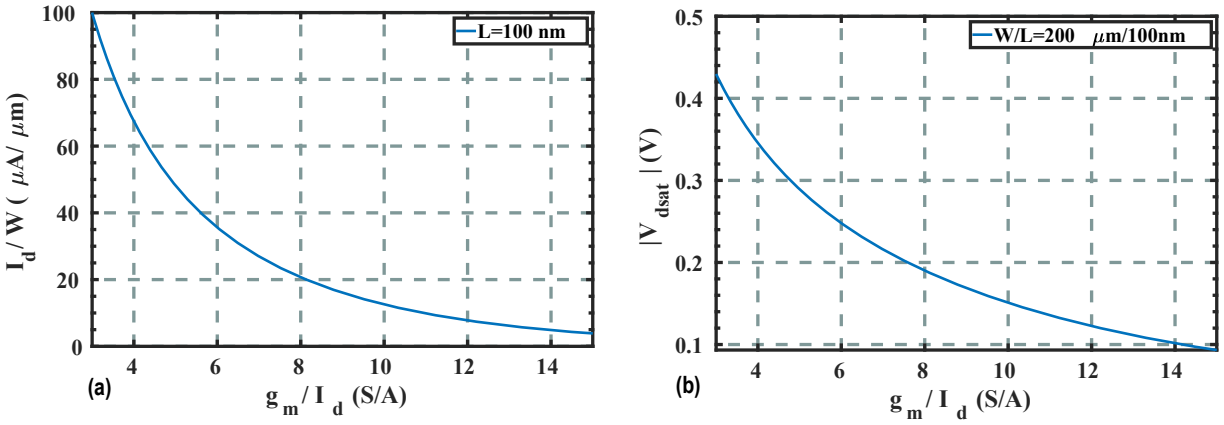



Figure 4.3: (a) Current density and (b) overdrive voltage of the pass transistor for different $g_m/I_D$ values.

divided into two categories [21], the PSR profiles of which are sketched in Fig. 4.2 (b). To have the dominant pole located at $V_{\mathrm{OUT}}$ [3, 22–26], one can increase $C_{\mathrm{OUT}}$. In this scenario, the LDO can easily achieve a high PSR at high frequencies, as the output capacitor provides a low-impedance path to ground for the supply ripple. This is represented by the blue curve in Fig. 4.2 (b). To guarantee stability, the output capacitor is increased to a value in the $\mu$F range. For LDOs with the dominant pole located at the gate of $\mathrm{M_P}$ ($\omega_{\mathrm{D}} = \omega_{\mathrm{G}}$) [13–15, 26–28], the value of $C_{OUT}$ is reduced significantly. The corresponding PSR is sketched with a red curve in Fig. 4.2 (b). For $\omega_{\mathrm{G}} < \omega < \omega_{\mathrm{OUT}}$, due to reduced loop gain, the PSR degrades and a hump in the PSR curve is observed. However, at $\omega > \omega_{\mathrm{OUT}}$, the output capacitor provides a low-impedance path to ground, thereby improving the PSR. In order to favor full-system integration, the cap-less LDO solution is chosen, whose dominant pole needs to be located at the switching frequency of the DC-DC converter (e.g. $f_{\mathrm{D}} = f_{\mathrm{CLK}} = 10\,\mathrm{MHz}$).

The peak of the PSR hump is located at the unity gain frequency and it is equal to $\dfrac{R_{\mathrm{EQ}}}{R_{\mathrm{EQ}} + r_{\mathrm{DS,P}}}$, where $R_{\mathrm{EQ}} = R_{\mathrm{L}}||(R_{\mathrm{F1}} + R_{\mathrm{F2}})$. To guarantee a PSR of 0.5 around the hump, $r_{\mathrm{DS,P}} = R_{\mathrm{EQ}} \approx R_{\mathrm{L}}$ is required. Hence, the length of $\mathrm{M_P}$ can be calculated as

$$r_{\mathrm{ds,P}} = \frac{1}{\lambda I_{\mathrm{L}}} = \frac{V_{\mathrm{a}} L_{\mathrm{P}}}{I_{\mathrm{L}}} \Rightarrow L_{\mathrm{P}} = \frac{R_{\mathrm{EQ}} I_{\mathrm{L}}}{V_{\mathrm{a}}} = 0.1\,\mu m \tag{4.20}$$

where $V_{\mathrm{a}} = 10\,V/\mu m$.

To guarantee a phase margin of 60° with a PSR of $-40\,\mathrm{dB}$, the frequency of the non-dominant pole should be located a frequency $\sim 400$ times higher than the dominant one, i.e., $f_{\mathrm{ND}} > 400 f_{\mathrm{CLK}}$. Consequently, by employing Eq. (4.19), the total output capacitance should be $< 100\,fF$.

As will be shown shortly, the width of $\mathrm{M_P}$ should be maximized to reduce its overdrive voltage and improve the LDO's efficiency. Therefore, it is desired that the parasitic capacitance of $\mathrm{M_P}$ absorbs all available $C_{\mathrm{out}}$. Also, any extra decoupling capacitance would push the non-dominant pole closer to the dominant one, potentially affecting the stability of the LDO. $C_{\mathrm{out}}$ is dominated

Table 4.1: Summary of LDO performance and component values

| Component | Value | Parameter | Value | Efficiency degradation |
|---|---|---|---|---|
| $M_{1:4}$ | $\frac{30\,\mu m}{500\,\text{nm}}$ | $\mathbf{V}_{\text{OD}}$ | 125 mV | $\frac{1}{0.89}$ |
| $M_P$ | $\frac{200\,\mu m}{100\,\text{nm}}$ | $\mathbf{I}_{\text{Q}}$ | $145\,\mu A$ | $\frac{1}{0.87}$ |
| $\mathbf{R}_{\text{F1}}, \mathbf{R}_{\text{F2}}$ | $5.3\,\text{k}\Omega, 7\,\text{k}\Omega$ | $\mathbf{I}_{\text{res}}$ | $80\,\mu A$ | $\frac{1}{0.92}$ |
| $\mathbf{I}_{\text{L}}$ | 1 mA | - | - | - |

by the drain-to-bulk, $C_{\text{db}}$, and drain-to-gate, $C_{\text{dg}}$, capacitances of $M_P$:

$$\begin{aligned} C_{\text{out}} &= C_{\text{db}} + C_{\text{dg}} = C_{\text{ov}}W + 0.5C_{\text{jbd}}WE + C_{\text{jbdsg}}W \approx \\ &\approx 500\,\text{pF/m} \cdot W \end{aligned} \tag{4.21}$$

where $C_{\text{ov}} = 50\,\text{pF/m}$ is the overlapped capacitance per unit width, $C_{\text{jbd}} = 1.4\,\text{mF/mm}^2$ is the bulk-to-drain junction capacitance per unit area, $E = 140\,\text{nm}$ and $C_{\text{jbdsg}} = 300\,\text{pF/m}$[1]. Hence, the maximum width of $M_P$ to guarantee enough PSR at $f_{\text{CLK}}$ is $W_P = 200\,\mu m$.

Fig. 4.3 (a) shows the current density for different $g_m/I_D$ values for the pass transistor. Given that $I_L = 1\,\text{mA}$ and $W_P = 200\,\mu m$, a $g_m/I_D$ of 12 can be achieved. Consequently, $M_P$ can operate in the weak-inversion region with a $V_{\text{OD}}$ of only 125 mV, as can be gathered from Fig. 4.3 (b). This further degrades the power efficiency of the LDO by a factor of $\frac{1}{0.89}$.

If $P_{\text{DC}}$ increases, $R_L$ proportionally decreases for a constant $V_{\text{OUT}}$. Hence, to keep $\omega_{\text{OUT}}$ the same, $C_{\text{OUT}}$ should be increased by the same ratio. This, in turn, leads to an increase in the width of $M_P$, which makes the current density of the pass transistor relatively constant, resulting in a similar overdrive voltage. Consequently, the power efficiency degradation due to $V_{\text{OD}}$ is not a function of $P_{\text{DC}}$.

### 4.3.4 Satisfying the PSR Requirement

The PSR at frequencies below the dominant pole of the LDO can be expressed as

$$PSR = \frac{SM}{1 + LG_{\text{DC}}} \approx \frac{SM}{A_{\text{EA}}A_{M_P}\beta} \tag{4.22}$$

[1]Note that $C_{\text{ov}}$, $C_{\text{jbd}}$, and $C_{\text{jbdsg}}$ are technology-dependent parameters and the values used here are from a 40-nm CMOS technology.

where $SM = \dfrac{R_{\text{eq}}}{R_{\text{eq}} + r_{\text{DS,P}}}$, $LG_{\text{DC}} = A_{\text{EA}} A_{\text{M}_\text{P}} \beta$ is the loop gain of the LDO at DC, $\text{A}_{\text{EA}}$ is the voltage gain of the EA, while $\text{A}_{\text{M}_\text{P}}$ is the voltage gain of the pass transistor and can be written as

$$A_{\text{M}_\text{P}} = g_{\text{m}_\text{P}} R_{\text{OUT}} = g_{\text{m}_\text{P}} \cdot R_{\text{L}} || (R_{\text{F1}} + R_{\text{F2}}) || r_{\text{DS,P}}. \tag{4.23}$$

$A_{\text{EA}}$ can be written as

$$A_{\text{EA}} = g_{\text{m}} r_{\text{O,EA}} = 0.5 \frac{g_m}{I_{\text{Q}}} V_{\text{a}} L_1. \tag{4.24}$$

Consequently, the length of the error amplifier devices to satisfy the PSR requirement can be calculated by

$$L_1 > \frac{2SM}{\frac{g_m}{I_{\text{Q}}} \cdot V_a \cdot \beta \cdot A_{\text{M}_\text{P}} \cdot PSR} \tag{4.25}$$

By considering PSR = -40 dB, and the relevant parameters calculated in the previous sub-sections, the minimum length of the transistors in the error amplifier should be 280 nm.

### 4.3.5 Verification

To verify the guidelines developed in the previous sub-sections, an LDO has been designed accordingly, and its simulation results are compared with the requirements and calculations. Table 4.1 reports the component values used in the simulations.

Fig. 4.4 (a) shows the magnitude and the phase of the open-loop transfer function. The location of the dominant pole, $f_{\text{D}} \sim 10\,\text{MHz}$, and non-dominant pole, $f_{\text{ND}} \sim 4\,\text{GHz}$, are in close accordance with the calculated values, leading to a phase margin of $\sim 60^\circ$. Fig. 4.4 (b) shows the closed-loop transfer function from $V_{\text{ref}}$ to $V_{\text{OUT}}$ normalized to $1/\beta$. This shows that, for frequencies below $f_{\text{ND}}$, any noise at the input of the error amplifier appears at its output without being filtered, proving that the noise generated by the feedback resistors and the error amplifier plays an important role and should therefore be minimized.

Fig. 4.5 (a) shows the simulated output noise of the LDO versus frequency. The noise floor is $< 38\,\text{nV}/\sqrt{\text{Hz}}$, which is in line with the calculations, thereby satisfying the requirements. If this requirement is not met, the phase noise of the oscillator would be degraded, as shown in Fig. 4.6, where external white noise of $80\,\text{nV}/\sqrt{\text{Hz}}$ is added to its supply. From Fig. 4.5 (a), we can see that the output noise of the LDO begins to be filtered at $f > 200\,\text{MHz}$. This is not expected, as the output noise is filtered only at frequencies above the non-dominant pole, which from Eq. 4.19 (and confirmed by Fig 4.4 (a)) is at $\sim 4\,\text{GHz}$. This discrepancy is to be attributed to a wrong setup of the test-bench used in this simulation.

Fig. 4.5 (b) shows the simulated PSR of the LDO. The PSR hump $\sim -1.5\,\text{dB}$, which is close to the predicted value of PSR = 0.5 = -3dB. The frequency of the hump should be located around the unity gain frequency, which from Fig. 4.4(a) is $\sim 110\,\text{GHz}$. However, from Fig. 4.5 (b) we can see that the frequency of the hump is around 200 MHz. Therefore, there is a discrepancy between the calculated and the expected results and it should be attributed to a wrong setup of the test-bench used in this simulation. At frequencies below the dominant pole (i.e., $f_{\text{D}} \approx 10\,\text{MHz}$), the PSR is

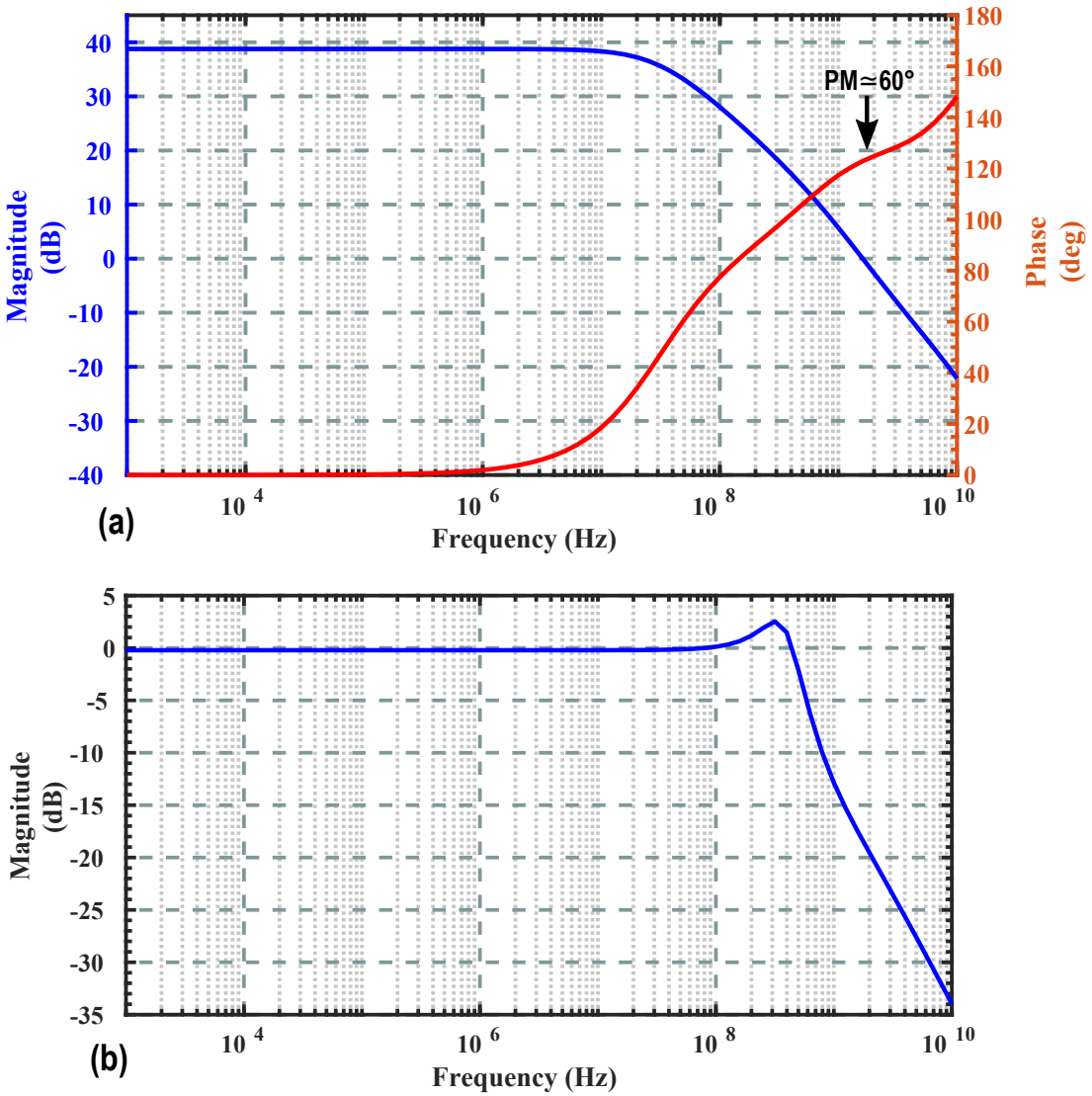



Figure 4.4: (a) Open-loop transfer function of the LDO and (b) its transfer function from $V_{\text{ref}}$ to $V_{\text{OUT}}$ normalized to $1/\beta$.

$\sim -40\,\text{dB}$, which is in line with Eq. (4.22). In the simulation, the efficiency degradations due to $I_{\text{res}}$, $I_{\text{Q}}$, and $V_{\text{OD}}$ are $\frac{1}{0.92}$, $\frac{1}{0.87}$ and $\frac{1}{0.89}$, respectively, leading to a total power efficiency of 71%. Those values are in agreement with our analysis.

## 4.4 Top-Level Power Management Strategy Using LDOs

In a complex System-on-Chip (SoC), there might be some noise coupled to the output of the LDO due to the activity of other aggressor modules. In this section, its side effects on the LDO's input and output voltages are investigated. Fig. 4.7 (a) shows the equivalent small-signal representation of the LDO. It is assumed that the LDO is powered by a battery, the output resistance of which is

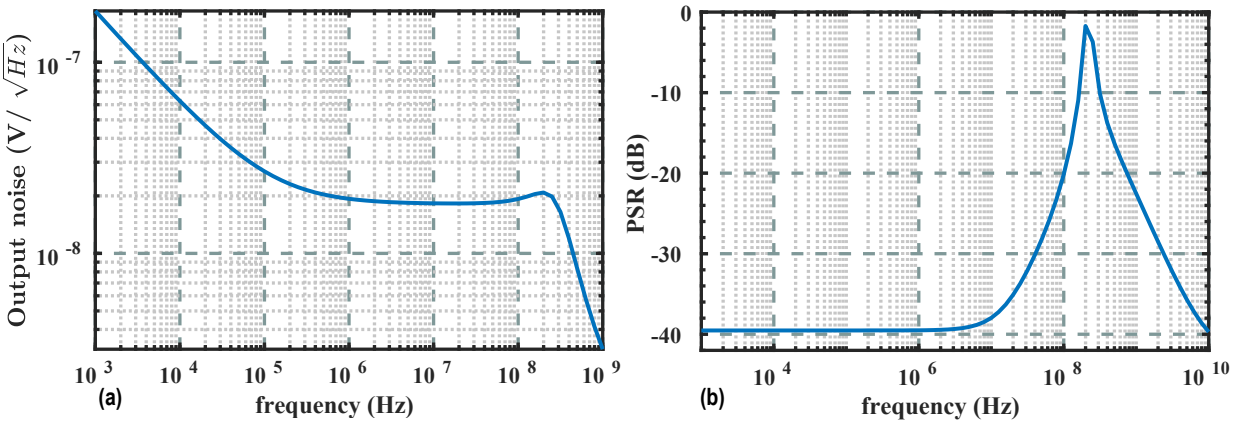



Figure 4.5: (a) Simulated output noise and (b) PSR of the LDO using the component values reported in Table 4.1.

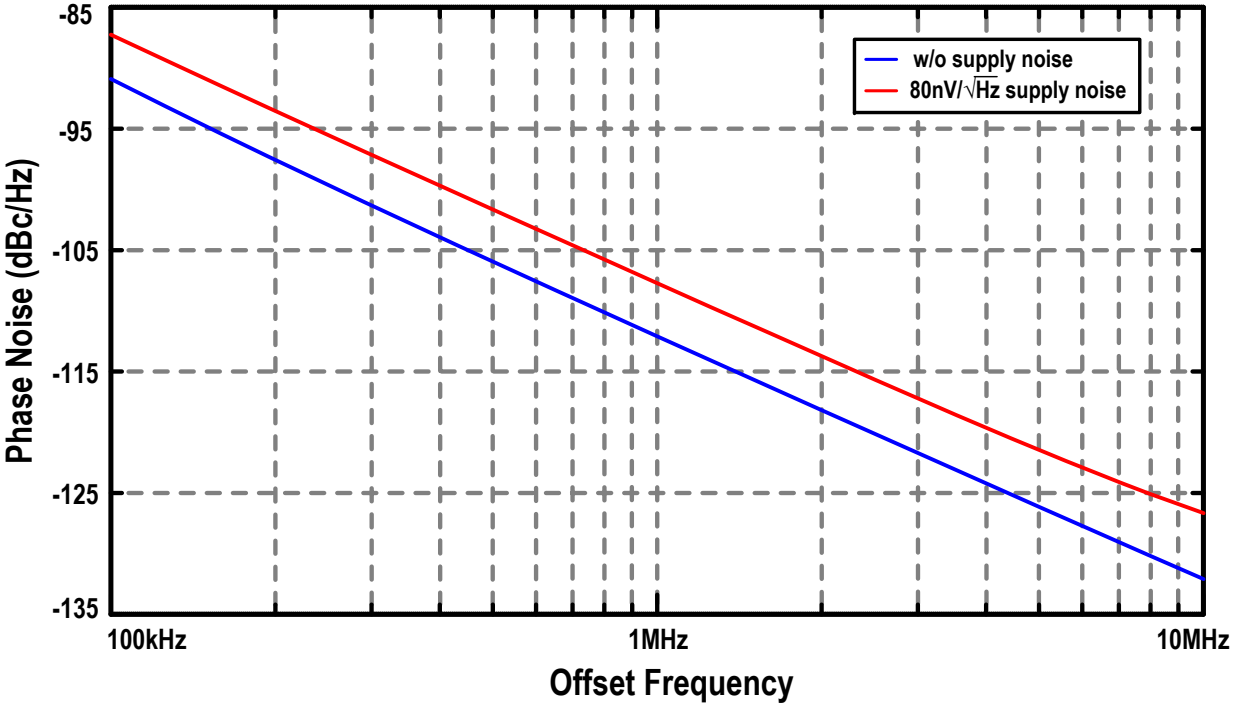



Figure 4.6: Simulated phase noise degradation of the LC oscillator when its supply noise exceeds the value estimated by Eq. (4.8).

$R_S$. When a noise current, $i_n$, is injected at the output of the LDO, the input current $i_{n,in}$ can be written as:

$$i_{n,in}(s) = \frac{g_{m_P}}{1 + g_{m_P} R_S} A(s)\beta v_{n,out}(s). \tag{4.26}$$

With the aid of Kirchhoff's current law at the output node, voltage $v_{n,out}$ can be expressed as

$$v_{n,out}(s) = \frac{i_n Z_L (1 + g_{m_P} R_S)}{1 + g_{m_P} R_S + g_{m_P} Z_L A(s)\beta}. \tag{4.27}$$

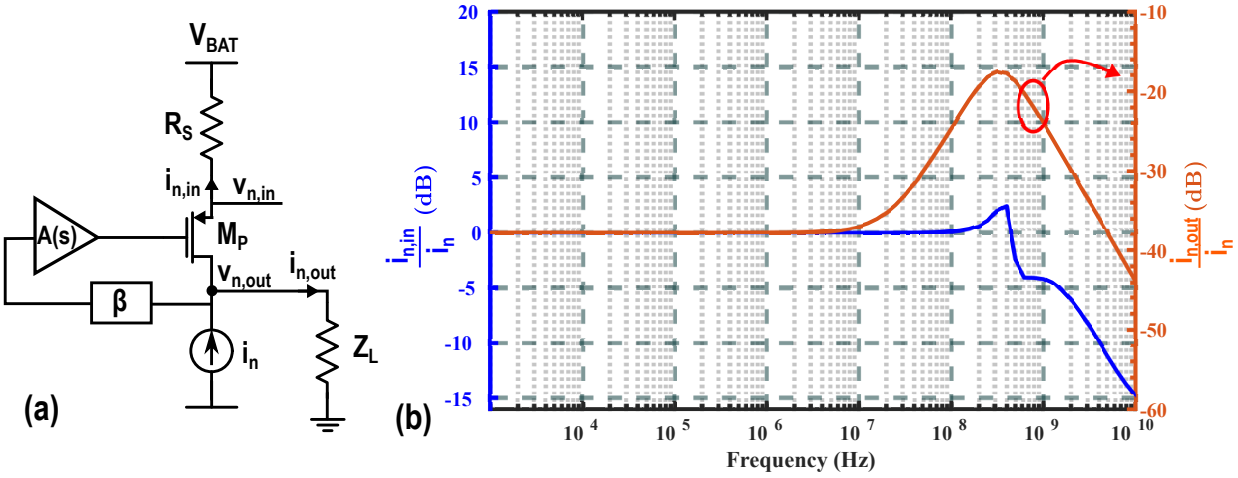



Figure 4.7: (a) Equivalent small-signal circuit of the LDO with (b) its simulated transfer functions from $i_{\mathrm{n}}$ to $i_{\mathrm{n,in}}$ and $i_{\mathrm{n,out}}$ when $R_{\mathrm{S}} = 2\,\Omega$.

The transfer function from $i_{\mathrm{n}}$ to $i_{\mathrm{n,in}}$ can be written as

$$\frac{i_{\mathrm{n,in}}}{i_{\mathrm{n}}}(s) = \frac{g_{\mathrm{mP}} A(s) \beta Z_{\mathrm{L}}}{1 + g_{\mathrm{mP}} R_{\mathrm{S}} + g_{\mathrm{mP}} Z_{\mathrm{L}} A(s) \beta}, \tag{4.28}$$

where $g_{\mathrm{mP}} A(s) \beta Z_{\mathrm{L}}$ is the open-loop gain (LG) of the LDO, which is much larger than $g_{\mathrm{mP}} R_{\mathrm{S}}$ and 1 for frequencies below the dominant pole. Hence, at low frequencies, Eq. (4.28) can be approximated as

$$\frac{i_{\mathrm{n,in}}}{i_{\mathrm{n}}}(s) \sim 1. \tag{4.29}$$

Eq. (4.29) indicates that the injected current noise directly appears at the input, and is then converted into voltage noise by resistor $R_{\mathrm{S}}$. Similarly, due to $i_{\mathrm{n}}$, the current noise flowing to the LDO's load ($i_{\mathrm{n,out}}$) can be expressed as

$$\frac{i_{\mathrm{n,out}}}{i_{\mathrm{n}}}(s) = \frac{1 + g_{\mathrm{mP}} R_{\mathrm{S}}}{1 + g_{\mathrm{mP}} R_{\mathrm{S}} + LG}. \tag{4.30}$$

At frequencies lower than the dominant pole, $LG \gg 1 \gg g_{\mathrm{mP}} R_{\mathrm{S}}$. Hence, Eq. (4.30) can be simplified to

$$\frac{i_{\mathrm{n,out}}}{i_{\mathrm{n}}}(s) = \frac{1}{LG_{\mathrm{DC}}}. \tag{4.31}$$

As such, the LDO attenuates any noise injected at its output by the loop gain.

Fig. 4.7 (b) illustrates the simulation results related to the injected current noise, $i_{\mathrm{n}}$, at the LDO output with $R_{\mathrm{S}} = 2\,\Omega$ and the LDO parameters as described in Table 4.1. As expected from the above analysis, the LDO does not offer any filtering at $f \leq f_{\mathrm{D}}$, and all the injected noise directly appears at the input. On the other hand, only a small fraction of the injected noise flows through the load. However, for frequencies $f > f_{\mathrm{D}}$, this amount significantly increases due to the reduction

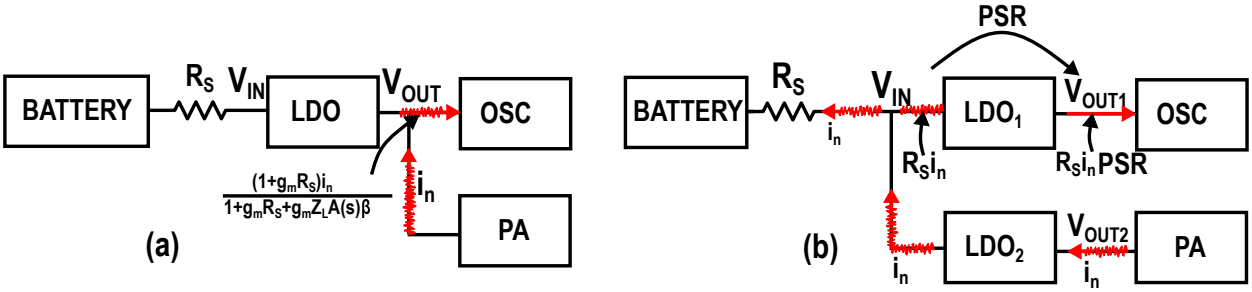



Figure 4.8: Sketch of (a) Scenario 1 in which one LDO is used to supply all the RF blocks and (b) Scenario 2 in which each RF block is powered by a dedicated LDO.

of the EA gain until the output non-dominant pole provides a low impedance path to ground for the noise.

With the insights of the above analysis, there are two different scenarios in which the power management unit of a complex SoC can be organized.

- **Scenario 1: one LDO for all the supplied blocks.** In this scenario, one LDO supplies the current required by the whole system, as shown in Fig. 4.8 (a). If a current noise $i_{\mathrm{n}}$ is injected at $\mathrm{V_{OUT}}$ (e.g., due to the switching activity of the PA), the amount of noise that reaches the oscillator's supply can be predicted by Eq. (4.30) and is equal to

$$i_{\mathrm{n,out}}(s) = i_{\mathrm{n}} \frac{1 + g_{\mathrm{mP}} R_{\mathrm{S}}}{1 + g_{\mathrm{mP}} R_{\mathrm{S}} + g_{\mathrm{mP}} Z_{\mathrm{L}} A(s)\beta}. \tag{4.32}$$

  At low frequencies, the isolation is guaranteed by the loop gain of the LDO. However, at frequencies $f > f_D$, as the loop gain decreases, the noise performance of this topology deteriorates until the noise is being filtered by the output non-dominant pole. To overcome this problem, and to offer the required isolation among the RF blocks, one LDO should be used for each of the supplied circuits, as discussed in the next scenario.
- **Scenario 2: one LDO for each of the supplied blocks.** In this scenario, each of the RF blocks is powered by a dedicated LDO. All the LDOs are connected to the same battery, the output resistance of which is $R_{\mathrm{S}}$, as shown in Fig. 4.8 (b). Any current noise $i_{\mathrm{n}}$ at the output of $\mathrm{LDO_2}$ directly appears at its input and it is converted into voltage noise by resistor $R_{\mathrm{S}}$. The noise can then reach the output of $\mathrm{LDO_1}$, while being attenuated by its PSR. Hence, the total noise at node $\mathrm{V_{OUT_1}}$ can be written as

$$v_{\mathrm{n,out1}} = R_{\mathrm{S}} i_{\mathrm{n}} PSR. \tag{4.33}$$

  As can be deduced from Eq. (4.33), the isolation between the OSC and the PA is guaranteed at frequencies lower than $f_{\mathrm{D}}$. At frequencies between the dominant and the non-dominant pole, $f_{\mathrm{D}} < f < f_{\mathrm{ND}}$, the loop gain of the LDO and its PSR gradually degrade, thereby affecting the noise performance. Therefore, it is important to use a voltage supply with a very low $R_{\mathrm{S}}$ (e.g., a battery) such that the noise at the input of the LDOs can be minimized. At frequencies above the non-dominant pole, the noise is filtered by the parasitic capacitance

at nodes $V_{OUT_1}$ and $V_{OUT_2}$.

## 4.5 Conclusion

This chapter has presented guidelines for designing supply voltage blocks of LC oscillators to preserve their spectral purity. First, the requirements on the ripple and noise of the supply have been quantified. Then an analog LDO was designed to meet those requirements and its power efficiency degradation has been quantified. Given the poor LDO power efficiency, in the next chapter another supply block that is also powered from a fixed input to provide a fixed output voltage will be analysed and used as a supply block for an LC oscillator.

Chapter

# 5

# Analysis, Design and Implementation of a 2:1 or 3:2 Switched-Capacitor DC-DC Converter to Power up LC Oscillators

Given the clear disadvantages in terms of area, output noise and efficiency of an LDO-based approach, in this chapter an alternative solution is proposed. A 2:1 or 3:2 reconfigurable switched-capacitor (SC) DC-DC converter directly powers up an LC oscillator[1].

In Section 5.1, a power efficiency and noise analysis of a 2:1 and 3:2 SC DC-DC converter is carried out. A closed-form equation to estimate the output noise of the SC DC-DC converter is derived merely based on its equivalent resistance and capacitance. The insights of this analysis are then used to design an SC DC-DC converter that meets the supply requirements (noise level and ripple amplitude) discussed in Chapter 4. As a result, a new scheme in which a DC-DC converter directly powers up an LC oscillator is presented in Section 5.2. To mitigate the effects of the ripple generated by the DC-DC converter, the biasing network of the oscillator embeds a spur reduction block [29], which reduces its supply sensitivity and therefore the spurs level in its output spectrum. Section 5.3 presents the measurement results as well as a comparison with the state of the art. In Section 5.4, two possible system-level power management solutions using only SC DC-DC converters are analysed, discussed and compared with the LDO-based power management solutions presented in Section 4.4. Finally, this chapter is concluded in Section 5.5.

[1]This chapter has been published in the IEEE Transactions on Circuits and Systems I: Regular Papers [9].

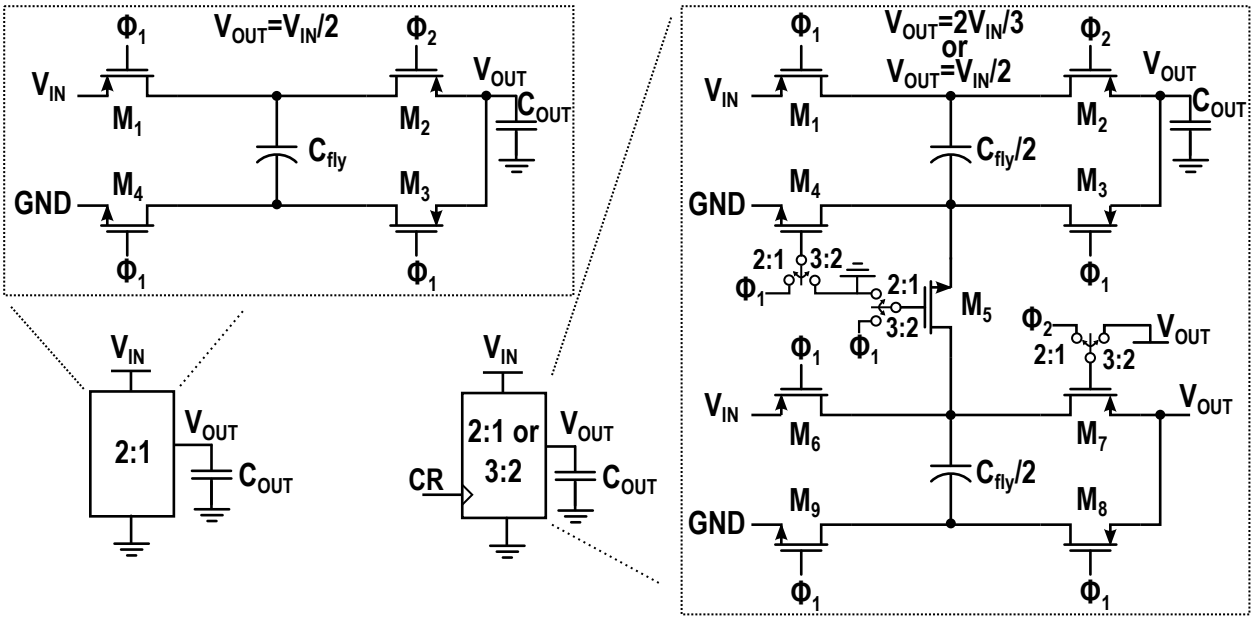



Figure 5.1: Circuit representation of a 2:1 topology (left); and a reconfigurable 2:1, 3:2 switched-capacitor DC-DC converter (right).

## 5.1 DC-DC Converter, Analysis and Design

The left side of Fig. 5.1 shows the circuit representation of a 2:1 switched-capacitor (SC) DC-DC converter. It is made of a charge transfer capacitor, $C_{\text{fly}}$, and four (two PMOS and two NMOS) switches driven by two non-overlapping clock phases, $\phi_1$ and $\phi_2$. Using an energy-conservation analysis, one can express the output voltage, $V_{\text{OUT}} = V_{\text{IN}}/2$ [30].

Two 2:1 stacked topologies are connected by an additional switch, $M_5$, allowing the implementation of a 3:2 topology ($V_{\text{OUT}} = 2V_{\text{IN}}/3$), as shown in the right side of Fig. 5.1. When used in the 2:1 configuration, $M_5$ is always turned off and the two 2:1 topologies are connected in parallel. When used in the 3:2 configuration, switches $M_4$ and $M_7$ are always off and the two flying capacitors are charged in parallel and discharged in series.

### 5.1.1 Power Loss Analysis

Fig. 5.2 (a) shows the equivalent model of an SC DC-DC converter, in which $\text{CR} = \left\{\frac{1}{2}, \frac{2}{3}\right\}$ is the conversion ratio. Its output voltage can be written as

$$V_{\text{OUT}} = V_{\text{IN}} \cdot \text{CR} - R_{\text{S}} \cdot I_{\text{L}}, \tag{5.1}$$

where $R_{\text{S}}$ is the equivalent output impedance of the converter and $I_{\text{L}}$ is the load current.

The key power-loss contributions in an SC DC-DC converter are the switching losses (due to the dynamic operation of the switches) and the conduction losses (due to the output impedance of

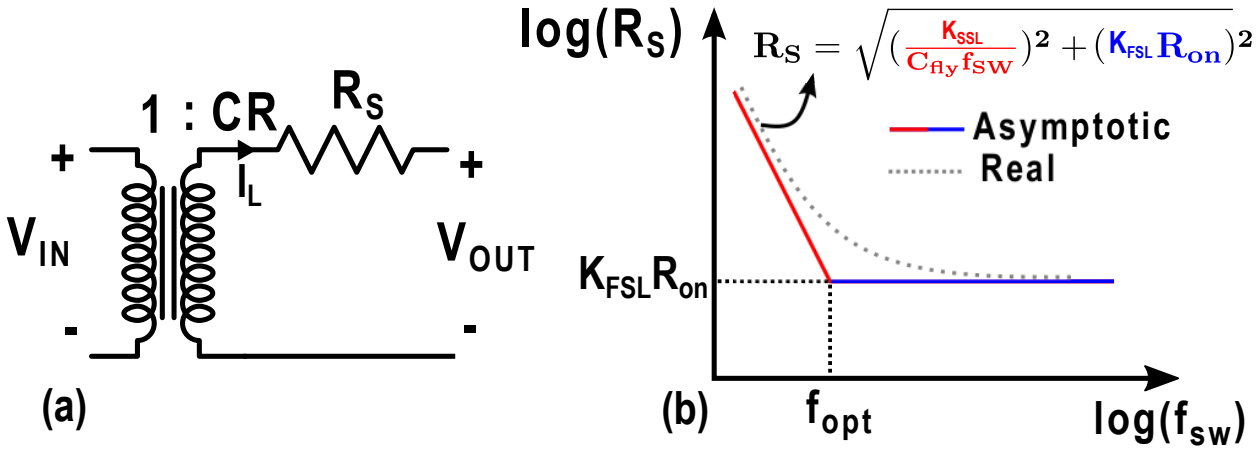



Figure 5.2: (a) Equivalent model of an SC DC-DC converter; and (b) its equivalent output resistance as a function of switching frequency.

the converter). Consequently,

$$P_{\text{LOSS}} = \text{n} C_{\text{g}} V_{\text{sw}}^2 f_{\text{SW}} + R_{\text{S}} I_{\text{L}}^2, \tag{5.2}$$

where n is the number of switches operating at $f_{\text{SW}}$ with a clock voltage swing of $V_{\text{sw}}$, and $C_{\text{g}}$ is the equivalent gate capacitance of each switch. $R_{\text{S}}$ is the converter's output impedance, and can be estimated by [31, 32]

$$R_{\text{S}} = \sqrt{R_{\text{SSL}}^2 + R_{\text{FSL}}^2} = \sqrt{\Big(\frac{K_{\text{SSL}}}{C_{\text{fly}} f_{\text{SW}}}\Big)^2 + (K_{\text{FSL}} R_{\text{on}})^2}, \tag{5.3}$$

where $K_{\text{SSL}} = \{\frac{1}{4}, \frac{2}{9}\}$ and $K_{\text{FSL}} = \{2, \frac{14}{9}\}$ are topology-dependent parameters in the 2:1 and 3:2 topology, respectively. $R_{\text{SSL}}$ and $R_{\text{FSL}}$ are the resistances in the slow (red curve) and fast (blue curve) switching region, respectively (see Fig. 5.2 (b)). To simultaneously reduce the output voltage ripple and maximize the power efficiency, it is required that the converter operates at the boundary of the slow and the fast switching regions. Hence, $R_{\text{S}} = \sqrt{2} K_{\text{FSL}} R_{\text{on}}$, and the contribution of the resistances in the two different regions should be the same, leading to

$$R_{\text{SSL}} = R_{\text{FSL}} \Rightarrow f_{\text{SW}} = f_{\text{opt}} = \frac{K_{\text{SSL}}}{K_{\text{FSL}} C_{\text{fly}} R_{\text{on}}}. \tag{5.4}$$

By substituting the optimum frequency to Eq. (5.2), the power loss can be expressed as

$$P_{\text{LOSS}} = \frac{n \cdot K_{\text{SSL}} \cdot C_{\text{g}} V_{\text{sw}}^2}{K_{\text{FSL}} C_{\text{fly}} R_{\text{on}}} + \sqrt{2} K_{\text{FSL}} R_{\text{on}} I_{\text{L}}^2. \tag{5.5}$$

As can be gathered from this equation, the power loss is a function of $C_g$, and $R_{on}$, which both

Table 5.1: Summary of the DC-DC converter key parameters

| Parameter | 2:1 mode | 3:2 mode |
|---|---|---|
| $\mathbf{W}_{\text{opt}}$ | $160\,\mu m$ | $117\,\mu m$ |
| $\mathbf{P}_{\text{loss}}$ | $150\,\mu W$ | $160\,\mu W$ |
| $\eta$ | 86.9% | 86.2% |

are related to the switch width ($W$). Hence, $P_{\text{LOSS}}$ can be rewritten as

$$P_{\text{LOSS}} = \frac{n \cdot K_{\text{SSL}} \cdot \overline{C_g} V_{\text{sw}}^2 W^2}{K_{\text{FSL}} C_{\text{fly}} \overline{r_{\text{on}}}} + \sqrt{2} K_{\text{FSL}} \frac{\overline{r_{\text{on}}}}{W} I_{\text{L}}^2, \tag{5.6}$$

where $\overline{C_{\text{g}}}$ and $\overline{r_{\text{on}}}$ are the capacitance and on-resistance of a unit-width transistor, respectively. To maximize the power efficiency, Eq. (5.6) should be minimized with respect to $W$, leading to

$$W_{\text{opt}} = \left( \frac{C_{\text{fly}}}{2 \cdot n \cdot K_{\text{SSL}} \cdot \overline{C_{\text{g}}}} \right)^{\frac{1}{3}} \left( \frac{\sqrt{2} K_{\text{FSL}} \overline{r_{\text{on}}} I_{\text{L}}}{V_{\text{SW}}} \right)^{\frac{2}{3}}. \tag{5.7}$$

Assuming $\overline{r_{\text{on}}} = 5 \cdot 10^3\,\Omega \cdot \mu m$, $\overline{C_{\text{g}}} = 6 \cdot 10^{-15}\,\frac{F}{\mu m}$, $C_{\text{fly}} = 1$ nF, $V_{\text{SW}} = 2$ V and $P_{\text{OUT}} = 1\,mW$ ($V_{\text{OUT}}$=1 V, and $I_{\text{L}} = 1\,mA$), the optimal width is $W_{\text{opt}} = 130\,\mu m$, resulting in $f_{\text{SW}} \sim$ 10 MHz. Table 5.1 reports the optimal switch width, the minimum power loss and the estimated efficiency for the DC-DC converter in the 2:1 and 3:2 configurations, respectively.

It is worth to mention that the power efficiency does not depend upon the delivered output current. As $I_{\text{L}}$ increases, $C_{\text{fly}}$ should also increase accordingly to keep the ripple amplitude constant (see Eq. (4.3)). Consequently, as can be gathered from Eqs. (5.7) and (5.6), $W_{\text{opt}}$ and $P_{\text{LOSS}}$ increase linearly with $I_{\text{L}}$. As a result, both the the power efficiency and $f_{opt}$ remain constant with respect to $I_{\text{L}}$.

### 5.1.2 Noise Analysis

From a noise point of view, a switched-capacitor DC-DC converter can be modeled by the equivalent circuit shown in Fig 5.3 (a). $R_{eq}$ is the equivalent resistance of the switches that are involved in each phase of the conversion. Assuming all the switches have the same $R_{on}$,

$$R_{eq} = \begin{cases} 2R_{\text{on}}, & \text{in } \phi_1 \text{ and } \phi_2 \text{ of the 2:1 mode} \\ 2R_{\text{on}}, & \text{in } \phi_1 \text{ of the 3:2 mode} \\ 3R_{\text{on}}, & \text{in } \phi_2 \text{ of the 3:2 mode} \end{cases} \tag{5.8}$$

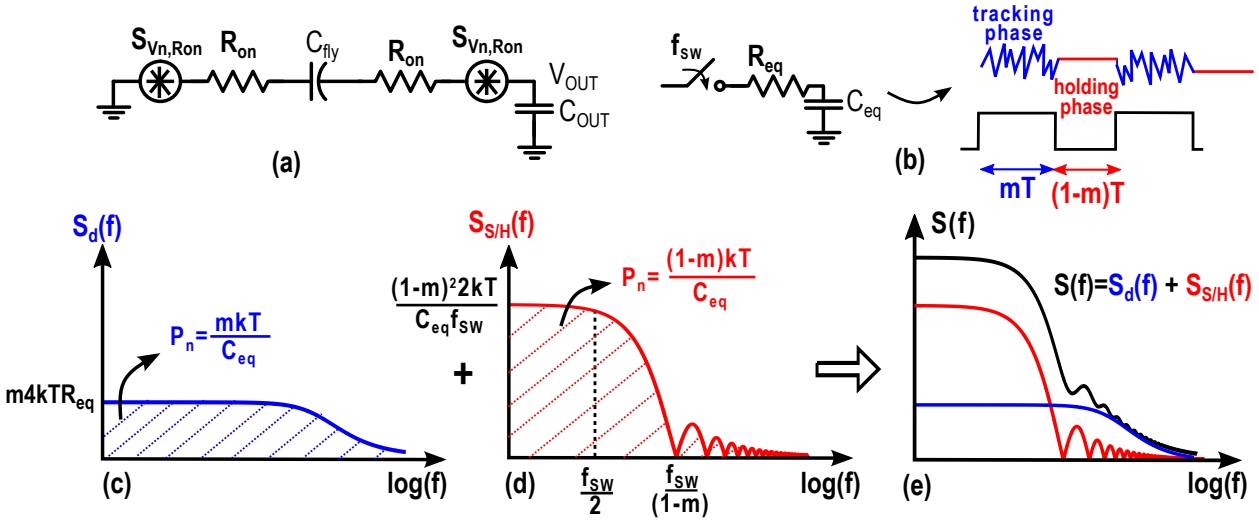



Figure 5.3: (a) Equivalent circuit model for the DC-DC converter in the 2:1 mode (b) output noise waveform during the tracking and the holding phases (c) PSD of the resistor ($R_{\rm eq}$) shaped by the capacitor ($C_{\rm eq}$) during the tracking phase (d) PSD during to the holding phase and (e) a sketch of the total PSD (black line) due to the aliasing of the sampled noise.

On the other hand, the equivalent capacitance can be calculated by

$$C_{eq} = \begin{cases} \dfrac{C_{\rm fly}C_{\rm OUT}}{C_{\rm fly}+C_{\rm OUT}}, & \text{in } \phi_1 \text{ and } \phi_2 \text{ of the 2:1 mode} \\ \dfrac{C_{\rm fly}C_{\rm OUT}}{C_{\rm fly}+2C_{\rm OUT}}, & \text{in } \phi_1 \text{ of the 3:2 mode} \\ \dfrac{C_{\rm fly}C_{\rm OUT}}{4C_{\rm OUT}+C_{\rm fly}}, & \text{in } \phi_2 \text{ of the 3:2 mode.} \end{cases} \tag{5.9}$$

During the tracking phase (blue phase in Fig. 5.3 (b)) the switches, due to their $R_{\rm on}$, produce a noise voltage with a PSD equal to $m4kTR_{\rm eq}$, where $m = 0.5$ is the duty cycle. As can be gathered from Fig. 5.3 (c), the thermal noise generated by the resistors is shaped by $C_{\rm eq}$ with a time constant of $\tau = R_{\rm eq}C_{\rm eq}$. As a result, the PSD of the noise voltage across the equivalent capacitor during the tracking phase can be written as

$$S_{\rm d}(f) = \frac{m4kTR_{\rm eq}}{1+(2\pi f\tau)^2}. \tag{5.10}$$

At the end of tracking phase, the switches are opened and the noise previously sampled is now held on $C_{\rm eq}$ (red phase in Fig. 5.3 (b)). As a consequence, aliasing due to the sampling of the noise occurs [33]. In particular, the noise at frequencies greater than $\frac{f_{\rm SW}}{2}$ is folded back into the 0-to-$\frac{f_{\rm SW}}{2}$ range and adds up to the thermal noise. The PSD due to the aliasing of the sampled noise during the holding phase is sketched in Fig. 5.3 (d). It has a sinc$^2$ shape, and can be written as

$$S_{\rm fol}(f) = (1-m)^2\frac{sin^2[(1-m)\pi f/f_{\rm SW}]}{[(1-m)\pi f/f_{\rm SW}]^2}\frac{2kT}{C_{\rm eq}f_{\rm SW}}. \tag{5.11}$$

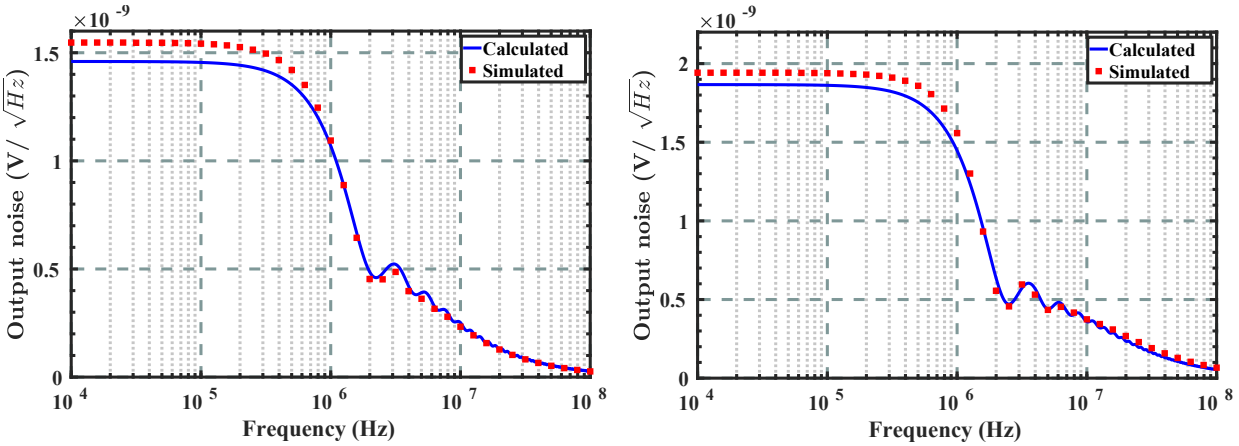



Figure 5.4: Calculated (solid line) and simulated (dotted line) output noise of the DC-DC converter for the (a) 2:1 and (b) 3:2 configurations with $C_{\text{fly}} = 1\,\text{nF}$, $C_{\text{OUT}} = 1\,\text{nF}$, $R_{on} = 30\,\Omega$ and $f_{\text{SW}} = 1.25\,\text{MHz}$.

If the bandwidth of the equivalent circuit ($BW = \dfrac{1}{2\pi R_{\text{eq}} C_{\text{eq}}}$) is larger than $f_{\text{SW}}/2$, the summation of all the folded noise leads to a flat PSD over the 0-to-$\dfrac{f_{\text{SW}}}{2}$ range with an amplitude that is $\left(\dfrac{(1-m)^2}{m}\dfrac{\pi BW}{f_{\text{SW}}}\right)$ times higher than the PSD of the switches' resistance itself [33, 34], as illustrated in Fig. 5.3 (d). In this region, the PSD of the converter is dominated by $\dfrac{2kT(1-m)^2}{C_{\text{eq}} f_{\text{SW}}}$, thus further reducing $R_{\text{on}}$ would increase the switching losses of the converter without improving the noise performance. However, at frequencies between $\dfrac{f_{\text{SW}}}{2}$ and $BW$, the noise due to aliasing starts to fade out and the total PSD is dominated by the thermal noise of the equivalent resistance. At frequencies greater than $BW$, the noise due to $R_{\text{eq}}$ is filtered by the equivalent capacitor.

Since the noise across $C_{\text{eq}}$ is uncorrelated during phases $\phi_1$ and $\phi_2$ of the converter, their PSDs should be added together. Hence, the total output-referred, single-sided PSD can be written as

$$S(f) = A_{\text{V}}^2 \Big( S_{d\phi_1}(f) + S_{d\phi_2}(f) + S_{fol\phi_1}(f) + S_{fol\phi_2}(f) \Big), \tag{5.12}$$

where $S_{d\phi_1}(f)$, $S_{d\phi_2}(f)$, $S_{fol\phi_1}(f)$ and $S_{fol\phi_2}(f)$ are the PSD due to the direct and the folded noise during $\phi_1$ and $\phi_2$. $A_{\text{V}}$ is a scaling factor for referring the noise to the output and can be calculated by

$$A_{\text{V}} = \frac{C_{\text{eq}}}{C_{\text{OUT}}}. \tag{5.13}$$

### 5.1.3 Verification

The noise of a DC-DC converter with $C_{\text{fly}} = 1\,\text{nF}$, $C_{\text{OUT}} = 1\,\text{nF}$, $f_{\text{SW}} = 1.25\,\text{MHz}$ and $R_{\text{on}} = 30\,\Omega$ has been simulated in Cadence by means of a Pnoise simulation. As shown in Fig. 5.4, the simulation results are in close accordance with the predicted values of Eq. (5.12) for the 2:1 and 3:2 configurations. At any frequency, the noise of the DC-DC converter is well below the noise

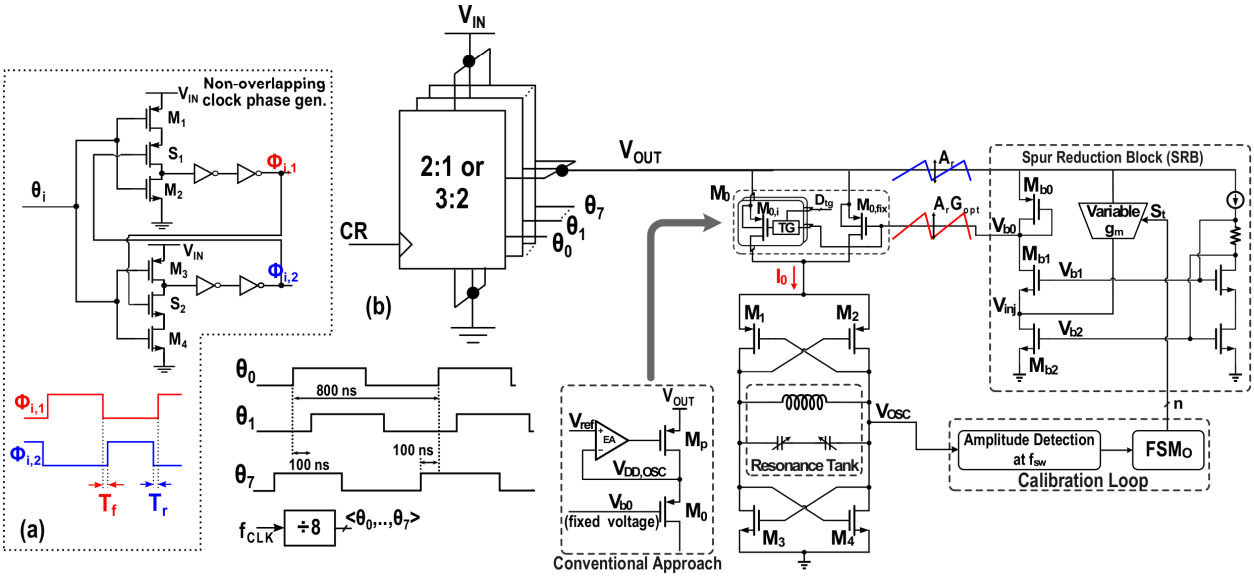



Figure 5.5: (a) Schematic of the non-overlapping phase generator; (b) System-level representation showing the 2:1 or 3:2 reconfigurable SC stage directly connected to the oscillator.

voltage tolerated by an LC oscillator (e.g., from Eq. (4.8), $V_{\mathrm{n,supply}} \leq 38\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ for an oscillator with FOM $= 190\,\mathrm{dBc/Hz}$, $K_V = 40\,\mathrm{MHz/V}$, $f_0 = 5\,\mathrm{GHz}$ and $P_{\mathrm{DC}} = 1\,\mathrm{mW}$).

## 5.2 System-Level Design

With the insights of the above analysis a new scheme is proposed, in which the DC-DC converter directly powers up the LC oscillator.

### 5.2.1 DC-DC Converter Design

The DC-DC converter consists of a 2:1 or 3:2 stage, as discussed in the previous section. The stage is divided into 8 smaller units driven by 8 interleaved phases ($\Phi_0, .., \Phi_7$), as shown in Fig. 5.5 (b). The total on-chip capacitance $C_{\mathrm{fly}} = 1\,\mathrm{nF}$ is equally divided into the 8 units, while each switch has a width of $\sim \frac{W_{\mathrm{opt}}}{8}$ and is operated at $f_{SW} = \frac{f_{\mathrm{CLK}}}{8} = 1.25\,\mathrm{MHz}$, as discussed in the previous section. The practical implementation of this technique comes at the expense of circuit overhead due to the generation and routing of all the different phases. From circuit simulations, 8 interleaving units are found to be the best trade-off between circuit overhead and benefits coming from the interleaving technique. By implementing an interleaved converter, the output capacitance $C_{\mathrm{OUT}}$ can be omitted, as each unit sees a load capacitance equal to the flying capacitance of the four units operated in the opposite phase. In [35], the benefits of adopting such an interleaving technique are further discussed.

Each unit generates two non-overlapped clock phases, $\phi_1$ and $\phi_2$ directly from $\varphi_i$. To ensure the non-overlapped condition between $\phi_1$ and $\phi_2$, each of the 8 units embeds a non-overlapping circuit, whose schematic is shown in Fig. 5.5 (a). To quantify the non-overlapping time, $T_{\mathrm{f}}$ ($T_{\mathrm{r}}$) is defined as the time difference between the falling (rising) edge of $\phi_1$ ($\phi_2$) and the rising (falling)

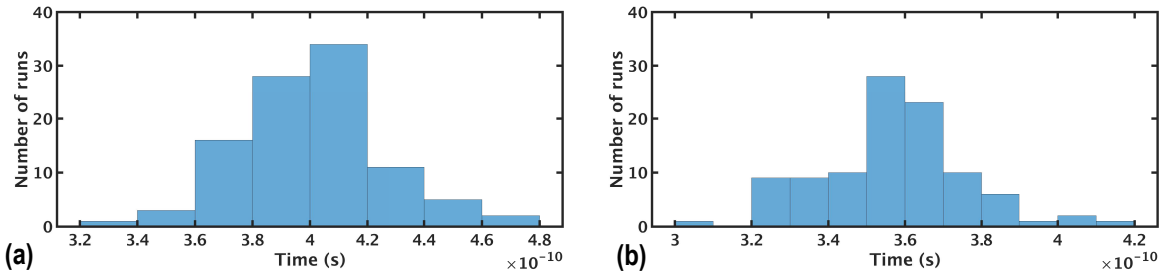



Figure 5.6: Monte Carlo simulations (100 runs) of the non-overlapping time between $\Phi_1$ and $\Phi_2$ (a) for the rising ($T_\mathrm{r}$), and (b) for the falling event ($T_\mathrm{f}$).

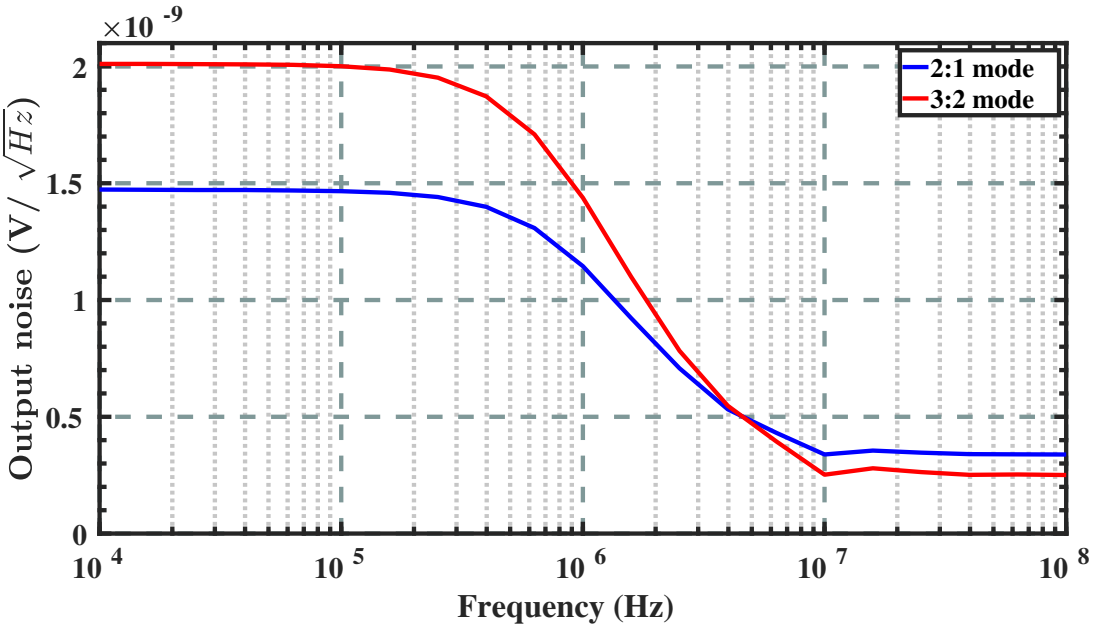



Figure 5.7: Simulated output noise of the 8-unit interleaving converter for the two different configurations.

edge of $\phi_2$ ($\phi_1$). By adding switches $S_1$ and $S_2$, which are directly driven by $\phi_2$ and $\phi_1$, each phase of the clock can change state only when the other phase has already switched, thus guaranteeing the non-overlapping condition. To guarantee that the non-overlapping condition is satisfied over process variation and device mismatch, a Monte-Carlo simulation with 100 points has been performed, and the results are shown in Fig. 5.6. Both $T_\mathrm{r}$ and $T_\mathrm{f}$ are always greater than zero, proving that the non-overlapping condition is met.

Fig. 5.7 shows the simulated output noise of the interleaved DC-DC converter in the 2:1 and 3:2 mode. The output noise of the converter is always below the noise requirement derived in Section 4.2 (i.e., $< 38\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$), thereby preserving the oscillator inherent PN.

### 5.2.2 Spur Reduction Block Design

Fig. 5.5 (b) shows the block diagram of the oscillator with its spur-reduction block (SRB), which is based on [29]. In the conventional LDO-based approach, the tail transistor, $M_0$, which is used to adjust the DC level of the oscillator current, $I_0$, is placed in cascade with the pass transistor of the LDO, $M_p$, the function of which is to stabilize the internal supply voltage of the oscillator. By removing the LDO, the source terminal of $M_0$ is now directly connected to the DC-DC converter output, and the voltage headroom required by $M_p$ is avoided. In this design, $M_0$ also contains a bank of unit transistors $M_{0,i}$ that can be switched on separately through the corresponding transmission gate (TG, which are driven by the corresponding control signals $D_{tg}$) to set the DC level of $I_0$ for optimum oscillator performance. As shown in [29], $I_0$, and the corresponding oscillation amplitude, $V_{osc}$, should be stabilized to reduce the oscillator's supply pushing, since the variation of the oscillation frequency mainly stems from the variation of the equivalent value of the voltage-dependent parasitic capacitance of the core transistors. To accomplish this, a conventional oscillator biasing network is modified into the SRB with only $20\,\mu$A extra power consumption. The SRB replicates the supply ripple to the gate terminal of $M_0$ with a proper gain G, in order to stabilize $I_0$ under supply variation. To account for the finite output resistance of $M_0$, the gain of the replica is properly tuned by varying the control code of the variable $g_m$ stage. The optimal code, $G_{opt}$, is automatically found with the on-chip calibration loop that sweeps the control code using an FSM ($FSM_O$). For each control code setting, the amplitude detector estimates the variation of the oscillation amplitude at $f_{SW}$. Once the monitored oscillation amplitude variation at $f_{SW}$ reaches its minimum, $FSM_O$ fixes the corresponding gain as $G_{opt}$. Such a calibration process is only performed at the system start-up, and the same calibrated $G_{opt}$ is used for the rest of the operation. For good enough spur suppression, it is required that the replicated ripple has very low phase shift with respect to the supply ripple. Therefore, the bandwidth of the single-pole SRB is chosen to be much larger than $f_{SW}$ (i.e., $SRB_{BW} \sim 200\,$MHz). At lower $f_{SW}$, the oscillator inherently suffers from a lower spur suppression due to a higher tank impedance, requiring tighter $I_0$ variations and higher gain resolution. Since the SRB is fully integrated into the oscillator biasing network, only the noise of its extra variable $g_m$ stage degrades the oscillator PN by a negligible amount (i.e., $\sim$0.06 dB). Moreover, the current consumed by the SRB is only $20\,\mu A$, which leads to a current efficiency of 98%. A more detailed description of the SRB can be found in [29].

## 5.3 Experimental Results and Comparison

The DC-DC converter and the oscillator have been fabricated in the same standard 40-nm CMOS process. Their chip micrographs, as well as a photo highlighting their direct connection, are shown in Fig. 5.8. The two circuits occupy an active area of $0.6\,\text{mm}^2$ and $0.23\,\text{mm}^2$, respectively. The $f_{CLK} = 10\,$MHz clock signal of the DC-DC converter is provided externally, while the 8 phases at $f_{SW} = 1.25\,$MHz are generated on chip.

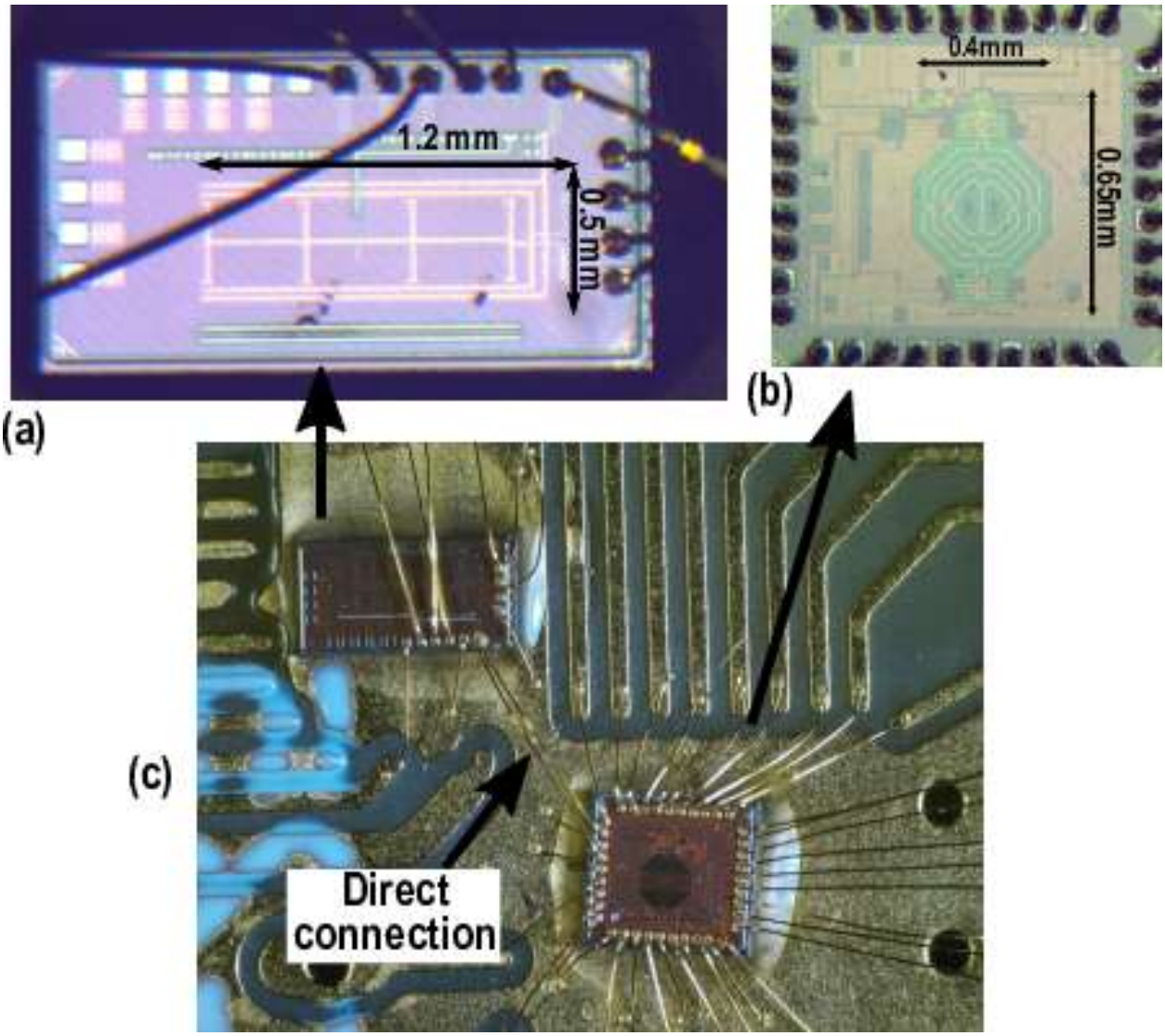



Figure 5.8: Chip micrographs of (a) the DC-DC converter, and (b) the oscillator; (c) A photo highlighting their direct connection.

### 5.3.1 Measurement Results

In Fig. 5.9 (a), the simulated and the measured power efficiency of the DC-DC converter in the two configurations and for different $V_{\mathrm{IN}}$ values are shown. The average currents needed to compute the power efficiency have been measured with a Keithley 6430 source-meter. The peak power efficiency is $\sim 83\%$ and $\sim 81\%$ for the 2:1 and the 3:2 mode, respectively. In the 3:2 mode, the output impedance of the converter increases, degrading the power efficiency, as predicted by Eq. (5.6). The overdrive voltage of the switches is proportional to $V_{\mathrm{IN}}$. As a consequence, at lower values of $V_{\mathrm{IN}}$, the $R_{\mathrm{on}}$ of the switches increases and therefore the power efficiency tends to degrade. Fig. 5.9 (b) shows the DC-DC converter output voltage waveform in the 2:1 mode, while powering up the oscillator. The ripple frequency equals the converter's switching frequency (i.e., 10 MHz),

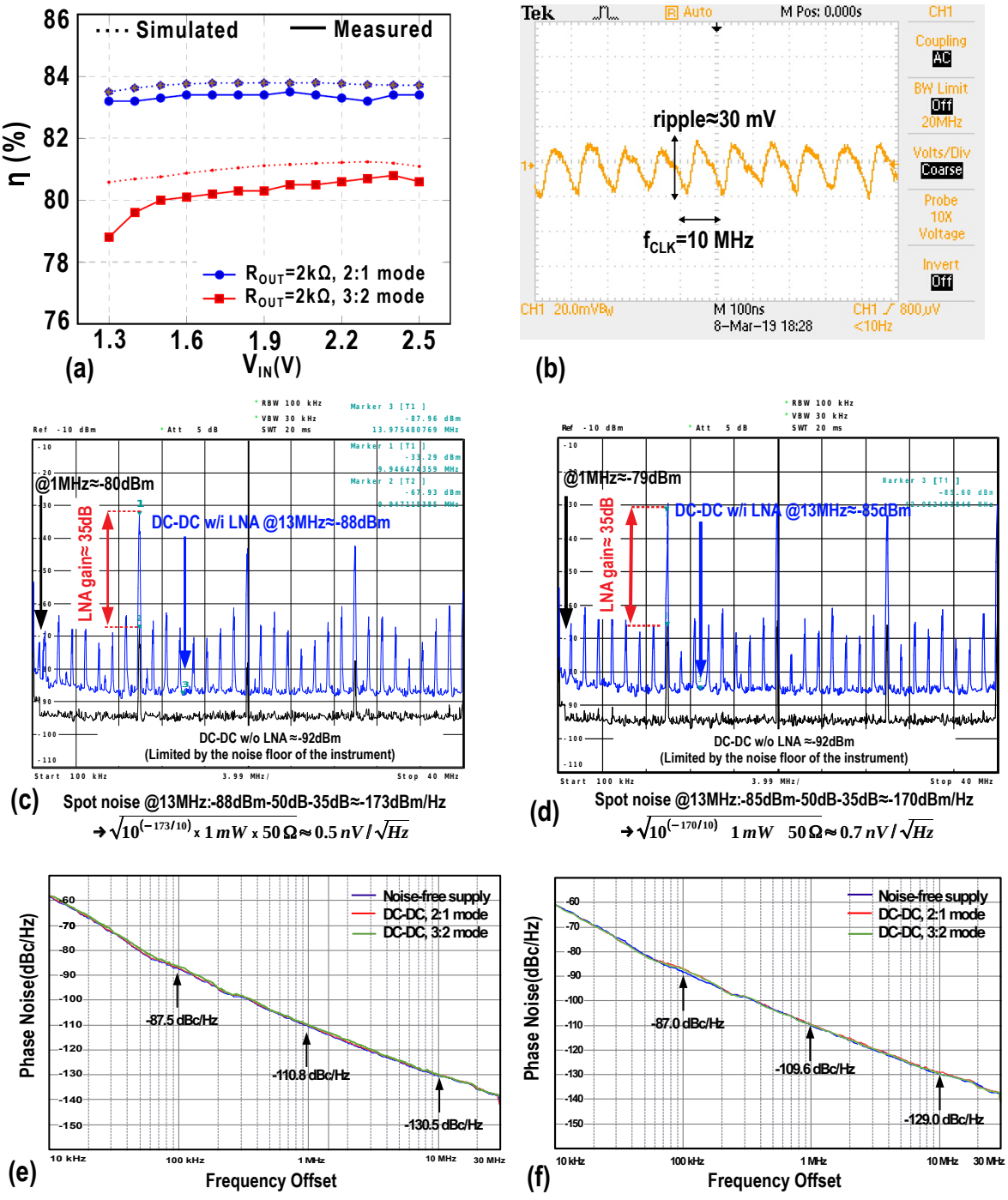



Figure 5.9: (a) Measured power efficiency versus $V_{IN}$; (b) output voltage of the DC-DC converter when directly connected to the oscillator; (c) spectrum of the output voltage of the DC-DC converter with (blue line) and without (black line) the use of an LNA in the 2:1 mode and (d) the 3:2 mode; (e) phase noise of the oscillator when powered by an ideal supply and the DC-DC converter in the 2:1 mode and 3:2 mode for $f_0 = 5.56\,\text{GHz}$ and (f) $f_0 = 4.9\,\text{GHz}$.

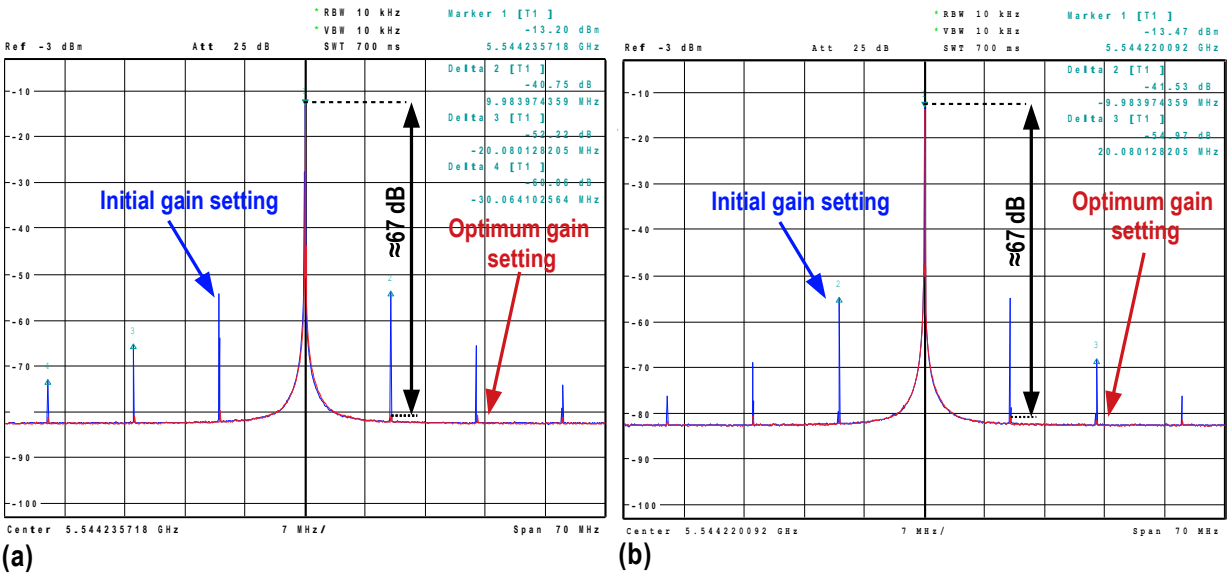



Figure 5.10: Oscillator spectrum before and after calibration when directly powered from the DC-DC converter in 2:1 (a) and 3:2 mode (b).

while the ripple amplitude is $\sim 30\,\text{mV}$.

The spectrum of the output voltage of the DC-DC converter is shown in Fig. 5.9 (c) and (d) (black line) for the 2:1 and 3:2 configurations, respectively. The main tones are located at multiple integers of $f_{\text{CLK}}$, whereas the frequency components due to the interleaving technique are located at multiple integers of $f_{\text{CLK}}/8 = 1.25\,\text{MHz}$. Those components are much smaller than the main tones, hence they do not appear in the spectrum of the oscillator, as the SRB will greatly suppress them. The measurement of the output noise of the DC-DC converter is limited by the noise floor of the spectrum analyzer. Hence, a Low-Noise Amplifier (LNA) with a gain of 35 dB is placed after the DC-DC converter. The resulting spectrum is shown in Fig. 5.9 (c) and (d) (blue curve) for the 2:1 and the 3:2 configuration, respectively. When the LNA is used, the amplitude of the peaks is amplified by 35 dB, whereas the noise is amplified by only 7 dB (in the 3:2 mode), proving that the measurement is not longer limited by the noise floor of the spectrum analyzer. At around 13 MHz, the measured noise in the 2:1 configuration integrated over the resolution bandwidth of the spectrum analyzer (100 kHz) is $\approx -88\,\text{dBm}$. As a result, the spot noise at around 13 MHz is $-88\,\text{dBm} - 35\,\text{dB} - 10log_{10}(100kHz) = -173\,\text{dBm/Hz} \approx 0.5\,\text{nV}/\sqrt{\text{Hz}}$. It is in close accordance with the simulated value (Fig. 5.7), and much lower than the supply noise tolerated by the oscillator ($38\ nV/\sqrt{Hz}$ @ 10 MHz).

Fig. 5.9 (e) and (f) show the phase noise of the oscillator when powered from a noise-free supply and from the DC-DC converter in the two different configurations for the oscillator frequencies of 5.56 GHz and 4.9 GHz, respectively. The inherent PN of the oscillator is not degraded, proving that the condition imposed by Eq. (4.7) is met and the supply does not limit the oscillator performance. The spectrum of the oscillator powered by the converter is also shown in Fig. 5.10. The spur level at the initial gain setting of the SRB, which corresponds to $G \approx 1$, is as high as -40 dBc. After

performing an automatic calibration to find the optimum gain setting, the spur level is reduced by about 27 dB and reaches -67 dBc. It is worth mentioning that 27 dB represents the difference of the spur levels between the initial and optimal gain setting of the SRB, which does not represent the PSR of the SRB.

### 5.3.2 Comparison with the State of the Art

Table 5.2 summarizes the performance of the system and compares it with a conventional LDO-based approach. Since the SRB is always functioning, the equivalent PSR of the proposed approach in this table is calculated by the difference between the spur level measured at the optimum setting and the calculated one based on the simulated $K_{\mathrm{V}}$ of the oscillator without SRB. Compared to [2] and [6], exhibits the lowest PSR without the use of an LDO or any external component, thereby avoiding the LDO voltage headroom while achieving the highest power efficiency. Moreover, the converter achieves the lowest output noise thereby preserving the oscillator phase noise performance. Two independent LDO designs ( [24, 36]) with relatively high PSR are also added to the table of comparison to highlight the advantages of our structure. [24] requires an external output capacitor, making the voltage regulator bulky. [36] employs a cap-less solution with a drop-out voltage of 200 mV, bringing its power efficiency below 80%.

## 5.4 Top-Level Power Management Strategy Using SC DC-DC Converters

Similarly to the approach used in the previous chapter for LDOs, this section investigates the side effects of noise coupled into the output of the DC-DC converter. When a current noise, $i_{\mathrm{n}}$, is injected at the output node of the converter shown in Fig. 5.11 (a), the current noise that reaches the input can be expressed as

$$\frac{i_{\mathrm{n,in}}}{i_{\mathrm{n}}} = CR \cdot \frac{R_{\mathrm{L}}}{R_{\mathrm{L}} + R_{\mathrm{S}} + R_{\mathrm{IN}} \cdot CR^2}. \tag{5.14}$$

Since $R_{\mathrm{L}} \gg (R_{\mathrm{S}} + R_{\mathrm{IN}} \cdot CR^2)$, Eq. (5.14) can be simplified to

$$\frac{i_{\mathrm{n,in}}}{i_{\mathrm{n}}} \approx CR. \tag{5.15}$$

In contrast to the LDO structure, the injected current noise is *firstly* attenuated by CR (e.g., CR = 0.5 or 0.66) when it is referred to the input and then be converted into voltage noise through resistor $R_{\mathrm{IN}}$. Similarly, due to $i_n$, the current noise that flows through the load can be written as

$$\frac{i_{\mathrm{n,out}}}{i_{\mathrm{n}}} = \frac{R_{\mathrm{S}} + R_{\mathrm{IN}} \cdot CR^2}{R_{\mathrm{L}} + R_{\mathrm{S}} + R_{IN} \cdot CR^2} \approx \frac{R_{\mathrm{S}}}{R_{\mathrm{L}}}. \tag{5.16}$$

This equation reveals that the output current noise is also reduced by the converter. However, the attenuation is smaller compared to that of the LDO, where the noise is attenuated by the open-loop

Table 5.2: PERFORMANCE SUMMARY AND COMPARISON WITH STATE OF THE ART

| | | This work | JSSC15 [2] | ESSCIRC14 [6] | JSSC17 [24] | CICC17 [36] |
|---|---|---|---|---|---|---|
| **System Architecture** | | DC-DC+ OSC | LDO+ OSC** | LDO+ OSC | LDO | LDO |
| **CMOS tech** | | 40 nm | 55 nm | 65 nm | 130 nm | 65nm |
| **$V_{IN}$ (V)** | | 2.2@2:1<br>1.65@3:2 | 1.4 | 0.6 | 1.05-2.0 | 1.2 |
| **$V_{OUT}$(V)** | | 1.0 | 1.2 | 0.4 | 1.0 | 1.0 |
| **$C_{OUT}$(F)** | | - | >6p | 390p | 1µ | <240p |
| **Noise (nV/$\sqrt{Hz}$)** | | <0.7@ 13MHz<br>0.9 @1MHz | - | 22.4#@ 10MHz | 100@ 1MHz | - |
| **#ext. components** | | 0 | 0 | 0 | 1 | 0 |
| **η (%)** | | 83@2:1<br>81@3:2 | <80 | <60 | <95 | <80 |
| **LDO voltage headroom (mV)** | | 0 | 200 | 200 | 50 | 200 |
| **PSR (dB)** | **@5MHz** | -48.9* | -20 | -31† | -27† | -48 |
| | **@10MHz** | -45* | -20 | -26† | -33† | -50 |

*PSR of the SRB (simulated value) **Oscillator is part of the whole transceiver

#Calculated from phase noise with $K_{SUP}$=50 MHz/V †Simulated value

gain (see Eq. (4.31)).

Fig. 5.11 (b) shows the simulation results related to the injected current noise at the converter's output. At DC, the simulation results are in close accordance with Eqs. (5.14) and (5.16). For frequencies above 10 MHz, the input-referred noise is gradually being filtered by the on-chip flying capacitance of the converter, whereas the output-referred noise is hardly filtered, as can be gathered from the red curve.

With the insights of the above analysis, a power management unit made by SC DC-DC converters can be organized in the two following scenarios.

- **Scenario 1: One DC-DC converter for all the supplied blocks:** In this scenario, only one DC-DC converter supplies the current required by the whole system, as shown in Fig.5.12 (a). The current noise, $i_n$, injected (e.g., due to the switching activity of the

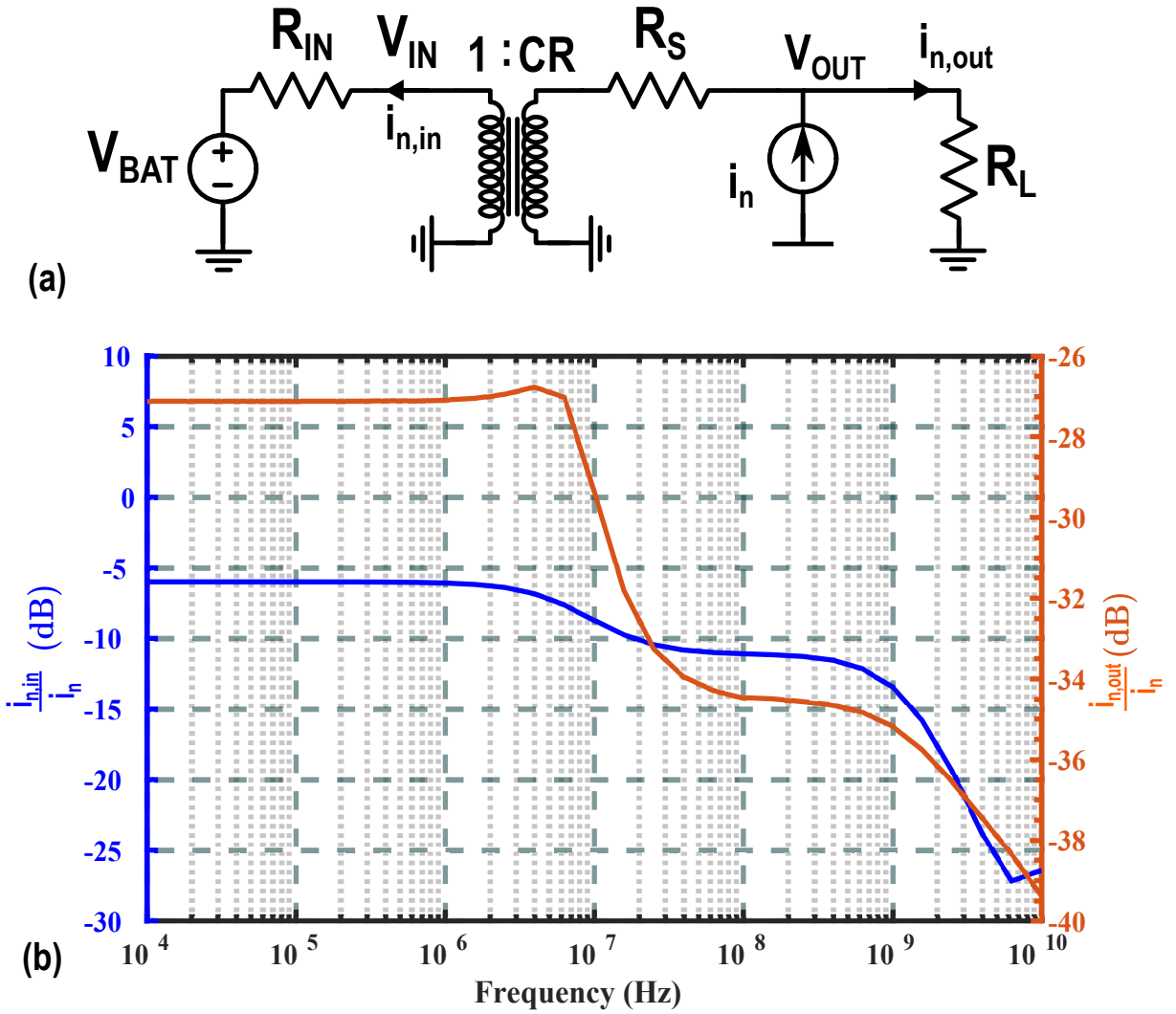



Figure 5.11: (a) Equivalent model of an SC DC-DC converter with the noise current $i_n$ used for the calculation of the transfer function; (b) the simulated transfer functions from $i_{\rm n}$ to $i_{\rm n,in}$ and $i_{\rm n,out}$.

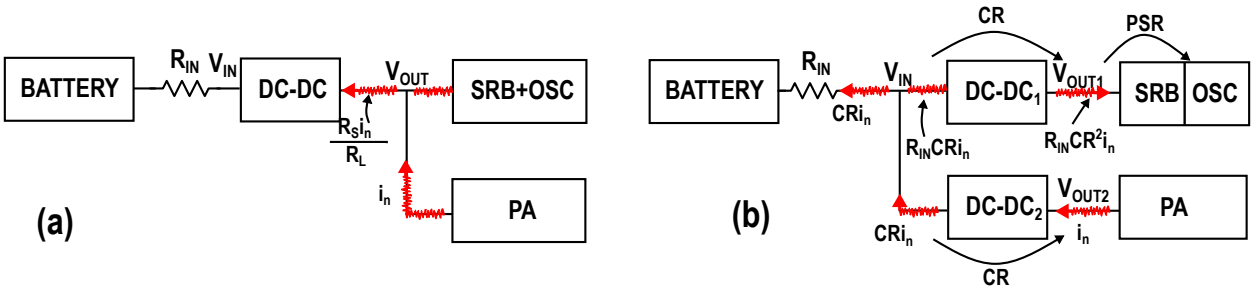



Figure 5.12: Sketch of Scenarios (a) 1 in which one DC-DC converter is used to supply all the RF blocks and (b) 2 in which each RF block is powered by a dedicated DC-DC converter.

PA) reaches the output of the DC-DC converter while being attenuated by $R_{\rm S}/R_{\rm L}$ (see Eq. (5.16)). As we discussed previously, the noise at node $\rm V_{OUT}$ is hardly filtered due to the lack

Table 5.3: Performance summary of the four system-level power management unit scenarios

| **Scenario** | **Topology** | $\mathbf{f < f_D}$ | $\mathbf{f_D < f < f_{ND}}$ |
|---|---|---|---|
| Scenario 1 | One LDO for the whole system | Average | Poor |
| Scenario 2 | One LDO for each block | Good | Average |
| Scenario 1 | One DC-DC for the whole system | Poor | Poor |
| Scenario 2 | One DC-DC for each block | Good | Good |

of output decoupling capacitance in SC DC-DC converters. Hence, this solution, irrespective of the frequency, offers a low degree of isolation at heavy load (low $R_{\mathrm{L}}$).
To overcome this problem, and therefore provide a good degree of isolation among the supplied blocks, a dedicated DC-DC converter for each of the supplied blocks can be used, as discussed in the next scenario.

- **Scenario 2: One DC-DC converter for each of the supplied blocks:** In this scenario, each of the RF blocks is powered by a dedicated SC DC-DC converter designed according to the analysis presented in this chapter. All the DC-DC converters are connected to the same battery, the output resistance of which is $R_{\mathrm{IN}}$, as shown in Fig. 5.12 (b). As predicted by Eq. (5.14), any current noise $i_n$ at the output of DC-DC$_2$ is multiplied by the conversion ratio (CR) (e.g., CR=0.5 or CR=0.66) when referred to its input and converted into voltage noise by the resistance $R_{\mathrm{IN}}$. The voltage noise can then reach the output of DC-DC$_1$, by again being multiplied by CR, leading to a voltage noise at $\mathrm{V_{OUT1}}$ equal to

$$V_{\mathrm{OUT1}} = R_{\mathrm{IN}}\mathrm{CR}^2\mathrm{i_n}. \tag{5.17}$$

From Eq. (5.17) we can see that the factor $\mathrm{CR}^2$ attenuates the noise injected. At frequencies within the bandwidth of the SRB, the noise is further attenuated by the PSR of the SRB, thereby avoiding any degradation of the oscillator spectrum. At frequencies above the SRB bandwidth, the noise is still attenuated by the factor $\mathrm{CR}^2$ while being filtered by the on-chip flying capacitance of the DC-DC converter, as can be seen from Fig. 5.11, the blue curve.

### 5.4.1 Discussion

To summarize and compare the power management strategies using LDOs (presented in Section 4.4) and SC DC-DC converters, Table 5.3 classifies the four topologies based on the amount of isolation offered in a certain frequency range.

Both Scenarios 1 (i.e., one supply block for the whole system) offer very poor performance, and should therefore be avoided. On the other hand, both Scenarios 2 (i.e., a dedicated supply for each block) offer a similar degree of isolation when an energy source with a low $R_{\mathrm{IN}}$ is used. In particular, the solution with a DC-DC converter + SRB offers a slightly better isolation at $f < f_{\mathrm{D}}$ due to the $\mathrm{CR}^2$ factor. At $f > f_{\mathrm{D}}$, the LDO degrades its PSR, thereby degrading the noise performance, while the DC-DC converter begins to filter the noise.

## 5.5 Conclusion

A 2:1 or 3:2 switched-capacitor DC-DC converter is introduced along with its power loss analysis and optimum switch sizing. Moreover, a noise analysis that allows to estimate its output noise merely based on the on-resistance of the switches and the equivalent flying capacitance is presented. As a result of the above-mentioned analysis, and taking into consideration the oscillator's supply requirements discussed in the previous chapter, a new scheme in which the DC-DC converter directly powers up the oscillator is presented. To mitigate the side effects of the ripple generated by the DC-DC converter, the biasing network of the oscillator embeds a spur reduction block that reduces the oscillator's supply sensitivity.

Measurement results show a converter's peak power efficiency of 83%, with an output noise $< 0.9\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 1 MHz which does not degrade the inherent phase noise of the oscillator. The spur reduction block embedded in the oscillator suppresses the spurs induced by the DC-DC converter ripple down to $-67\,\mathrm{dBc}$.

Finally, two possible system-level power management strategies using DC-DC converters are discussed and compared to the LDO-based solutions presented in Chapter 4.

Chapter

# 6

# A Recursive Switched-Capacitor DC-DC Converter to Power up LC Oscillators

The 2:1 or 3:2 SC DC-DC converter presented in the previous chapter, together with an Spur Reduction Block (SRB) can be employed as a replacement of the LDO shown in Fig. 4.1. However, in order to provide a 1-V supply voltage for the oscillator, the input voltage of the 2:1 or 3:2 SC DC-DC converter converter should be a fixed and stable voltage of $V_{\mathrm{IN}} = 2.2\,\mathrm{V}$ for the 2:1 mode and $V_{\mathrm{IN}} = 1.66\,\mathrm{V}$ for the 3:2 mode. To overcome this limitation, and design an SC DC-DC converter that can regulate the output voltage of the storage element (which is the input of the DC-DC converter and can vary over time) while directly powering up the LC oscillator, this chapter presents a recursive switched-capacitor (RSC) DC-DC converter directly connected to the same LC oscillator discussed in the previous chapter (see Fig. 6.1)[1]. To keep the output voltage of the converter ($V_{\mathrm{OUT}}$) relatively constant over $V_{\mathrm{IN}}$ ($1.3\,\mathrm{V} < V_{\mathrm{IN}} < 2.2\,\mathrm{V}$) or $I_{\mathrm{L}}$ ($I_{\mathrm{L}} < 2\,\mathrm{mA}$) variations, a finite-state-machine (FSM)-based conversion ratio (CR) modulation is introduced, which allows having a predictable spectrum of the converter output voltage and facilitate the connection to the oscillator. A gate-driver circuit is embedded in all the switches of the converter and guarantees minimum switch on-resistance across process variations and the entire input voltage range. The converter has been designed to meet the oscillator's supply requirements discussed in Section 4.2.

Section 6.1 derives the requirements on the conversion ratio of the converter and introduces a recursive switched-capacitor (RSC) topology along with an analysis of its output resistance. An FSM-based digital control is introduced, which allows to keep the output voltage of the converter

[1]This chapter has been published in the IEEE Transactions on Circuits and Systems I: Regular Papers [37].

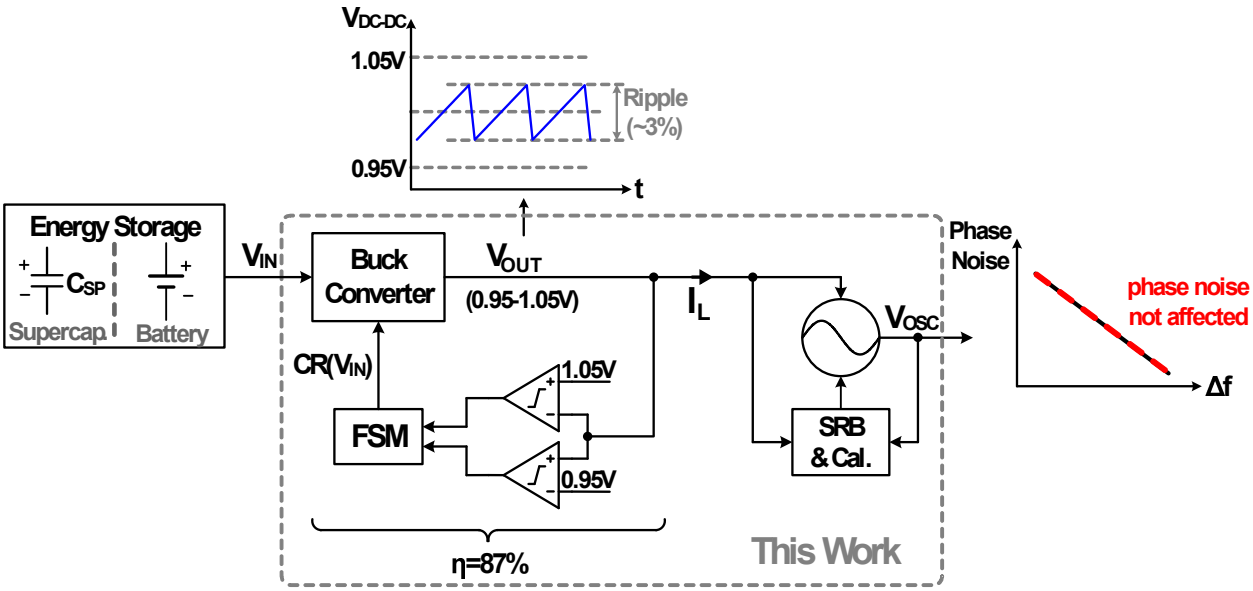



Figure 6.1: Block diagram of the proposed system in which, the DC-DC converter regulates the output voltage of the storage element while providing a constant supply voltage for the oscillator.

within 5% of its nominal value against $V_{\mathrm{IN}}$ or $I_{\mathrm{L}}$ variations. Section 6.2 introduces a gate-driver circuit for the switches, which guarantees a constant switch on-resistance across PVT variations. Section 6.3 presents the measurement results as well as a comparison with the state of the art. This chapter is concluded in Section 6.4.

## 6.1 DC-DC Converter Design

In this section, the required conversion-ratio (CR) range and resolution are derived. A converter topology that meets the CR requirement is then presented along with its output resistance analysis. To continuously adjust the CR, a digital FSM-based control is introduced. Finally, the losses of the resulting converter topology are analysed, to determine the optimal switch sizes.

According to the equivalent model of an SC DC-DC converter shown in Fig. 5.2 (a) the converter's output voltage can expressed as

$$V_{\mathrm{OUT}} = V_{\mathrm{IN}} \cdot \mathrm{CR} - R_{\mathrm{S}} \cdot I_{L}, \tag{6.1}$$

where $R_{\mathrm{S}}$ is the equivalent output resistance of the converter and $I_{\mathrm{L}}$ is the load current. During operation, the CR and/or $R_{\mathrm{S}}$ must be adaptively adjusted for $V_{\mathrm{IN}}$ and $I_{\mathrm{L}}$ variations to keep the output voltage within the $\pm 5\%$ of the oscillator nominal supply voltage (i.e., $V_{\mathrm{OUT}} = 1\mathrm{V}$). $R_{\mathrm{S}}$ can be modulated through the switching frequency ($f_{\mathrm{SW}}$) or the converter capacitance ($C_{\mathrm{fly}}$). However, the former requires to modulate $f_{\mathrm{SW}}$ by several orders of magnitude [38–41], making it difficult for the spur-reduction-block (SRB) circuit embedded in the oscillator to keep the spur level low enough over the entire $f_{\mathrm{SW}}$ range. The latter involves a significant reduction of $C_{\mathrm{fly}}$ [42, 43], resulting in larger ripples, further worsening the oscillator spurs. Consequently, in this design, we mainly modulate the

conversion ratio to simplify the converter control but still to obtain a predictable $f_{SW}$, facilitating its direct connection to the oscillator.

With the aid of Eq. (6.1), and considering the targeted $V_{OUT}$ accuracy (i.e., ±5%), across the $V_{IN}$ and $I_L$ ranges, one can easily calculate the lowest and the highest CR by

$$\begin{cases} \mathrm{CR}_{min} = \dfrac{0.95V_{OUT} + R_S I_{L,min}}{V_{IN,max}} \\ \mathrm{CR}_{max} = \dfrac{1.05V_{OUT} + R_S I_{L,max}}{V_{IN,min}}. \end{cases} \tag{6.2}$$

On the other hand, at a constant input voltage, the difference between the output voltage corresponding to two consecutive CRs should be finer than the targeted $V_{OUT}$ accuracy. Consequently,

$$V_{OUT,i+1} - V_{OUT,i} < 0.1V_{OUT}. \tag{6.3}$$

Considering the worst-case scenario ($V_{IN} = V_{IN,max}, I_L = I_{L,min}$), Eq. (6.3) can be written as

$$V_{IN,max}(\mathrm{CR}_{i+1} - \mathrm{CR}_i) - (R_{S_{i+1}} - R_{S_i})I_{L,min} < 0.1V_{OUT}. \tag{6.4}$$

Assuming a constant $R_S$, the required CR resolution can then be estimated by

$$\mathrm{CR}_{res} = (\mathrm{CR}_{i+1} - \mathrm{CR}_i) < \frac{0.1V_{OUT}}{V_{IN,max}}. \tag{6.5}$$

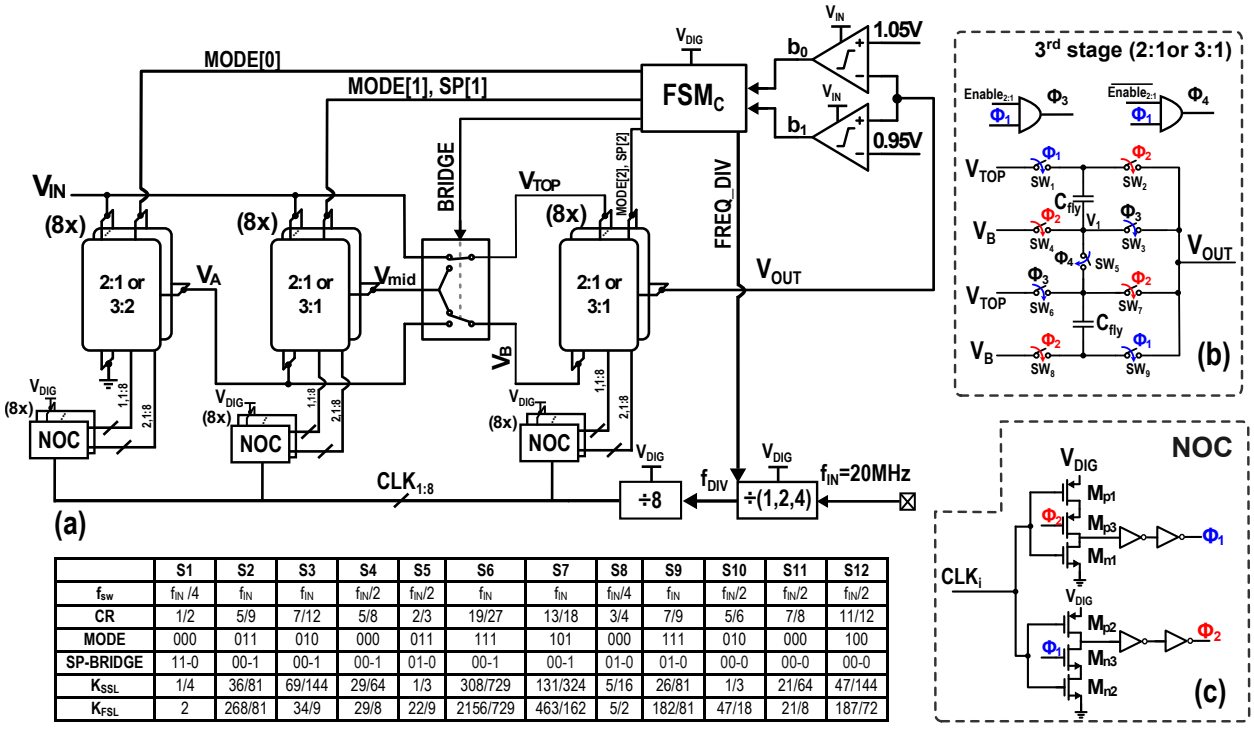
Eq. (6.5) indicates that the CR resolution should be improved if a larger input voltage or a finer $V_{OUT}$ accuracy is targeted. This increases the total number of CRs, which, in turn, adversely impacts on the complexity of the converter and its power efficiency.

With $R_S$ of 50 Ω, 1.3 V < $V_{IN}$ < 2.2 V, and 0.5 mA < $I_L$ < 2 mA, the resulting CR varies from 0.5 to 0.9 with a resolution of 0.045. Considering the side effects of the converter ripple, the number of CRs has been increased from 9 to 12.

### 6.1.1 Topology Definition

Several SC topologies have already been published in literature that could meet the CR range and resolution requirements. In particular, a Successive-Approximation-Register (SAR) SC converter, such as the one presented in [44], offers a resolution of $V_{IN}/2^N$ (where N is the number of stages), but it suffers from a limited power density as a flying capacitance of 2.24 nF is required to deliver a current <0.3 mA. An asymmetric shunt SC converter was presented in [45] that increases the number of CRs even further but at a cost of increasing the losses in the slow-switching-limit (SSL) region. A recursive switched-capacitor (RSC) converter, introduced in [38], offers the same resolution as the SAR but with a lower SSL loss for the same number of stages. However, to achieve our required resolution, it would require *five* 2:1 stages, thus degrading the converter's output impedance and efficiency.

To cover the required CRs, while minimizing the SSL losses and avoiding cascading many RSC




| | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | S11 | S12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{sw}$ | $f_{IN}$/4 | $f_{IN}$ | $f_{IN}$ | $f_{IN}$/2 | $f_{IN}$/2 | $f_{IN}$ | $f_{IN}$ | $f_{IN}$/4 | $f_{IN}$ | $f_{IN}$/2 | $f_{IN}$/2 | $f_{IN}$/2 |
| CR | 1/2 | 5/9 | 7/12 | 5/8 | 2/3 | 19/27 | 13/18 | 3/4 | 7/9 | 5/6 | 7/8 | 11/12 |
| MODE | 000 | 011 | 010 | 000 | 011 | 111 | 101 | 000 | 111 | 010 | 000 | 100 |
| SP-BRIDGE | 11-0 | 00-1 | 00-1 | 00-1 | 01-0 | 00-1 | 00-1 | 01-0 | 01-0 | 00-0 | 00-0 | 00-0 |
| $K_{SSL}$ | 1/4 | 36/81 | 69/144 | 29/64 | 1/3 | 308/729 | 131/324 | 5/16 | 26/81 | 1/3 | 21/64 | 47/144 |
| $K_{FSL}$ | 2 | 268/81 | 34/9 | 29/8 | 22/9 | 2156/729 | 463/162 | 5/2 | 182/81 | 47/18 | 21/8 | 187/72 |

Figure 6.2: (a) Detailed block diagram of the three-stage recursive switched-capacitor (RSC) DC-DC converter with a table showing the control signals for all the converter states (S); (b) detailed representation of a 2:1 or 3:1 stage and (c) the non-overlapping clock (NOC) generator.

stages as in [38], we propose a 3-stage RSC topology but with two CR options (2:1, 3:2 or 3:1) per each stage. This allows to have a resolution of $V_{\mathrm{IN}}/3^{\mathrm{N}}$ while reducing the required number of stages from five to three.

The implemented three-stage RSC converter is shown in Fig. 6.2 (a), while the detailed representation of a 2:1 or 3:2 SC cell is shown in Fig. 6.2 (b). Since $\mathrm{CR_{min}}$ is about 0.5, the first stage does not need the 3:1 configuration and its output should always be connected to the bottom voltage of the second stage, thereby allowing for a higher CR. The second and third stage operates only in the 2:1 and 3:1 modes with one set of bridge switches placed between them. This allows connecting the output of the second stage to either the top or the bottom voltage of the third stage.

Each stage of the converter is divided into eight smaller interleaved units. This allows to avoid the need for an output capacitor and to reduce the switching losses of the converter [35]. Moreover, each unit embeds the non-overlapping clock (NOC) circuit shown in Fig. 6.2 (c). The clock $f_{\mathrm{IN}} = 20\,\mathrm{MHz}$ is provided externally, while the frequency division (of 1, 2 or 4) to generate $f_{\mathrm{DIV}}$ is implemented internally by means of a flip-flop-based frequency divider. Then, the eight interleaved clock phases ($CLK_{1:8}$) are generated by further dividing $f_{\mathrm{DIV}}$. The NOC embedded in each unit generates the two non-overlapped phases ($\Phi_1$ and $\Phi_2$).

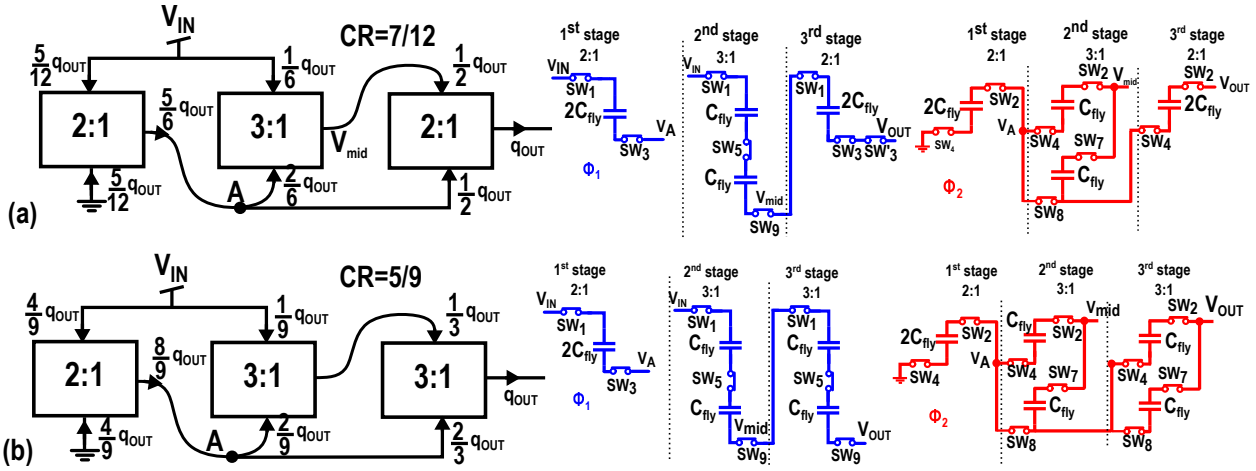



Figure 6.3: Charge flow through the inter-stage connections for a conversion ratio of: (a) 7/12, and (b) 5/9, along with the their equivalent circuits for 1 of the 8 units during $\Phi_1$ and $\Phi_2$.

### 6.1.2 Charge Flow and Impedance Analysis

To always guarantee $V_{\mathrm{OUT}} = 0.95 - 1.05\,\mathrm{V}$, while $V_{\mathrm{IN}} \in \{1.3 - 2.2\}\,\mathrm{V}$, the stages of the RSC converter are rearranged in a series/parallel configuration. This has an impact on the charge flow of each stage, and, therefore, the output impedance of the converter.

Figs. 6.3 (a) and (b) illustrate two configurations which realize CRs of 7/12 and 5/9, along with their equivalent circuits for one of the 8 units. Please notice that node $\mathrm{V_A}$ during $\Phi_1$ ($\mathrm{V_{mid}}$ during $\Phi_2$) is not floating as it is connected to the other four units operating in the opposite phase.

In Fig. 6.3 (a), the last stage loads half of the output charge $q_{\mathrm{OUT}}$ from the second stage. Given that the second stage has a CR of 3:1 ($V_{\mathrm{mid}} = \frac{V_{\mathrm{IN}}+2V_{\mathrm{A}}}{3}$), the charge taken from the node A ($\frac{2}{6}q_{\mathrm{OUT}}$) is twice that from $V_{\mathrm{IN}}$ ($\frac{1}{6}q_{\mathrm{OUT}}$). Applying KCL at node A, the charge delivered by the first stage is found to be $\frac{5}{6}\,q_{\mathrm{OUT}}$, and it is equally divided between its top and bottom voltages ($V_{\mathrm{A}} = \frac{V_{\mathrm{IN}}}{2}$). Fig. 6.3 (b) shows a similar example of charge flow for CR=5/9.

In the conventional RSC topology with only 2:1 stages, irrespective of the converter configuration, the output current of each stage is a binary-weighted fraction of the load current (i.e., $I_{\mathrm{L}}/2^{\mathrm{N-i}}$), thus the switches and capacitors are sized based on the current flowing through them. However, in the topology shown in Fig. 6.2 (a), the charge flow of each stage depends on the particular configuration, as shown in the two previous examples. Hence, in this design, all the stages are sized identically.

To compute $R_{\mathrm{SSL}}$ and $R_{\mathrm{FSL}}$, one can use the charge multiplier vectors $\mathbf{a_c}$ and $\mathbf{a_s}$ that can be directly computed from the charge flow analysis and represent the charge flowing through each capacitor and each switch, respectively [38, 45–47]. Assuming that all the switches have the same $R_{\mathrm{on}}$, the resistances in the slow- and fast- switching limits can be written as

$$R_{\mathrm{SSL}} = \sum_{i=1}^{N} \frac{\mathbf{a}_{\mathrm{c,i}}^{\mathbf{2}}}{f_{\mathrm{SW}} C_{\mathrm{i}}}, \tag{6.6}$$

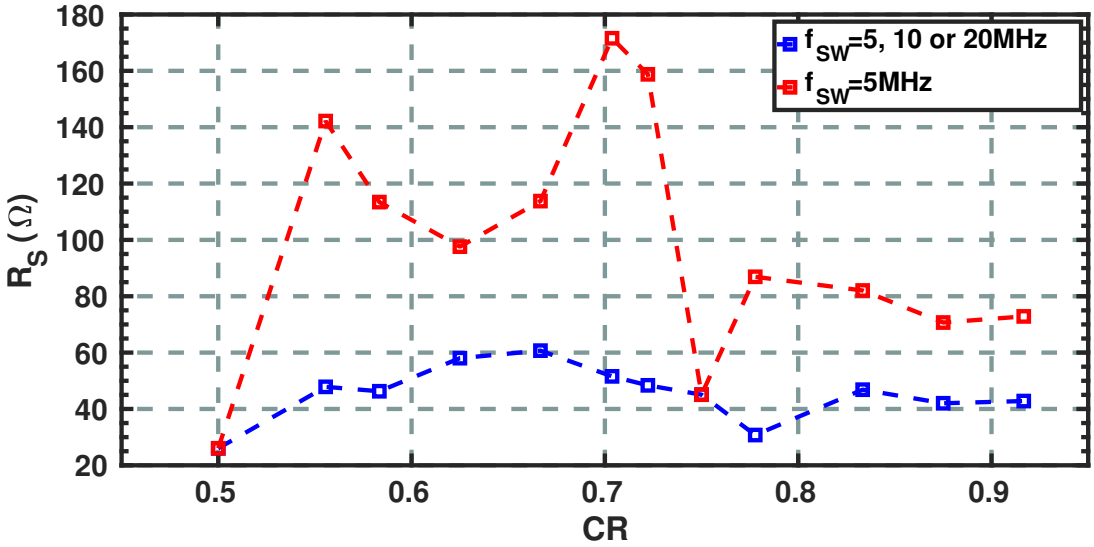



Figure 6.4: Calculated output resistance of the converter with fixed (red) and adaptive (blue) switching frequency.

and

$$R_{\mathrm{FSL}} = \sum_{i=1}^{N} \sum_{\mathrm{j}=1}^{switches} 2\mathbf{a}_{\mathrm{s,i,j}}^{\mathbf{2}} R_{\mathrm{on}}, \tag{6.7}$$

where the summation over $i$ accounts for the number of stages N, while the summation over $j$ accounts for the number of switches in each stage. $C_{\mathrm{i}}$ is the flying capacitance of the $i^{\mathrm{th}}$ stage. In the example shown in Fig. 6.3 (a), the charge multiplier vectors are

$$\begin{aligned} \mathbf{a_c} &= \begin{bmatrix} \frac{5}{12} & \frac{1}{6} & \frac{1}{6} & \frac{1}{2} \end{bmatrix} \\ \mathbf{a}_{\mathrm{s,i}} &= \begin{bmatrix} \frac{5}{12} & \frac{1}{6} & \frac{1}{2} \end{bmatrix}^T, \end{aligned} \tag{6.8}$$

while for the example shown in Fig. 6.3 (b) the charge multiplier vectors are

$$\begin{aligned} \mathbf{a}_{\mathrm{c}} &= \begin{bmatrix} \frac{4}{9} & \frac{1}{9} & \frac{1}{9} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \\ \mathbf{a}_{\mathrm{s,i}} &= \begin{bmatrix} \frac{4}{9} & \frac{1}{9} & \frac{1}{3} \end{bmatrix}^T. \end{aligned} \tag{6.9}$$

When a stage is used in the 3:1 or 3:2 configuration, two flying capacitors and seven switches are operated, leading to two identical elements in vector $\mathbf{a}_{\mathrm{c}}$.

With the aid of the charge multiplier vectors and Eqs. (6.6)–(6.7), the output resistance of the proposed converter versus CR is calculated at $f_{\mathrm{SW}} = 5\,\mathrm{MHz}$ and depicted in Fig. 6.4. As can be gathered from the red line, $R_{\mathrm{S}}$ greatly varies with the particular configuration used, dramatically

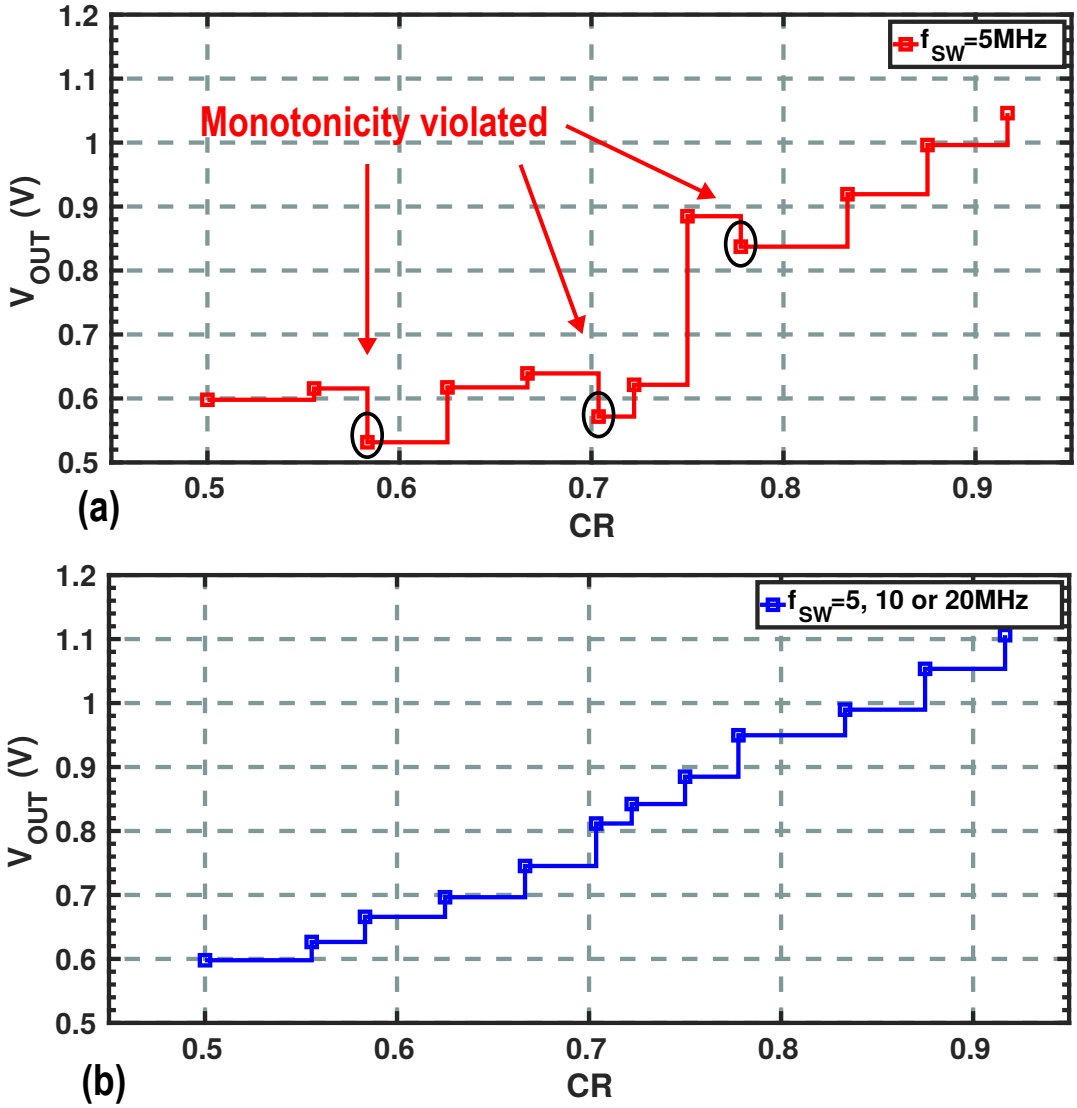



Figure 6.5: Output voltage of the converter versus CR with (a) fixed and (b) adaptive switching frequency, when $V_{\mathrm{IN}} = V_{\mathrm{IN}}^{\mathrm{min}}, I_{\mathrm{L}} = I_{\mathrm{L}}^{\mathrm{max}}$

affecting the converter efficiency. Moreover, even with a constant load current, moving towards a higher CR might lead to a lower output voltage due to the $R_{\mathrm{S}}$ increase. It is therefore necessary to guarantee the monotonicity of the output voltage as a function of CR. This condition can be modelled by the following equation

$$V_{\mathrm{OUT,i+1}} - V_{\mathrm{OUT,i}} > 0, \ \forall \mathrm{i} \in \{\mathrm{CRs}\}. \tag{6.10}$$

Considering the worst-case scenario for the monotonicity ($V_{\mathrm{IN}} = V_{\mathrm{IN,min}}, I_{\mathrm{L}} = I_{\mathrm{L,max}}$), Eq. (6.10), can be rewritten as

$$V_{\mathrm{IN,min}}(\mathrm{CR_{i+1}} - \mathrm{CR_i}) - (R_{S_{\mathrm{i+1}}} - R_{\mathrm{S_i}})I_{\mathrm{L,max}} > 0. \tag{6.11}$$

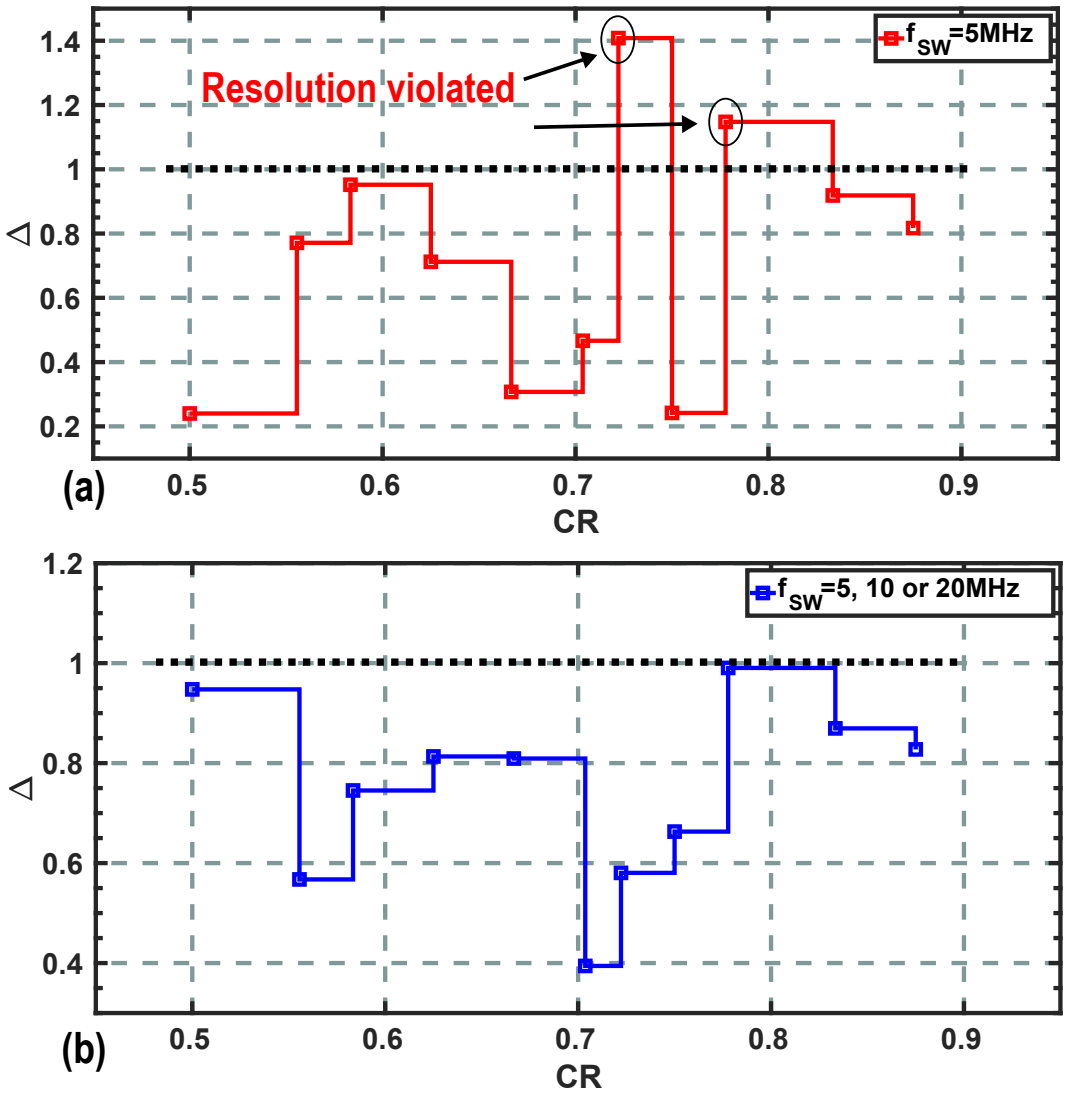



Figure 6.6: Calculated resolution of the converter in the worst-case scenario ($V_{\mathrm{IN}} = V_{\mathrm{IN}}^{\mathrm{max}}, I_{\mathrm{L}} = I_{\mathrm{L}}^{\mathrm{min}}$) for (a) fixed, and (b) adaptive switching frequency.

Fig. 6.5 (a) plots $V_{\mathrm{OUT}}$ for different CRs with $V_{\mathrm{IN}} = V_{\mathrm{IN,min}}$, $I_{\mathrm{L}} = I_{\mathrm{L,max}}$ and $f_{\mathrm{SW}} = 5$ MHz. $V_{\mathrm{OUT}}$ should always increase when moving from one CR to the next higher one. However, for CR of $\frac{7}{12}$, $\frac{19}{27}$ and $\frac{7}{9}$, $V_{\mathrm{OUT}}$ decreases, proving that in those two configurations the monotonicity condition is violated.

On the other hand, large $R_{\mathrm{S}}$ variations can also violate the resolution requirement imposed by Eq. (6.4). To better investigate the resolution requirement, a parameter $\Delta$ is introduced and defined as the voltage difference of the output voltages corresponding to two consecutive CRs normalized to the resolution. Hence, $\Delta$ can be written as

$$\Delta = \frac{V_{\mathrm{OUT,i+1}} - V_{\mathrm{OUT,i}}}{0.1 V_{\mathrm{OUT}}}. \tag{6.12}$$

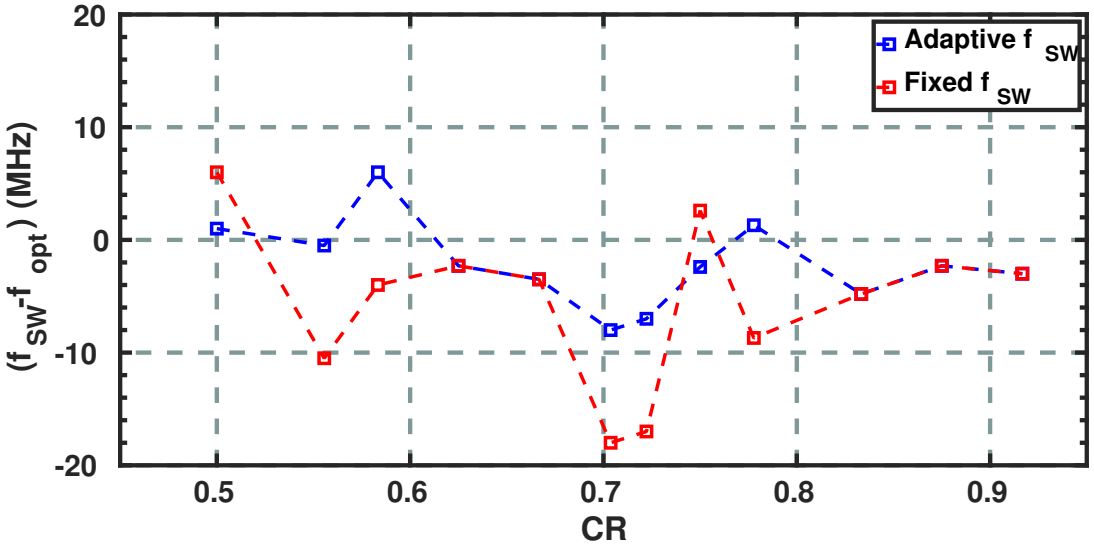



Figure 6.7: Difference between the frequency at which the converter is operated and the optimum one in case of fixed and adaptive switching frequencies.

Fig. 6.6 (a) plots the parameter $\Delta$ versus CRs for a fixed $f_{\mathrm{SW}} = 5\,\mathrm{MHz}$. For each point, the corresponding value on the x-axes represents the lowest of the two consecutive CRs used to plot that particular point. For example, the $\Delta$ at CR=0.5 is the resolution of the converter when going from CR=0.5 to CR=0.556 As can be seen from Fig. 6.6 (a), when going from $\mathrm{CR} = \frac{13}{18}$ to $\mathrm{CR} = \frac{3}{4}$ as well as when going from $\mathrm{CR} = \frac{7}{9}$ to $\mathrm{CR} = \frac{5}{6}$, $\Delta > 1$, thereby violating the resolution requirement.

To overcome the above mentioned problems, the switching frequency in the configurations with a higher $R_{\mathrm{S}}$ can be modulated by a factor of $2\times$ or $4\times$, resulting in the resolution and monotonicity conditions being always met (see Figs. 6.5(b) and 6.6(b)). Moreover, Fig. 6.4 shows that by adapting $f_{\mathrm{SW}}$ to the particular configuration, the output resistance of the RSC converter can be kept fairly constant, thereby maximizing the power efficiency.

Finally, as a general design guide, Eqs. (6.4) and (6.11) can be combined into Eq. (6.13), which provides a compact expression for the two main requirements of SC converters, namely *resolution* and *monotonicity*.

$$\begin{cases} V_{\mathrm{IN,max}}(\mathrm{CR_{i+1}} - \mathrm{CR_i}) - (R_{S_{\mathrm{i+1}}} - R_{\mathrm{S_i}})I_{\mathrm{L,min}} < 0.1V_{\mathrm{OUT}} \\ V_{\mathrm{IN,min}}(\mathrm{CR_{i+1}} - \mathrm{CR_i}) - (R_{S_{\mathrm{i+1}}} - R_{\mathrm{S_i}})I_{\mathrm{L,max}} > 0. \end{cases} \tag{6.13}$$

### 6.1.3 FSM-Based Digital Control

During operation, $V_{\mathrm{OUT}}$ is compared with two reference levels, 0.95 V and 1.05 V, at a rate of 1 MHz. Two bits ($\mathrm{b_{0,1}}$) are generated to indicate whether $V_{\mathrm{OUT}}$ is within the range, higher or lower. The converter's FSM ($\mathrm{FSM_C}$) then decides to keep the same State (S) or move to the next

higher/lower one. Each state has a unique set of control signals (MODE, SP, BRIDGE, FREQ_DIV). The signal MODE determines whether a stage should be operated in 2:1 (i.e., MODE=0) or 3:1 (3:2 for the first stage) (i.e., MODE=1) mode. The signal SP determines whether a stage should be connected in parallel (SP=1) with respect to the previous stage or in series (SP=0) (the first stage does not need this signal). The signal BRIDGE controls the bridge switches which allow to connect the output of the second stage ($V_{\mathrm{mid}}$) either to the top (i.e., BRIDGE=1) or the bottom (i.e., BRIDGE=0) voltage of the third stage. The signal FREQ_DIV determines the switching frequency $f_{\mathrm{SW}}$ by controlling a programmable frequency divider. The table in Fig. 6.2 reports all the converter's states ($\mathrm{S}_1$...$\mathrm{S}_{12}$) and their control signals.

### 6.1.4 Steady-State Loss Analysis

By using a similar approach for the power loss analysis performed in Chapter 5, the optimal $f_{\mathrm{SW}}$ can be written as

$$f_{\mathrm{SW}} = f_{\mathrm{opt}} = \frac{\sum_{i=1}^{N} \frac{\mathbf{a_{c,i}^2}}{C_i}}{R_{\mathrm{FSL}}} = \frac{\rho}{R_{\mathrm{FSL}}}. \tag{6.14}$$

Fig. 6.7 shows the difference between the frequency at which the converter is operated and $f_{\mathrm{opt}}$. By modulating the switching frequency by only a factor of 2× or 4×, the DC-DC converter can be operated relatively close to its optimal $f_{\mathrm{SW}}$. Similarly, the total losses can be written as

$$P_{\mathrm{LOSS}} = \frac{n \cdot \overline{C_g}\ V_{\mathrm{sw}}^2\ W^2\ \cdot \rho}{K_{FSL}\overline{r_{\mathrm{on}}}} + \sqrt{2}\ \frac{\overline{r_{\mathrm{on}}}}{W}\ K_{\mathrm{FSL}}\Big(I_{\mathrm{L,max}}\Big)^2. \tag{6.15}$$

The optimal switch width ($W_{\mathrm{opt}}$) can be found by minimizing Eq. (6.15) with respect to W, leading to

$$W_{\mathrm{opt}} = \left(\frac{\sqrt{2}K_{FSL}^2\overline{r_{\mathrm{on}}^2}\Big(I_{\mathrm{L,max}}\Big)^2}{2n\overline{C_g}\rho V_{\mathrm{sw}}^2}\right)^{\frac{1}{3}}. \tag{6.16}$$

For thin-oxide transistors with minimum channel-length, $\overline{r_{\mathrm{on}}}$ and $\overline{C_g}$ can be assumed to be $1 \cdot 10^3\,\Omega \cdot \mu m$ and $1 \cdot 10^{-15}\,\frac{F}{\mu m}$, respectively. After the circuit optimization, the implemented switch width was chosen to be $W = 130\,\mu m$.

## 6.2 Gate-Driver Design

In this section, a new gate-driver circuit is introduced, which offers constant on-resistance across PVT variations without compromising the reliability of the whole converter.

In nanometer CMOS technology, the breakdown voltage of a thin-oxide device is well below the maximum input voltage of the converter. To resolve this issue, prior arts apply different supply rails (e.g., $\mathrm{V_{IN}}$ and $\mathrm{V_{OUT}}$ in Fig. 6.8 (a)) as the high and low voltage levels for driving the switch gates. However, as $V_{\mathrm{IN}}$ decreases, the gate-source voltage, $|V_{\mathrm{GS}}|$, of the switches approaches $|V_{\mathrm{th}}|$, leading to an exponential increase in their on-resistance, significantly increasing $R_{\mathrm{FSL}}$, as depicted in Fig. 6.8 (b). This impacts the converter power efficiency, the monotonicity and the resolution

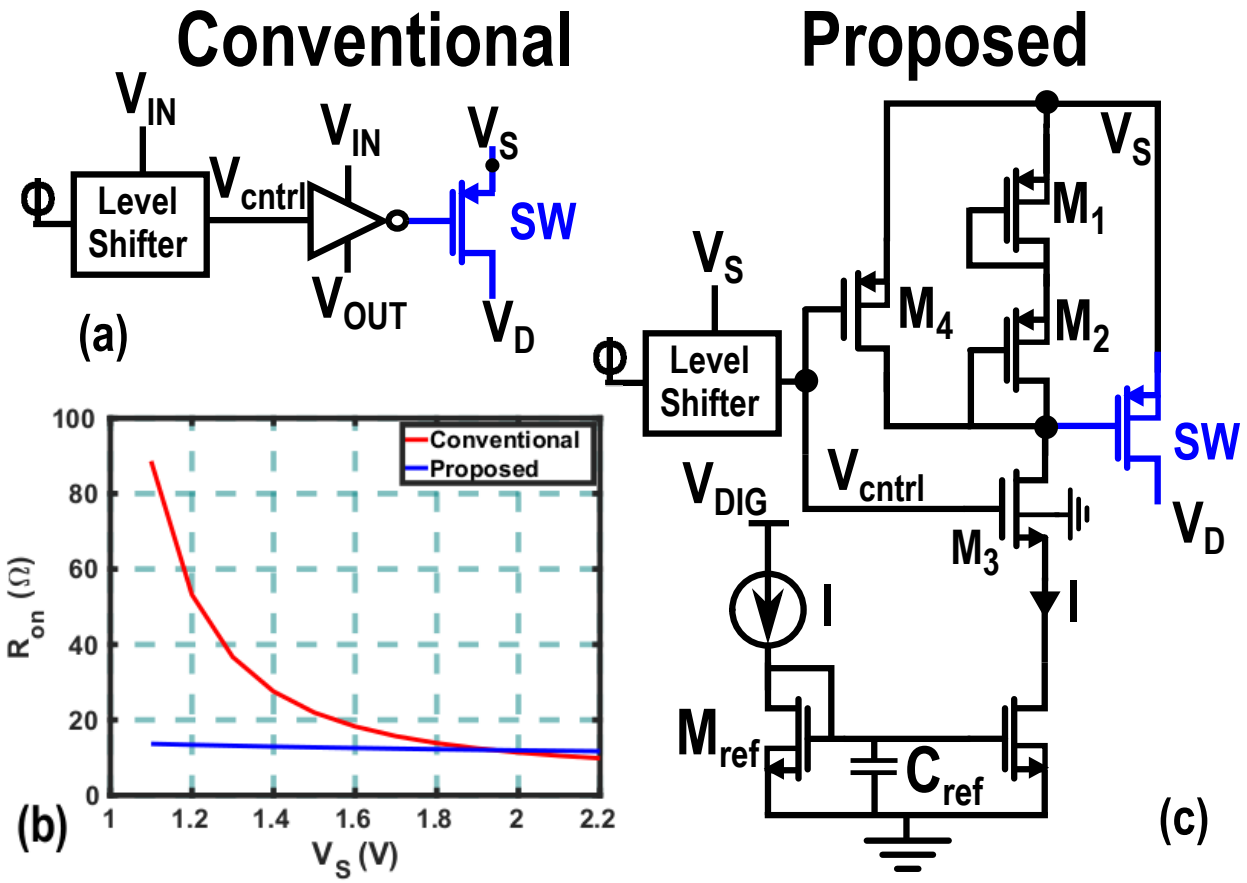



Figure 6.8: (a) Schematic of a conventional gate-driver circuit, with (b) the equivalent series resistance versus the supply voltage, and (c) the proposed gate driver circuit, resulting in a constant $R_{\text{on}}$.

conditions. Fig. 6.9 (a) plots $\Delta$ versus CR. For each point, the corresponding value on the x-axes represents the highest of the two consecutive CRs used to plot that particular point. For example, the $\Delta$ at CR=0.556 is the resolution of the converter when going from CR=0.5 to CR=0.556. Fig. 6.9 (b) plots $V_{\text{OUT}}$ versus CR for different $R_{on}$, while the switching frequency is adapted to the particular CR in accordance with the table in Fig. 6.2 (a). When $R_{\text{on}} \geq 40\,\Omega$, changing CR from 0.5 to 0.556 (moving from S1 to S2 in the table of Fig. 6.2) reduces the output voltage, thereby violating the converter's monotonicity condition. Similarly, the resolution when moving from S4 to S5 is greater than the required output voltage accuracy, thereby violating Eq. (6.13).

To resolve the aforementioned issues, we propose a gate-driver circuit [9], as shown in Fig. 6.8 (b). When the control voltage $V_{\text{cntrl}}$ for the switch SW is high, the bias current $I$ flows through two cascaded diode-connected transistors, $M_{1,2}$, to generate the desired $|V_{\text{GS}}|$ (e.g., $\sim 1\,V$) for the switch. $M_{1,2}$ are minimum-width but long-length devices to achieve a higher resistance, minimizing the bias current and avoiding any serious efficiency degradation. However, when $V_{\text{cntrl}}$ goes 0 to turn off the switch, the time constant associated with the discharging process of the gate-to-source capacitance of the switch is high due to this large resistance, slowing down the discharging process. Consequently, $M_4$ is added to provide a low-impedance path for speeding up the discharging procedure. $M_{3,4}$ are

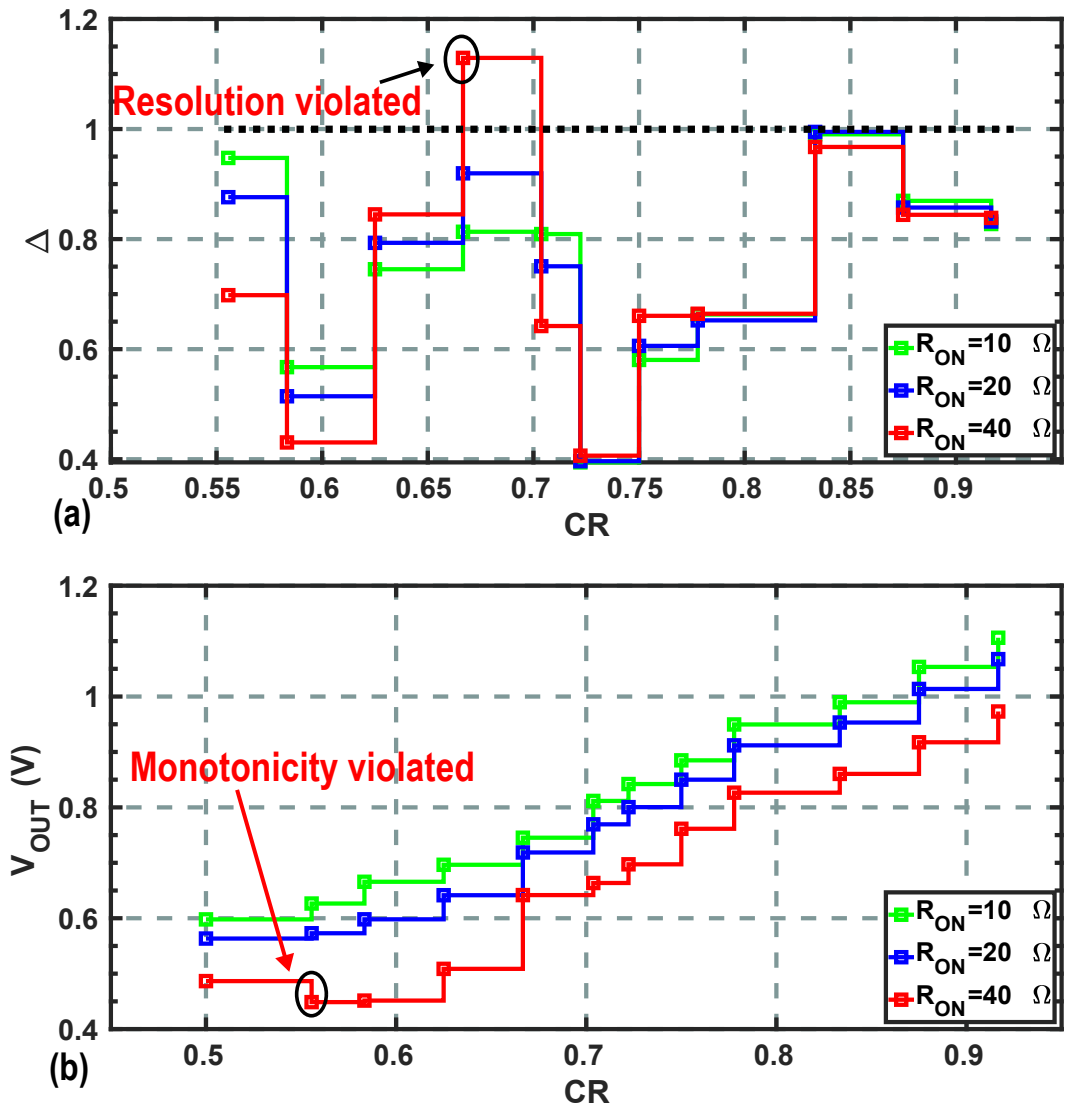



Figure 6.9: (a) Resolution and (b) monotonicity conditions versus CR for different values of $R_{\text{on}}$ using an adaptive switching frequency.

thick-oxide devices, thus contributing to an increase in the dynamic losses. However, their size is much smaller than that of the switch, leading to a negligible power-efficiency degradation. In the proposed circuit, $M_{1,2}$ and switch SW are of the same type. Hence, their $V_{\text{th}}$ changes in the same direction with PVT variations, leading to an almost constant $|V_{\text{GS}}|-|V_{\text{th}}|$ and ON-resistance of the channel. This has been verified by means of a Monte Carlo simulation with 100 samples, as shown in Fig. 6.10(b). Moreover, by providing a constant overdrive voltage to all the switches, the switching losses of the converter merely depend on the number of switches being operated.

To properly drive the gates of $M_{3,4}$, a level shifter (LS) is required since the clock signal $\Phi$ is in the low-voltage domain. However, the LS only drives $M_{3,4}$, which are much smaller than the main switch SW. In the worst-case scenario, the LS output swings from 0 to $V_{\text{IN}} = V_{\text{INmax}} = 2.2\,\text{V}$, while

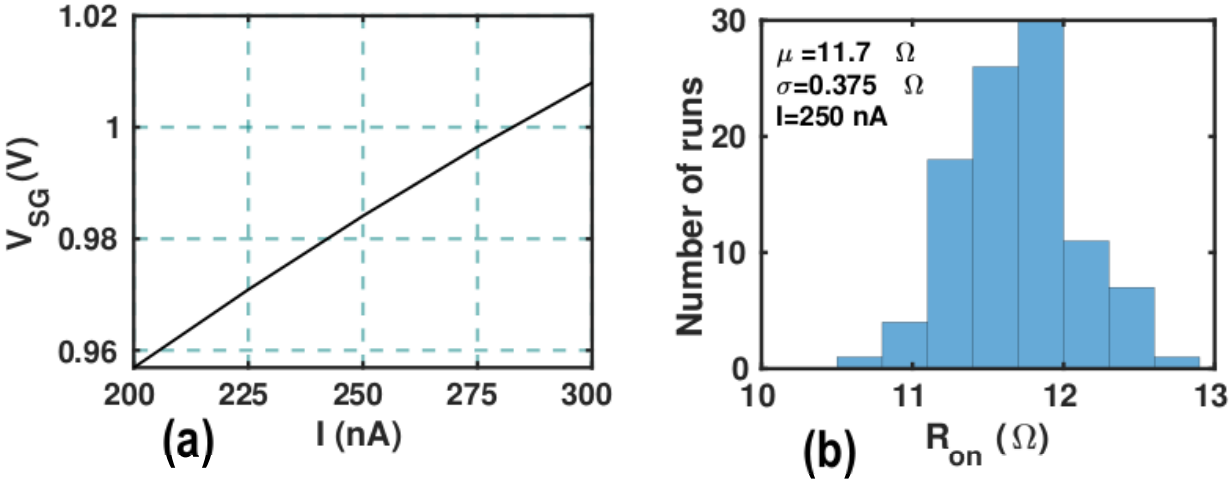



Figure 6.10: (a) $V_{\mathrm{SG}}$ of switch SW when a biasing current variation of ±30% is applied; (b) Monte Carlo simulation of its $R_{on}$.

consuming ∼ 104 nW. There is a total of 240 switches, of which, in the worst-case scenario (State S6), only 168 are operated simultaneously with a 50% duty-cycle, leading to a power overhead of 17.5 $\mu W$, which is negligible when compared to the delivered output power. Moreover, the non-overlapping condition after the LS is still guaranteed, as its propagation delay (hundreds of ps) is much smaller than the non-overlapping time (several ns).

### 6.2.1 Practical Design Considerations

The transistor type, its terminals connections, and especially the body-diode direction of the converter's main switches are of relevant interest to the designer. In this design, the body and source terminals of a PMOS switch are connected, as shown in in Fig. 6.8 (c). Therefore, to guarantee that the body-diode is always reverse biased, the potential of the source terminal, $V_{\mathrm{S}}$, must always be higher than the drain voltage, $V_{\mathrm{D}}$. However, when either the second or third stage works in the 3:1 mode, the use of a single PMOS switch as SW3 in Fig. 6.2 (b) cannot satisfy this requirement. To resolve that, SW3 comprises here two cascaded PMOS switches whose drain terminals are connected. This ensures that when the stage operates in the 3:1 mode, at least one of the two switches is always off. Moreover, both switches follow $\Phi_1$ during the 2:1 mode.

With the conventional gate-driver circuit (see Fig. 6.8 (a)), the switches in each converter's stage operate in different voltage domains. Therefore, it becomes challenging to guarantee the non-overlapping condition between two clock phases over the entire input voltage range, potentially affecting the functionality and performance of the converter. With the proposed gate-driver circuit, the realization of the non-overlapping clocks is simplified as all switches operate in the same voltage domain and are powered by the stable output voltage of the converter ($V_{\mathrm{OUT}} = 1\,\mathrm{V}$). The non-overlapping clock generator circuit is shown in Fig. 6.2(c). By adding transistors $M_{\mathrm{n3}}$ and $M_{\mathrm{p3}}$, each phase of the clock can change state only when the other phase has already altered, thus guaranteeing the non-overlapping condition.

### 6.2.2 Noise Analysis

The three main noise sources of the proposed converter are the transistors in the current mirror of the gate driver circuit, the two comparators and the on-resistance of the switches of the DC-DC converter.

Transistor $M_{\text{ref}}$ in Fig. 6.8 generates current noise $I_{\text{n}}$ that is mirrored at the source terminal of $M_3$. Its noise contribution can be filtered by the capacitor $C_{\text{ref}}$ when

$$Z_{C_{\text{ref}}} \ll \frac{1}{g_{\text{m,ref}}}. \tag{6.17}$$

Hence, the minimum value of $C_{\text{ref}}$ should be

$$C_{\text{ref}} \gg \frac{I}{f\pi(V_{\text{GS}} - V_{\text{th}})}. \tag{6.18}$$

To filter the noise at frequencies above $f = 10\,\text{kHz}$, $C_{\text{ref}} \approx 100\,\text{pF}$ is required, which is negligible when compared to the total on-chip flying capacitance.

The comparators' outputs directly drive the $\text{FSM}_{\text{C}}$. Hence, when the $\text{FSM}_{\text{C}}$ does not change state, the gain from the output of the comparators to the converter's output is zero, resulting in a null noise contribution of the comparators.

The output-referred noise of the comparator does not reach the converter output as the two bits generated ($b_0$ and $b_1$) drive the FSM. Hence, when the FSM does not change state the gain from the output of the comparators to $V_{\text{OUT}}$ is zero.

The SC converter acts as an $RC$ circuit from a noise point of view. Hence, the output noise due to the on-resistance of the switches can be estimated by following a similar analysis to the one presented in Section 5.1.2. In particular, one can recalculate the equivalent resistance and capacitance of the converter in all the different states and estimate the output noise with the aid of Eq. (5.12). By employing the gate driver proposed in the previous section, the noise spectral density of the proposed converter is more predictable and well-behaved against PVT. Fig. 6.11 shows the simulated output noise in different converter states. At lower frequencies ($f < 10\,\text{kHz}$), the output noise is dominated by the flicker noise component of $M_{\text{ref}}$. As the frequency increases, its noise contribution is filtered by capacitor $C_{\text{ref}}$, while the total output noise is dominated by the thermal noise of the switches' on-resistance. At any frequency, the noise of the DC-DC converter is well below the noise voltage tolerated by an LC oscillator (e.g., from Eq. (4.8), $V_{\text{n,supply}} \leq 38\,\text{nV}/\sqrt{\text{Hz}}$ for an oscillator with $\text{FOM} = 190\,\text{dBc/Hz}$, $K_V = 40\,\text{MHz/V}$, $f_0 = 5\,\text{GHz}$ and $P_{DC} = 1\,\text{mW}$). It is worth mentioning that, contrary to the LDO approach, such low noise is achieved without consuming any additional current or using any external components.

## 6.3 Measurement Results

The proposed DC-DC converter and the oscillator have been fabricated in the same standard 40-nm CMOS process. To prove that also the DC-DC converter designed in this chapter meets

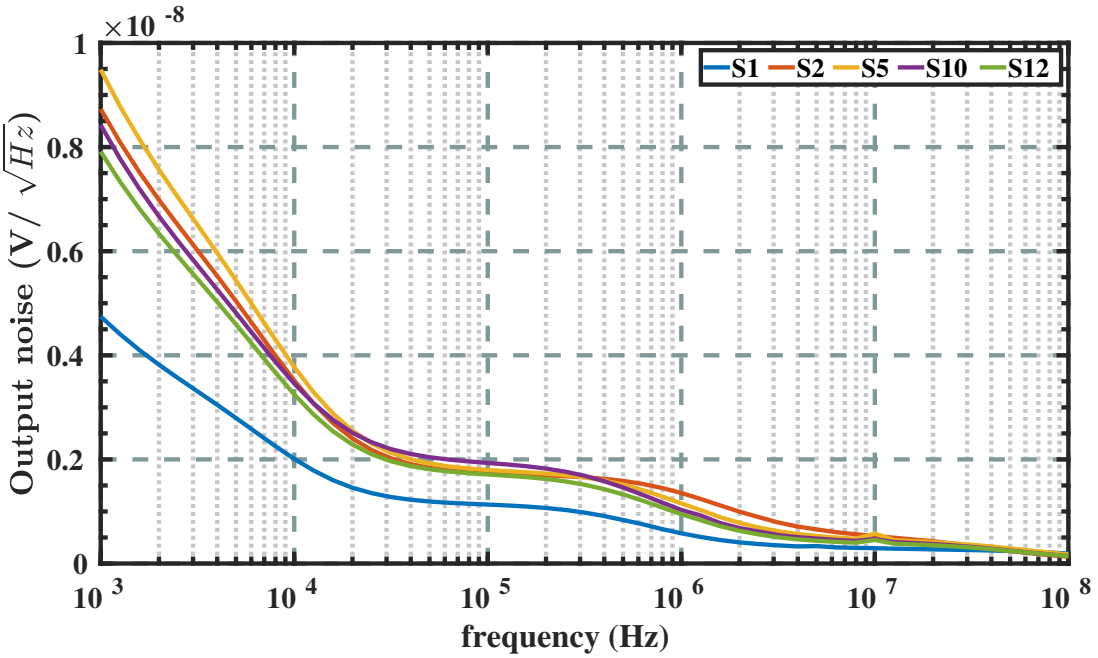



Figure 6.11: Output noise of the DC-DC converter when operated in different configurations.

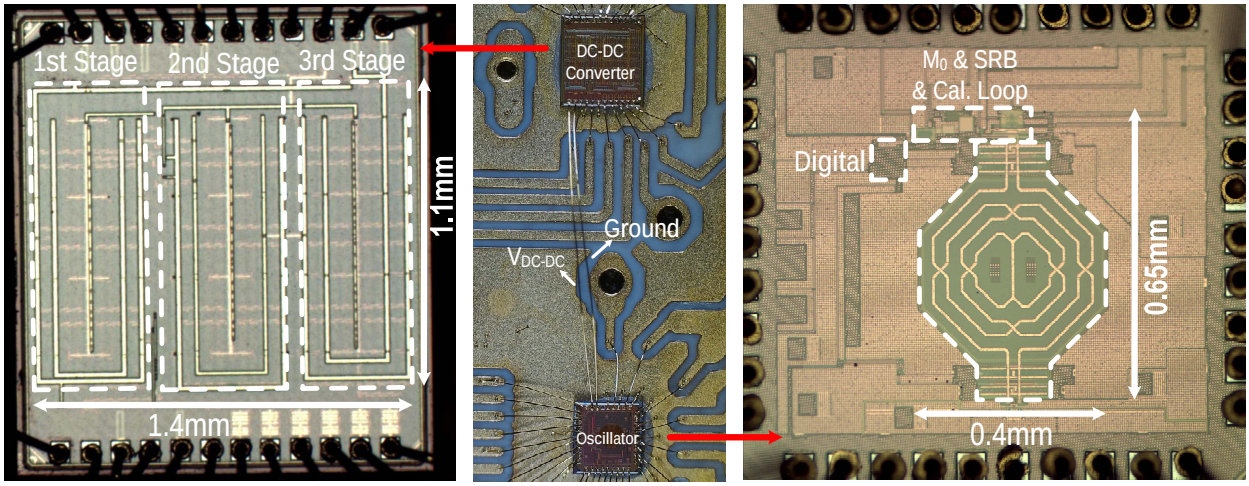



Figure 6.12: Die micrographs of the DC-DC converter (left), the oscillator (right), and photo highlighting their direct connection (middle).

the supply requirements discussed in Chapter 4, the LC oscillator that embeds the spur reduction block (SRB) described in Section 5.2.2 has been (re)characterized when powered by the 3-stage RSC converter.

The chip micrographs of the DC-DC converter and the oscillator, as well as a photo highlighting the direct connection of the converter's output to the oscillator supply rail, are shown in Fig. 6.12. They occupy an active area of 1.54 mm$^2$ and 0.23 mm$^2$, respectively. The total on-chip capacitance of the DC-DC converter $C_{\text{fly}} = 2.7$ nF is equally divided among the three stages, as discussed in Section 6.1.2.

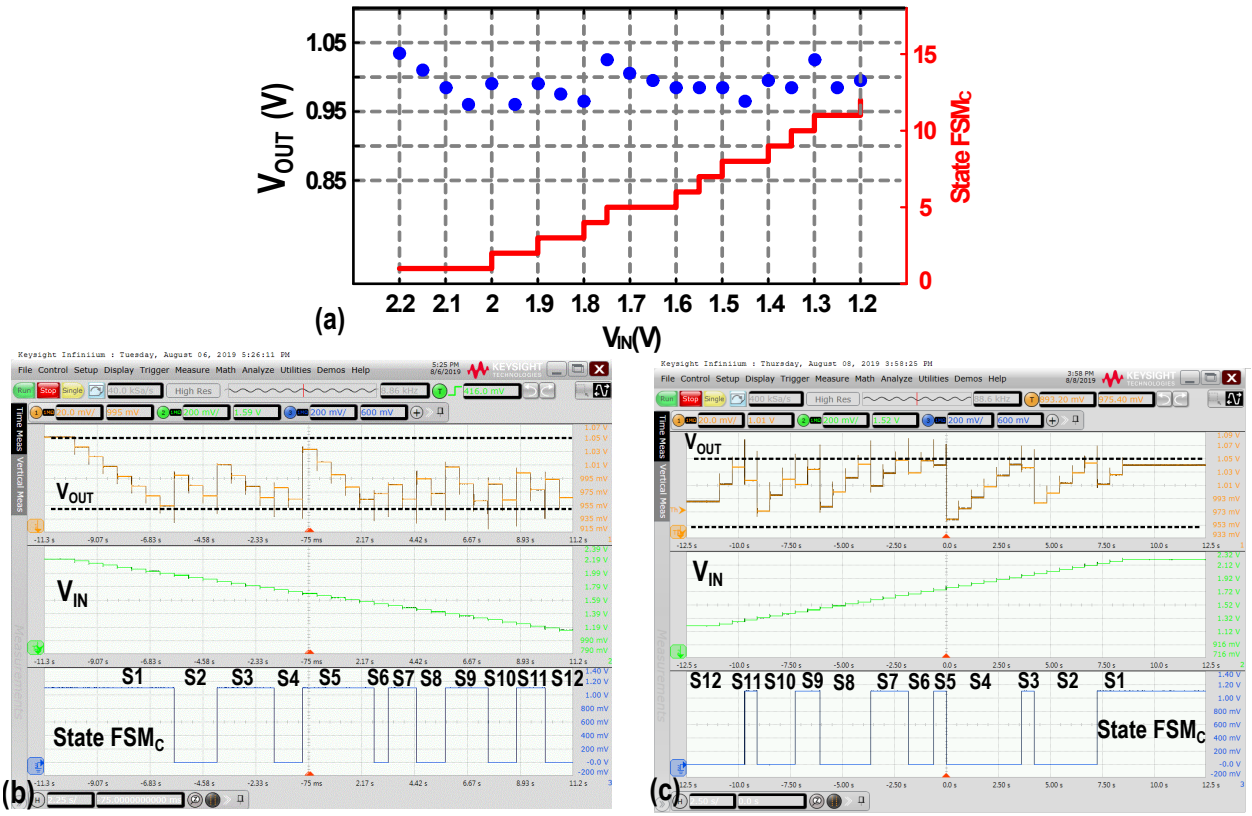



Figure 6.13: (a) Measured output voltage of the DC-DC converter versus $V_{IN}$ for $I_L = 1\,mA$; (b) transient waveform of $V_{OUT}$ for descending and (c) ascending $V_{IN}$ values along with the signal that triggers the change in the FSM.

### 6.3.1 DC-DC Converter Measurements

Fig. 6.13 (a) shows the line regulation of the converter for $I_L = 1\,mA$ along with the state of the $FSM_C$. Figures 6.13 (b) and (c) show that as $V_{IN}$ decreases (or increases), CR changes accordingly to keep $V_{OUT}$ within the desired range.

Fig. 6.14 (a) shows that the parameter $\Delta$, as defined in Section 6.1.C, in the worst-case scenario ($V_{IN} = V_{INmax} = 2.2\,V$ and $I_L = I_{Lmin} = 0.5\,mA$) is always lower than 1, proving that the first condition imposed by Eq. (6.13) is met. Fig. 6.14 (b) illustrates the output voltage of the converter (orange line) and the signal (blue line) that changes the state of $FSM_C$. As CR rises, $V_{OUT}$ increases monotonically, proving that, in the worst-case scenario for the monotonicity ($V_{IN} = V_{INmin} = 1.3\,V$ and $I_L = I_{Lmax} = 2\,mA$), the second condition imposed by Eq. (6.13) is also met.

Fig. 6.15 (a) shows the converter's power efficiency versus $V_{IN}$ for different load currents. The power efficiency of an ideal LDO is added as a comparison. The converter's efficiency stays >80% across the entire 1.3–2.2 V input voltage range for $I_L$=1.5 mA. Fig. 6.15 (b) shows that inaccuracy of the biasing current of the gate-driver circuit, $I = 300\,nA$ ±30%, leads to a negligible degradation of its power efficiency, proving that the static current consumed by the gate driver circuit has negligible effects on the power efficiency, as explained in Section 6.2. For $V_{IN} > 2\,V$, the power efficiency is the

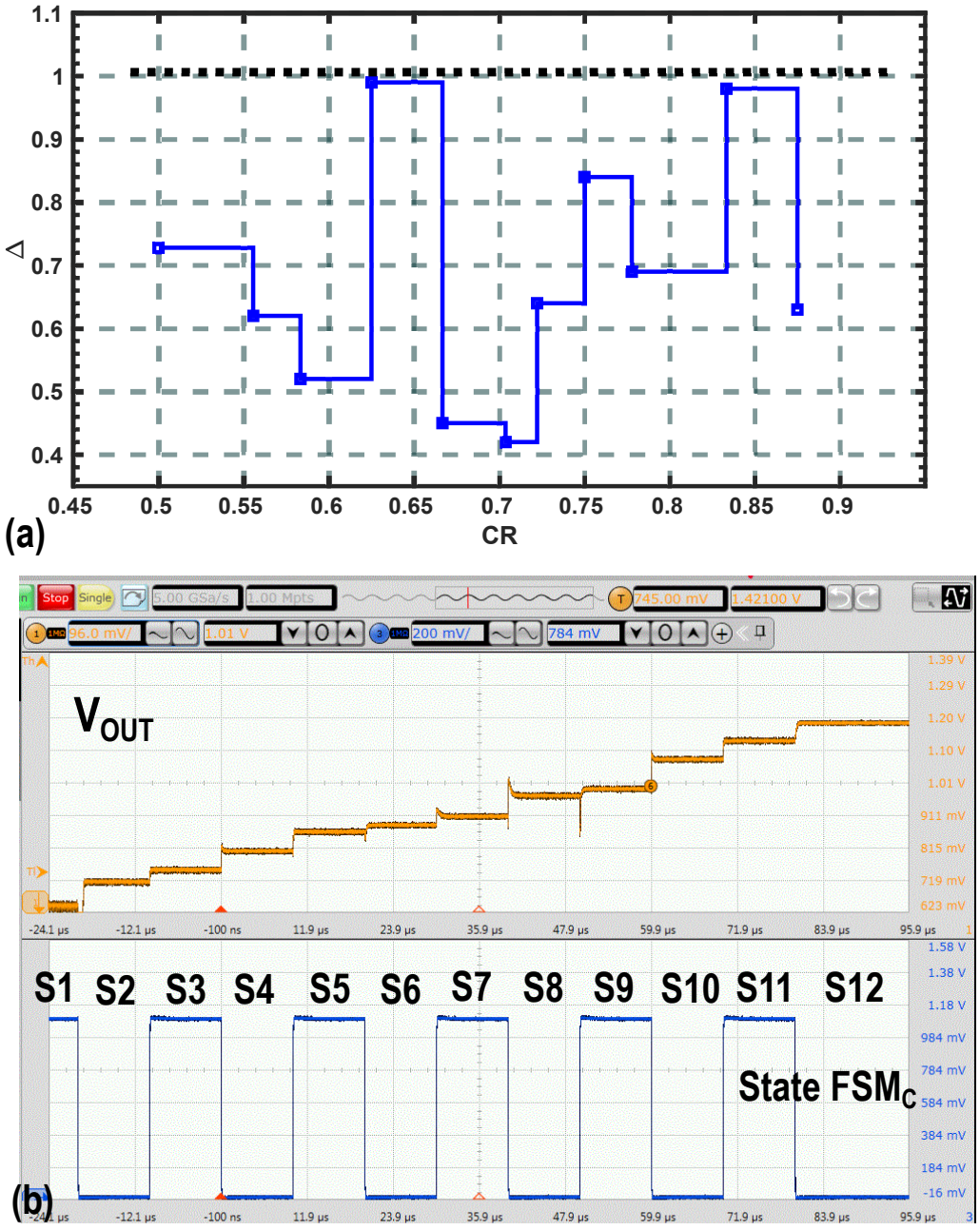



Figure 6.14: Measurement results of (a) the resolution of the converter for $V_{\mathrm{IN}} = V_{\mathrm{INmax}} = 2.2\,\mathrm{V}$ and $I_L = I_{\mathrm{Lmin}} = 0.5\,\mathrm{mA}$; (b) the monotonicity of the converter for $V_{\mathrm{IN}} = V_{\mathrm{INmin}} = 1.3\,\mathrm{V}$ and $I_L = I_{\mathrm{Lmax}} = 2\,\mathrm{mA}$.

highest, since the converter operates at the lowest CR=1/2, in which it exhibits the lowest output resistance due to the lowest number of operating switches, as discussed in Section 6.1.4.

Fig. 6.16 shows that the converter can recover back to the desired range right after two $\mathrm{FSM_C}$ clock cycles (i.e., $2\,\mu\mathrm{s}$) while facing a 0–2 mA current step with a 10 ns rise time.

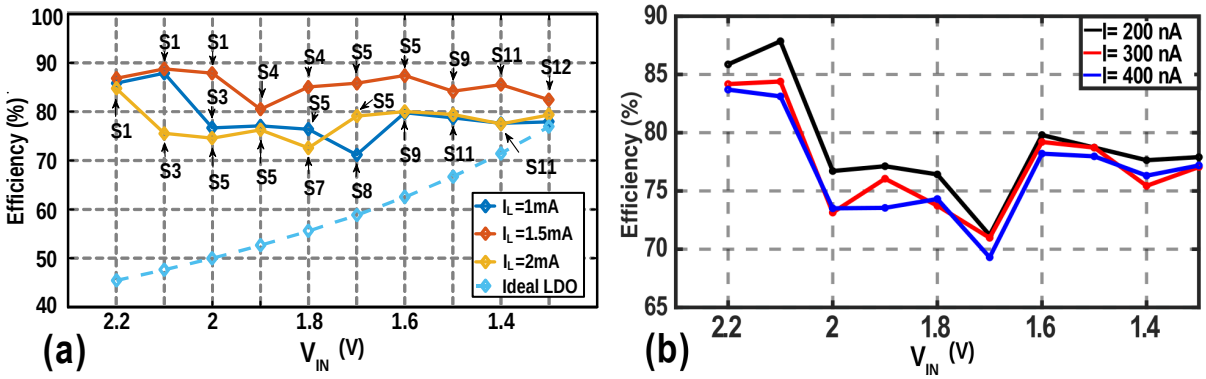



Figure 6.15: Measured power efficiency versus $V_{\mathrm{IN}}$ for different values of (a) load current, and (b) biasing current of the gate driver circuit with $I_{\mathrm{L}} = 1\,\mathrm{mA}$.

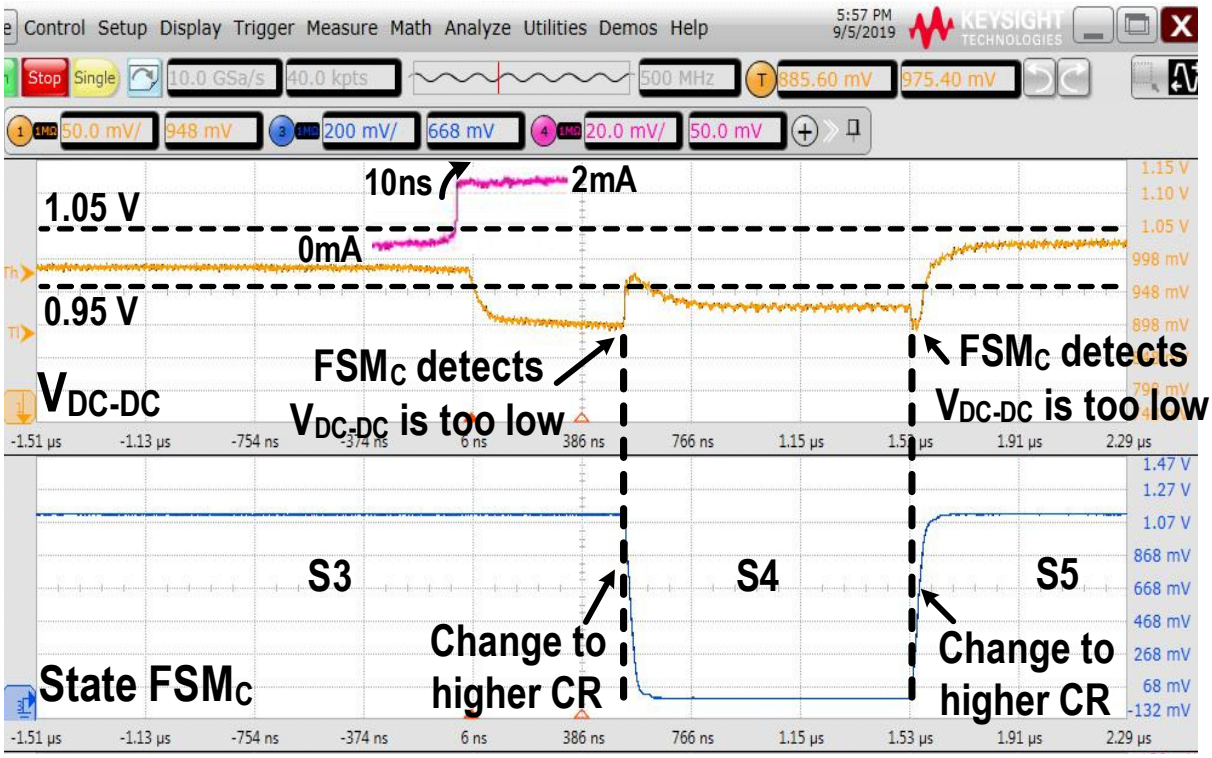



Figure 6.16: Response of the converter (orange line) to a current step from $0 - 2\,\mathrm{mA}$ (purple line) along with the signal that triggers the change in the $\mathrm{FSM_C}$ (blue line).

The measurement of the output noise of the DC-DC converter is limited by the noise floor of the spectrum analyzer. Hence, an LNA with a gain of 35 dB is placed after the DC-DC converter. The resulting spectrum is shown in Fig. 6.17 (a) (blue curve) for the $\mathrm{FSM_C}$ in State S2. When the LNA is used, the amplitude of the peaks is amplified by 35 dB, whereas the noise is amplified by only 10 dB, proving that the measurement is no longer limited by the noise floor of the spectrum analyzer. At around 6 MHz, the measured noise integrated over the resolution bandwidth of the spectrum analyzer (100 kHz) is $\approx -81\,\mathrm{dBm}$. As a result, the spot noise at around 6 MHz is

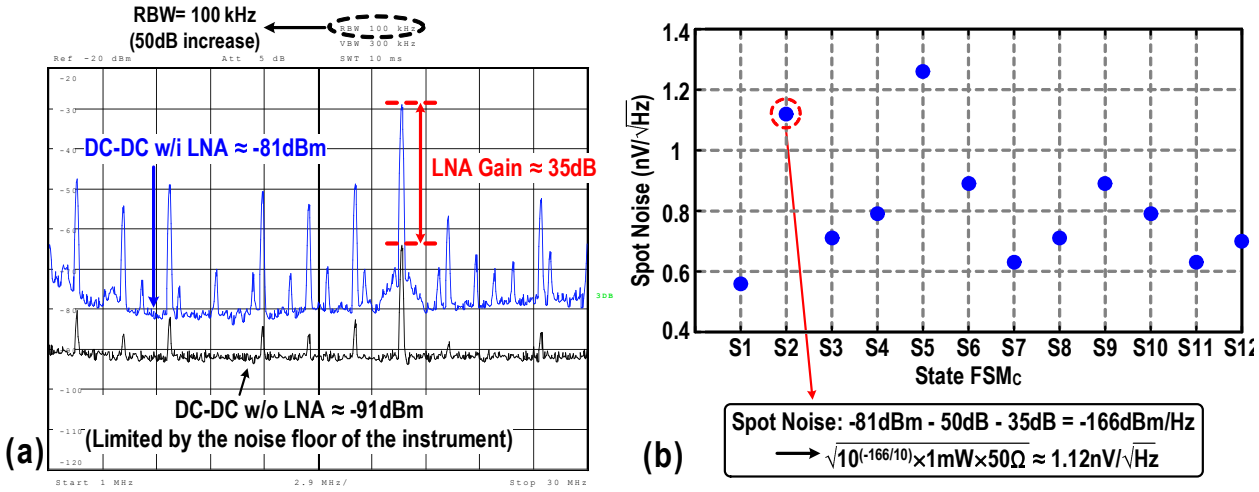



Figure 6.17: (a) Spectrum of the output voltage of the DC-DC converter with (blue line) and without (black line) the use of an LNA; (b) spot noise of the converter across different $\mathrm{FSM_C}$ states.

Table 6.1: COMPARISON WITH DC-DC ARCHITECTURES

| | This work | [44] JSSC16 | [38] JSSC14 | [54] JSSC17 | [45] TPE19 | [53] JSSC19 |
|---|---|---|---|---|---|---|
| **Topology** | 3b Multiratio | 7b SAR | 4b binary | 2-/3- Phase SC Conv. | Asymmetrical Shunt | Algebraic Series/Parallel |
| **CMOS tech** | 40 nm | 180 nm | 250 nm | 130 nm | 250nm | 65nm |
| **$V_{IN}$ (V)** | 1.3-2.2 | 3.4-4.3 | 2.5 | 1.6-3.3 | 3.3 | 0.25-1 |
| **$V_{OUT}$(V)** | 1 | >0.45 | 0.1-2.2 | 0.5-3.0 | 0.4-2.8 | 1 |
| **$I_{OUT}$(mA)** | <2 | <0.3 | <2 | <250 | <10 | <20.1 |
| **$\eta_{MAX}$ (%)** | 87 | 72 | 85 | 91 | 87 | 80 |
| **$f_{SW}$ (MHz) (Range)** | 5,10,20 (X4) | 0.08-2.7 (X34) | 0.2-9 (X45) | <10 (>X1) | NA | NA |
| **#CR** | 12 (Theory,22) | 117 (Theory,127) | 15 | 6 | 187 | 7 |
| **$C_{fly}$(F)** | 2.7n | 2.24n | 3n | 2x(1µ) | 10n | 3n |
| **$C_{OUT}$(F)** | 0 | NA | 0 | 1µ | 0 | 0 |
| **Power density (mW/mm²)** | 1.3 | 0.27 | 0.95 | - | 1.01 | 22.7 |

$-81\,\mathrm{dBm} - 35\,\mathrm{dB} - 10\log_{10}(100\,\mathrm{kHz}) = -166\,\mathrm{dBm/Hz} \approx 1.12\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. Furthermore, the output spot-noise level at $\sim 6\,\mathrm{MHz}$ has also been measured over different converter states and shown in

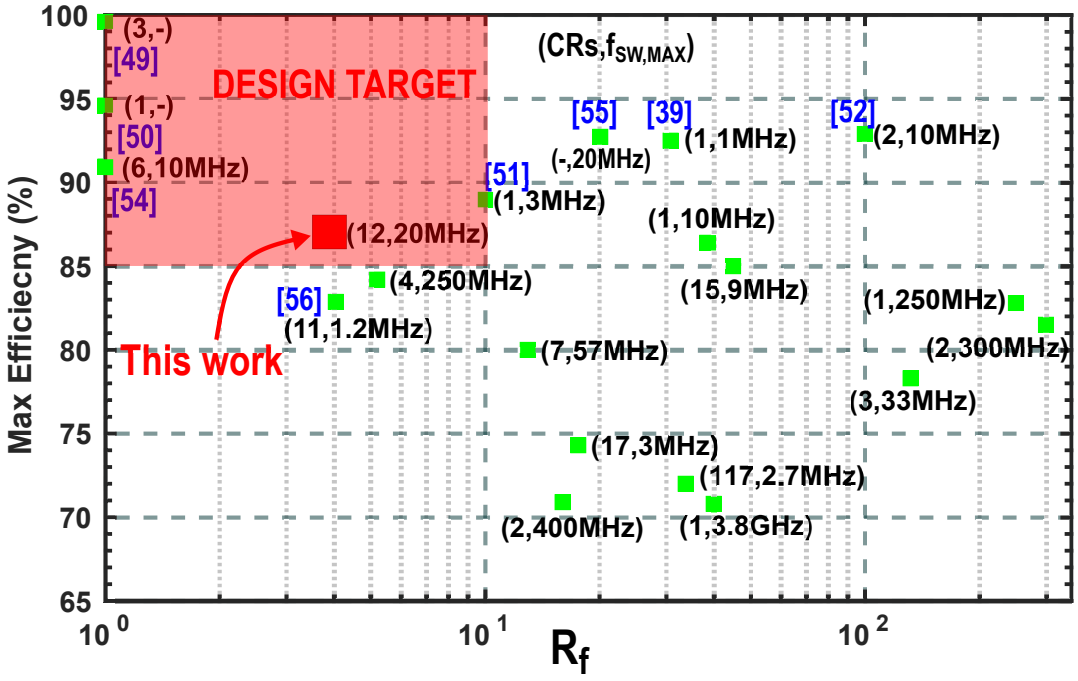



Figure 6.18: Peak power efficiency of state-of-the-art DC-DC converters versus the ratio of maximum-to-minimum switching frequency ($R_f = \frac{f_{SW,max}}{f_{SW,min}}$). The number of implemented CRs, and $f_{SW,max}$ are reported inside the parentheses.

Fig. 6.17 (b). The noise is always $< 1.5\,nV/\sqrt{Hz}$ which is well below the supply noise requirement of the oscillator ($V_n < 23\,nV/\sqrt{Hz}$), as discussed in Section 4.2.2.

Table 6.1 provides a comparison with other DC-DC converters targeting a high number of conversion ratios. Fig. 6.18 reports the peak power efficiency of state-of-the-art DC-DC converters versus the ratio of maximum-to-minimum switching frequency ($R_f = \frac{f_{SW,max}}{f_{SW,min}}$) required for the voltage regulation. $R_f$ should normally be limited to relax the design complexity of the SRB and to avoid lowering the power efficiency, as discussed in Section 5.2.2. At the same time, the number of CRs should be large enough to provide a *fairly* constant output voltage in the face of input voltage and load current variations. As can be gathered from Fig. 6.18, the proposed converter achieves one of the highest peak efficiencies with 12 CRs and an $R_f$ as low as 4. References [39, 49–52] achieve higher power efficiency, but with a very limited number of CRs (e.g., 1–3). [54] implements 6 different CRs by using two off-chip flying capacitors of $1\,\mu F$ each, making the whole converter bulky. the $R_f$ of [39, 52] and [55] is also much larger than in our work, leading to a more complex design of the SRB.

### 6.3.2 System-Level Measurements

Fig. 6.19 (a) shows the phase noise of the oscillator when powered from a noise-free supply and from the DC-DC converter in different $FSM_C$ states for the oscillator frequency of 5.5 GHz. The

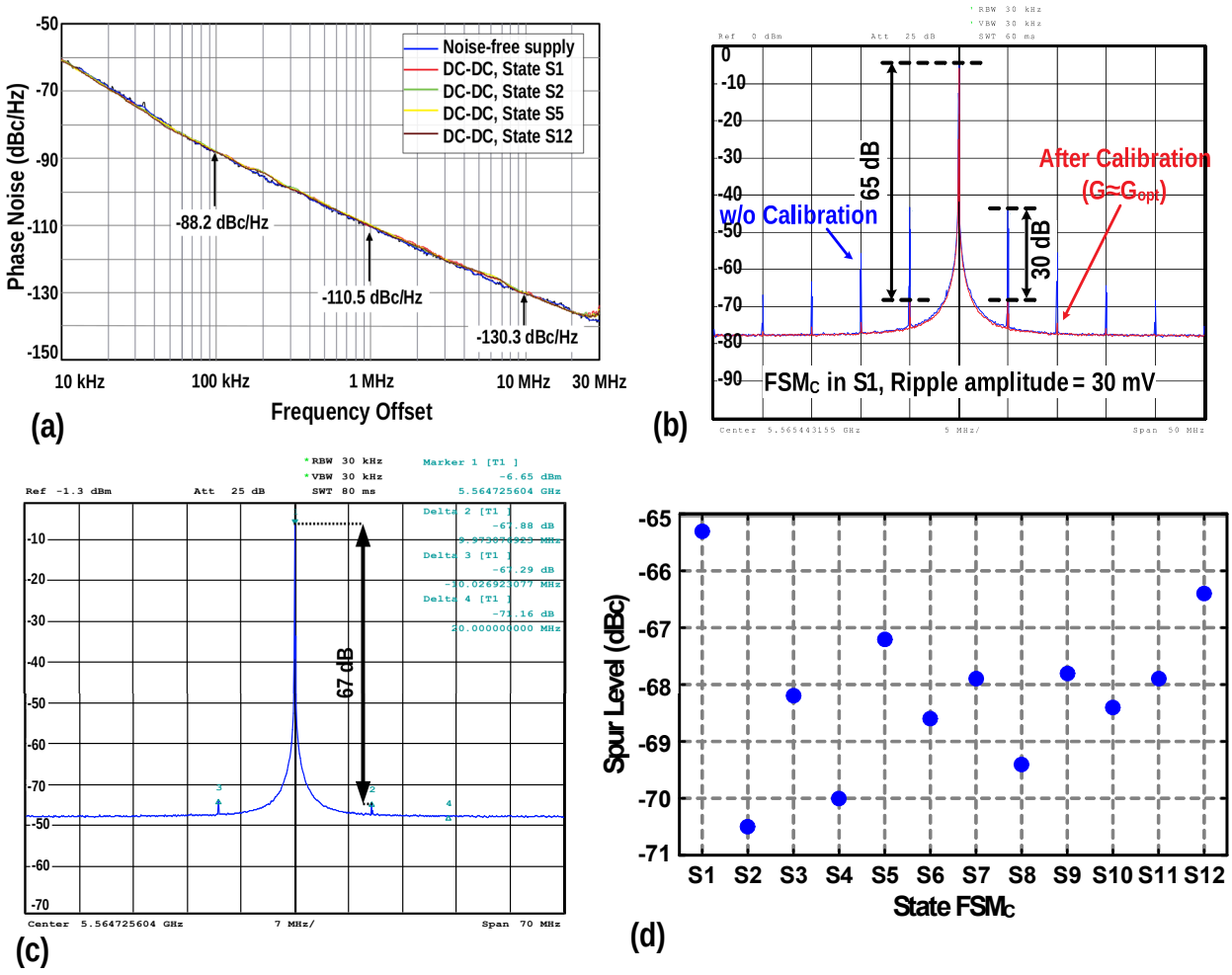



Figure 6.19: (a) Measured oscillator PN performance at $f = 5.56\,\text{GHz}$ and (b) its spectrum before and after calibration of the SRB with $\text{FSM}_\text{C}$ in State S1 and (c) State S5; (d) spur level across different converter states when the oscillator is calibrated only at State S1.

inherent PN of the oscillator is not degraded, proving that the condition imposed by Eq. (4.8) is met and the supply does not limit the oscillator performance. Fig. 6.19 (b) shows the spectrum of the oscillator before and after calibration when powered from the DC-DC converter with a ripple amplitude of $\sim 30\,\text{mVpp}$. The spur level is reduced by 30 dB and reaches $-65\,\text{dBc}$ after the calibration. A similar measurement is also performed while the oscillator is powered from the DC-DC converter in State S5, and the spectrum is depicted in Fig. 6.19 (c). Fig. 6.19 (d) shows the spurious level of the oscillator across all the states of the $\text{FSM}_\text{C}$ when the SRB of the oscillator is only calibrated in State S1. The spur level always stays below -65 dBc.

Table 6.2 summarizes the performance of the whole system and compares it with prior art. Our work is more suitable for a full system integration by avoiding external components and demonstrates the highest system peak power efficiency thanks to the removal of the LDO voltage headroom. Since the SRB is always engaged, the equivalent PSR of our approach is calculated in this table from the difference (in dB) between the spur level measured at the optimum setting and the calculated one

Table 6.2: COMPARISON WITH SYSTEMS POWERING UP LC OSCILLATORS

| | | This work | [2] | [57] | [58] | [6] |
|---|---|---|---|---|---|---|
| **System Architecture** | | DC-DC+ OSC | DC-DC+ LDO+OSC** | DC-DC+ LDO†† | LDO+ OSC | LDO+ OSC |
| **CMOS tech** | | 40 nm | 55 nm | 65 nm | 250 nm | 65 nm |
| **$V_{IN}$ (V)** | | 1.3-2.2 | 1.6-3.3# | 2.4-2.6 | - | - |
| **$V_{IN-LDO}$ (V)** | | X | 1.4 | 1.05 | 2-2.5 | 0.6 |
| **$V_{OUT-LDO}$ (V)** | | 1.0 | 1.2 | 1 | 1.5-2 | 0.4 |
| **$V_{LDO,DROP}$ (mV)** | | 0 | 200 | 50 | 500 | 200 |
| **$\eta_{DC-DC}$ (%)** | | 87 | 92 | 80.3 | - | - |
| **$\eta_{LDO}$(%)** | | X | <85.7 | <94.9 | <79 | <60 |
| **$\eta_{SRB}$(%)** | | 98 | X | X | X | X |
| **$\eta_{TOTAL}$(%)** | | 85 | <79 | <76.2 | <79 | <60 |
| **#ext. comp** | | 0 | 2 | 0 | 1 | 0 |
| **Osc. supply noise (nV/$\sqrt{Hz}$)** | | 1.26 (S5) @10MHz | - | 14.1# @10MHz | 32 @100KHz | 22.4*** @10MHz |
| **$C_{LDO}$(F)** | | X | - | 41p | 50n | 390p |
| **Quiescent Current (µA)** | | 20 | - | 10 | 120 | 500 |
| **PSR (dB)** | **@5MHz** | 48.9* | 20 | 12.8† | 35 | 31† |
| | **@10MHz** | 43* | 20 | 12.8† | - | 26† |

*PSR of the SRB **Oscillator is part of the whole transceiver †Simulated value

#Extracted from the measurement result ††Can be used to power up an oscillator

***Calculated from phase noise with $K_{SUP}$=50 MHz/V X=Not needed

based on the simulated $K_V$ of the oscillator without the SRB. Compared to the systems with LDOs, our fully integrated SC converter exhibits >10× lower supply noise and our SRB shows >15 dB higher power supply rejection, preserving the oscillator's spectral purity for IoT applications.

## 6.4 Conclusion

This chapter presents a recursive switched-capacitor (RSC) DC-DC converter directly connected to an LC oscillator without using any LDOs or external components. The CR of the DC-DC converter is automatically adjusted by means of an FSM-based digital control which modulates

the CR of the converter such that its output voltage is kept at 1 V±5%. A gate-driver circuit is proposed to guarantee a constant low $R_{\text{on}}$ of the converter's switches, thereby meeting the resolution and monotonicity requirements while avoiding efficiency degradation. The converter peak power efficiency is 87% with an output noise $<1.5\,\text{nV}/\sqrt{\text{Hz}}$. This does not degrade the oscillator phase noise performance, while the spur reduction block (SRB) embedded in the oscillator's biasing network suppresses the ripple-induced spurs to $< -65\,\text{dBc}$ .

Chapter

# 7

# Conclusions

This dissertation focuses on the design of power-efficient DC-DC converters for two different applications. In the first part of the thesis, an inductor-based DC-DC converter is used as the core of a multi-channel neurostimulator circuit. The second part of this thesis presents a fully-integrated switched-capacitor DC-DC converter which is designed to directly power up an LC oscillator. In both applications the goal is to maximize the system power efficiency, thereby extending the battery-cycle and limiting or even avoiding battery replacement.

Section 7.1 provides a summary of the work while highlighting the scientific achievements. Section 7.2 discusses recommendations for future work.

## 7.1 Thesis Outcomes and Original Contributions

Electrical stimulation has been used for many years to treat neural disorders, restore hearing, restore vision, etc. In those applications, there is the need for an increasing number of independent stimulating channels to accommodate a larger number of stimulating sites, which allows to achieve a larger spatial resolution. However, multi-channel operation, high power efficiency and safety are not trivial to achieve simultaneously.

In Chapter 3, a neurostimulator circuit achieving 68% peak power efficiency with 16 fully-reconfigurable electrodes and only one external inductor is presented. A novel *zero-current detection circuit* allows to remove the freewheel diode typically used in inductor-based DC-DC converters. As a consequence, the power efficiency is boosted especially at light loads (i.e., low output voltage). To allow for a biphasic stimulation cycle, an H-bridge is used. The switches of the H-bridge are

implemented using thin-oxide transistors operated as high-voltage switches and driven with a current directly. This allows to avoid the use of an external high-voltage supply and improve the system power efficiency.

The second part of this thesis aims to improve the power efficiency of the power management unit (PMU) for IoT devices. In Chapter 4, the power supply rejection and the noise requirements of an oscillator's supply are derived. The well known power efficiency and noise equations of the traditional LDO design are *extended to a guideline for designing LDOs* for RF oscillators. The derived closed-form equations directly relate the system specifications to the LDO's components parameters. The design guide offers many design insights, and trade-offs, ranging from the contribution of each LDO element to the power efficiency degradation with its noise and efficiency analysis to the optimum sizing of the LDO's components. The result of this guideline is used to quantify the efficiency degradation of an LDO.

Given the clear disadvantages of an LDO-based approach, in Chapter 5, a 2:1 or 3:2 switched-capacitor (SC) stage is introduced. The well-known noise analysis of switched-capacitor circuits is *extended to SC DC-DC converters*. This allowed reaching a closed-form formula that estimates the noise of SC DC-DC converters merely based on the on-resistance of the switches and the total flying capacitance. The equation is very general and can be applied to any SC topology by simply re-calculating the equivalent resistance and capacitance. To mitigate the output ripple of the DC-DC converter, the oscillator's biasing network embeds a spur reduction block that allows to reduce its supply sensitivity. At the peak power efficiency of 83%, the DC-DC converter output noise is $< 0.9\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 1 MHz, which does not degrade the inherent phase noise of the oscillator.

To further extend the advantages of the above-mentioned topology, Chapter 6 presents a fully-integrated recursive SC DC-DC converter. To keep the output voltage of the converter relatively constant against input voltages or output current variations, *finite state machine (FSM) based conversion ratio modulation is introduced*. The requirements on the conversion ratio (CR) range, resolution and monotonicity of the output voltage are derived. A *gate-driver circuit* is embedded in all the switches of the converter and guarantees minimum switch on-resistance across PVT variations. The converter has been designed to meet both the oscillator's supply requirements discussed in Chapter 4, as well as the CR requirements and output voltage monotonicity. When compared to the state of the art, the DC-DC converter achieves one of the highest peak efficiencies while 12 different CRs have been implemented with the converter's switching frequency range ratio as little as 4.

## 7.2 Recommendations for Future Work

The results of the research presented in this thesis open new opportunities for further research and development.

It has been discussed that in applications like retinal implants, there is the need to increase the number of stimulating channels, while keeping the number of external components at a minimum. However, in the current architecture, the switching losses increase with the total number of channels implemented. Therefore, there exists a trade-off between the number of channels and the maximum power efficiency that can be achieved by the topology.

An approach to circumvent this problem could be to group the electrodes in several stimulation units (SUs). Each SU is then connected to the only inductor by using an additional switch. Hence, every time a current pulse is generated by the core circuit, the digital control modules indicates which SU is operated and within the SU which pair of electrodes is being used for stimulation. Moreover, the switching frequency of the core circuit should be modulated according to the number of SUs being operated. This allows to increase the number of stimulating channels while limiting the additional losses introduced by the higher number of electrodes.

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# List of Publications

**Journal Papers**

- **A. Urso**, Y. Chen, R. B. Staszewski, J. F. Dijkhuis, S. Stanzione, Y. Liu, W. A. Serdijn and M. Babaie, "A Switched-Capacitor DC-DC Converter Powering an LC Oscillator to Achieve 85% System Peak Power Efficiency and -65 dBc Spurious Tones", in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 11, pp. 3764-3777, Nov. 2020.
- **A. Urso**, Y. Chen, J. F. Dijkhuis, Y. Liu, M. Babaie and W. A. Serdijn, "Analysis and Design of Power Supply Circuits for RF Oscillators," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 12, pp. 4233-4246, Dec. 2020.
- **A. Urso**, V. Giagka, M. van Dongen and W. A. Serdijn, "An Ultra High-Frequency 8-Channel Neurostimulator Circuit With 68% Peak Power Efficiency," in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 13, no. 5, pp. 882-892, Oct. 2019.
- Y. Liu, **A. Urso**, R. M. Da Ponte , T. Costa, V. Valente, V.Giagka, W. A. Serdijn, T. G. Constandinou and T. Denison, "Bidirectional Bioelectronic Interfaces: System Design and Circuit Implications," in *IEEE Solid-State Circuits Magazine*, vol. 12, no. 2, pp. 30-46, Spring 2020.
- **A. Urso**, V. Giagka and W. A. Serdijn, "Comments on "Compact, Energy-Efficient High-Frequency Switched Capacitor Neural Stimulator with Active Charge Balancing"" in IEEE Transactions on Biomedical Circuits and Systems, vol. 13, no. 2, pp. 480-480, April 2019.

**Conference Papers**

- **A. Urso** and W. A. Serdijn, "A Switched Capacitor DC-DC Buck Converter for a Wide Input Voltage Range ," *in IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, May 2018. pp. 1–5.
- A. Das, S. Rout **A. Urso**, and W. A. Serdijn, "Activity Dependent Multichannel ADC Architecture using Level Crossing Quantisation for Atrial Electrogram Recording," *in IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Nara, Oct. 2019, pp. 1–4.

# Summary

This thesis focus on improving the power efficiency of DC-DC converters for two different applications.

In the field of implantable medical devices, electrical stimulation has been used as an established treatment for several diseases. It aims to deliver a well-defined amount of charge to the tissue in order to build up a specific electric field and generate or block an action potential. To achieve a large spatial resolution, there is the need for an increasing number of independent stimulating channels to accommodate a large number of stimulating sites. This, however, increases the overall size of the stimulator while potentially affecting the power efficiency.

In this respect, the first part of this thesis proposes a multi-channel neural stimulator in which the power efficiency does not depend upon the number of channels being operated simultaneously.

On the other hand, in the recently established field of IoT, energy harvesters are increasingly used to ensure a perpetual, but heavily duty-cycled, load operation. However, their typically low output voltage would normally require a boost converter cascaded with a buck converter and low drop-out (LDO) linear regulators to generate multiple supplies of ≈1V VDD nominal voltage to supply nanoscale CMOS circuits and systems. However, LDOs are noisy, bulky and inefficient. Hence, it seems beneficial for IoT devices to be directly connected to the buck converter. However, the lack of (LDO) isolation exposes supply-sensitive blocks such as LC oscillators to the converter output fluctuations that could severely degrade the system performance. In the second part of this thesis (Chapters 4-6), a noise analysis of a switched-capacitor DC-DC converter reveals that those type of voltage regulators can have an output noise level that is much lower than that of LDOs. They are therefore suitable to power up supply-sensitive blocks. This leads to a new scheme in which an SC DC-DC converter directly powers up an LC oscillator, without consuming additional current or requiring any external component.

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