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Study of Back-end DC/DC Converter for 3.7 kW Wireless Charging System according to SAE J2954

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***Abstract*—In a wireless charging system, a back-end DC/DC converter can be used after the coil rectification stage to match the battery charging requirements and to optimize the resonant converter operation. In this paper, a synchronous boost converter is selected according to suggested coil parameters from SAE J2954 standards on a WPT1 3.7 kW power class. This converter is analysed while cascaded to a resonant converter with series-series (S-S) compensation. The semiconductor and inductor losses under hard-switched continuous conduction mode (CCM) and triangular current mode (TCM) are calculated and compared. A benchmark study shows that both the TCM and CCM operations have similar performance of efficiency in constant current (CC) charging profile while TCM has a higher efficiency in the constant voltage (CV) charging profile of a Nissan Leaf EV battery.**

***Index Terms*—S-S, CCM, TCM, Boost Converter, Inductor, Battery**

I. Introduction

The existence of the regulations and standards for wireless charging power transfer (WPT) system facilitates the design compatibility from different manufacturers [1]. The standards of SAE J2954 covers the reference design up to 11.1 kVA input power. Therein, three power level classes are defined [2]: WPT1 for 3.7 kVA system, WPT2 for 7.7 kVA, and WPT3 for 11.1 kVA.

According to [2], the DC input voltage after the grid-connected power factor correction (PFC) stage can vary between 380-500 V of a single-phase grid connection. To charge a conventional electric vehicle (EV) battery, the voltage range of 280-420 V needs to be covered.

When charging an EV battery, the constant current/constant voltage (CC/CV) charging strategy is often used. A battery charging profile of a commercial EV will be used for analysis in this paper. In order to cover the battery voltage required by the J2954 standard, suppose in CC stage, the battery is charged from 280 V to 420 V with a maximum charging power 3.3 kW at 420 V, then, the battery charging enters into CV stage, the charging current drops accordingly. During the CC stage, the battery can be charged up to its 80% of capacity [3]. Take the 2011 Nissan Leaf high voltage battery as an example, its nominal capacity is 24 kWh and its nominal voltage is 360 V [4]. Therefore, for a 24 kWh battery, if the battery is charged from 20% state of charge (SoC) to 80% of SoC, then the charging time is 5.24 h. In the CV stage, with different charging current drop rate, the charged energy will also vary in a certain charging period.

Although, the real charging details can be different, the focus of this paper is to analyse the performance and design freedom of the back-end DC/DC converter in a three conversion stage WPT system. A critical look is given on the operation and efficiency performance of the back-end circuit while operating under different possible charging voltages and currents. Therefore, the charging profile shown in Fig. 1, which is equivalent to a 2011 Nissan Leaf EV, is deemed appropriate to be used for this analysis purpose. The curve uses sampled points to represent the possible battery charging voltages and currents.

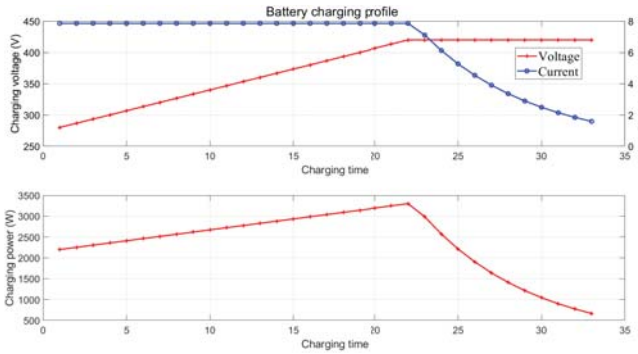

Fig. 1: Battery charging profile used for analysis

In Fig. 1, the battery stops charging at a current which is 20% of the value in the CC stage. As it will be seen later in Section II and III, due to the voltage boost limitation and low efficiency, the charging cut-off point may be shifted earlier under the poor coil coupling in a S-S compensated WPT system.

The paper is organized as follows. Section II describes the possible WPT coil parameters and coupling status based on the standards SAE J2954. This delimits the operating range of the S-S compensated resonant converter stage which is fed by a single-phase PFC circuit. This calls for the use of a boost-type DC/DC converter for the back-end circuit. The operation of a suitable DC/DC boost converter with CCM and TCM mode is explained. In Section III and IV, the inductor design and circuit losses derivation under CCM and TCM are given respectively. Finally, the efficiency performance is compared in Section V.

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II. WPT DC/DC CONVERTER STAGE

A. Compensated S-S resonant and cascaded DC/DC converter

The circuit diagram of a S-S compensated WPT system with a back-end DC/DC converter is given in Fig. 2. Therein, V_{DC} is the input voltage after the PFC converter stage, which is assumed to operate with controlled voltage set as 400 V. V_1 is the input voltage to the back-end DC/DC converter while V_2 is the EV battery voltage. There are three different vertical distance classes (Z-classes) between the ground assembly (GA) and the vehicle assembly (VA) [2]. They are: Z1 = 100-150 mm, Z2 = 140-170 mm and Z3 = 170-250 mm. The ground clearance and the offset position of the coils will influence the coil coupling coefficients [5]. The normative design specifications are given for three different Z-classes and are summarized in Table I. Therein: L_1 and L_2 are the primary and secondary side coil self-inductance respectively; k is the magnetic coupling coefficient and M is the derived mutual inductance.

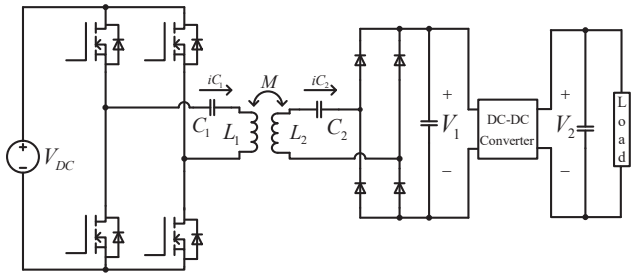


Fig. 2: Circuit of a S-S compensated WPT system with a back-end DC/DC converter

TABLE I: Summary of the parameters

	Z1	Z2	Z3
L_1 min (μH)	185	212	224
L_1 max (μH)	217	223	227
L_2 min (μH)	214	207	198
L_2 max (μH)	232	214	203
k min	0.1	0.085	0.084
k max	0.249	0.221	0.243
M min (μH)	19.89	17.80	17.69
M max (μH)	55.87	48.28	52.16

The maximum and minimum M are calculated through $M_{\max(\min)} = \mathrm{k}_{\max(\min)}\sqrt{L_{1\max(\min)}L_{2\max(\min)}}$.

When the H-bridge inverter of the resonant S-S converter operates at the natural resonant frequency with bipolar-like modulation, e.g. 50% duty cycle, based on first harmonic analysis (FHA) [6], the root-mean-square (rms) current through C_2 is $I_{C_2} = \frac{2\sqrt{2}V_{DC}}{\pi\omega_0 M}$, the average value of the rectified current is $I_{ave} = \frac{2\sqrt{2}}{\pi}I_{C_2} = \frac{8V_{DC}}{\pi^2\omega_0 M}$, therefore, the relation between V_1 and V_{DC} can be expressed by (1):

$$P_o = \frac{8}{\pi^2}\frac{V_{DC}V_1}{\omega_0 M}, \tag{1}$$

where P_o is the output power of the WPT system neglecting losses and ω_0 is the resonant angular frequency. The resonant frequency is chosen as 85 kHz [2]. Based on (1), when the power is fixed, a higher mutual inductance results in a higher voltage of V_1. From Table I, the maximum mutual inductance can be 55.87 μH. Fig. 3 shows the voltages of V_1 and V_2 when $M = 55.87$ μH based on the charging profile in Fig. 1.

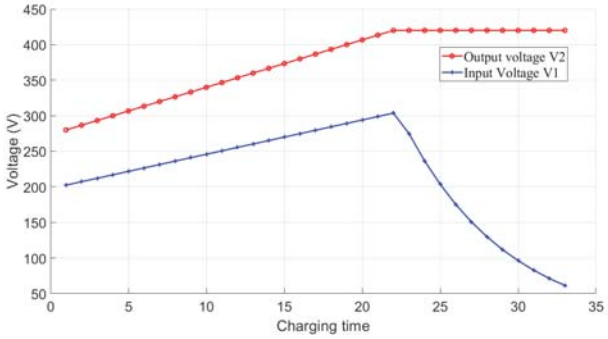


Fig. 3: V_1 and V_2 voltage range when $M = 55.87$ μH

According to Fig. 3, a boost-type circuit needs to be selected as the back-end DC/DC converter. In Fig. 4 the input voltage V_1 range is given with different mutual inductances as delimited by Table I, e.g. M = 20 μH to 50 μH.

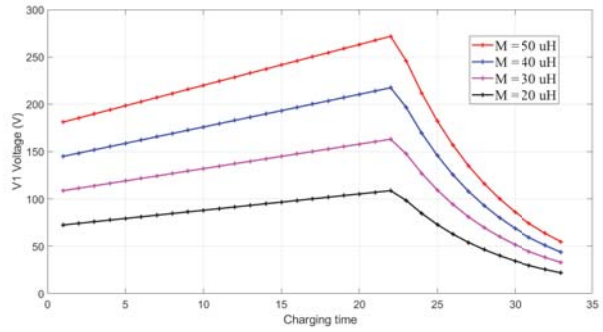


Fig. 4: V_1 range under different mutual inductances

B. Analysis of synchronous boost converter

Fig. 5 shows the circuit diagram of a synchronous boost-type DC/DC converter with inductor current waveforms.

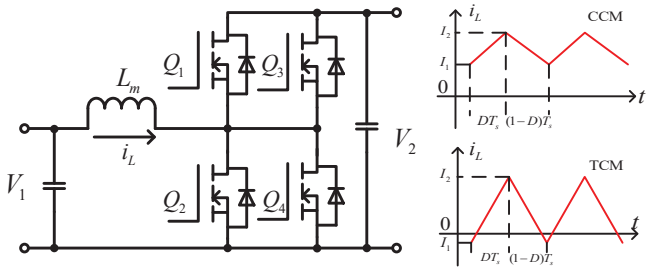


Fig. 5: Circuit of a boost converter with CCM and TCM inductor current waveforms

Both the upper and lower switch consists of two MOSFETs to increase the current rating. The gating signals of switch

Q_1 and Q_2 are complementary. Therefore, the voltage gain is given by (2) under different load conditions.

$$\frac{V_2}{V_1}=\frac{1}{1-D}, \tag{2}$$

where D is the duty cycle of Q_2. Fig. 6 shows the duty cycle at different mutual inductances.

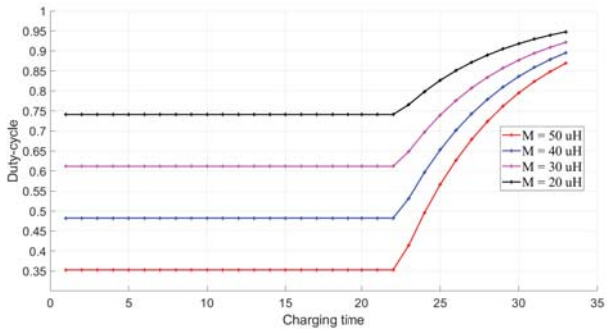


Fig. 6: Duty cycle under different mutual inductances

As it can be seen from Fig. 6, the duty cycle will be relatively high when the output power drops in the CV stage, particularly when M is small.

1) CCM mode: In hard-switched CCM mode, the inductor current is always larger than zero. In order to operate in CCM mode, (3) needs to be satisfied.

$$L_m f_s > \frac{V_2 D(1-D)^2}{2I_o} \tag{3}$$

Where L_m is the indutance, f_s is the switching frequency, I_o is the output current.

In CCM mode, Q_1 can be turned on at zero-voltage-switching (ZVS), however, Q_2 will be hard-switched.

2) TCM mode: In TCM mode, the inductor current becomes negative before Q_2 turns on, therefore, the current through the body-diode of Q_2 enables Q_2 to turn on with ZVS [7] [8]. Fig. 5 shows the inductor current waveforms in TCM mode.

Equation (4) can be written based on Fig. 5:

$$\begin{cases} \frac{I_1+I_2}{2}(1-D)V_2 = P_o \\ I_2 = I_1 + \frac{V_1 D}{L_m f_s}, \end{cases} \tag{4}$$

where I_1 and I_2 are the minimum and maximum inductor current respectively. Based on (2) and (4), switching frequency is:

$$f_s = \frac{1}{2L_m(P_o - V_1 I_1)} \frac{V_1^2(V_2 - V_1)}{V_2} \tag{5}$$

III. Design and Loss Analysis in CCM Mode

In this section, the selection and design of the inductor of the back-end converter will be given and the loss in CCM mode will be derived.

The dominant losses of the semiconductors are the conduction and switching losses. For the consideration of an unipolar semiconductor technology, e.g. MOSFET, the conduction loss is composed of body-diode conduction loss and MOSFET channel conduction loss. The switching loss is composed of the turn-on, turn-off and the body-diode reverse recovery losses [9]. In this paper, the SiC MOSFET C3M0065100K is used. To simplify the calculations, it is assumed that the inductor current is evenly distributed between the parallel MOSFETs. The total circuit switch loss will then be twice the sum of losses of Q_1 and Q_2.

A. Switch loss compositions

1) Channel conduction loss: The conduction loss in the Q_1 MOSFET channel is:

$$P_{Q_1\_cond} = I^2_{Q_1\_rms} R_{ds(on)}, \tag{6}$$

where $R_{ds(on)}$ is the on-state resistance, $I_{Q_1\_rms}$ is the rms current through the channel of Q_1. Similar expression can be derived for the conduction loss of Q_2

2) Body-diode conduction loss: In hard-switched CCM mode, only the upper MOSFET diode will conduct during the dead time (Refer to Fig. 5).

The body-diode conduction loss of Q_1 is:

$$P_{Q_1\_diode} = V_F(\frac{I_1}{2} + \frac{I_2}{2}) t_{dead} f_s \tag{7}$$

Where V_F is the diode forward conduction voltage, t_{dead} is the dead time between gate pulses, $I_1 = I_L - \frac{1}{2}\Delta I$, $I_2 = I_L + \frac{1}{2}\Delta I$. $I_L = \frac{I_o}{1-D}$ is the average inductor current and $\Delta I = \frac{V_1 D}{L_m f_s}$ is the inductor current ripple.

3) Switching loss: Since the upper MOSFETs turn on at ZVS and the channel current shifts to the body-diode when it is turned off, only the switching loss of the lower MOSFETs needs to be considered. A reasonable assumption is to scale the switching loss linearly [4] or nonlinearly [10] as below:

$$P_{sw} = f_s E_{on+off} (\frac{I_{ds}}{I_{ref}})^{K_i} (\frac{V_{ds}}{V_{ref}})^{K_v}, \tag{8}$$

where I_{ref} and V_{ref} are the reference current and voltage, I_{ds} is the drain current and V_{ds} is the drain source voltage, K_i and K_v are the scaling coefficients. However, both E_{on} (turn-on energy) and E_{off} (turn-off energy) depend on the value of the flowing drain current, therefore using a second order polynomial to calculate the switching loss is adopted here [11]. Fig. 7 shows the switching energy with different drain currents from the C3M0065100K datasheet with a 2.5 Ω gate resistor [12].

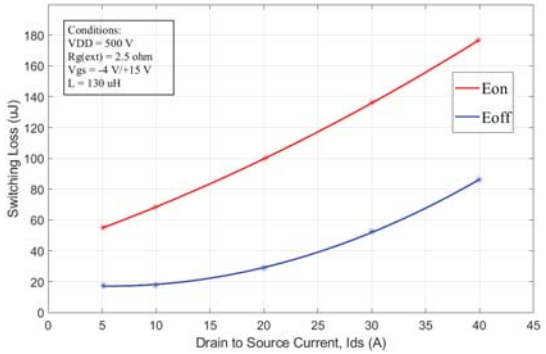


Fig. 7: Switching energy under different drain current

The marked points in Fig. 7 are the ones from the datasheet. Through curve fitting, the switching energy can be expressed by:

$$E_{on}(I_{ds}) = 0.0249I_{ds}^2 + 2.3733I_{ds} + 42.256 \ \mu\text{J} \quad (9)$$

$$E_{off}(I_{ds}) = 0.0587I_{ds}^2 - 0.6613I_{ds} + 18.941 \ \mu\text{J} \quad (10)$$

Therefore, the switching loss of Q_2 is calculated by:

$$P_{Q_2\_sw} = \frac{V_2}{V_{ref}} E_{on}(\frac{I_1}{2}) f_s + \frac{V_2}{V_{ref}} E_{off}(\frac{I_2}{2}) f_s \quad (11)$$

4) Reverse recovery loss: Only the upper MOSFETs body-diodes will have the reverse recovery loss which is:

$$P_{Q_1\_rr} = Q_{rr} V_2 f_s, \quad (12)$$

where Q_{rr} is the reverse recovery charge.

B. Selection of the Back-end converter inductor

A higher switching frequency will lead to a more compact design with smaller passive components while the switching loss will be higher. In this paper, the switching frequency for the DC/DC converter is defined from 20 kHz to 100 kHz. Based on (3), the boundary inductance to make the converter operate in CCM mode is given by Fig. 8 when $f_s = 40$ kHz.

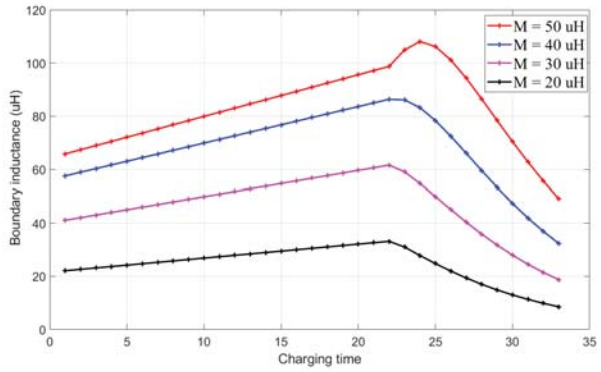
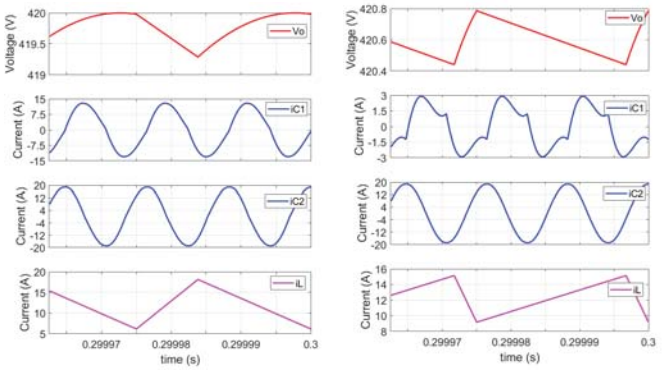


Fig. 8: Boundary inductance when f_s = 40 kHz

From Fig. 8, the inductance can be selected larger than 110 μH to make the converter operate in CCM mode. A larger inductance results in a small current ripple, however, the size of the inductor will also become larger. Here, the inductance is chosen as 200 μH and f_s = 40 kHz for the remains of the analysis.

Fig. 9 shows the simulation results in CCM mode when $M = 50$ μH. L_1 and L_2 are chosen as 200 μH and 220 μH respectively. iC1 and iC2 are the primary and secondary side resonant current (Refer to Fig. 2), iL is the inductor current.



(a) Charging at 420 V 3.3 kW (b) Charging at 420 V 666 W

Fig. 9: Simulation waveforms at CCM when $M = 50$ μH

C. Semiconductor Loss

1) Semiconductor loss at different frequencies: Based on the analysis above, the switch loss (loss of four total MOSFETs, same as below) under different switching frequencies can be derived. Fig. 10 shows the result when $M = 50$ μH.

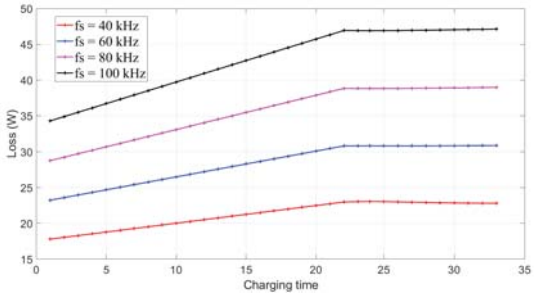


Fig. 10: Switch loss at different frequencies

2) Semiconductor loss at different mutual inductances: Fig. 11 shows the semiconductor loss under different mutual inductances when f_s is 40 kHz.

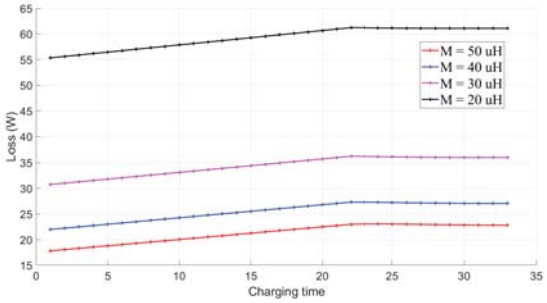


Fig. 11: Switch loss at different mutual inductances

From Fig. 11, the semiconductor loss under 20 μH mutual inductance is much higher than others. Due to the lower input voltage at a lower mutual inductance, the conduction loss increases considerably.

D. Inductor design and loss

Inductor design is based on the area product method, the product of window area (A_w) and core cross section (A_e) is:

$$A_p = A_e A_w = \frac{L_m \hat{I} I_{rms}}{J_c k_w \hat{B}}, \tag{13}$$

where J_c is the current density, k_w is the window usage factor, $\hat{B}$ is the peak flux density, L_m is the inductance, $\hat{I}$ is the peak current. Based on (13) the inductor is designed when M is 20 μH and it can be made by attaching two sets of E70/33/32 cores together in parallel. The number of turns and air gap length are:

$$N = \frac{L_m \hat{I}}{A_e \hat{B}} \tag{14}$$

$$l_g = \frac{N^2 A_e \mu_0}{L_m} - \frac{l_e}{\mu_r}, \tag{15}$$

where μ_0 is the air permeability, μ_r is relative permeability and l_e is the effective magnetic path length of the core. Assuming a maximum magnetic flux density of 0.26 T, the winding turns is calculated to be 20 and air gap length is 3.345 mm.

The core loss can be estimated through Steinmetz equation. Traditional Steinmetz equation (SE) for gapped magnetic cores can be found in [13]. Improvements of the traditional Steinmetz equation including the modified Steinmetz equation (MSE) [14], improved generalized Steinmetz equation (iGSE) [15] and natural Steinmetz equation (NSE) [16] can be applied to get a more accurate core loss result. Both iGSE and NSE will lead to a same result in this paper's application. An example applying MSE to a DC/DC converter can be found in [17]. Due to the more accuracy of iGSE compared with MSE proved in [15], the iGSE method will be used here. Although a further check shows that the core loss derived through these methods does not differ much in this application. (16) shows the traditional SE and (17) shows the iGSE.

$$P_{core\_SE} = k f^{\alpha} \hat{B}^{\beta} V_e \tag{16}$$

$$P_{core\_iGSE} = \frac{1}{T_s} \int_0^{T_s} k_i \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} V_e dt, \tag{17}$$

where k, α and β are the Steinmetz coefficients, ΔB is the peak to peak flux density, $\hat{B}$ is the peak flux density which equals to $\frac{\Delta B}{2}$, V_e is the core volume and k_i can be expressed as (18) when α is from 0.5 to 3 [15].

$$k_i = \frac{k}{2^{\beta+1}\pi^{\alpha-1}(0.2761 + \frac{1.7061}{\alpha+1.354})} \tag{18}$$

Based on (17), the equation to calculate the core loss can be expressed as:

$$P_{core\_iGSE} = k_i \Delta B^{\beta} \frac{1}{T_s^{\alpha}} [D^{1-\alpha} + (1-D)^{1-\alpha}] V_e \tag{19}$$

For N87 material, the Steinmetz coefficients are $k = 4.17$, $\alpha = 1.36$, $\beta = 2.64$ at 100 °C based on SI unit derived from the curve fitting of [18] and k_i is then 0.245.

Dowell's equation is used to estimate the winding loss [19]:

$$\frac{R_{ac}}{R_{dc}} = \Delta\left[\frac{\sinh 2\Delta + \sin 2\Delta}{\cosh 2\Delta - \cos 2\Delta} + \frac{2(p^2-1)}{3} \frac{\sinh \Delta - \sin \Delta}{\cosh \Delta + \cos \Delta}\right] \tag{20}$$

Where p is the number of layers, as for Δ of solid-round-wire winding, it is: $\Delta = \sqrt[x]{\frac{\pi}{4}} \frac{d}{\delta_0} \sqrt{\eta}$, x is chosen as 0.75 in [20], and 1 in [21]. The diameter of the winding wire is d, δ_0 is the skin depth, η is the porosity factor defined as d/l, herein, l is the distance between the centers of adjacent round conductors in the same winding layer.

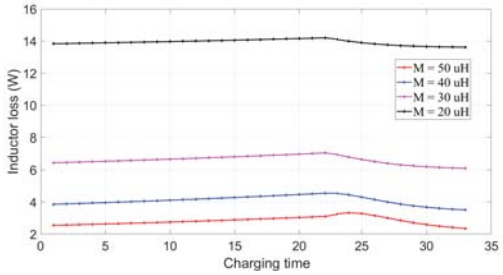
At 40 kHz, the skin depth is $\delta_0 = 0.375$ mm at 100 °C [22]. The diameter of the selected wire could be less than twice the skin depth. Since the rms current at 3.3 kW when $M = 20$ μH is 30.5 A, the Litz wire of 0.3 mm strand diameter with 75 strands is used with an equivalent cross section area of 5.3 mm^2. The windings have two layers with 10 turns for each layer. During calculation based on (20), it is assumed that the Litz wire is arranged $\sqrt{n} \times \sqrt{n}$ in a bundle (n is the number of strands).

The total winding loss can be calculated by (21) [19]:

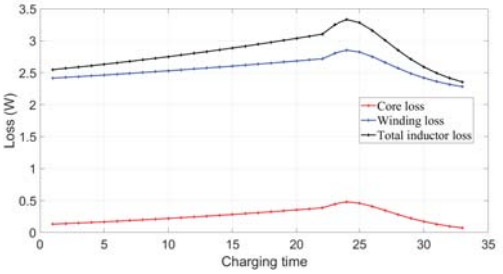
$$P = R_{dc} I_{dc}^2 + R_{dc} \sum_{n=1}^{\infty} k_{pn} I_n^2 \tag{21}$$

where k_{pn} is the ac resistance factor at the nth harmonic frequency and I_n is the nth harmonic rms current. Here, only the first harmonic will be considered. The first harmonic rms value of a non-symmetrical triangle wave is: $|\frac{\Delta I \sin(\pi D)}{\sqrt{2} D(1-D)\pi^2}|$ (Refer to Fig. 5, $\Delta I = I_2 - I_1$ is the current ripple).

With the dimensions of the core and copper resistivity, the calculated R_{dc} is 14.8 mΩ and R_{ac} at fundamental frequency is 48 mΩ. Fig. 12 shows the inductor loss at different mutual inductances and also the core and winding losses when $M = 50$ μH.



(a) Inductor loss at different mutual inductances



(b) Core and winding loss when $M = 50$ μH

Fig. 12: Inductor loss at CCM mode when $f_s = 40$ kHz

IV. Design and Loss analysis in TCM mode

In this section, the inductor design and loss calculation of TCM mode will be described in detail.

A. Inductance selection

To realise TCM mode operation, the frequency can be fixed or adapted. In [23], the switching frequency was fixed for TCM mode, however, the current ripple can be higher compared with the one with a fixed I_1, thus leading to a higher rms value. Therefore, in this paper the switching frequency is adapted accordingly to keep the current I_1 constant.

The absolute value of I_1 should not be too small, otherwise, the reverse current can not charge Q_1 and Q_3, and discharge Q_2 and Q_4. I_1 can be estimated through $|I_1|= 4C_{oss}\frac{\Delta V}{\Delta t}$, where C_{oss} is the MOSFET output capacitance which is around 80 pF at V_{ds} = 400 V [12], ΔV is the output voltage and assuming Δt is 100 ns, substitute these data, I_1 is -1.344 A, then, I_1 = -2 A is selected.

The product of L_m and f_s can be calculated based on (5), considering that the frequency set from 20 kHz to 100 kHz, then L_m can be selected as 40 μH. However, with L_m = 40 μH, when M is 20 μH and 30 μH, the switching frequency of some charging points at CV stage will be lower than 20 kHz as given in Fig. 13. The loss will be only calculated above 20 kHz in this paper.

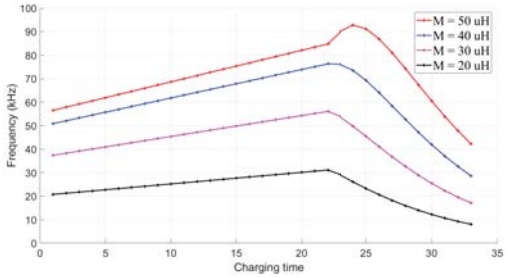
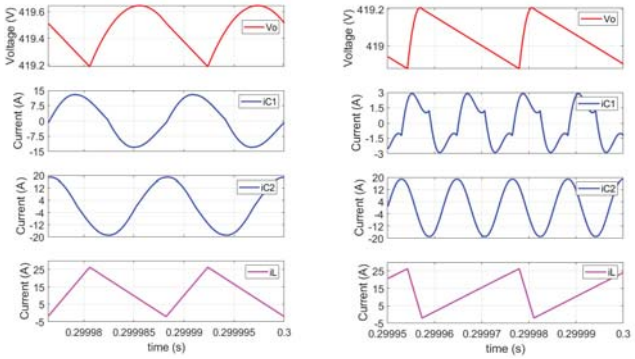


Fig. 13: TCM switching frequency at different mutual inductances

B. Simulation waveforms

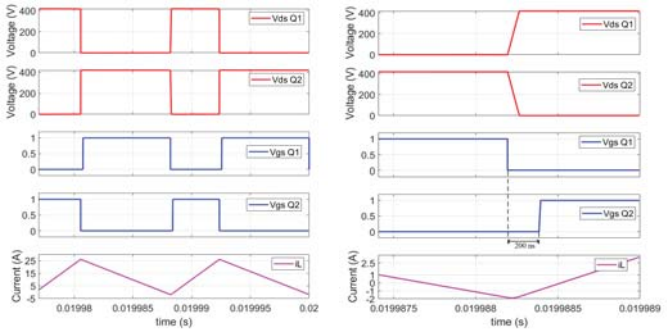
Fig.14 shows the simulation results at 3.3 kW and 666 W charging power when $M = 50$ μH.



(a) Charging at 420 V 3.3 kW (b) Charging at 420 V 666 W

Fig. 14: Simulation waveforms at TCM when $M = 50$ μH

From simulation results, the minimum inductor current is kept at -2 A. Fig. 15 shows the turn-on and turn-off transients with the MOSFET parameters R_{ds} = 90 mΩ, C_{oss}= 80 pF and dead-time of 200 ns at maximum input voltage of the DC/DC converter. The reason to use a maximum input voltage is that since the inductance value is smaller in TCM mode, a longer dead time with a high input voltage may not result in ZVS for the lower switches.



(a) Turn-on and off transients (b) Zoom-in of transients

Fig. 15: Simulation waveforms at turn-on and off transients

As can be seen from Fig. 15, the lower switch is also turned on at ZVS.

C. Semiconductor loss

Now, both the upper and lower switches turn-on at ZVS. There is also no body-diode reverse recovery loss.

The turn-off loss of Q_1 is:

$$P_{Q_1\_off} = \frac{V_2}{V_{ref}} E_{off}(\frac{|I_1|}{2}) f_s - \frac{1}{2} C_{oss} V_2^2 f_s \qquad (22)$$

The turn-off loss of Q_2 is calculated in a similar way. The body-diode conduction loss of Q_1 is:

$$P_{Q_1\_diode} = \frac{1}{2} V_F I_2 t_{dead} f_s \qquad (23)$$

The body-diode conduction loss of Q_2 is calculated in a similar way. Fig. 16 shows the switch loss under TCM mode at different mutual inductances.

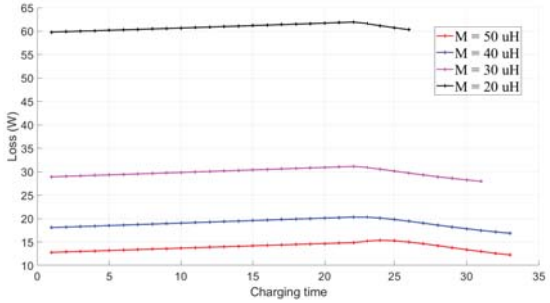


Fig. 16: Semiconductor loss of TCM mode at different mutual inductances

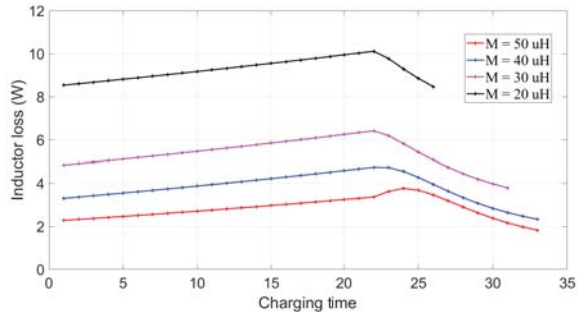
D. Inductor loss

The design and loss calculation of the inductor can follow the previous procedures described in CCM mode operation. Unlike in CCM mode, the inductor peak and rms current are constant once the mutual inductance is determined, the expressions for these two currents are given below:

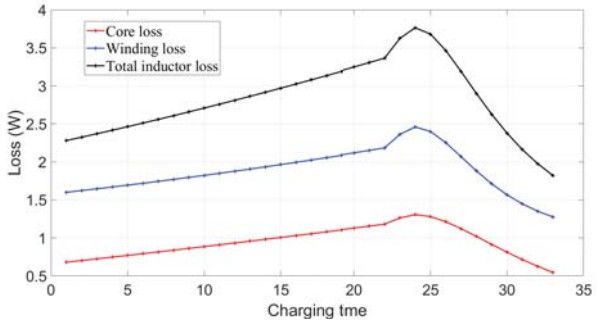
$$I_2 = \frac{16V_{DC}}{\pi^2\omega_0 M} - I_1 \tag{24}$$

$$I_{L\_rms} = \sqrt{\frac{1}{3}[(\frac{16V_{DC}}{\pi^2\omega_0 M})^2 - \frac{16V_{DC}}{\pi^2\omega_0 M}I_1 + I_1^2]} \tag{25}$$

When $M = 20$ μH, the peak current $I_2 = 62.7$ A and $I_{L\_rms} = 35.6$ A. One set of E70/33/32 is adopted with 14 turns winding, the air gap is calculated to be 4.12 mm. The skin depth at 100 kHz is 0.238 mm at 100 °C [22]. Litz wire of 0.2 mm strand diameter with 200 strands is used which has an equivalent cross section area of 6.28 mm^2. For loss calculation, suppose the windings have two layers with 7 turns of each layer. The calculated R_{dc} is 5.4 mΩ. Fig. 17 shows the inductor loss of TCM mode at different mutual inductances and also the core and winding loss when $M = 50$ μH.



(a) Inductor loss with different mutual inductances



(b) Core and winding loss when $M = 50$ μH

Fig. 17: Inductor loss at TCM mode

V. Efficiency comparison

The power efficiency considering the sum of losses from the semiconductor and inductor is compared at different mutual inductances under hard-switched CCM and soft-switched TCM operation modes. Fig. 18 shows the calculated efficiency comparison results. The efficiency is calculated through $\eta_e = \frac{P_o}{P_o + P_{loss}}$, where P_{loss} represents the sum of loss from the switches and the inductor.

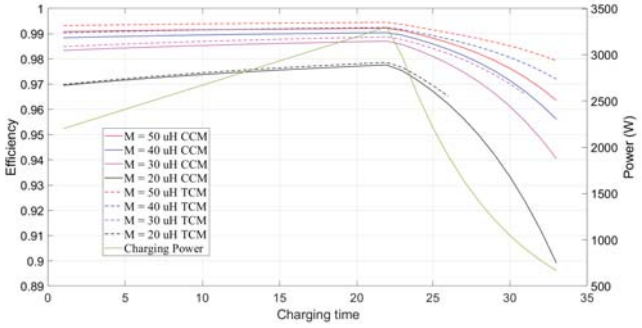


Fig. 18: Efficiency comparison at CCM and TCM modes during charging profile

As it can be seen from Fig. 18, the efficiency in TCM mode is always higher than that in CCM mode especially in the CV charging stage. However, several points should be clarified here.

Firstly, due to the ZVS realization at TCM mode, the turn-on loss of the lower switches is eliminated, besides, there is no reverse recovery diode loss for both the upper and lower switches.

Secondly, from Fig. 10, a lower switching frequency leads to a lower total switch loss, therefore, if the hard-switched CCM mode operates at a lower frequency, the efficiency will improve, however, the trade-off is that a larger inductor may be needed.

Thirdly, for the inductor loss, comparing Fig. 12 and Fig. 17, although the core loss of the CCM mode is lower because of the smaller current ripple, due to the larger size of the core and the number of winding turns, the copper loss of the CCM mode is higher.

Fourthly, the efficiency for both CCM and TCM modes drops at CV stage due to the decrease of both the charging power and the input voltage of the boost converter.

Finally, TCM mode suffers from a large frequency variation, besides, the peak current is too high in this application when the mutual inductance is low, for example, the peak inductor current is 62.7 A when $M = 20$ μH which poses a high current requirement to the semiconductors.

VI. Conclusion and future work

This paper studies the back-end DC/DC converter based on the 3.7 kW wireless charging system specified in the SAE J2954 standards. The topology of synchronous boost converter is selected accordingly. Two modulation methods: CCM and TCM are studied and compared. Both modulation methods have similar efficiency performance while TCM shows a minor lead in the CC charging stage and a major lead in the CV stage. Also, the inductor size required for TCM mode is smaller than that for the CCM mode. However, TCM mode needs a large switching frequency range, besides, the peak inductor current and the switch current are considerably larger than those in CCM mode. However, this does not pose a considerable disadvantage in relation to power efficiency.

A prototype needs to be built in the future to verify the design and theoretical analysis developed in this paper.

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