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# A 10 kW Solar-Powered Bidirectional EV Charger Compatible With Chademo and COMBO

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**Abstract**—Charging electric vehicles (EVs) from photovoltaic panels (PV) provides a sustainable future for transportation. This paper presents the development of a 10 kW EV charger that can be powered from both a PV array and the three-phase ac grid. The goal is to realize a high power density and high-efficiency three-port power converter that integrates the EV, PV, and grid and meets the Chademo and combined charging standard/Combo EV charging standards. The EV port is designed to be isolated and bidirectional, so that both charging and vehicle-to-grid can be implemented. As PV and EV are both dc by nature, the converter uses a central dc link to exchange power between the EV and PV, thereby increasing efficiency. The use of silicon carbide devices and powdered alloy core inductors enables high switching frequency and power density. The closed-loop control allows four different power flows: PV → EV, EV → grid, grid → EV, and PV → grid. Hence, the converter operates as a PV inverter, a bidirectional EV charger, and a combination of both. A 10 kW prototype has been successfully tested, and its experimental waveforms and measured efficiency are presented. It has three times the power density and higher partial and peak load efficiency when compared to existing solutions.

**Index Terms**—Charging, electric vehicle (EV), photovoltaic systems (PV), powered alloy core, silicon carbide (SiC).

## NOMENCLATURE

$P_{\text{nom}}$	Nominal power of the converter.	$V_{\text{dc}}^*, V_{\text{dc}}$	Nominal and actual dc-link voltage.
$V_{\text{ac}}, I_{\text{ac}}, P_{\text{ac}}$	RMS voltage, current, and nominal power of ac grid connection, respectively.	$f_{\text{sw}}$	Switching frequency.
$V_{\text{pv}}, I_{\text{pv}}, P_{\text{pv}}$	PV maximum power point voltage, current, and power, respectively.	$N_i$	Number of interleaved stages.
$\Delta I_{\text{in}}, \Delta I_{\text{in}(p-p)}\%$	PV current ripple and in percentage, respectively (peak–peak).	$D$	Duty cycle of the switch (for both IBC and IBFC).
$\Delta V_{\text{pv}(p-p)}$	PV voltage ripple (peak–peak).	$d_1$	Duty cycle of diode conduction in the IBC.
$V_{\text{ev}}, I_{\text{ev}}, P_{\text{ev}}$	EV voltage, current, and (dis)charging power, respectively.	$\Delta I_L$	Inductor ripple current (peak–peak).
$P_{\text{loss}}$	Total losses in the power converter.	$I_{L(\text{max}), I_{L(\text{min})}}$	Maximum and minimum inductor current.
		$N_{\text{on}}$	Maximum number of switches that are simultaneously ON in the IBC.
		$A_L$	Permeance of the core.
		$A_c, V_c$	Core area and volume of the core, respectively.
		$l_e$	Magnetic path length of the core.
		$B_{\text{max}}$	Maximum flux density in the core during operation.
		$\Delta B$	Peak–peak change in flux density of the core ( $B_{\text{pk}} = \Delta B/2$ ).
		$P_L$	Total inductor/transformer losses.
		$P_{\text{core}}, P_{\text{cu}}$	Core losses and winding copper losses of the inductor, respectively.
		$P_v$	Core losses of inductor per unit volume.
		$R_L$	Inductor winding resistance.
		$f_{\text{eq}}$	Equivalent frequency for the modified Steinmetz equation.
		$I_L$	Inductor winding current.
		$C_{\text{in}}$	Input capacitance of the IBC.
		$P_S$	Total losses in the switch (conduction and switching losses).
		$P_{S,\text{con}}, P_{S,\text{sw}}$	Conduction losses and switching losses of the switch, respectively.
		$I_{\text{DS}}$	Switch drain–source current.
		$R_{\text{DS(on)}}$	Switch ON-state resistance.
		$V_{\text{DS}}, V_{\text{DS(max)}}$	Switch drain–source voltage and its maximum value, respectively.
		$T_j$	Semiconductor device junction temperature.
		$T_a$	Ambient temperature.
		$V_{\text{GS}}$	Switch gate voltage.
		$R_G$	Switch gate resistance.
		$E_{\text{on}}$	Turn-ON energy of the switch.
		$E_{\text{off}}$	Turn-OFF energy of the switch.
		$I_D$	Diode current.
		$P_D$	Total losses in the diode (conduction and switching losses).

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$P_{D,\text{con}}$ , $P_{D,\text{sw}}$	Diode conduction losses and turn-OFF losses, respectively.
$V_{R,D}$	Diode reverse voltage in the OFF state.
$U_{D0}$	Diode forward voltage during the ON state.
$R_D$	Diode equivalent series resistance.
$E_{D\text{ch}}$	Energy stored in parasitic junction capacitance of the diode.
$P_{\text{filter}}$	Total losses in input, output, and EMI filters.
$P_{\text{ctrl}}$	Power consumed by the control circuit.
$D_1$	Duty cycle of diode conduction in the IBFC.
$I_{L1A(\text{pk})}, I_{L3A(\text{pk})}$	Peak current of primary and secondary winding of a flyback transformer, respectively.
$k, M$	Coupling coefficient and mutual inductance of a flyback transformer, respectively.
$E_L$	Energy stored in the flyback inductor.
$V_{\text{trans}}$	Transient voltage overshoot on MOSFET due to leakage inductance.
$T_F$	Half the time period for quasi-resonance.
$I_{\text{ev}(m)}$	EV current at the output of one of the four interleaved IBFCs, $I_{\text{ev}(m)} = I_{\text{ev}} / 4$ .
$V_{\text{valley}}$	Quasi-resonance valley voltage during switch turn ON.
$C_{\text{ds}(\text{net})}$	Net drain-source capacitance across primary-side MOSFET in the IBFC.
$C_{\text{ds},S}$	Output capacitance of the MOSFET.
$C_{\text{DD}}$	Parasitic junction capacitance of the diode.
$C_{\text{xmer}}$	Parasitic capacitance of transformer winding.
$g$	Inductor air gap.
$C_{\text{ev}(\text{net})}$	EV-side output filter capacitor of the IBFC.
$E_{\text{QR}1}$	Turn-ON energy due to the discharging of the MOSFET-side QR capacitor.
$E_{\text{QR}2}$	Turn-ON energy due to charging of the diode-side QR capacitor.
$C_{\text{dc}}$	DC-link capacitance.

## I. INTRODUCTION

LECTRIC vehicles (EVs) are considered to be the future mode of transportation. They are more efficient and have no emissions when compared to fossil fuel powered vehicles. However, EVs are currently charged from an electricity grid whose fuel mix is mainly dominated by fossil fuels [1]. In order to make EVs sustainable, it is essential to charge EVs from sustainable sources of electricity. Hence, the charging of EVs from photovoltaic (PV) panels is a sustainable proposition for the future [2]–[5].

At the same time, PV generation is characterized by both diurnal and seasonal variations. This necessitates a grid connection to ensure reliable power supply for charging the EVs. Workplaces like office buildings, factories, and industrial area are ideal places to facilitate solar EV charging where the building rooftops and car parks can be installed with PV panels. There are several advantages to charging EVs from PV.

- 1) EV charging power demand on the grid is reduced as the charging power is locally generated by PV.
- 2) EV battery can serve as an energy storage for the PV and reduces the negative impact of large-scale PV integration in the distribution network [6].
- 3) Long parking time of EVs at workplaces results in low charging power requirements and enables implementing vehicle-to-grid (V2G) technology, where the EVs act as a controllable power source [7], [8].

### A. Literature Review

In order to charge EVs from PV, separate converters for the EV and PV that are connected to the ac grid can be used [9], [10]. Alternately, a single integrated converter that connects to the EV, PV, and grid can be utilized [3]. A key requirement of the EV charging standards is that the EV charger must be isolated from all power sources, namely, PV and the grid [11]–[13].

Several studies have presented a three-port power converter for charging the EV from PV. Direct dc charging of the EV from PV using a zero voltage transition (ZVT) pulselwidth modulation (PWM) buck converter interlinked on a 210 V dc bus was presented in [14], [15]. A closed-loop control was developed, and a 2.4 kW prototype is built that offers EV charging but not V2G. In [16], a dc nanogrid is used for charging the EV from PV, fuel cells, and the ac grid, and 1.5 kW dc–dc full-bridge *LLC* resonant converter is used as a building block for the system. In [17] and [18], a 3.3 kW bidirectional three-port converter with 380 V dc link was made that integrates EV, PV, and single-phase ac grid. The integrated converter showed an improved efficiency of 7–15% when compared to separate converters for EV and PV. A total of two dc–dc converters were used for charging an EV from PV via a 48 V buffer battery in [19]. The 3.3 kW system does not have bidirectional power flow connection to the grid or isolation for the EV. In [20], a solar charging system for e-scooters is developed with single-phase V2G/V2H (vehicle to home) functionally using  $2 \times 12$  V low-voltage batteries. Buck and boost converters are used for the dc–dc power conversion and an H-bridge for the inverter operation.

In the above-mentioned studies, the designs are not suited for three-phase high-power applications ( $>5$  kW). There is no consideration for the EV charging standards with respect to charging current ripple, EMI, and/or isolation. Similarly, a review of several EV–PV topologies concluded that most designs neglected the EV isolation requirements [3].

In [21] and [22], a high-frequency ac link based on a multi-winding transformer was used for integrating EV, battery storage, and renewable energy sources. While the topology provides the benefit of isolation between all the ports and is applicable for high powers, it is not useful for EV–PV application because of two reasons. European regulations do not stipulate a need for isolation between the PV and the grid. Second, PV and EV are both dc by nature, so the ac link will lead to unnecessary conversion steps.

A 10-kW, nonisolated, bidirectional converter to charge the EV from PV is presented in [23]. A 575 V dc bus is used to

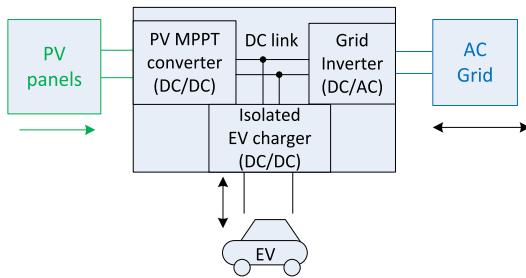


Fig. 1. Block diagram of the grid-connected bidirectional 10 kW three-port EV-PV charger.

integrate EV, PV, and grid, and the closed-loop control is designed to reduce PV intermittency. A symmetrically isolated 5 kW Z-source converter was used for EV charging from PV in [24]. The performance was compared with transformer-less and high-frequency transformer-isolated topologies indicating the overall superiority of the Z-source converter. Similarly, a 3.3 kW prototype of a solar EV charger based on the modified Z-source inverter with isolation is proposed in [25]. However, the Z-source topologies cannot be modularly scaled up for higher powers, require large passive components to make the impedance network, and have a high ripple at the PV port reducing the efficiency of the maximum power point tracking (MPPT).

### B. Contributions

This paper presents the development of a high power density, modular, V2G-enabled, integrated power converter for charging EVs from PV panels and the ac grid. Fig. 1 shows the block diagram of the three-port converter for solar charging of the EV with a central dc link. There are three subconverters inside: a unidirectional dc–dc converter for the PV, a bidirectional dc–ac inverter to connect to the ac grid, and a bidirectional isolated dc–dc converter for the EV. DC charging of the EV is implemented here as opposed to ac charging as Chademo and combined charging standard (CCS) facilitates smart charging, fast charging, and V2G [12], [26], [27]. Smart charging can enable the EV charging to follow the PV generation, energy prices, and regulation prices [28], [29].

The developed three-port architecture has three advantages. First, since EV and PV are inherently dc by nature, an internal dc link is used to exchange power among the three subconverters. Second, the grid inverter is intrinsically bidirectional as it needs to feed PV power to the grid and draw EV charging power from the grid. Hence, by making the isolated dc–dc converter for EV bidirectional as well, V2G operation can be implemented. Third, a single dc–ac inverter is sufficient to connect both PV and EV to the grid. This makes the converter cheaper and smaller. Typically, if an integrated converter is not used, two inverters would be needed, one each for PV and EV.

The critical aspects of the converter design are achieving high efficiency, high power density, modularity, and low cost. The contributions of this work compared to earlier works are

- 1) Developing a high power bidirectional, isolated, three-port power converter for direct dc charging of an EV from

PV and ac grid. It can be seen from the literature review that such a converter does not currently exist.

- 2) The combined use of silicon carbide (SiC) devices, high switching frequency, interleaving, and KoolM $\mu$  inductors has resulted in the developed converter to have much higher partial and peak load efficiency and three times the power density when compared to existing solutions.
- 3) Designing a closed-loop control that enables four different power flows using the converter: PV → EV, PV → grid, grid → EV, and EV → grid (i.e., V2G).
- 4) The developed converter is modularly built to be operated either as a dc V2G EV charger or as a solar-powered dc V2G EV charger. Furthermore, several dc V2G EV charger modules can be operated in parallel to scale up the power from 10 up to 100 kW for fast charging of EVs. State-of-the-art solar EV chargers do not exhibit such high levels of modularity.
- 5) The converter is designed to be compatible with IEC, Chademo, and CCS/Combo dc charging standard with respect to ripple, harmonic, voltage range, and isolation requirements, and the charge/V2G operation has been tested using a Nissan Leaf EV. Currently developed solar EV chargers do not meet these criteria for commercial usability.

### C. Paper Organization

Section II describes the specifications of the EV–PV power converter and requirements from the EV charging standards. Sections III, IV, and V provide the detailed design procedure and loss models for the isolated dc–dc converter for the PV, bidirectional dc–ac grid inverter, and the dc–dc converter for the EV charging, respectively. Section VI presents the closed-loop control for each of the three subconverters. Section VII describes the experimental prototype developed and measured waveforms and efficiency of the three-port converters. Section VIII presents the conclusion.

## II. EV–PV POWER CONVERTER

### A. Specifications

Table I shows the specifications of the three-phase, grid-connected EV–PV power converter. The voltage range, isolation, and ripple requirements are compatible with the EV charging standards [11], [13]. A 10 kW<sub>p</sub> PV array connected to the PV port is the primary power source. The internal dc-link voltage is rated at 750 V. As the maximum EV current  $I_{ev}$  is 30 A, power curtailment occurs at low EV voltages, as shown in Fig. 2. The critical operating point is when EV voltage  $V_{ev}$  is 333.3 V, where both maximum power and maximum current have to be supplied to the EV battery.

The power difference among the EV charging demand  $P_{ev}$ , PV power  $P_{pv}$ , and the converter losses  $P_{loss}$  is met by the grid power  $P_{ac}$ . For V2G operation,  $P_{ev}$  is negative. The power balance equation is

$$P_{ac} = P_{ev} - P_{pv} + P_{loss}. \quad (1)$$

TABLE I  
SPECIFICATIONS OF A 10 KW EV–PV CONVERTER

Parameter	Symbol	
PV MPPT Voltage, Current	$V_{pv}, I_{pv}$	350–700V, 0–30A
PV current ripple (pk-pk)	$\Delta I_{in(p-p)}\%$	< 10% of $I_{pv(max)}$
PV voltage ripple (pk-pk)	$\Delta V_{pv(p-p)}$	<500mV
EV voltage	$V_{ev}$	50–500V
EV current	$I_{ev}$	-30A to +30A
Internal DC-link voltage	$V_{dc}$	750V
EV current ripple (rms)	$\Delta I_{ev(rms)}$	<1 Arms @ 10kW
EV voltage ripple (pk-pk)	$\Delta V_{ev(p-p)}$	<500mV
Nominal AC connection	$V_{ac}, I_{ac}$	400V, 50Hz, 16A
Isolation monitoring @ PV		800kΩ
Isolation for EV		4kV (Input-Output)

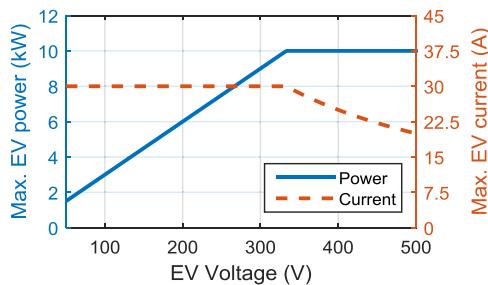


Fig. 2. Maximum power and current of the EV charger for different EV battery voltages.

### B. Topology

Fig. 3 shows the topology of the three subconverters in the EV–PV charger: an interleaved boost converter (IBC) for the PV, an interleaved bidirectional flyback converter (IBFC) for the EV, and a three-phase voltage source inverter for the ac grid. The neutral of the ac grid is connected to the midpoint of the dc link. The flyback converter is operated in a quasi-resonant (QR) mode to achieve soft switching, while the PV and grid converter are operated with hard switching.

### C. Achieving High Efficiency and High Power Density

The EV–PV power converter has four different power flows: PV → EV, PV → grid, grid → EV, and EV → grid. It is, hence, essential to ensure high efficiency for the four power flows. In particular, high partial-load efficiency is vital as smart charging is done by controlling the charging power below the rated power. Second, it is crucial that the converter has a high power density and occupies less space when installed at the parking lot. In order to achieve these two objectives, three techniques are implemented: interleaving, use of silicon carbide (SiC) devices, and powdered alloy core inductors.

Interleaving is used in the both PV and EV dc–dc converters, with the use of three and four interleaved stages, respectively. Interleaving has four advantages.

- 1) Current through the switches and inductors in each leg is reduced by a factor of  $(1/N_i)$ , where  $N_i$  is the number of interleaved stages. Thus, smaller inductors and lower-rated switches can be used.

- 2) The volume  $L_{vol}$  of an inductor is directly proportional to the energy it processes as given by  $L_{vol} \propto LI^2$ . By interleaving, the total volume  $L_{vol(n)}$  of all the interleaving inductors reduces by a factor  $N_i$ .
- 3) Effective frequency as seen at the input is increased by a factor of  $N_i$ . This facilitates the operation of each leg at a lower frequency, thus lowering the switching losses.
- 4) As the currents in each leg are phase shifted by an angle of  $360^\circ/N$ , the input current ripple is reduced by a factor of  $(1/N_i)$  and the voltage ripple by  $(1/N_i)^2$ .

To achieve high power density, it is crucial to increase the switching frequency while still maintaining high efficiency. SiC represents a revolution in power semiconductor technology, which can help realize high switching frequency [30], [31]. SiC MOSFETs exhibit very low switching losses, while SiC Schottky diodes have no reverse recovery and have very low turn-ON voltage. SiC MOSFET of >1 kV is now commercially available and can replace >1 kV silicon insulated gate bipolar transistor (Si IGBT) in high-power applications. In this paper, SiC MOSFETs and Schottky diodes are used to reduce switching losses and hence achieve higher switching frequency.

Powdered alloy cores are different from ferrite cores as they have a distributed air gap and much higher saturation flux density (typically 2–3 times higher). This means that powdered cores can handle much higher currents without saturation, which is useful for high-power applications. The main disadvantages of powdered cores, when compared to ferrites, are their higher core losses, higher cost, and inductance variation [32]. So, if the switching frequency is not too high, they could be excellent replacements for ferrites in higher power density applications. In this work, KoolM $\mu$  cores from Magnetics are extensively used in the grid inverter and solar converter [33], [34]. Kool M $\mu$  cores are chosen over other powdered cores due to the relatively lower core losses.

### III. DC–DC CONVERTER FOR PV

The dc–dc PV converter is built using an IBC with three interleaved stages, as shown in Fig. 3 [31], [35]. The detailed design of the converter and its comparison to an IGBT and ferrite-based design are shown in [31]. SiC Schottky diodes (CREE C4D15120A), SiC MOSFETs (CREE C2M0080120D), and Kool M $\mu$  40 $\mu$  powdered alloy inductors are used in each leg. Each leg operates at a switching frequency  $f_{sw}$  of 47 kHz.

#### A. Operation of the Interleaved Boost Converter

Operating waveforms of the IBC are shown in Fig. 4. The input PV current is shared equally among the three legs, and the average inductor current is given by  $I_{L(\text{avg})} = I_{PV}/3$ . When the switch is ON from 0 to  $(DT)$ , the current in the inductor rises from  $I_{L(\text{min})}$  to  $I_{L(\text{max})}$  due to the positive PV voltage. When the switch is OFF, the inductor current decreases and flows through the diode. The voltage ratio of input and output voltage is the same as a normal boost converter for continuous conduction mode (CCM) and discontinuous conduction mode

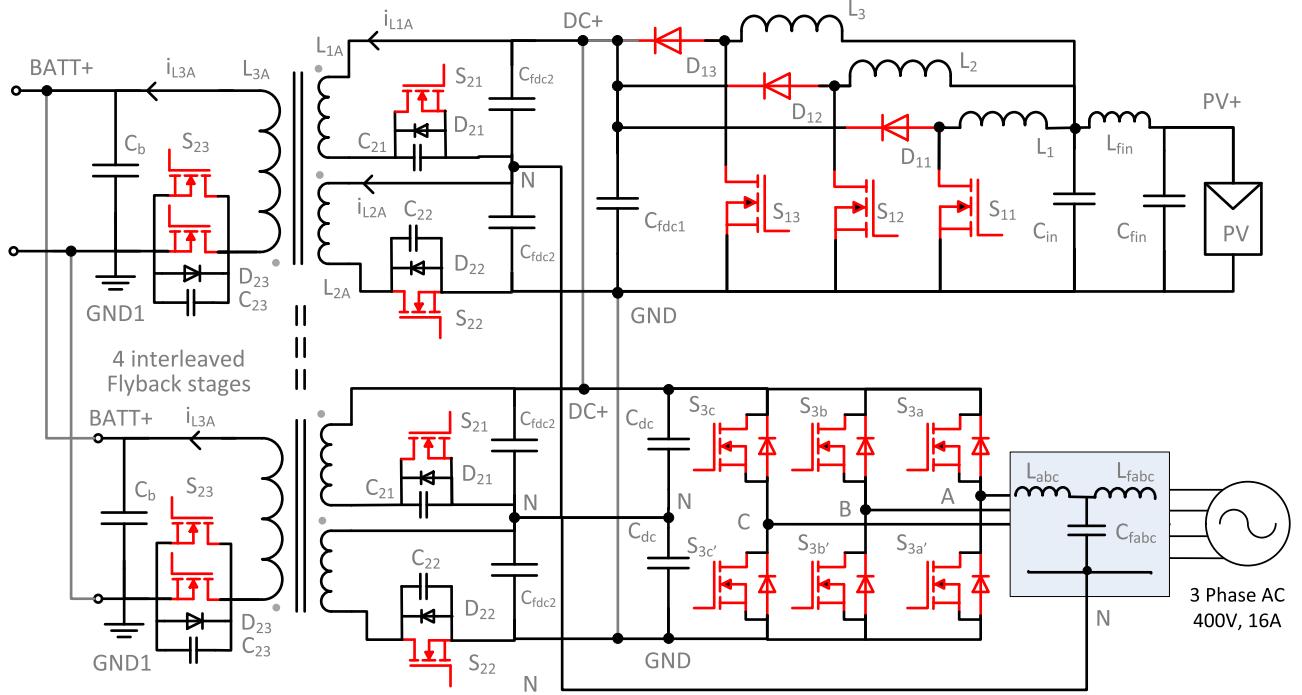


Fig. 3. Topology of the three-port EV-PV converter with a central dc link.

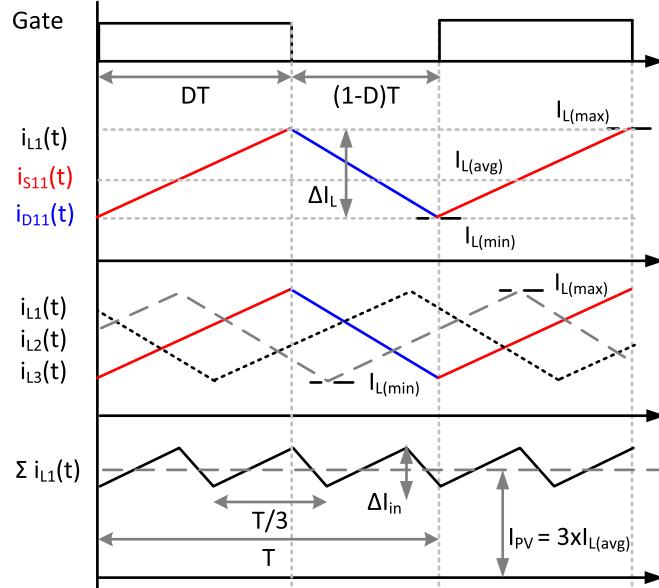


Fig. 4. Waveforms of the IBC (top to bottom): Gate signal for  $S_{11}$ ; currents through the inductor  $L_1$ , switch  $S_{11}$ , and diode  $D_{11}$ ; phase-shifted current through the inductors  $i_{L1}, i_{L2}, i_{L3}$  of each interleaved leg; net input current of the three legs in CCM operation.

(DCM):

$$\frac{V_{dc}}{V_{PV}} = \frac{d_1 + D}{d_1} \quad (2)$$

where  $D$  is the duty cycle of the switches and  $d_1$  is the period when current flows through the diode. In the CCM,  $d_1 = 1 - D$ .

The inductor ripple is vital in designing the PV converter as it directly translates to the input capacitor sizing, inductor size,

and the efficiency of the MPPT operation. The peak-to-peak inductor ripple  $\Delta I_L$  is

$$\Delta I_L = \frac{V_{PV} D}{f_{sw} L} = \frac{(V_{dc} - V_{PV}) d_1}{f_{sw} L} = I_{L(max)} - I_{L(min)} \quad (3)$$

where  $I_{L(max)}, I_{L(min)}$  are the maximum and minimum inductor current and  $L$  is the inductance, respectively. It can be seen from (3) that we either need to use a high switching frequency or a large inductor in order to have a low ripple. Both these methods have the drawback of increased switching losses and increased inductor losses and require a larger inductor core and heat sink.

The benefit of interleaving is that the maximum input current ripple  $\Delta I_{in}$  is  $(1/N_i)$  of the maximum inductor ripple:

$$\Delta I_{in}(D) = \frac{V_{PV}}{f_{sw} L} \left( \frac{N_{on} - N_i D}{1 - D} \right) \frac{1}{N_i} (N_i D - N_{on} + 1) \quad (4)$$

where  $N_{on}$  is the maximum number of switches that are simultaneously ON for the given duty cycle.

Fig. 5 shows the input ripple as a function of duty cycle for different numbers of interleaved stages. The peak input ripple occurs at  $D = (1/2N_i)$ , and the input ripple is zero when  $D = (1/N_i)$ . With three interleaved stages, the input current and voltage ripple reduce by a factor of three and nine, respectively.

### B. Inductor Design and Losses

For the inductor design, the vital parameter is the maximum input ripple,  $\Delta I_{in(max)}$ . The duty cycle for the maximum input ripple can be determined from (4) by setting  $d(\Delta I_{in})/dD = 0$  and solving for  $D$ , where  $A_{int}$  takes odd integral values from 1

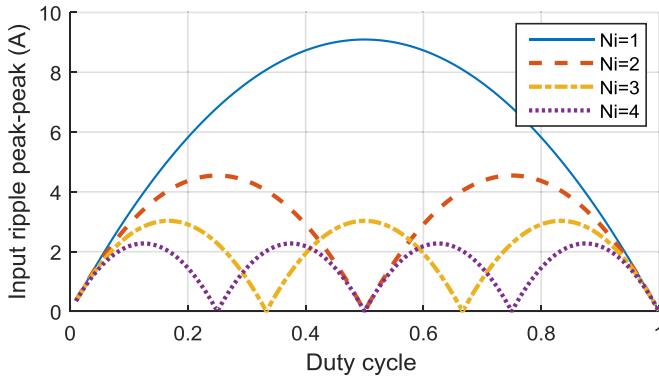


Fig. 5. Peak-to-peak input ripple ( $\Delta I_{\text{in}}$ ) as a function of duty cycle ( $D$ ) for different numbers of interleaved stages of the IBC ( $N_i$ ) for  $V_{\text{dc}} = 750 \text{ V}$ ,  $f_{\text{sw}} = 47 \text{ kHz}$ ,  $L_1 = 443 \mu\text{H}$ .

to  $2 N_i$ :

$$\Delta I_{\text{in}(\text{max})} = \frac{V_{\text{dc}}}{4f_{\text{sw}}LN_i} @ D = \frac{A_{\text{int}}}{2N_i}. \quad (5)$$

For a three-leg IBC, the maximum input ripple occurs at odd integral multiples of  $D = 1/6$ , as seen in Fig. 5. It must be kept in mind that the maximum ripple in inductor  $\Delta I_{L(\text{max})}$  always occurs at  $D = 0.5$  irrespective of  $N_i$ . The inductor is sized at the point where the PV feeds the maximum current ( $I_{\text{pv}} = I_{\text{pv}(\text{max})} = 28.5 \text{ A}$ ,  $V_{\text{pv}} = 350 \text{ V}$ ), given by

$$L = \frac{V_{\text{dc}}}{4f_{\text{sw}}N_i (\Delta I_{\text{in}(p-p)} \% I_{\text{PV}(\text{max})})}. \quad (6)$$

Using (6), the required inductance for 47 kHz is  $443 \mu\text{H}$ . The inductor is built using Kool M $\mu$  E65 cores as they are suitable for printed circuit board (PCB) mounting and have a large core area to reduce the core losses. The parameters of the  $40\mu$  E65 core are permeance  $A_L = 230 \text{ nH/T}^2$  at zero dc bias, core area  $A_c = 540 \text{ mm}^2$ , magnetic path length  $l_e = 147 \text{ mm}$ , and core volume  $V_e = 79400 \text{ mm}^3$ . Table II shows the design of the Kool M $\mu$  inductor considering the inductance variation due to soft saturation [32]. The skin depth for 47 kHz is approximately  $300 \mu\text{m}$ . Hence, a litz wire of  $1000 \times 0.071 \text{ mm}$  is used in order to reduce the skin effect.

Equations (7) and (8) are used to determine the number of turns  $N$  and the maximum flux density in the core  $B_{\text{max}}$ . While 47 turns are required for an inductance of  $443 \mu\text{H}$ , the bobbin can only accommodate a maximum of 42 turns. Therefore, the inductor is redesigned with 42 turns resulting in an inductor of  $L = 405 \mu\text{H}$  at zero current and  $L = 355 \mu\text{H}$  at the maximum current, due to soft saturation. The smaller inductor will require a larger input capacitor to limit the input voltage ripple:

$$L = A_L N^2 \quad (7)$$

$$B_{\text{max}} = \frac{A_L N I_{L(\text{max})}}{A_c}. \quad (8)$$

The inductor losses  $P_L$  comprising the copper losses  $P_{\text{cu}}$  and core losses  $P_{\text{core}}$  are estimated using the modified Stein-

TABLE II  
KOOL M $\mu$  40 $\mu$  INDUCTOR DESIGN AND LOSS AT 350 V, 10 kW INPUT

Inductance ( $\mu\text{H}$ )	$L$	405	Avg. Inductor current (A)	$I_{L(\text{avg})}$	9.52
Inductance ( $\mu\text{H}$ )	$L_{\text{least}}$	355	Inductor ripple (p-p) (A)	$\Delta I_L$	11.03
Number of turns	$N$	42	Core Loss (W)	$P_{\text{core}}$	11.75
Winding resistance ( $\text{m}\Omega$ )	$R_L$	28	Copper loss (W)	$P_{\text{cu}}$	3.77
Peak flux variation (mT)	$B_{\text{pk}}$	78.6	Total inductor loss (W)	$P_L$	15.53

metz equation (MSE) [36]. For a boost converter, the equivalent frequency  $f_{\text{eq}}$  for the MSE is

$$P_L = P_{\text{core}} + P_{\text{cu}} = (Af_{\text{eq}}^{a-1} B_{\text{pk}}^b) f_{\text{sw}} V_e + I_{L(\text{rms})}^2 R_L \quad (9)$$

$$f_{\text{eq}} = \frac{2}{\Delta B^2 \pi^2} \int_0^T \left( \frac{dB}{dt} \right)^2 dt = \frac{2}{\pi^2} \left( \frac{D + d_1}{Dd_1 T} \right) \quad (10)$$

where  $\Delta B$  is the peak-peak change in flux density,  $B_{\text{pk}} = \Delta B/2$ , and the measured value of  $R_L$  is  $28 \text{ m}\Omega$ . MSE parameters are  $A = 120$ ,  $b = 2.09$ ,  $a = 1.46$  for the  $40\mu$  Kool M $\mu$  core, when  $P_{\text{core}}$  is in  $\text{mW/cm}^3$ ,  $f_{\text{sw}}$  in kHz,  $B_{\text{pk}}$  in T, and  $V_e$  in  $\text{cm}^3$  [37]. The inductor losses are shown in Table II, where 15.5 W is lost per inductor at the maximum input power. Since the skin depth at 47 kHz is much higher than the litz diameter, the losses due to skin and proximity effect are not considered for the IBC.

The main advantage of the much lower core losses and saturation flux density of Kool M $\mu$  is that only a single core set is required per inductor. Using other powdered alloy core inductors will lead to much higher core losses, while using ferrites will require two parallel E65 core sets. Second, the powder cores exhibit a gradual reduction in inductance under a fault condition, which makes the control of the converter easier and robust. Third, powder cores have a distributed air gap, which causes very low copper losses because of the fringing flux.

### C. Sizing of Input and Output Capacitor

When using an IBC, an input capacitor  $C_{\text{in}}$  is sized to supply the ripple current  $\Delta I_{\text{in}}$ :

$$C_{\text{in}} = \frac{1}{2} \left( \frac{T}{2N_i} \right) \left( \frac{V_{\text{dc}}}{8f_{\text{sw}}LN_i} \right) \left( \frac{1}{\Delta V_{\text{in}}} \right) @ D = \frac{A_{\text{int}}}{2N_i}. \quad (11)$$

Here, an input capacitor of  $10 \mu\text{F}$  is used, which results in a maximum voltage ripple of  $\Delta V_{\text{in}} = 0.32 \text{ V}$ . An  $LC$  filter ( $L_{\text{fin}} = 47 \mu\text{H}$ ,  $C_{\text{fin}} = 10 \mu\text{F}$ ) is used between the input capacitor and PV to further reduce this ripple voltage. A  $470 \text{ nF}$  film capacitor is connected close to the output of each interleaved leg to filter the high-frequency output ripple.

### D. Converter Loss Estimation

The IBC operates in CCM and DCM depending on the PV voltage and current. The conduction losses in the diode ( $P_{D,\text{con}}$ ,  $P_{D,\text{sw}}$ ) and the conduction and switching losses in the MOSFET

$(P_{S,\text{con}}, P_{S,\text{sw}})$  are estimated as

$$P_S = P_{S,\text{con}} + P_{S,\text{sw}} \quad (12)$$

$$P_{S,\text{con}} = I_{\text{DS},\text{rms}}^2 R_{\text{DS}(\text{on})}(T_j, V_{\text{GS}}, I_{\text{DS}}) \quad (13)$$

$$P_{S,\text{sw}} = f_{\text{sw}} (E_{\text{on}}(V_{\text{DS}}, I_{\text{DS}}, R_G, T_j) + E_{\text{off}}(V_{\text{DS}}, I_{\text{DS}}, R_G, T_j)) \quad (14)$$

$$\begin{aligned} P_D &= P_{D,\text{con}} + P_{D,\text{sw}} \\ &= I_{D,\text{avg}} U_{D0}(T_j) + I_{D,\text{rms}}^2 R_D(T_j) + f_{\text{sw}} E_{D\text{ch}} \end{aligned} \quad (15)$$

$$P_{\text{loss}} = 3(P_D + P_S + P_L) + P_{\text{filter}} + P_{\text{ctrl}} \quad (16)$$

where  $P_S, P_D$  are the total switch and diode losses;  $I_{\text{DS}}, I_D$  are the switch and diode current;  $R_{\text{DS}(\text{on})}, R_D$  are the ON-state resistance of the MOSFET and diode;  $E_{\text{on}}, E_{\text{off}}$  are the switch turn-ON and turn-OFF energy;  $E_{D\text{ch}}$  is the loss due to the energy stored in the diode parasitic capacitance; and  $U_{D0}$  is the ON-state voltage of the diode. As indicated in the equations mentioned above, the switch and diode parameters themselves are a function of the junction temperature  $T_j$ , the gate resistance  $R_G$ , gate voltage  $V_{\text{GS}}$ , blocking voltage of the device  $V_{\text{DS}}$ , and the device current  $I_{\text{DS}}/I_D$  for the specific operating conditions [35].

$P_{\text{filter}}$  is the total losses in the filters, namely, the input common mode filter (4 mΩ resistance), fuse, input LC filter (11 mΩ for  $L_{f\text{in}}$ , 13 mΩ equivalent series resistance (ESR) for  $C_{f\text{in}}$ ), and the output capacitor ( $C_{f\text{dc}}$  with  $\tan\delta = 0.03$ ).  $P_{\text{ctrl}}$  is the power consumed in the control and protection circuitry: three 20 mΩ shunt resistors added to the MOSFET source for current control; gate drive, power supply, and control ICs; and in the extra diode (VS-40EPS) added at the output of the IBC to protect against reverse currents. Reverse recovery losses due to the Schottky diode are neglected as they are extremely small in SiC devices. The turn-ON and turn-OFF gate resistance are 9.4 and 4.7 Ω, respectively, and  $V_{\text{GS}} = 20$  V. The ambient and junction temperature are assumed to be 25 and 100 °C, respectively.

The total converter losses and split up of losses within the converter for different PV voltages and power are shown in Fig. 6(a) and (b), respectively. The worst-case operating point is when  $V_{\text{PV}} = 350$  V,  $P_{\text{PV}} = 10$  kW with losses of 160.4 W. The key observation is the low switching and conduction losses in the MOSFET of 33 and 16 W, respectively. On the other hand, the three 40 μ powdered core inductors together have a relatively higher loss of 46.5 W. The higher losses are the disadvantage of the powdered alloy core, with the benefit of needing lesser number core sets with respect to ferrites. It is a tradeoff between power density and losses. Fig. 6(c) shows the efficiency of the IBC for different PV voltages. The peak efficiency is 99.29% at 10 kW, 700 V PV input.

For comparison, the same converter is designed using ferrite cores and silicon IGBT operating at 19 kHz in [31]. The net converter volume was 2.5 times higher, owing to the 3× larger inductors, and bigger heat sinks to dissipate the IGBT switching losses. Thus, the comparison shows that the use of SiC devices and powdered alloy cores can help achieve high power density and high efficiency.

#### IV. DC-AC GRID INVERTER

The dc-ac stage uses a standard three-phase inverter with three legs and six switches and operates from the 750 V dc link [38]–[40]. The converter is operated with sinusoidal PWM with  $f_{\text{sw}} = 47$  kHz. The inverter is designed to both draw and feed the current to the grid up to 16 A. Since the converter is operated with hard switching, SiC C2M0025120D MOSFETs with a lower  $R_{\text{ds}(\text{on})}$  are used, along with its body diode. The gate resistances are 15.1 Ω for turn ON and 5.1 Ω for turn OFF.

At the inverter input, six 470 μF electrolytic capacitors connected two in series form the dc link. A total of three LCL filters, one per phase, are used at the inverter output for filtering out the harmonics, as shown in Fig. 3 [41], [42]. It is composed of  $L_{abc} = 236$  μH (E65 40 μ KoolMμ,  $N = 32$ ,  $R_L = 11$  mΩ),  $L_{fabc} = 140$  μH (E42 N87,  $N = 36$ ,  $R_L = 21$  mΩ), and a capacitor  $C_{f1} = 8$  μF. Detailed control using sinusoidal PWM and loss modeling of the three-phase inverter are well studied in the literature and hence not presented again in this paper [38]–[42]. The estimated converter efficiency including the losses in the switches, filters, and control circuitry (based on Section III-D) is shown in Fig. 6(c) with a peak value of 98.05%.

#### V. ISOLATED BIDIRECTIONAL DC-DC CONVERTER FOR THE EV

The bidirectional, isolated dc-dc converter for the EV is composed of four interleaved flyback converters (see Fig. 3). MOSFETs and antiparallel diodes are used on both sides of the transformer for bidirectional operation. Each 2.5 kW flyback module has a three-winding transformer (1:1:1 turns ratio) with two series-connected windings on the dc-link side (primary) and a third winding on the EV battery side (secondary), as shown in Fig. 3. For  $I_{\text{ev}} = 30$  A, the corresponding output secondary current in each 2.5 kW unit is  $I_{\text{ev}(m)} = 7.5$  A.

The secondary-side voltage ranges between 50 and 500 V, while the primary voltage is  $V_{\text{dc}} = 750$  V. This difference in primary and secondary voltages leads to high secondary-side currents (up to 30 A). Therefore, two MOSFETs are connected in parallel at the secondary side to reduce the conduction losses. The flyback uses C4D15120A diodes and C2M0080120D MOSFETs with 20 Ω turn-ON and 10 Ω turn-OFF gate resistance.

The main reason for picking the flyback for the EV converter is twofold. First, the topology provides isolation as required by the EV charging standards. Second, the flyback as implemented here can realize bidirectional operation with just four switches (two on the dc-link side and two in parallel on the EV side). With other topologies, like a dual active bridge or a resonant converter, we would need eight switches (or more in parallel for higher current).

##### A. Operation of Interleaved Bidirectional Flyback in Quasi-Resonance

The flyback converter is operated in a QR mode for both charging and V2G operation, and this has four main advantages. First, it enables valley switching of the MOSFET, which results in reduced turn-ON losses due to zero-voltage (ZVS) or low-voltage

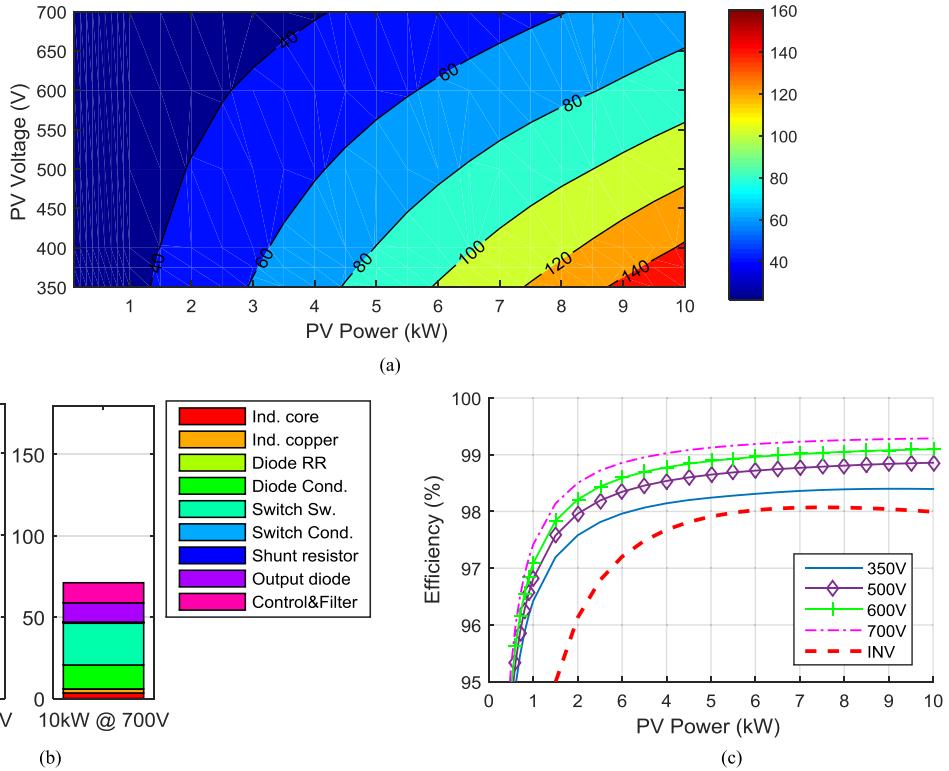


Fig. 6. (a) Total losses of the IBC as a function of input PV voltage and PV power. (b) Split up of losses for 10 kW PV input for 350 V and 700 V PV voltage. (c) Estimated efficiency of the IBC as a function of PV power for different voltages. Also shown is the efficiency of the three-phase inverter as a function of power.

switching (LVS). The resonant capacitor ( $C_{21}, C_{22}, C_{23}$ ) absorbs the turn-OFF energy, and hence the turn-OFF losses are nearly zero. Third, the noise at turn OFF ( $dV/dt$ ) is reduced by the resonance capacitor. Finally, the QR operation is on the borderline between DCM and CCM and has lower rms currents than the DCM. Fig. 7 shows the QR operating waveforms when in a charge mode.

$0 < t < DT$ : When MOSFETs  $S_{21}, S_{22}$  are turned ON simultaneously, the currents  $i_{L1A}, i_{L2A}$  rise from zero to its peak value  $I_{L1A(\text{pk})}$  and energy is stored in the flyback transformer as follows:

$$I_{L1A(\text{pk})} = \frac{(V_{\text{dc}}/2) D}{(L_{1A} + M) f_{\text{sw}}} \quad (17)$$

where  $M = k\sqrt{L_{1A} L_{2A}}$  is the mutual inductance,  $D$  is the duty cycle, and  $f_{\text{sw}}$  is the switching frequency.

$DT < t < (D + D_1)T$ : When the switch is turned OFF, the energy stored in the flyback transformer is delivered to the load. The secondary-side diode  $D_{23}$  conducts for a time interval  $D_1/f_{\text{sw}}$  till the inductor current  $i_{L3A}$  goes to zero. Due to the much lower ON-state voltage of the SiC Schottky diode, the MOSFET body diode does not conduct the load current. The peak current in the secondary inductor,  $I_{L3A(\text{pk})} = 2I_{L1A(\text{pk})}$ , assuming  $k = 1$ :

$$I_{L3A(\text{pk})} = \frac{V_{\text{ev}} D_1}{L_{3A} f_{\text{sw}}} = 2I_{L1A(\text{pk})} \quad (18)$$

$$(V_{\text{dc}}/2) D = V_{\text{ev}} D_1. \quad (19)$$

The power transferred  $P_{\text{ev}}$  can be related to the peak inductor currents and energy stored in the inductor  $E_L$ :

$$\begin{aligned} E_L &= \frac{P_{\text{ev}}}{f_{\text{sw}}} = 2 \left( \frac{1}{2} L_{1A} I_{L1A(\text{pk})}^2 \right) + M I_{L1A(\text{pk})} I_{L2A(\text{pk})} \\ &= \frac{1}{2} L_{3A} I_{L3A(\text{pk})}^2 \end{aligned} \quad (20)$$

$$I_{L1A(\text{pk})} = \sqrt{\frac{P_{\text{ev}}}{2L_{1A} f_{\text{sw}}}} = \frac{1}{2} \frac{(V_{\text{dc}}/2) D}{L_{1A} f_{\text{sw}}} = \frac{1}{2} \frac{V_{\text{ev}} D_1}{L_{3A} f_{\text{sw}}}. \quad (21)$$

When the secondary diodes are conducting, the voltage across the switch is the sum of the input voltage  $V_{\text{dc}}/2$  and the reflected secondary voltage  $V_{\text{RO}}$ . Based on Table I,  $V_{\text{RO}} = V_{\text{ev}}$  and ranges from 50 to 500 V. The maximum MOSFET drain-source voltage  $V_{\text{ds(max)}}$  is

$$\begin{aligned} V_{\text{ds(max)}} &= V_{\text{dc}}/2 + V_{\text{RO(max)}} + V_{\text{trans}} \\ &= 375 + 500 + V_{\text{trans}} \leq 1200 \text{ V} \end{aligned} \quad (22)$$

where  $V_{\text{trans}}$  is the turn-OFF voltage transient due to the leakage inductance of the transformer (see Fig. 7). Split windings are, hence, used on the primary side to ensure that  $V_{\text{ds(max)}} < 1200$  V.

$(D + D_1)T < t < T$ : As soon as the diode current reaches zero, the resonant capacitors  $C_{21}, C_{22}$  begin to exchange energy with the primary inductors. This causes an LC oscillation on the MOSFET drain-source voltage with a period of  $(2T_F)$ , as shown in Fig. 7. The MOSFET is, hence, turned ON at the bottom of the

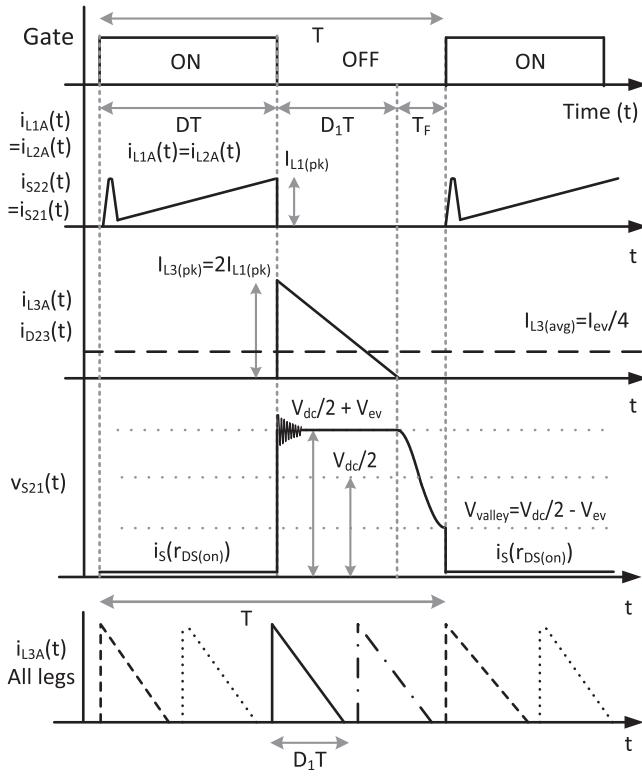


Fig. 7. Waveforms for quasi-resonant operation of the IBFC with two primary and one secondary winding (top to bottom): gate signal for switch  $S_{21}$ ; current through inductors  $L_{1A}, L_{2A}$  and switches  $S_{21}$  and  $S_{22}$ ; current through inductor  $L_{3A}$  and switch  $S_{23}$ ; drain–source voltage  $V_{S21}$  across switch  $S_{21}$ ; net output current from all four interleaved IBFCs.

valley when the voltage is at its lowest to reduce the turn-ON losses:

$$V_{ds(\min)} = V_{valley} = V_{dc}/2 - V_{ev} \quad (23)$$

$$T_F = \pi \sqrt{L_{1A} C_{ds(\text{net})}} \quad (24)$$

$$C_{ds(\text{net})} = C_{21} + C_{ds,S} + C_{DD} + C_{xmer} \quad (25)$$

where  $C_{ds(\text{net})}$  is the net drain–source capacitance due to the QR capacitor  $C_{21}, C_{22}$  and due to the parasitic capacitance of the MOSFET  $C_{ds,S}$ , Schottky diode  $C_{DD}$ , and the transformer windings  $C_{xmer}$ . Depending on the difference  $(V_{dc}/2 - V_{ev})$ , valley switching results in either ZVS or LVS at turn ON. Therefore, the net switching losses are dramatically reduced and can be zero for LVS and ZVS, respectively. This is the primary benefit of the QR operation. The sizing of the resonant capacitor must be such that it is large enough to store the maximum turn-OFF energy of the MOSFET considering all the operating points.

From the above-mentioned equations, the duty cycle  $D$  and frequency  $f_{sw}$  for this flyback can be calculated as

$$D = \frac{2}{(V_{dc}/2)} \sqrt{\frac{P_{ev} L_{1A} f_{sw}}{2}} \quad (26)$$

$$f_{sw} = \frac{1}{T_F} \left( 1 - D - \frac{(V_{dc}/2)}{V_{batt}} D \right). \quad (27)$$

TABLE III  
LVS AND ZVS OPERATING REGIONS OF THE 2.5 kW FLYBACK TRANSFORMER

Situation	CH		V2G	
	Mode	$V_{valley}$	Mode	$V_{valley}$
$V_{ev} > V_{dc}/2$	ZVS	0	LVS	$V_{ev} - V_{dc}/2$
$V_{ev} < V_{dc}/2$	LVS	$V_{dc}/2 - V_{ev}$	ZVS	0
$V_{ev} = V_{dc}/2$	ZVS	0	ZVS	0

Hence, to increase the EV charging power, a larger duty cycle, a higher inductor peak current, and lower switching frequency are required, as shown in Fig. 8(a). The operation of the flyback in the V2G mode is similar to the charge mode described above. The difference being that in the V2G mode, the two switches  $S_{23}$  are turned ON first and the diodes  $D_{21}$  and  $D_{22}$  conduct during the OFF period of the switch. Since there are four modules operating interleaved, the gate signals are phase shifted by  $90^\circ$ . The net output current  $I_{ev}$  is the sum of the output current  $I_{ev(m)}$  of each of the four interleaved modules, as shown in Fig. 7.

Table III shows the operating regions of the MOSFET for ZVS and LVS for the charge (CH) and V2G modes.  $V_{ev}$  ranges from 50 to 500 V and is less than  $(V_{dc}/2) = 375$  V for the majority of the operating range. Hence, the converter operates in ZVS for a large part of the V2G mode and in LVS for a large part of the charge mode.

### B. Flyback Transformer Design

The 2.5 kW flyback transformer is essentially three coupled inductors on a common magnetic core. Since QR results in variable switching frequency, the limits are set between 30 and 350 kHz. The required size of the inductor is determined by the maximum power to be handled at the lowest input voltage ( $V_{ev} = 50$  V,  $I_{ev(m)} = 7.5$  A). From (17) to (26), the required inductance can be estimated, and it was found to be  $L_{1A} = 78.42 \mu\text{H}$ :

$$L_{1A} = \frac{2(V_{dc}/2)^2 D^2}{4P_{ev} f_{sw}}. \quad (28)$$

The transformer is built using an Epcos E65 N87 core set [43]. The permanence of the core  $A_L$  varies with the air-gap length  $g$  according to (29), where  $K_1 = 716$  and  $K_2 = (-0.762)$ :

$$g = (A_L/K_1)^{\frac{1}{K_2}}. \quad (29)$$

Using (7) and (29), the required number of turns  $N = 18$  when using 2 mm spacers on the outer leg and  $g = 4$  mm. The transformer design is shown in Table IV, where  $L_{1A}, L_{2A}, L_{3A} = 80.06 \mu\text{H.A}$ , litz wire of  $200 \times 0.071$  mm is used for the winding. The windings are built in seven parallel-connected layers to reduce the leakage inductance: layers 1, 3, 5, 7 for the two primary windings, and layers 2, 4, 6 for the secondary winding.

### C. Variable Frequency QR and DCM Operation

Fig. 8(a) shows the variable frequency QR operation of the IBFC. The switching frequency reduces as the EV charging

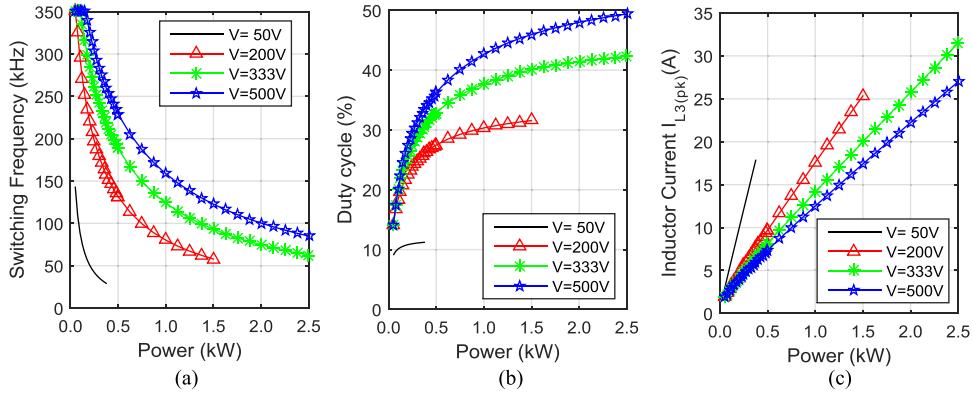


Fig. 8. Variation of the (a) switching frequency  $f_{\text{sw}}$ , (b) duty cycle  $D$ , and (c) peak inductor current  $I_{L3A(\text{pk})}$  as a function of EV charging power for different EV voltages  $V_{\text{ev}}$ .

TABLE IV  
2.5 kW FLYBACK TRANSFORMER DESIGN

Transformer core, Air gap	$A_c, l_e, g$	Epcos E65 N87, 4mm net air gap
Turns	$N$	18:18:18
Parallel layers		2:2:3
Litz wire		200 x 0.071mm litz
Inductance	$L_{1A}, L_{2A}, L_{3A}$	80.06 $\mu\text{H}$
Winding resistance	$R_L$	27.5 m $\Omega$ , 31.5 m $\Omega$ , 19 m $\Omega$

power increases. The lowest switching frequency of 30 kHz is observed when  $V_{\text{ev}} = 50 \text{ V}$  and  $I_{\text{ev}(m)} = 7.5 \text{ A}$ . At very low powers, the maximum switching frequency is restricted to 350 kHz and the converter moves to the DCM with valley skipping. The duty cycle and peak inductor current  $I_{L1A(\text{pk})}$ ,  $I_{L3A(\text{pk})}$  increase as the charging power increases, as seen in Fig. 8(b) and (c), respectively. The maximum secondary inductor current  $I_{L3A(\text{pk})} = 31.5 \text{ A}$  occurs at the crucial operating point of  $V_{\text{ev}} = 333 \text{ V}$ ,  $I_{\text{ev}} = 30 \text{ A}$ , and  $I_{\text{ev}(m)} = 7.5 \text{ A}$

#### D. Sizing of Filter Capacitors

Fig. 7 shows the flyback output current for one 2.5 kW stage and the total output current for the four interleaved stages. The output ripple reduces by four times due to the interleaved operation. To keep the output voltage ripple within limits, the required output capacitance can be estimated as follows:

$$\Delta V_{\text{ev}(p-p)} = \frac{\Delta Q}{C_{\text{ev(net)}}} = \frac{I_{\text{ev}} (1 - D_1)}{C_{\text{ev(net)}}} \left( \frac{T}{4} \right). \quad (30)$$

For each 2.5 kW IBFC, a capacitance of  $C_b = 3 \mu\text{F}$  is used at the EV output side. The four IBFC stages are then connected in parallel, and two  $1.5 \mu\text{F}$  capacitors, common-mode and differential mode filters, are connected to the common output (not shown in Fig. 7).

#### E. IBFC Losses and Efficiency

Equations (9) and (10) for the inductor losses and (12) to (15) for the semiconductor losses are used for the loss estimation. The key losses in the IBFC occur in the inductor and

semiconductor with minor losses in the capacitors and control circuitry. The estimated losses for one 2.5 kW unit for different EVs and different powers and voltages can be seen in Figs. 9 and 10 for CH and V2G mode, respectively. In this design, the resonant capacitor  $C_{21} = C_{22} = C_{23} = 470 \text{ pF}$ . Based on the output capacitance of the MOSFET and the diode at 400 V, the corresponding value of  $T_F = 1.596 \mu\text{s}$ .

1) *Flyback Transformer Losses*: For the N87 ferrite core, the Steinmetz parameters are given by  $A = 47.66$ ,  $b = 2.63$ ,  $a = 1.4062$  when  $P_{\text{core}}$  is in  $\text{kW/m}^3$ ,  $f_{\text{sw}}$  in kHz,  $B_{\text{pk}}$  in mT, and  $V_e$  in  $\text{m}^3$  [43]. Due to the same shape of flux density waveforms for both the boost and flyback converter, the same equivalent frequency  $f_{\text{eq}}$  is applicable for both. A critical aspect of the flyback transformer losses is the ac copper losses  $P_{\text{cu}}$  due to the high switching frequency between 30 and 350 kHz. The losses due to skin and proximity effects are estimated based on [44].

Figs. 9(a) and 10(a) show the estimated losses in the flyback transformer for CH and V2G modes, respectively. Typical for any flyback in QR, the core and copper losses increase with power due to higher flux swing in the core and higher rms currents, respectively. The relatively high copper losses at low powers are due to the skin and proximity effect due to the high switching frequency. There is no difference in flyback transformer losses between CH and V2G mode, as the same power is handled in both cases.

2) *Semiconductor Losses*: The semiconductor losses are largely dominated by the occurrence of ZVS or LVS, as described in Table III. In case of QR, the turn-OFF energy is always stored in the QR capacitor, and the turn-OFF losses are nearly zero. For ZVS, the turn-ON losses are zero as well. In case of LVS, the turn-ON losses are dominated by the energy stored in the QR capacitor on both the primary and secondary side. Hence, (14) is modified for the IBFC for LVS to include the turn-ON losses due to the discharging of the MOSFET-side QR capacitor  $E_{\text{QR1}}$  and charging of the diode-side QR capacitor  $E_{\text{QR2}}$ :

$$P_{S,\text{sw}} = f_{\text{sw}} (E_{\text{on}}(V_{\text{DS}}, I_{\text{DS}}, R_G, T_j) + E_{\text{off}}(V_{\text{DS}}, I_{\text{DS}}, R_G, T_j) + E_{\text{CQR1}} + E_{\text{QR2}}). \quad (31)$$

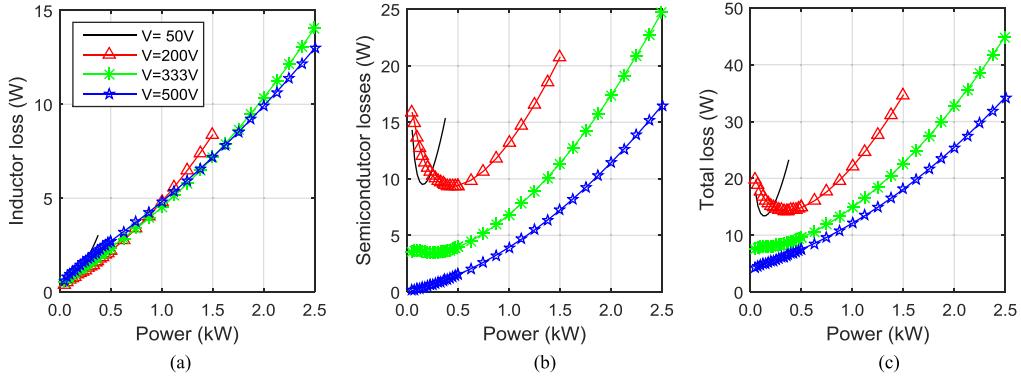


Fig. 9. Estimated losses in a 2.5 kW IBFC for a charge mode for different EV voltages and power. (a) Flyback inductor. (b) Semiconductor. (c) Total losses.

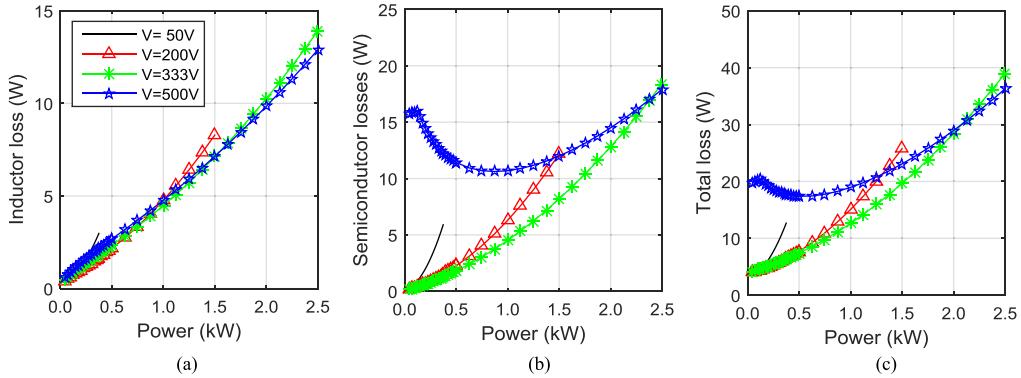


Fig. 10. Estimated loss in a 2.5 kW IBFC for the V2G mode for different EV voltages and power. (a) Flyback inductor. (b) Semiconductor. (c) Total losses.

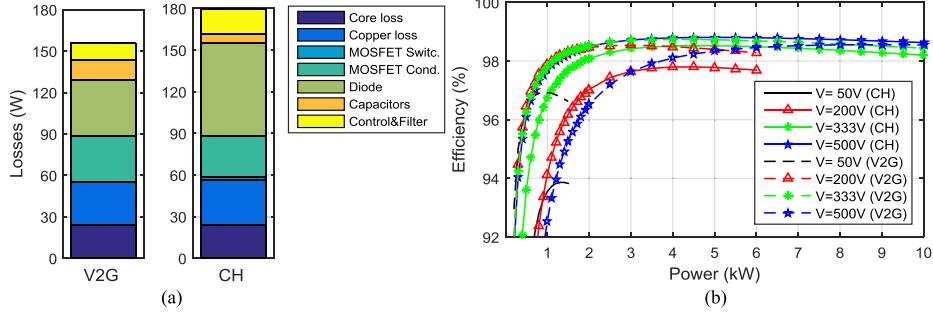


Fig. 11. (a) Split up of losses for  $V_{ev} = 333$  V, 10 kW power for CH and V2G modes. (b) Efficiency of the 10 kW IBFC for CH and V2G modes.

For the CH mode

$$\begin{aligned} E_{QR1} + E_{QR2} &= \frac{1}{2} C_{ds(\text{net})} (V_{dc}/2 - V_{ev})^2 \\ &+ \frac{1}{2} C_{ds(\text{net})} \left\{ \left( \frac{V_{dc}}{2} + V_{ev} \right)^2 - (2V_{ev})^2 \right\}. \end{aligned} \quad (32)$$

In practice, the leakage inductance causes a significant part of  $E_{QR2}$  to be fed to the source/load. Hence, it is assumed here that only 25% of  $E_{QR2}$  is lost. Figs. 9(b) and 10(b) show the total MOSFET and diode losses for CH and V2G mode, where ZVS occurs when  $V_{ev} > 375$  V for the CH mode and when  $V_{ev} < 375$  V for V2G. For both modes, the semiconductor losses increase with increasing power owing to higher rms

currents. However, when LVS occurs, the switching losses dramatically increase at lower powers owing to the higher switching frequency, as seen in Figs. 8(a), 9(b), and 10(b). Hence, the total semiconductor losses have a U-shaped curve when LVS occurs.

**3) Total Losses:** Figs. 9(c) and 10(c) show the total losses of a 2.5 kW IBFC unit including the capacitor and the 2 W power of the control circuit. The maximum losses of 44.9 W occur at  $V_{ev} = 333$  V and  $P_{ev} = 10$  kW. The corresponding split-up of losses for CH and V2G modes for the 10 kW IBFC is shown in Fig. 11(a). The diode conduction losses are high in the CH mode, as there is only a single diode at the secondary and not two in parallel, like the MOSFET. The efficiency of the 10 kW IBFC is shown in Fig. 11(b) and the peak efficiency is 98.8% ( $V_{ev} = 500$  V, CH). The efficiency plot clearly reflects the occurrence of ZVS for CH and V2G mode, as shown in

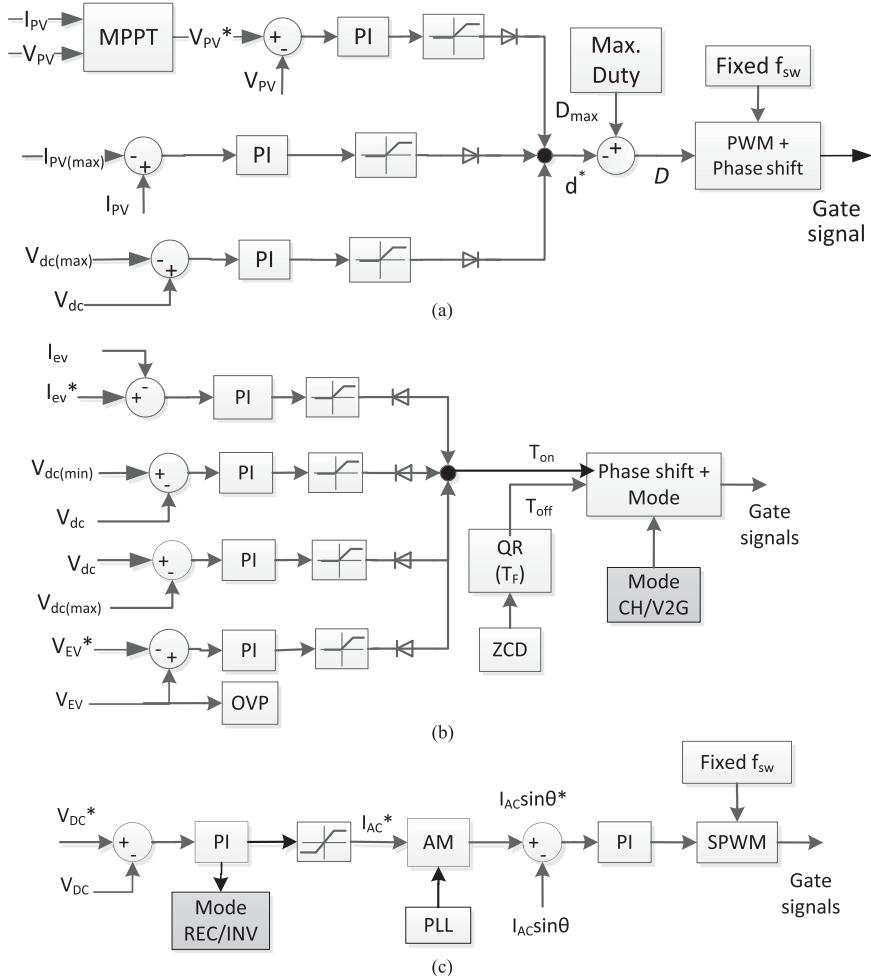


Fig. 12. Schematic of the closed-loop control. (a) PV converter. (b) EV charger. (c) Grid inverter.

Table III. Commercial EVs typically have voltages in the range of 200–500 V; hence, the converter has a peak efficiency above 97.8% in this voltage range.

## VI. CLOSED-LOOP CONTROL

The converter is capable of four different power flows, namely, PV → EV, PV → grid, grid → EV, and EV → grid and this enabled by the closed-loop control. The closed-loop control is modularly organized into three control loops, one for each of the three converters (see Fig. 12). The primary purpose of the control for the PV IBC, EV IBFC, and grid inverter is MPPT, control of EV charging, and power balance, respectively. The inverter uses the dc-link voltage to perform the power balance and PV, and the EV converter implements power curtailment if the dc-link voltage is out of bounds.

### A. PV Converter

The IBC's control has three control loops working in parallel to control the duty cycle  $D$ , as in Fig. 12(a):

$$D = D_{max} - d^*. \quad (33)$$

The control output  $d^*$  is the maximum value as dictated by all the three loops (indicated by the diode) and the maximum duty cycle  $D_{max} = 62.5\%$ . The first loop is for MPPT that uses a microcontroller to continuously adjust the duty cycle by a perturb-and-observe method [45]. The second and third loops are used to limit duty cycle if the PV current  $I_{PV}$  is more than  $I_{PV(max)} = 32$  A or if the dc-link voltage is beyond  $V_{dc(max)} = 810$  V.

### B. DC-DC Bidirectional EV Charger

The IBFC control for the EV charging has four control loops acting in parallel, as seen in Fig. 12(b). The first loop controls the MOSFET ON-time  $T_{on}$  based on the current reference  $I_{ev}^*$ . The next two loops are used for curtailment of charging and V2G power if the minimum (700 V) and maximum (810 V) dc-link voltage are reached, respectively. The last loop is used to limit the ON-time when the maximum battery voltage  $V_{ev}^*$  is reached. The MOSFET OFF-time  $T_{off}$  is determined by the zero-current detection and QR valley detection circuit. The phase shift block is responsible for maintaining 90° phase shift between the interleaved modules. Depending on charge or V2G mode, the gate signals are provided to the appropriate MOSFETs.

### C. DC–AC Grid Inverter

The dc–ac inverter is responsible for maintaining the dc-link voltage at  $V_{dc}^* = 750$  V by controlling the grid current  $I_{ac} \sin \theta$  that is either drawn (rectifier mode, REC) or fed to the grid (inverter mode, INV). A phase-locked loop is used to estimate the voltage phase and maintain a high power factor, as shown in Fig. 12(b). There are two PI loops, the outer loop controls the dc-link voltage, while the fast inner loop is used to control the current.

### D. Modular Implementation

The control design is, hence, simple as it only requires an external voltage  $V_{ev}^*$  and current set point for the EV  $I_{ev}^*$ . If the inverter is disconnected suddenly, then both the PV and EV converters move to the power curtailment mode and ensure safety. Second, no modifications in the control are needed if the bidirectional EV charger is used without the solar dc–dc converter.

The stability of the multiloop control of the converter is addressed by three factors. First, at any point in time, only one of the parallel loops is in operation for each of the PV and EV control. This is due to the parallel diodes in the control loop with one common point at the output, which ensures that only one diode is forward biased at a given time. Second, a large energy buffer is created on the dc link through the use of several electrolytic capacitors ( $6 \times 450$  V,  $470 \mu\text{F}$ ). Since the dc-link voltage  $V_{dc}$  is used by all the three controls (inverter, IBC, IBFC), a large energy buffer provides sufficient time for response during fast power variations. Finally, the stability of the control is tested individually and collectively by running several test cases at both low and high powers.

## VII. EXPERIMENTAL SETUP AND VERIFICATION

### A. Prototype of the EV–PV Converter

Fig. 13 shows the prototype of the developed EV–PV converter with the PV IBC, EV IBFC, and the grid inverter. The converter is modularly built with the PV IBC and its controller on a separate PCB. Therefore, the converter can be used either as a solar-powered EV charger or as a bidirectional EV charger without solar. Due to the modular nature of the converter control, several bidirectional EV charger modules (i.e., flyback converter + inverter) can be operated in parallel by giving them a common current set point  $I_{ev}^*$ . By doing so, the charging power can be scaled up from 10 kW to reach up to 100 kW. Hence, the developed charger can be used for both level 2 medium power charging and level 3 fast charging.

The converter is  $50 \times 42 \times 12$  cm $^3$  with the control board placed at the back-side PCB. Based on cabinet dimensions, the power density of the PV converter, EV + grid converters, and the complete EV–PV converter is 1380, 555, and 396 W/l, respectively. In order to make it commercially usable, the prototype is designed to be compatible with EN60950 for safety and EN55011 (class A), EN61000-4-2 to EN61000-4-6, EN61000-4-11 for Emission (Industrial).

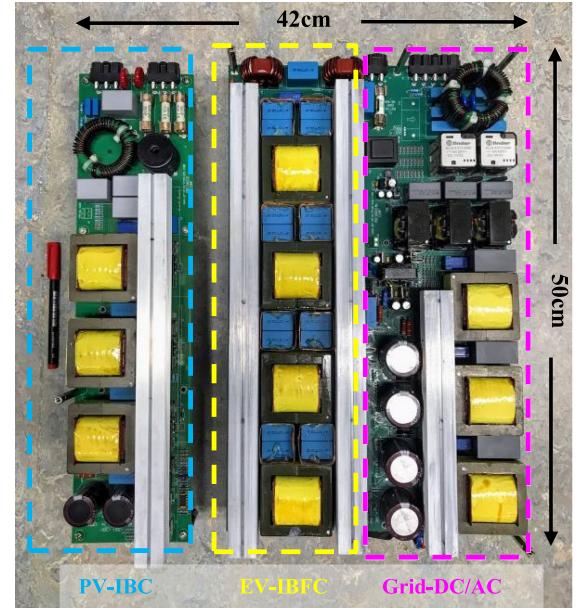


Fig. 13. Experimental prototype of a 10 kW three-port EV–PV converter built over two PCBs.

### B. Experimental Waveforms and Efficiency

Fig. 14 shows the operating waveforms of the PV IBC for CCM and DCM, where a PV emulator is used as input. During the CCM, the inductor current  $I_{L(1)}$  rises when the gate voltage  $V_{GS(1)}$  is ON and then begins to fall once the gate is OFF, in Fig. 14(a). In the DCM, the inductor current  $I_{L(1)}$  goes to zero before the end of the switching cycle, causing the drain–source voltage  $V_{ds(1)}$  to oscillate as it goes from  $V_{ds(on)}$  to  $V_{PV}$ , in Fig. 14(b).

Fig. 15 shows the MOSFET drain–source  $V_{ds(1)}$  and the gate–source voltage  $V_{gs(1)}$  for one of the four interleaved stages of the EV IBFC. The quasi-resonant operation can be clearly seen in Fig. 15(a) where the switch is turned on exactly when the quasi-resonant valley is detected. At lower powers, the maximum frequency setting of 350 kHz ensures that valley skipping occurs, as shown in Fig. 15(b). The quasi-resonant time period was measured to be  $=1.52 \mu\text{s}$ , close to the estimated value.

Finally, Fig. 16 shows the waveforms of the AC current fed to the grid in V2G mode by the DC–AC inverter. The waveforms are obtained at the full power of  $P_{ev} = 10$  kW at  $V_{ev} = 402$  V. The corresponding total harmonic distortion (THD) measurements in the grid current is 2.95% at full load, at 0.987 power factor.

Fig. 17 shows the measured efficiency of the converter for different power flows: PV → EV, PV → Grid, Grid → EV when  $V_{ev} = 400$  V. The peak efficiencies were 95.2%, 96.4% and 95.4%, respectively. The efficiency of EV → Grid was nearly the same as Grid → EV.

### C. Comparison With Conventional Design

The developed three-port converter is compared to a conventional solar EV charger that uses a 10 kW solar inverter [46] and 10 kW unidirectional EV charger [47], based on silicon IGBTs

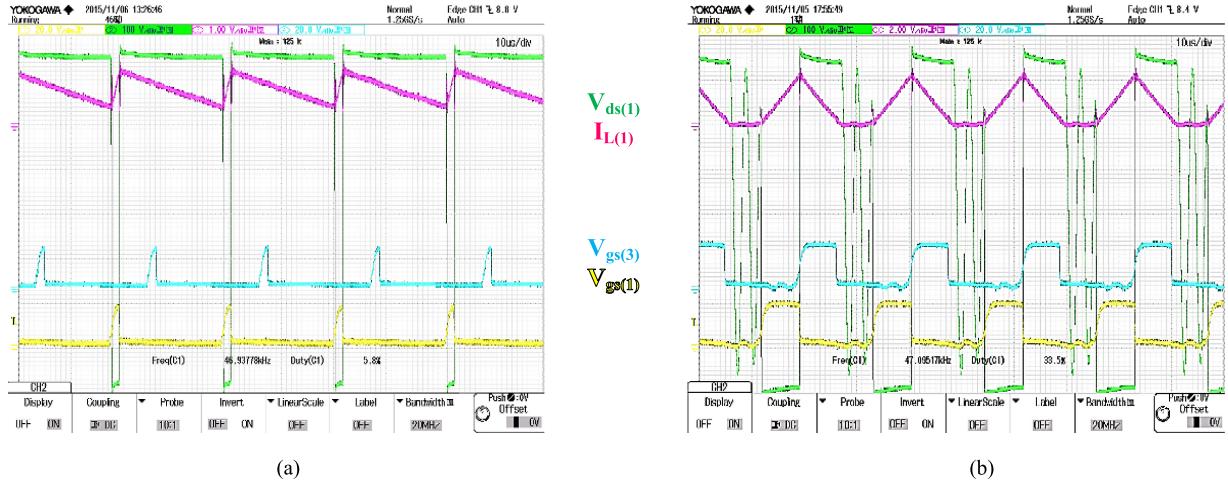


Fig. 14. Waveforms for the PV IBC for the phase-shifted gate voltage  $V_{gs}$ , inductor current  $I_L$ , and MOSFET drain–source voltage  $V_{ds}$  for (a) CCM ( $V_{pv} = 700$  V,  $I_{pv} = 10$  A) and (b) DCM ( $V_{pv} = 400$  V,  $I_{pv} = 10.75$  A).

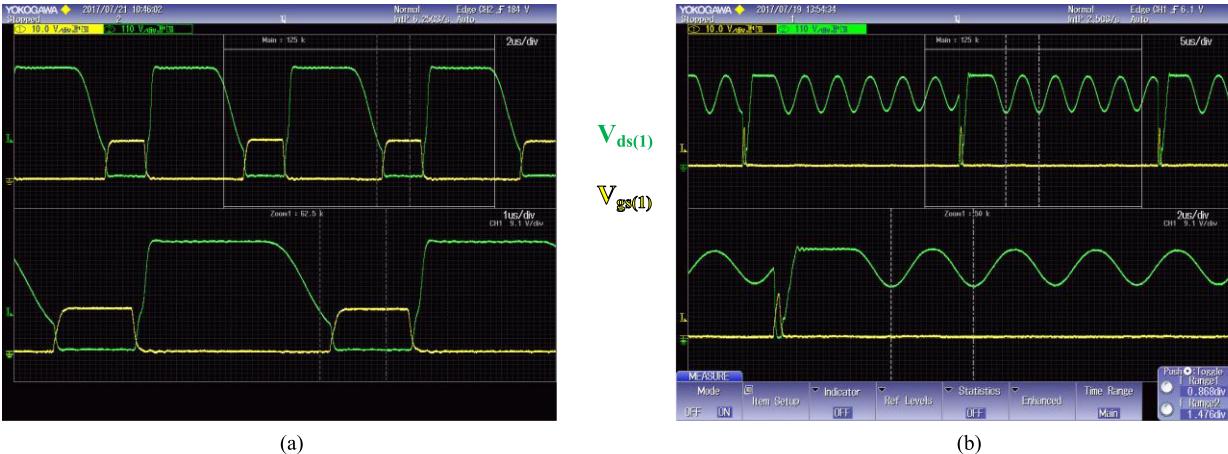


Fig. 15. Drain–source voltage  $V_{ds}$  and gate voltage  $V_{gs}$  for one phase of the IBFC for CH. (a) Quasi resonant operation LVS for  $V_{ev} = 250$  V,  $I_{ev} = 5$  A. (b) Valley skipping and DCM operation at low powers for  $V_{ev} = 100$  V,  $I_{ev} = 1$  A.

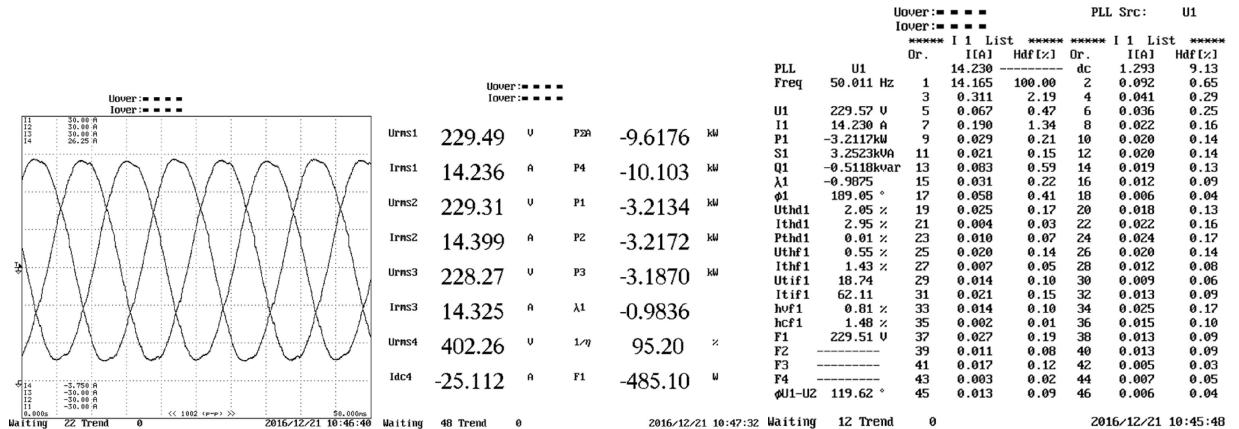


Fig. 16. Waveforms of the ac current fed to the grid in the V2G mode for  $P_{ev} = 10$  kW,  $V_{ev} = 402$  V, and the corresponding power and THD measurements.

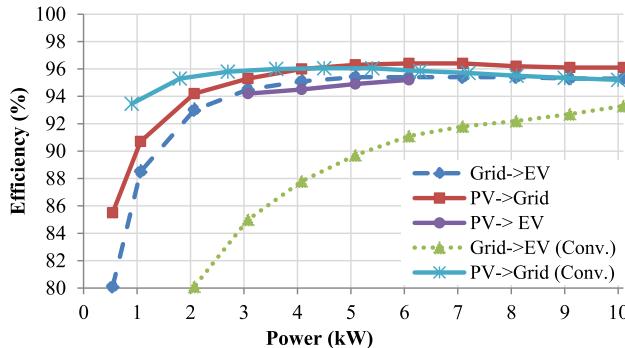


Fig. 17. Measured efficiency of the converter for power flow paths: PV → EV, PV → grid, and grid → EV.

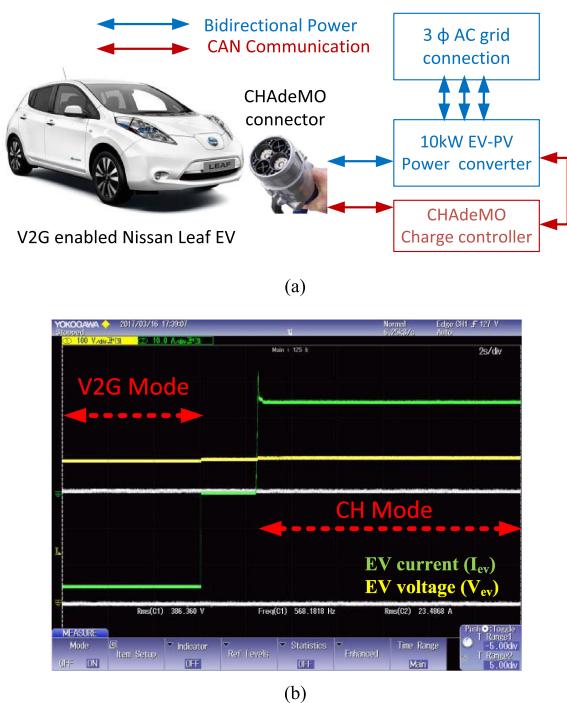


Fig. 18. (a) Block diagram of the test setup of the EV-PV charger with a CHADEMO charge controller connected to a V2G-enabled Nissan Leaf EV. (b) Scope showing the Nissan Leaf during V2G and CH operation using the developed power converter with the battery voltage  $V_{ev}$  in yellow and charging/discharging current  $I_{ev}$  in green.

and ferrite cores. In [46] and [47], the same specifications are used as listed in Table I, but the ac grid is used to exchange power from the PV to EV, instead of dc. In [46], a three-phase resonant topology is used, while in [47], an IBC with a three-phase inverter is used.

First, for grid → EV, the developed converter has a much higher peak and a higher partial load efficiency than the resonant topology, as seen in Fig. 17. The high partial load efficiency makes it suitable for smart charging of EVs where the EV charging power is continuously varied [28]. Second, the power density of the developed charger (396 W/l) is three times that of the two converters combined (134 W/l). Third, the proposed converter is bidirectional for V2G, while the other is not.

#### D. Testing With a Nissan Leaf—Charging and V2G

Fig. 18(a) shows the testing of the converter to charge and discharge a V2G-enabled Nissan Leaf EV using an outdoor cabinet. A CHADEMO charge controller that implements the CAN communication with the EV was used to provide the voltage  $V_{ev}^*$  and current set points  $I_{ev}^*$  to the power converter. Fig. 18(b) shows the 386 V EV battery first being discharged (V2G) with a current and power of  $-23.5$  A,  $-9.07$  kW and then being charged with a current and power of  $23.5$  A,  $9.07$  kW, respectively. Due to the absence of PV panels at the test location, there was no PV power input.

### VIII. CONCLUSION

This paper presents the development of a 10 kW, three-port, bidirectional converter for direct dc charging of the EV from PV. The developed converter is compatible with CCS and CHADEMO EV charging standard and can operate with a PV array of wide voltage and power range. Interleaving of converters, SiC devices, and powdered alloy core inductors are extensively used to increase the switching frequency while keeping the converter losses within limits. This has helped to increase the power density by a factor of three when compared to conventional designs and reduce the voltage ripple at the EV and PV ports.

The converter is modularly designed with three subconverters connected on a 750 V central dc link: IBC for PV, a three-phase inverter for the ac grid, and an interleaved flyback converter for the EV. While the flyback is traditionally considered suitable only for low powers, this paper shows how the use of SiC devices in a QR mode flyback converter can achieve high efficiency even at high powers. Three closed-loop controls were developed and tested for the three subconverters, which enable four power flows: PV → EV, EV → grid, grid → EV, and PV → grid.

A 10 kW prototype was built and tested and exhibits a peak efficiency of 95.2% for PV → EV, 95.4% for grid → EV, and 96.4% for PV → grid. The developed prototype has a much higher peak efficiency, higher partial load efficiency, and three times higher power density than currently existing solutions based on ac power exchange. The charge and V2G operation at 10 kW were tested with a Nissan Leaf EV with a CHADEMO charge controller.

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Since 1999, he has been working together with his business partner J. Schijffelen. Since 2002, he has been the CEO of Power Research Electronics BV Power Developers, Breda, The Netherlands, as a specialist in power electronic design and manufacturing. He has several patents for solar and dc fast charging converters.



**Jos Schijffelen** received the Bachelor's degree in electric engineering from the HTS, Leeuwarden, The Netherlands, in 1998.

In 1998, he started his career with Mastervolt, Amsterdam, and was involved in design and manufacturing of solar inverters until 2002. In 2002, he took over the company Power Research Electronics BV (PRE), Breda, The Netherlands, together with M. Kardolus. PRE is a power electronics design and manufacturing company with the focus on renewable energy and innovative power electronics design with

more than 25 employees. From 2002 until now, he has been involved in numerous designs for renewable solar and wind applications, electric vehicle (fast) charger, and industrial power supplies. He currently holds 8 patents.



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Dr. Bauer is the Former Chairman of Benelux IEEE Joint Industry Applications Society, Power Electronics and Power Engineering Society Chapter, the Chairman of the Power Electronics and Motion Control Council, a Member of the Executive Committee of European Power Electronics Association, and also a Member of the International Steering Committee at numerous conferences. He was a recipient of the title Professor from the President of Czech Republic at the Brno University of Technology, Brno, Czech Republic, in 2008, and Delft University of Technology, in 2016.



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In 2007, he started his career with Wijdeven PS&IT, Oirschot, and was involved in designing and testing of different kind of power supplies until 2010. In 2010, he started working as an R&D Engineer with Power Research Electronics BV, Breda, The Netherlands, where he mainly works on inverters, battery-, and electric vehicle chargers.