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Review of Manufacturing Process Defects and Their Effects on Memristive Devices

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Abstract
Complementary Metal Oxide Semiconductor (CMOS) technology has been scaled down over the last forty years making possible the design of high-performance applications, following the predictions made by Gordon Moore and Robert H. Dennard in the 1970s. However, there is a growing concern that device scaling, while maintaining cost-effective production, will become infeasible below a certain feature size. In parallel, emerging applications including Internet-of-Things (IoT) and big data applications present high demands in terms of storage and computing capability, combined with challenging constraints in terms of size, power consumption and response latency. In this scenario, memristive devices have become promising candidates to complement the CMOS technology due to their CMOS manufacturing process compatibility, great scalability and high density, zero standby power consumption and their capacity to implement high density memories as well as new computing paradigms. Despite these advantages, memristive devices are also susceptible to manufacturing defects that may cause unique faulty behaviors that are not seen in CMOS, increasing significantly the complexity of test procedures. This paper provides a review about the manufacturing process of memristives devices, focusing on Valence Change Mechanism (VCM)-based memristive devices, and a comparative analysis of the CMOS and memristive device manufacturing processes. Moreover, this paper identifies possible manufacturing failure mechanisms that may affect these novel devices, completing the list of the already known mechanisms, and provides a discussion about possible faulty behaviors. Note that the identification of these mechanisms provides insights regarding the possible memristive devices' defective behaviors, enabling to derive more accurate fault models and consequently, more suitable test procedures.

Keywords Manufacturing process · CMOS · Memristive devices · Defects · Fault models

1 Introduction

During the last four decades, CMOS technology miniaturized according to Moore's and Dennard's laws, which predicted the number of transistors in the same area to double every eighteen months, and as the dimensions of a device shrink, so does power consumption [29, 5]. Limitations on the continued transistors' miniaturization and the increasing need for emerging applications requiring high performance systems with strict constraints already poses significant challenges to device technologies and computer architectures. Today it is possible to say that the device technology is facing the following three walls, which prevent further transistor miniaturization [12, 28]: (a) the reliability—wall associated to failure rate increase and lifetime reduction; (b) the leakage wall—meaning that the static power consumption becomes even more important than the dynamic

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power consumption, when considering the overall power consumption, and (c) the cost wall—showing that the cost per transistor via pure geometric scaling is plateauing, with no tendency to get cheaper. From the computer architecture point of view, the following walls can be identified: (a) the memory wall—due to the limited memory bandwidth that impacts performance and energy consumption of data-intensive applications as well as the growing gap between memory and processor speeds; (b) the power wall—as the practical power limit for cooling is reached and consequently, there is no possibility of further increasing CPU clock frequency; and (c) the Instruction Level Parallelism (ILP) wall—related to the always increasing complexity of keeping all cores running in parallel. The totality of these aspects limits the use of CMOS technology and *von Neumann* architectures as solutions for emerging applications like cognitive tasks and increases the necessity for novel devices and architectures able to deliver high performance systems. Memristive devices, quantum dots, and spin-wave devices are only some examples for emerging devices, while computation-in-memory, neuromorphic and quantum computing represent next generation's computing paradigms. In particular, memristive devices represent a promising candidate to complement the CMOS technology mainly due to their CMOS manufacturing process compatibility as well as high scalability and density [28]. However, the use of these novel devices within emerging applications depends on being able to guarantee their dependability after manufacturing. In this context it becomes crucial to properly test the fabricated devices. As already known from CMOS technology, the efficiency of test procedures depends on the understanding of manufacturing failure mechanisms, which allow the identification of possible defects and consequently, the definition of accurate fault models. Unfortunately, when considering memristive devices, the lack of information regarding manufacturing defects compromises the definition of more accurate fault models today. Thus, the main contribution of this paper is to provide a review and about the memristive device manufacturing process in order to better understand the possible defects that may affect these novel devices as well as identify the relation between manufacturing failure mechanisms and memristive devices' behavior. Further, this paper also provides some complementary insights regarding possible faults and defect injection scheme. In turn, this will guarantee the definition of accurate fault models and consequently, more efficient test procedures able to assure the device's required quality, avoiding test escapes and no trouble found components.

The paper has been organized as follows: Section 2 briefly introduces memristive devices. Section 3 provides a description of the memristive device manufacturing process taking into account some aspects regarding the CMOS manufacturing processes and possible manufacturing failure mechanisms. Section 4 provides insights regarding the possible defects that can affect novel devices followed by the presenting possible faulty behaviors. Section 5 presents the final considerations and points out open issues.

2 Memristive Devices

In 1971, Leon Chua postulated the fourth basic circuit element named memristive device, or memristor, while trying to establish a missing constitutive relationship between electrical charge and magnetic flux [2]. In theory, a memristive device is a passive element that can be described by the time integral of the current (charge q) through the time integral of the voltage (flux ϕ) across its two terminals [2]. In other words, the memristor is a device whose resistance is called memresistance, which is a charge dependent resistance, and its value varies as a function of current and flux. A memristor has at least two distinct states, the High Resistance State (HRS) and the Low Resistance State (LRS) and can switch from HRS (LRS) to LRS (HRS) by applying a voltage V_{SET} (V_{RESET}) with an absolute value larger than its threshold voltage V_{th}. The essential fingerprint of memristive devices is the pinched current–voltage (I-V) hysteresis loop, illustrated in Fig. 1a. Note that when the memristive device is floating or when the voltage $v(t)$ across the device is zero, the current $i(t)$ is also zero. The memresistance exhibits a hysteretic behavior, which can be exploited as non-volatile resistance switching memory cell [27]. Another important characteristic of memristive devices is that the pinched hysteresis loop shrinks with a higher switching frequency f, depicted in Fig. 1b. This originates from the highly non-linear switching kinetics which is controlled by temperature and field driven processes [37]. Figure 1c shows symbols used for representing memristive devices, where the black square represents the terminal for positive voltage switching.

In terms of classification, memristors can be initially classified in two types: (a) ionic thin film and molecular memristors, and (b) magnetic and spin-based memristor [16]. When used as a memory device, ionic thin film and molecular memristors are called resistive memories, more precisely Resistive Random Access Memories (RRAMs), being classified as a non-volatile memory [7–10]. An RRAM data storage element is a three-layer device consisting of a dielectric sandwiched between to metal electrodes. In more detail, the memory cell is based on Metal/Insulator/Metal (MIM) structure [35]. The "M" in MIM denotes any reasonably good electron conductor, often asymmetric for the two sides with respect to the materials' work function and oxygen affinity, while "I" stands for insulator, often an ion or mixed conducting oxide or higher chalcogenide. RRAMs can be further classified according to the switching mode, the conductive path

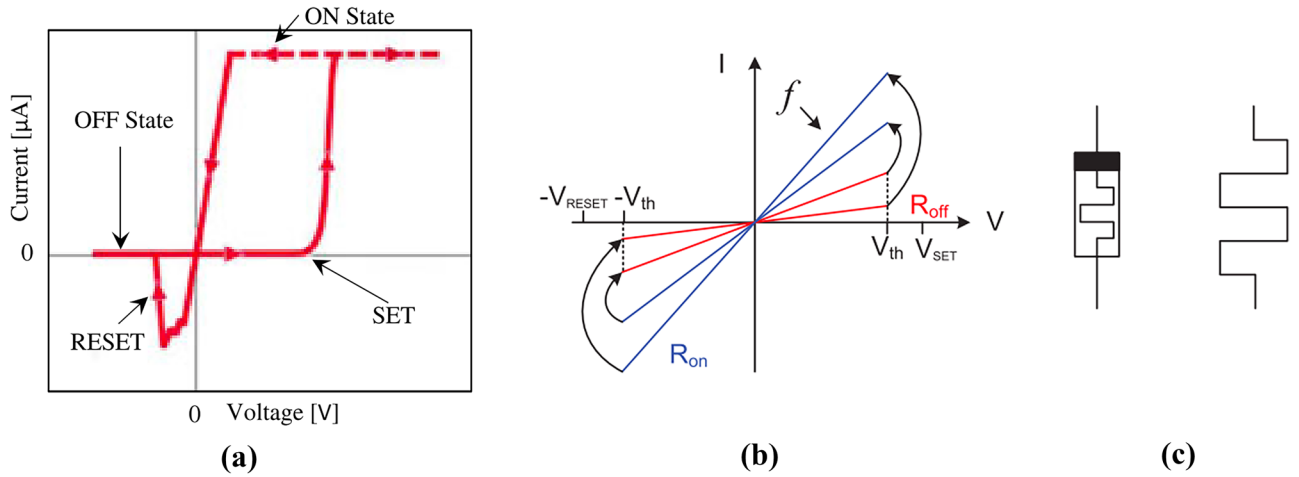


Fig. 1 (**a**) I-V characteristics of a biplar resistive switching device [34], (**b**) Influence of *f* on I-V hysteresis loop [38], and (**b**) Symbols used for representing memristive devices [38]

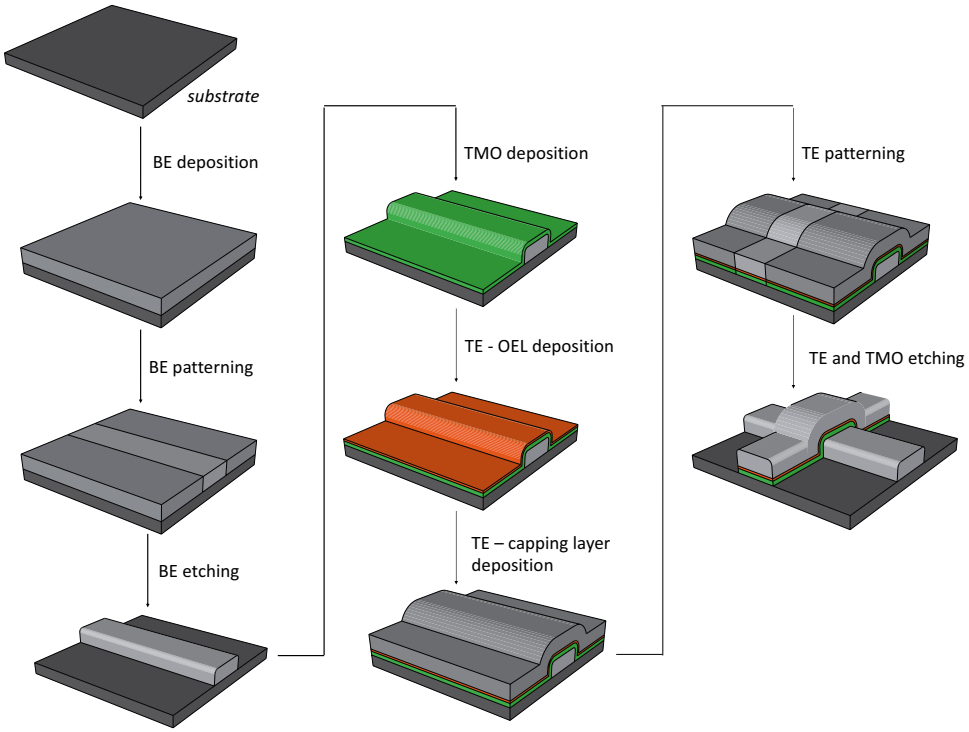
and the switching mechanism. The switching mode can be unipolar or bipolar, where the former one depends on the voltage amplitude and consequently, SET and RESET operations are controlled by the same polarity. In contrast, bipolar switching has the SET and RESET operations controlled by reverse polarities. Moreover, RRAMs can be categorized according to the type of chemical modification responsible for the conductance change as filamentary switching and area dependent switching. When considering the filamentary switching, the Conductive Filament (CF) is formed through the electroforming process, which is a soft breakdown phenomenon that creates a locally degraded region with high defect concentration [33]. Note that the CF is made out of metallic impurities or oxygen vacancies, which are responsible for charge transport. However, in the area dependent type the switching takes place homogenously along the whole area of the electrode-oxide interface. Finally, RRAMs can be further categorized according to their switching mechanisms: (a) Valence Change Mechanism (VCM), (b) Electrochemical Mechanism (ECM) and, (c) Thermochemical Mechanism (TCM) [35]. These three classes of switching phenomena involve electro and thermochemical effects in the resistance change of a MIM memory cell [35]. The switching process of VCM cells is based on the oxygen vacancy generation and migration. The conductive path is formed due to the positively charged oxygen vacancies, while the electric current is defined by the electrostatic barrier in the band diagram. The SET operation occurs when applying negative bias voltage on the memristor active electrode of high work function material, increasing the device conductivity. However, RESET operation is performed by reversing the bias polarity, allowing the oxygen recombination. The most common VCM RRAMs use *TaO*, *HfO* and *TiO*. As this work focuses on VCM devices, further information regarding the other two types of memristors can be found in [35].

3 Manufacturing Process and Possible Defects

This Section provides details about the manufacturing process of CMOS and memristive devices. When looking at the CMOS manufacturing process, considering most of the manufacturing steps, a certain area on the chip is masked out using the appropriate optical mask so that a desired processing step can be selectively applied to the remaining regions [9]. In more detail, the manufacturing of integrated circuits requires a large number of processes that are repeatedly performed until the circuit is completely built, first the Front-End-Of-Line (FEOL) and then the Back-End-Of-Line (BEOL). FEOL refers to the steps toward the device's development and BEOL to the steps to build the interconnections as well as any passive device required by the circuit. CMOS manufacturing process starts with the wafer preparation followed by (a) photolithography, (b) etching, (c) doping, (d) material deposition and (e) planarization. *Photolithography* is the process that allows creating a desired pattern on the wafer based on the following stages: (a) photoresist coating application, (b) mask alignment, (c) wafer exposure, (d) development and finally, (e) hard baking. The second step of the manufacturing process is *etching*, which consists of removing a portion of the material that was deposited or grown on the wafer. Usually, the etching process is performed using chemical solutions able to remove the unprotected parts, while the photoresist film defined by the photolithography acts as a protection. After removing the

Memristive Devices	
Manufacturing process steps:	**Possible process(es):**
1. BE deposition	Physical Vapor Deposition (PVD)
2. BE patterning	Nano Imprint Lithography (NIL) or Ebeam Lithography
3. BE etching	Reactive Ion Beam Etching (RIBE) or Reactive Ion Etching (RIE)
4. TMO deposition	PVD or Atomic Layer Deposition (ALD)
5. TE deposition	PVD
6. TE patterning	Ebeam Lithography
7. TMO and TE etching	RIBE

(a)



(b)

Fig. 2 (**a**) Memristive device manufactuirng process details and (**b**) Schematic view of the memristive device manufactuirng process

unprotected material, adding atoms to the remaining material in order to modify its electrical (conduction) properties is the next step. This process is called *doping*. In more detail, there are two common methods for doping a material: (a) *diffusion* and (b) *ion implantation*. The next step is named *deposition* and is used for creating thin layers of different materials. Such depositions are always laid out over the entire wafer by adopting chemical or physical methods, known as Chemical Vapor Deposition (CVD) and Physical Vapor Deposition (PVD), respectively. Finally, the *planarization* is the act of obtaining a flat and smooth surface out of a rough topography, being required because the deposition of different materials results in non-uniform topographies.

As previously mentioned, filamentary, memristive VCM cells can be manufactured using different materials, being classified according to their switching mode, conductive path and switching mechanism. Different implementations of a HfO2-based memristor (TiN/HfO2/TiN or TiN/HfO2/Ti/TiN) are described in [10, 11, 4, 23] and a TaOx based memristor (Ta2O5/TaOx) proposed by Panasonic is described in [15, 19, 15]. The manufacturing process of memristive devices aims to create devices composed of three main parts, the Bottom Electrode (BE), the Transition Metal Oxide (TMO) and finally, the Top Electrode (TE). The memristor can be manufactured on a silicon-based substrate or on a processed integrated circuit with planarized contact pads. In general terms, the memristor fabrication includes the same basic processes, such as lithography, deposition and etching [20, 39, 13, 20]. Note that the conduction mechanism in the deposited oxide relies on the bond breaking between metal and oxygen ions. Hence, an essential aspect regarding the manufacturing of memristors is that the process typically does not require doping, which eliminates a relevant source of process variation in standard CMOS circuits [25, 24].

For this study, mirco- and nanosized crossbar-type oxide-based memristive devices are taken as one prominent example [26]. Here, memristive cells are built at the lines' cross junctions. Replacing the electrode lines of a single device by word- and bit-lines of an array, it is easily anticipated that the single crossbar elements can be considered as building blocks of passive memristive crossbar arrays [21, 22]. A slightly different device form is the pillar cell, where the MIM layer stack is deposited as a whole and is finally etched into the desired shape. The BE and TE are contacted by vias [11]. Note that in this paper, the focus is laid on the crossbar cell design due to the possibility to build on every substrate, either a passive, planar disc or a CMOS-type substrate with contact pads reaching to the top surface [10]. It is important to highlight that after manufacturing, especially the oxide-based filamentary-type devices, usually have a very high electrical resistance and a large voltage is required for the very first SET operation, also known as the forming process [16]. This process, a controlled soft breakdown, drastically reduces the device resistance allowing the resistance switching behavior in the subsequent cycles for the filamentary regime. Figure 2a summarizes the main manufacturing process steps for a typical crossbar structured VCM-based memristive device [20, 39, 13, 20], including the possible processes, whereas Fig. 2b depicts the schematic view of the entire manufacturing process step-by-step.

Note that it is possible to adopt different processes, depending on the material used for fabricating the devices. For example, the etching of the BE, which is a high work function metal can be performed by Reactive Ion Etching (RIE), when using *TiN*, or Reactive Ion Beam Etching (RIBE), when adopting *Pt* as material. The BE is the first element fabricated, including the material deposition, patterning and etching. The second part to be manufactured is the TMO, the transition metal oxide, i.e., the regime where the resistive switching takes place, and which can be made from either single or double layers of metal oxides. The TE is composed of two different layers, the Oxygen Exchange Layer (OEL), which is formed from a low barrier, chemically active metal and a capping layer, which protects the reactive metal against atmosphere or further chemical process steps, as depicted in Fig. 2b. The TE is deposited and the patterning and etching are performed for all deposited layers, TMO and TE. Finally, after the structuring of the full device a passivation step can be performed.

Defining an accurate fault model for memristive devices based on realistic manufacturing defects represents a big challenge because the access to real data collected during a step-by-step inspection of manufactured devices is limited. In a first approach given in the literature, as adopted for CMOS technology, it is assumed that possible manufacturing defects can be modeled using linear resistances in order to identify the faults affecting memristive devices [34, 34]. In more detail, the defect injection scheme is based on the introduction of resistors connected in series with the memristive device. However, as shown in literature, the use of linear resistance to model the defects within RRAM at the terminals is inaccurate, as the resistance cannot properly reflect how defects impact the non-linearity (loop hysteresis) of the RRAM device [7]. In more detail, this approach can provide some insights regarding the possible faults, but it lacks accuracy. Analyzing the memristive device manufacturing process may allow to derive a more suitable defect injection mechanism and more accurate fault models. Table 1 summarizes the possible defects that can occur during the manufacturing of the analyzed novel crossbar-like memristive devices and their associated misbehaviors.

The possible defects included in Table 1 were derived from experience with the VCM-based memristive device manufacturing process, the continuum and compact models for filamentary switching, bipolar VCM-type resistance switching [36], and literature associated to CMOS technology as well to memristive devices as discussed in the following.

As previously mentioned, crossbar memristive device cells can be fabricated after FEOL, more precisely after the fabrication of the lower metal layers of the BEOL. The standard CMOS fabrication process (FEOL and BEOL) introduces defects that often are caused by impurity depositions, behaving as resistive defects at electrical level. Resistive defects represent the lumped effect of broken or irregular shaped metal lines, narrow, cracked or non-existent vias, and dust particles deposited between layers impeding proper electric conductivity [14]. The fabrication of lower metal layers adopts the standard CMOS process and consequently, the same defects may occur. Potential defects include incomplete wiring or via fills and thinner wires, which result in resistive opens, shorts and bridges caused by line-edge roughness or misalignment, for example [34]. As previously mentioned, the devices adopted for the analysis proposed in this paper can be manufactured on different substrate types, making a further investigation about the possible defects that can occur in this part of the circuit or even in the interface with the memristive devices essential. Note that pillar cells are fabricated following different manufacturing process steps and consequently, may be affected yet by other defects not to be discussed in this paper.

When considering the fabrication of VCM-based memristive devices, chemical and physical conditions can affect the composition as well as the microstructure of the deposited BE thin film and imprint residual stress, which in turn affects the quality of the forming process [14]. In more detail, the amplitude of the signal required for forming affects the LRS value. In extreme situations, this effect can prevent the forming process entirely, resulting in an open circuit-like behavior. BE deposition can also be contaminated by precursors,

Table 1 VCM-based filamentary, binary-type memristive devices based on TMO resistive switching layers: possible defects and faulty behaviors

Manufacturing process steps:	Possible defects:	Possible defective/faulty behavior(s):
BE deposition	Thickness variations (thinner of thicker)	Increased contact/line resistance; lower or higher heat conductance; lower or higher quality of forming process
	Poor or no bonding with contacts	
	Contamination associated to depostion process	
BE patterning	Contamination by residual photolayer/polymer	Increased resistance; lower heat conductance; undefined impurities on the BE surface; line length/resistance modified; switching area modified; well area undefined/high sheet resistance in the regime of reduced BE thickness
	Shift of the structure (markers)	
	Over-/under-development	
	Trapezoidal shape of the resist structure	
BE etching	Under etching (shorts and bridges)	Increased line resistance; increased capacitance; change in the electrode work function; electrical field variation (hot spots)
	Overetching (opens)	
	Contamination by etchant	
	Higher electrode roughness	
TMO deposition	Poor bonding with BE	Increased variability of I-V characteristics in the pristine state; increased variability of the electroforming voltage; inreased variability of the resistance; reduced switching stability; uncontrolled increase/decrease of the initial leakage; heat conductance modification; oxygen vacancy concentration variations
	TMO local composition variations in the metal to oxygen stoichiometry	
	TMO thickness variations	
	Contamination by carbon or hydroxy-impurities	
	Crystal structure variations	
TE deposition (including OEL and capping layer)	Thickness variations	Electroforming voltage variations; oxygen chemical potention between OEL and TMO variation; increased resistance; increased diffusion path; increased variability
	Contamination associated to depostion process	
	Poor bonding between OEL and capping layer	
TE patterning	Contamination by residual photolayer/polymer	Increased contact resistance
TE etching	Sidewall redeposition	Shorts; edge modficaiton or damage; weak spots for filament formation
	Etching damage	
Passivation & contact pad opening	Poor or no bonding with contacts	Increased or reduced resistance; lower or higher heat conductance
	Contamination	

materials related to previous production steps, dust/small particles, etc. Moreover, it is possible to observe BE thickness variations as well as poor or no bonding between BE and pads. These possible defects can cause memristive devices' deviations, increasing their resistance as well as reducing their heat conductance and the forming process quality. BE patterning can also be contaminated by residual photolayer/polymer, have over-/under-development and a modification of the resist structure shape. These possible defects may lead to increased resistance, lower heat conductance and variation of the switching area. BE etching could leave the metal surface rough, leading to large resistance variations. Under- and over-etching can introduce open, short and bridge defects, as observed in CMOS technology. Moreover, BE defects can also change the electrode work function and introduce variation of the electrical field (hot spots). Resuming, BE patterning and etching may lead to switching area variations, affecting the device performance [30, 32]. In more detail, the device's size affects its resistance because it alters the probability of forming the CF [10]. The TOM deposition is vulnerable to different problems related to precursors and cleaners, which may introduce thick or thin localized spots [34, 34]. Other important possible defects associated to TMO deposition include poor bonding with BE and variations in the crystal structure. The oxygen vacancies concentration and the oxide thickness have a strong impact on the device's performance [34]. Note that during the deposition process of TMO, an Oxygen Exchange Layer (OEL) and a capping layer are added. Further, a deficient capping layer deposition can lead to large variations in the characteristics of the forming process and the efficiency of the switching behavior [14]. The TE is fabricated on the top of the capping layer following a similar process as the BE. The etching step may lead to material redeposition along the device's sidewalls. This material can form a leakage path next to the VCM-based memristive device reducing the resistance and the forming voltage and increasing the device's variability [1, 1]. After manufacturing the TE, the memristor is pacified, which means that the device is isolated from the surroundings and the TE is connected to the metal layers. Finally, a further step is still required in order to have the manufactured device working. In more detail, the CF in the oxide has to be formed. The forming step may be performed by applying different schemes, most commonly voltage pulses with different pulse widths. Note that the current that flows through the memristor during the forming step has a severe impact on the CF shape, which in turn influences the device characteristics during operation [34]. The forming current needs to be kept constant, since variations will result in more resistive variations later on [31, 18]. Higher forming currents result in wider CF structures, leading to lower mean resistance and standard deviation, while lower currents generally lead to higher mean and standard deviation of the device resistance [34]. Thus, two different defects can occur during the forming step. The first one is an oxide breakdown of the memristor and the second occurs when the forming step fails, and no CF is formed. As result of the first defect, the device remains always in LRS, or if

less severe, the device is still able to switch, but the resistance has shifted below its intended value. However, when considering the second possible defect, the device is stuck in HRS.

4 Discussion about Memristive Device Fault Models

The development of efficient manufacturing test procedures requires realistic defect injection schemes and accurate fault models. From the previous Section it is possible to identify that manufacturing defects can affect different memristor's parameters causing the following main misbehaviors:

- Increased or decreased resistance of contacts and lines;
- Lower heat conductance;
- Lower quality or ineffective forming step;
- Increased BE-oxide interface oxygen vacancy concentration;
- Changes in oxygen vacancy concentration in the oxide.

The *increasing or decreasing resistance of the contacts and lines* may be modeled using a linear resistor, the same defect injection scheme adopted for CMOS technology. However, this defective behavior will be propagated as an analog deviation, which may require more complex test procedures, such as parametric test strategies.

The deviation associated to the *heat conductance* could affect the switching properties of the device. The stochastic properties of the switching behavior will significantly increase the complexity of properly model this misbehavior as well as test strategies. With respect to the possible faulty behaviors, it would be possible to identify four different situations: (a) the device is not able to correctly switch during the defined SET or RESET time, impacting the device's functionality, (b) the device presents parametric deviations, impacting its performance, (c) the device presents a random misbehavior, being observed in some occasions, and (d) the device's reliability is affected due to the degradation of the switching capacity over time caused by aging mechanisms. Note that the first situation represents Easy-To-Detect (ETD) faults, since the faulty behavior will be propagated at logic level, making its detection trivial [6]. However, the second and third situation represents Hard-To-Detect (HTD) faults that do not impact on the device's functionality, but can cause parametric deviations, increasing test complexity and requiring the use of e.g. defect-oriented test strategies. Note that HTD faults do not always lead to incorrect behavior; nevertheless, they compromise the device's reliability. Extensive studies including the impact of temperature on the behavior of memristive devices should be conducted to allow an accurate identification of the relation between heat and memristor's behavior.

Regarding the third point of the possible misbehaviors, *the correct formation of the CF during the forming process* is considered critical as it may lead to defective devices. Defective devices may remain in HRS, which leads to ETD faults, more precisely to stuck-at faults. However, there is also a possibility that devices may switch from HRS or even LRS to an undefined state. The detection of undefined states is not trivial, since it demands the measurement of analog values/states. To better illustrate this situation, electrical simulations of a RRAM (3×3 word cell array) with

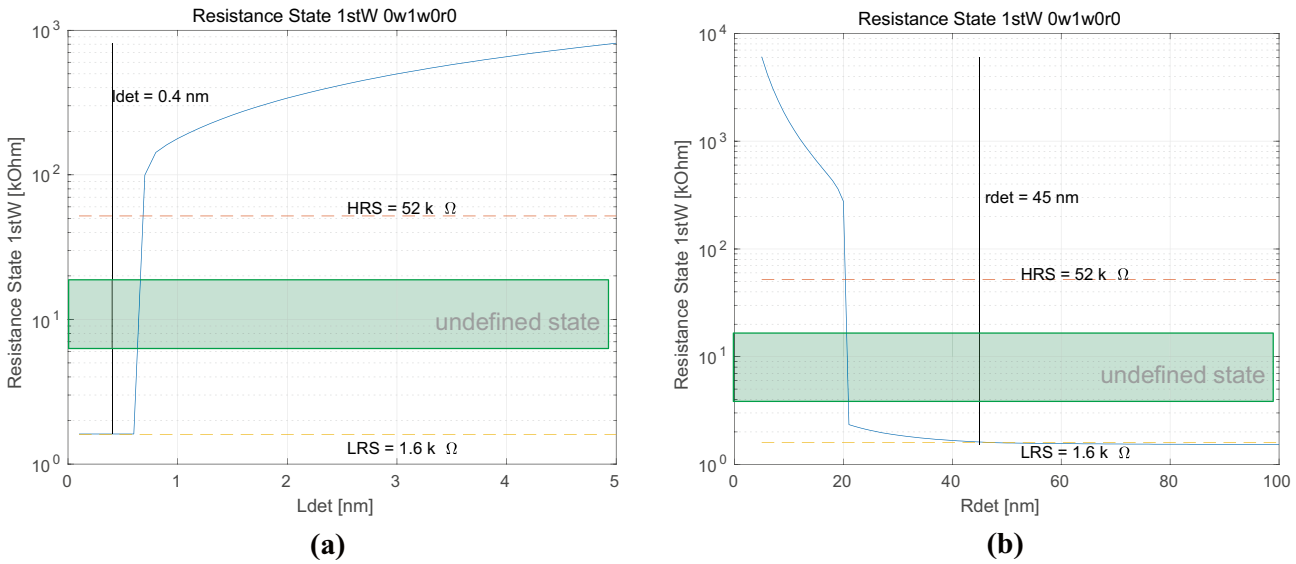


Fig. 3 (**a**) *Ldet* variation impact on resistance state of the memristor, and (**b**) *Rdet* impact of tne resistance state of the memristor

peripheral circuitry were performed. The memory array was implemented using the 130 nm Predictive Technology Model (PTM) for the CMOS-based circuits and the RRAM (Pt/HfO2/TiOx/Pt) compact model from [17]. The voltage adopted for performing a write '1'operation, or in other words a SET operation, is equal to 1.6 V. The RESET operation is performed by applying a voltage of—1.7 V, and READ operations require voltage pulses of 0.16 V. The forming step has a strong impact on the length (*Ldet*) and radius (*Rdet*) of the CF. For example, higher forming current will lead to wider and longer filaments, which have lower resistance, and vice versa. Figure 3 depicts the impact of varying these two different parameters associated to the CF. In Fig. 3a it is possible to see the impact of varying (*Ldet*), and in Fig. 3b *Rdet* [17, 3]. The resistance state values of the memristor were measured after performing the SET operation present in the operating sequence shown in Fig. 3a and b. Moreover, the range intervals adopted for performing these simulations were defined based on the constraints defined in [17], where the nominal value for *Ldet* is 0.4 nm and for *Rdet* is 45 nm.

Observing Fig. 3a, it is possible to see a linear dependency between *Ldet* and the resistance state of the memristive device. The resistance state of the memristor changes from 1.6kΩ to nearly 100KΩ when *Ldet* assumes a value higher than 0.6 nm, showing that the memristor is not able to properly switch from '0' to '1', SET operation. Figure 3b illustrates the relation between *Rdet* and resistance state of the memristor. The graph shows that *Rdet* needs to be larger than 20 nm to guarantee the correct execution of the write '1' operation, otherwise the memristor would remain at logic '0' (HRS). Thus, these results demonstrate that variation on the manufacturing parameters of the memristive devices, in this case more specifically to the forming step (length and radius of the CF), can compromise the correct behavior of the novel device. Further, the results plotted in these two graphs show that depending on the *Ldet* and *Rdet* values the device can assume an undefined state, since it reaches a value in between LRS and HRS, which can complicate the fault detection during the execution of manufacturing test procedures.

The defective behavior associated to *increased BE-oxide interface oxygen vacancy concentration* may affect the switching properties and the device resistance. Figure 4 depicts the memristor devices' behavior when changing the oxygen vacancy concentration, minimum (*Ndiscmin*) and maximum (*Ndiscmax*) [17]. Figure 4 depicts the resistance state of tthe cell when performing the second write operation related to the operation sequence *0w1w0r0*. In Fig. 4a, assuming an increment factor of 0.001 for *Ndiscmin*, it is possible to see that cell's correct behavior may only be guaranteed by keeping *Ndiscmin* smaller than 0.4×10^{26} m^{-3}, otherwise, the cell remains at LRS or even switches to an undefined state. When varying *Ndiscmax* from 10×10^{26} m^{-3} to 30×10^{26} m^{-3}, assuming an increment factor of 1×10^{26} m^{-3} during each simulation, the resistance state remains relatively constant, around 52 kΩ, when considering an Ndiscmax below 20×10^{26} m^{-3}. Note that from 20×10^{26} m^{-3} to 22×10^{26} m^{-3}, the resistance state gradually decreases until reaching values close to LRS, which means that the cell is going to be stuck-at-1. Thus, from Fig. 4a it becomes clear that the minimal oxygen vacancy concentration has an exponential effect on the HRS resistance. Hence, if the manufacturing process suffers from the last two main misbehaviors listed at the beginning of this Section, more and more faults leading to undefined states will be observed.

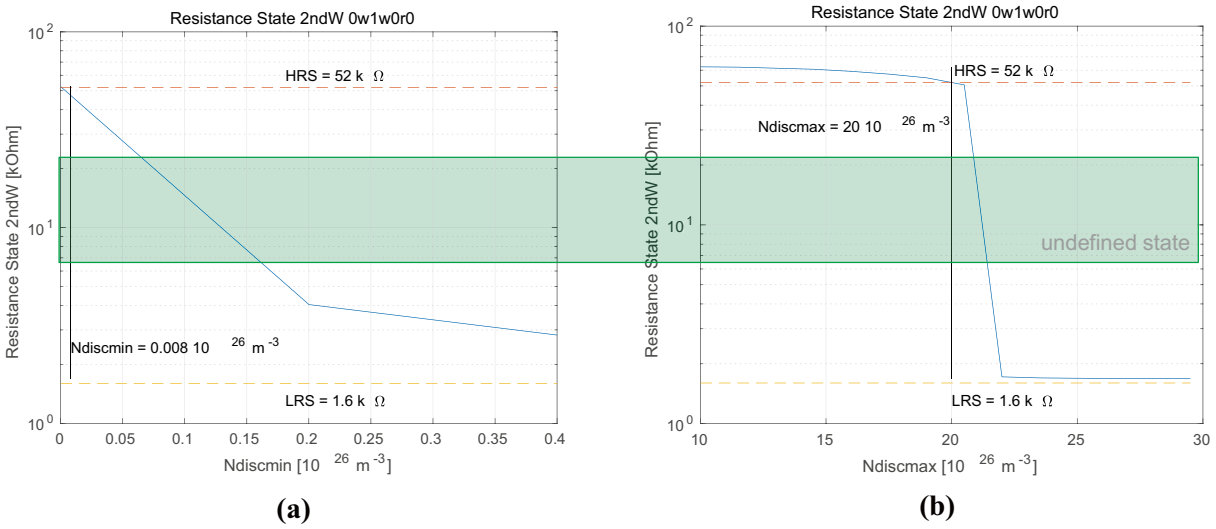


Fig. 4 (**a**) *Ndiscmin* variation impact on resistance state of the memristor, and (**b**) *Ndiscmax* impact of tne resistance state of the memristor

Read faults are also be observed more frequently, reducing the reliability of the memristor-based cells. Moreover, lower HRSs will be observed, which increase the energy consumption.

In general, more vacancies lead to faster switching and lower forming voltage. The latter may lead to oxide breakdown or even to different faults associated to READ operations, as observed in the CMOS technology. Changes in oxygen vacancy concentration inside the oxide may also affect the quality of the forming process, resulting in similar fault behavior as the previous defective behavior (*lower quality or ineffective forming step*). In general terms, these faulty behaviors can be observed at chemical and electrical level and, in order to derive an accurate fault model, need to be properly represented by a realistic defect injection scheme. Clearly, a linear resistor can not properly represent these defects because it affects the surroundings of the memristor only and not the internal state itself. One possibility for addressing this issue could be based on the directly modification of manufacturing parameters presents in the description of resistive device models, such as the models described in [17].

As observed in nanoscale CMOS technology, the expected defects do not necessarily propagate faults at logic level, hence deviations may be observed at electrical level only. The presence of parametric faults will require the adoption of not only software-based test approaches, able to detect functional faults at logic level, but also the adoption of hardware-based strategies able to perform parametric testing. Another important point that increases the test complexity when considering memristive devices is related to the fact that manufacturing defects can cause intermittent and random faults [8]. In [34] the authors defined two distinct fault models for RRAMs: (1) the conventional fault model and (2) the unique fault model. In more detail, the conventional fault model is composed of faults that are similar to the ones observed in traditional memories, while unique fault models represent a set of faults that emerge due to RRAMs specific nature. Thus, according to the information above, manufacturing defects affecting memristive devices tend to introduce HTD faults. This is due to the stochastic and analog nature of the device. Consequently, the development of test procedures becomes more complex and expensive, since either the adoption of hardware-based strategies is required in order to perform parametric testing or special test conditions need to be defined.

5 Final Considerations

The development of efficient manufacturing test procedures represents a critical aspect limiting the adoption of memristive devices for implementing emerging applications, since test escapes may directly affect the reliability of the entire application. Despite the similarities of the memristive device manufacturing process with the one adopted for CMOS devices, the possible defects affecting such novel devices may lead to specific faulty behaviors. As previously mentioned, the currently knowledge regarding these topics indicates that defective memristive devices cause different faulty behaviors, when comparing to the possible faults observed in the CMOS technology. These unique functional or electrical deviations occur due to the stochastic and analog nature of the memristive device, making the definition of a specific and realistic fault model and the respective defect injection scheme crucial. For properly addressing this challenge, companies and laboratories that are able to fabricate memristive devices should provide more information about their manufacturing processes. In more detail, a deep inspection strategy should be applied in order to accurately measure the functional and electrical deviations associated to each manufacturing process step. The results obtained by performing this kind of inspection could be used for identifying and characterizing the most common and critical defects, which in turn would allow the definition of a more realistic defect injection scheme and consequently, the identification of more accurate fault models. As future work, we intend to analyze the manufacturing process of memristive devices adopted at Research Center Jülich (FZJ), Germany, and define an manufacturing inspection strategy. The results obtained will be used for deriving a more accurate fault model, making the development of more suitable test procedures, able to deal with the unique memristive device nature, possible.

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