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Comparison of Two and Three-Level DC-AC Converters for a 100 kW Battery Energy Storage System

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***Abstract*—This paper discusses a qualitative comparison between Two and Three-Level Voltage Source Converter (VSC) topologies for battery energy storage applications. Three-Level Neutral Point Clamped (NPC) and T-Type circuit topologies are benchmarked versus the state-of-art Two-Level VSC in terms of efficiency and power density considering a 100 kW system. Analytical equations for determining the power losses in the semiconductor modules are given, and the procedure for designing the output *LCL* filter and the DC-link capacitors is described. The analysis, based on off-the-shelf circuit components, shows that the Three-Level topologies perform better than the Two-Level one in both considered metrics, mainly due to their lower switching losses that allow operating at higher switching frequency without significantly degrading the system efficiency, and, at the same time, increasing the system power density. Additionally, it is found that the T-Type topology shows better performances than the NPC topology at full and high partial loads, being then more suitable for applications that require most of the operation at maximum power.**

***Index Terms*—Battery energy storage systems, Voltage Source Converter, Neutral Point Clamped, T-Type.**

I. Introduction

Battery Energy Storage Systems (BESSs) are commonly interfaced with the distribution network through Power Electronics (PE) based Voltage Source Converters (VSCs). The conventional Two-Level (2L) or Three-Level (3L) circuits are mature technologies for Low to Medium Voltage power conversion and they have been widely applied in industrial applications and, above all renewable energy generation. For high power BESS and solar applications, the conventional three-phase 2L VSC, assembled with three half-bridge power modules, is the dominant circuit topology adopted by commercial products, mainly due to their robustness, low cost, and low complexity [1]–[3]. Nonetheless, in other fields, such as motor drives and wind power, multilevel topologies found more market attention, especially for Medium Voltage power conversion [4], [5].

Previous studies have shown how 3L VSCs can outmatch the conventional 2L VSC for moderate switching frequencies in terms of efficiency [6], [7]. In this paper such a comparison is performed for VSCs to be deployed for battery storage applications. The design of VSCs for storage applications is subject to different constraints and peculiarities from other power electronics applications, and so their design procedure can not be systematized based on the ones for other PE applications. BESSs, in fact, require highly efficient bi-directional operation and, depending on the grid service provided by the system, significant reactive power generation capabilities. Operation at partial loads for long periods of time may occur often. Additionally, BESSs are subject to the regulation of grid-connected systems, e.g., current harmonic injections, Low Voltage Ride Through, and voltage regulation at the point of common coupling [8], [9]. Another particularity of BESSs is related to the electrochemical battery, its impedance, in fact, strongly varies with the frequency, and its open-circuit voltage is related to the State of Charge (SoC) [10], affecting the converter's DC-link design.

In this paper, 100 kW 3L T-Type and Neutral Point Clamped (NPC) topologies for BESSs are benchmarked in terms of efficiency and power density versus the 2L circuit topology, Fig. 1. A low voltage DC-link is taken into consideration,

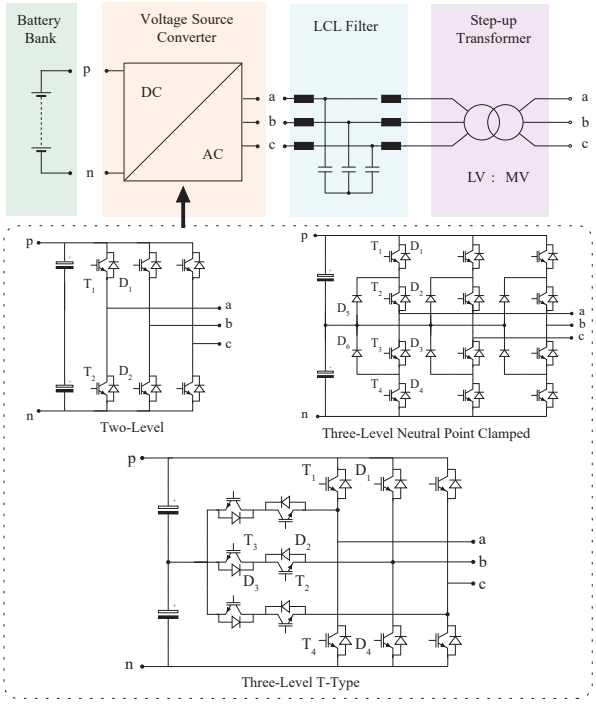

Fig. 1. BESS schematic and VSC circuit topologies considered in this study: Two-Level, Three-Level NPC, and Three-Level T-Type.

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compatible with the commercially available 89 kWh battery rack M3-R089 from Samsung [11]. The remainder of the paper is organized as follows. Section II analyses the Three-Level Converter (3LC) circuits considered in this study and Section III describes the analytical expressions to derive the semiconductors' efficiency. Section IV and V illustrate the methodology for the design and selection of the *LCL* filter and DC-link capacitors components. Section VI presents the conclusion of the study.

II. Three-Level Topologies

The schematic of a BESS together with the VSC circuit topology considered in this study are displayed in Fig. 1. The Two-Level Converter (2LC) is the topology that requires the least semiconductors; thus, it has reduced complexity and costs. Moreover, this topology has low conduction losses, since only one component at the time conducts the impressed AC current, and, at low switching frequencies, it offers overall outstanding performances. Nonetheless, the NPC topology for the same DC-link voltage as the 2LC, requires a lower voltage rating of the IGBT parts, since its components have to block half the DC-link voltage, and thus it shows lower switching losses. Besides, all components are of the same voltage class. The T-Type topology instead, is assembled with components of two different voltage classes, since the outer IGBTs, T_1 and T_4 have to block the full DC-link voltage; then it is subject to higher switching losses than the NPC due to the intrinsically lower switching performances of the higher voltage class devices. However, the terminal AC current conduction occurs through one semiconductor, when it is not flowing through the DC-link mid-point, offering an advantage in terms of conduction losses versus the NPC circuit.

For this study, the battery rack M3-R089 from Samsung has been considered [11]. Then, for all the semiconductors for the 2L VSC and for the semiconductors T_1/D_1 and T_4/D_4 of the 3L T-Type circuit, IGBT and diodes of the 1200V voltage class are selected. The devices T_3/D_3 and T_2/D_2 of the 3L T-Type circuit and all the one for the the 3L NPC, instead, allows the selection of a lower voltage rating, so the 650V voltage class is chosen. The converter AC output voltage is fixed to 400V line-to-line, and so the commercially available SKM300GB12T4, SEMiX305MLI07E4, SEMiX305TMLI12E4B TrenchGate IGBT4 modules rated at 300A are considered [12].

III. Semiconductor Efficiency

The power losses in the semiconductors can be analytically calculated based on the assumption that the switching frequency f_s is much greater than the grid frequency f_g. According to this assumption and considering Sinusoidal Pulse-Width-Modulation (S-PWM), the sinusoidal modulation waveform can be considered constant during one switching period. Then, given the on-state characteristics of the IGBTs and the diodes, modelled as a V_i and r_i circuit, the conduction losses are analytically predicted as function of the RMS and average current flowing through the component as:

$$P_\mathrm{c} = V_\mathrm{i} \cdot I_\mathrm{avg,i} + r_\mathrm{i} \cdot I^2_\mathrm{rms,i} \tag{1}$$

Switching losses, instead, are a function of the switching energies $E_\mathrm{on,off,rr}$ and must be scaled according to the switched voltage $V_\mathrm{dc,sw}$ and the datasheet reference voltage V_b:

$$P_\mathrm{s} = \frac{f_\mathrm{s} V_\mathrm{dc,sw}}{2\pi V_\mathrm{b}} \int_0^{2\pi} E_\mathrm{on,off,rr} \mathrm{d}\omega\mathrm{t}. \tag{2}$$

Furthermore, the switching energies as well as the on-state parameters are temperature dependant and they can be linearized as a function of the junction temperature. Then, to evaluate the losses, it is necessary to find the expression of the average and RMS current through the semiconductor. Following that, the current expressions are given, where the phase shift of the current with respect to the voltage at the fundamental frequency is indicated with φ, and the modulation index and the peak output AC current with m and $\hat{I}_\mathrm{ac}$ respectively. The components denomination is done according to Fig. 1.

A) Two-Level Converter:

$$I_{\mathrm{avg,T_{1,2}}} = \frac{\hat{I}_\mathrm{ac}}{8\pi}\Big(m\pi\cos\varphi + 4\Big) \tag{3}$$

$$I_{\mathrm{avg,D_{1,2}}} = \frac{\hat{I}_\mathrm{ac}}{8\pi}\Big(4 - m\pi\cos\varphi\Big) \tag{4}$$

$$I_{\mathrm{rms,T_{1,2}}} = \frac{\hat{I}_\mathrm{ac}}{2}\sqrt{\frac{8m\cos\varphi + 3\pi}{6\pi}} \tag{5}$$

$$I_{\mathrm{rms,D_{1,2}}} = \frac{\hat{I}_\mathrm{ac}}{2}\sqrt{\frac{3\pi - 8m\cos\varphi}{6\pi}} \tag{6}$$

B) Three-Level Neutral Point Clamped Converter:

$$I_{\mathrm{avg,T_{1,4}}} = m\frac{\hat{I}_\mathrm{ac}}{4\pi}\Big[(\pi - \varphi)\cos\varphi + \sin\varphi\Big] \tag{7}$$

$$I_{\mathrm{avg,T_{2,3}}} = \frac{\hat{I}_\mathrm{ac}}{4\pi}\Big(m\varphi\cos\varphi - m\sin\varphi + 4\Big) \tag{8}$$

$$I_{\mathrm{avg,D_{1,2,3,4}}} = m\frac{\hat{I}_\mathrm{ac}}{4\pi}\Big(\sin\varphi - \varphi\cos\varphi\Big) \tag{9}$$

$$I_{\mathrm{avg,D_{5,6}}} = \frac{\hat{I}_\mathrm{ac}}{2\pi}\left[m\left(\varphi - \frac{\pi}{2}\right)\cos\varphi - m\sin\varphi + 2\right] \tag{10}$$

$$I_{\mathrm{rms,T_{1,4}}} = \hat{I}_\mathrm{ac}\sqrt{\frac{m}{6\pi}}\Big(1 + \cos\varphi\Big) \tag{11}$$

$$I_{\mathrm{rms,T_{2,3}}} = \frac{\hat{I}_\mathrm{ac}}{2}\sqrt{1 + \frac{2m}{3\pi}\Big(2\cos\varphi - \cos^2\varphi - 1\Big)} \tag{12}$$

$$I_{\mathrm{rms,D_{1,2,3,4}}} = \hat{I}_\mathrm{ac}\sqrt{\frac{m}{6\pi}}\Big(1 - \cos\varphi\Big) \tag{13}$$

$$I_{\mathrm{rms,D_{5,6}}} = \frac{\hat{I}_\mathrm{ac}}{2}\sqrt{1 - \frac{4m}{3\pi}\Big(\cos^2\varphi + 1\Big)} \tag{14}$$

C) Three-Level T-Type Converter:

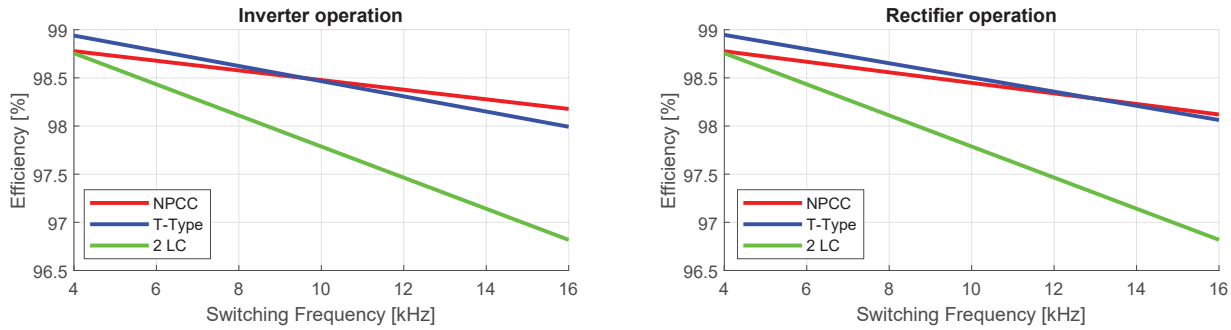

Fig. 2. Semiconductor efficiency of 3L and 2L topologies at maximum power for inverter and rectifier operation varying the switching frequency. 3L topologies provide higher efficiency than 2L in all the frequency range analysed.

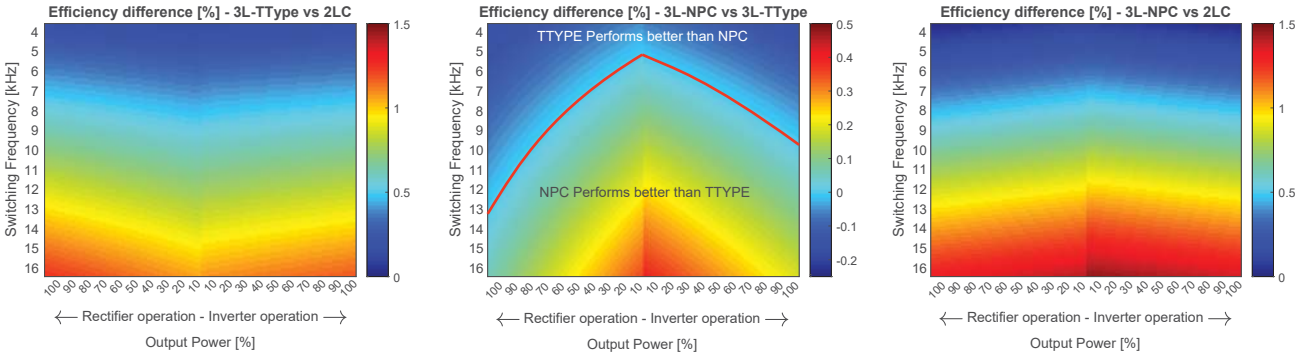

Fig. 3. Semiconductor efficiency gain of 3LCs over 2LC and difference between T-Type and NPC varying the output power and the switching frequency for a modulation index m=0.725.

$$I_{\mathrm{avg,T_{1,4}}} = m\frac{\hat{I}_{\mathrm{ac}}}{4\pi}\left[(\pi-\varphi)\cos\varphi+\sin\varphi\right] \tag{15}$$

$$I_{\mathrm{avg,T_{2,3},D_{2,3}}} = \frac{\hat{I}_{\mathrm{ac}}}{4\pi}\left[(2\varphi-\pi)m\cos\varphi-2m\sin\varphi+4\right] \tag{16}$$

$$I_{\mathrm{avg,D_{1,4}}} = m\frac{\hat{I}_{\mathrm{ac}}}{4\pi}\left(\sin\varphi-\varphi\cos\varphi\right) \tag{17}$$

$$I_{\mathrm{rms,T_{1,4}}} = \hat{I}_{\mathrm{ac}}\sqrt{\frac{m}{6\pi}}\left(1+\cos\varphi\right) \tag{18}$$

$$I_{\mathrm{rms,T_{2,3},D_{2,3}}} = \frac{\hat{I}_{\mathrm{ac}}}{2}\sqrt{1-\frac{4m}{3\pi}\left(\cos^2\varphi+1\right)} \tag{19}$$

$$I_{\mathrm{rms,D_{1,4}}} = \hat{I}_{\mathrm{ac}}\sqrt{\frac{m}{6\pi}}\left(1-\cos\varphi\right) \tag{20}$$

The switching losses are found integrating the switching energy as a function of the switched current during the switching time of each component, as shown in Equation (2). The switching energies are interpolated from the components datasheet and expressed as second-order polynomial functions, whose coefficients b_0, b_1, and b_2 are listed in Table I. The switching can then be found through:

A) Two-Level Converter:

$$P_{\mathrm{s,T_{1,2},D_{1,2}}} = \frac{f_s V_{\mathrm{dc}}}{2\pi V_{\mathrm{b}}}\left[\frac{\pi b_2 \hat{I}_{\mathrm{ac}}^2}{2}+2b_1\hat{I}_{\mathrm{ac}+\pi b_0}\right] \tag{21}$$

B) Three-Level Neutral Point Clamped Converter:

$$P_{\mathrm{s,T_{1,4},D_{5,6}}} = \frac{f_s V_{\mathrm{dc}}}{4\pi V_{\mathrm{b}}}\left[b_2\hat{I}_{\mathrm{ac}}^2\frac{(\pi-\varphi+\sin\varphi\cos\varphi)}{2}+ b_1\hat{I}_{\mathrm{ac}}(1+\cos\varphi)+b_0(\pi-\varphi)\right] \tag{22}$$

$$P_{\mathrm{s,T_{2,3},D_{1,4}}} = \frac{f_s V_{\mathrm{dc}}}{4\pi V_{\mathrm{b}}}\left[b_2\hat{I}_{\mathrm{ac}}^2\frac{(\varphi-\sin\varphi\cos\varphi)}{2}+ b_1\hat{I}_{\mathrm{ac}}(1-\cos\varphi)+b_0\varphi\right] \tag{23}$$

C) Three-Level T-Type Converter:

$$P_{\mathrm{s,T_{1,4},D_{2,3}}} = \frac{f_s V_{\mathrm{dc}}}{4\pi V_{\mathrm{b}}}\left[b_2\hat{I}_{\mathrm{ac}}^2\frac{(\pi-\varphi+\sin\varphi\cos\varphi)}{2} +b_1\hat{I}_{\mathrm{ac}}(1+\cos\varphi)+b_0(\pi-\varphi)\right] \tag{24}$$

$$P_{\mathrm{s,T_{2,3},D_{1,4}}} = \frac{f_s V_{\mathrm{dc}}}{4\pi V_{\mathrm{b}}}\left[b_2\hat{I}_{\mathrm{ac}}^2\frac{(\varphi-\sin\varphi\cos\varphi)}{2} +b_1\hat{I}_{\mathrm{ac}}(1-\cos\varphi)+b_0\varphi\right] \tag{25}$$

The parameters used in Equations (1)-(25) to estimate the power losses on the IGBT and diodes are listed in Table I. Fig. 2 displays the semiconductor efficiency of the 2LC and 3LC topologies at maximum power for inverter and rectifier operation varying the switching frequency, for a junction

TABLE I
PARAMETERS FOR ESTIMATING THE POWER LOSSES ON SEMICONDUCTOR MODULES - DERIVED FROM DATASHEET [12]

Topology		b_0	b_1	b_2	V_b [V]	V_i [V]	r_i [mΩ]
2LC	$T_{1,2}$	0	1.73e-4	4.83e-8	600	0.70	5.2
	$D_{1,2}$	0	1.13e-4	-1.14e-7	600	0.90	4.0
NPC	$T_{1,4}$	0	6.84e-5	-1.53e-8	300	0.82	3.1
	$T_{2,3}$	0	6.12e-5	-1.36e-8	300	0.82	3.1
	$D_{1,4}$	0	4.08e-5	-3.93e-8	300	0.85	2.7
	$D_{2,3}$	-	-	-	-	0.85	2.7
	$D_{5,6}$	0	2.38e-5	-2.61e-8	300	0.85	2.7
T-Type	$T_{1,4}$	0	9.17e-5	-1.51e-8	300	0.70	5.0
	$T_{2,3}$	0	7.94e-5	-3.73e-8	300	0.82	3.1
	$D_{1,4}$	0	7.94e-5	-1.67e-7	300	0.90	4.2
	$D_{2,3}$	0	6.45e-5	-1.18e-7	300	0.85	1.8

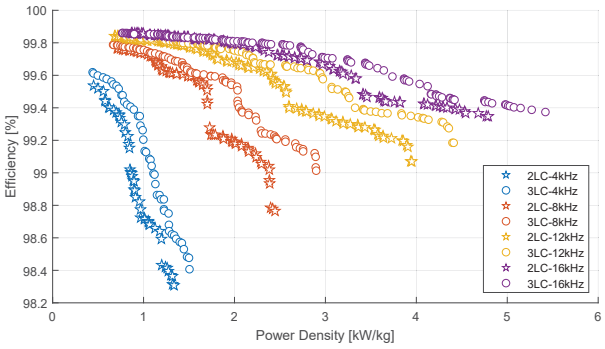

Fig. 4. Efficiency and power density of *LCL* filter designs for 2LC and 3LC for several switching frequencies.

temperature of 150°C. What stands out, is the declining of the 2LC efficiency at high switching frequencies. The 3L circuits, in fact, show better performances for moderate to high switching frequencies, i.e., >4 kHz, due to the lower switching energies. Additionally, in Fig. 3, the efficiency gain between the 3LC topologies versus the 2LC and between the NPC and the T-Type are displayed, varying both the switching frequency and the output power. As expected, the highest efficiency gain of the 3L topologies is for high switching frequencies. However, it can be noted that the 3L NPC offers better performances at low partial loads, while the 3L T-Type shows the opposite behaviour. Such consideration can be useful when designing the BESS's VSC for a specific application, e.g., for a mission profile that demands high operation at low partial load and/or high switching frequencies, the 3L NPC becomes the superior solution, while the 3L T-Type topology can become advantageous at higher powers and moderate switching frequencies, i.e., <12 kHz.

IV. *LCL* FILTER DESIGN

BESSs are devices connected to the electrical network; thus, they need to respect the connection rules imposed by the standards, e.g., the EN 50160 [9], regulating the voltage characteristics of distribution systems, and IEEE 519-2014 [8], regulating the current harmonics injection in the grid. PWM operated VSCs inherently generate voltage harmonics in the AC terminal, and in this context, a *LCL* filter is adopted to attenuate the resulting current harmonics injected in the grid to be compliant to the standards. The voltage harmonic spectrum produced by PWM modulated VSC can be calculated through the Bessel function as described in [13]. 3LC topologies have a lower harmonic content in the AC output with respect to the 2LC [13], [14]. Then, they require a lower attenuation by the filter and so a lower total inductance [15].

The design of the output *LCL* filter has to guarantee the attenuation of the high order harmonics, e.g., according to the standard IEEE 519-2014 I_h with h>35 has to be lower than 3% the nominal 50Hz current. The harmonic attenuation given by *LCL* filters can be approximated by [16]:

$$Att \approx \frac{1}{L_c L_g C \omega_h^3} \tag{26}$$

where L_c, L_g, and C are respectively the converter side and grid side inductance and the capacitance. $\omega_h = 2\pi f_h$ represents the first group of harmonics to be attenuated, generally a low order side-band of the switching frequency for the three-wire connection of the BESS. The resonance frequency of the filter f_{res} is generally chosen between $\frac{1}{6} f_s$ and $\frac{1}{2} f_s$, when the converter is controlled through the grid side current [17], for the digitally controlled VSC with sampling acquisition of $T_s = 1/f_s$ to fall into the stable region, and it is defined by the filter components as:

$$\omega_{res} = 2\pi f_{res} = \sqrt{\frac{L_c + L_g}{L_c L_g C}}. \tag{27}$$

From Equation (26) it can be noted that increasing ω_h the filter delivers the same attenuation with lower values of inductances and/or capacitance. Then, concerning the *LCL* output filter, the advantage of the 3LCs over the 2LC is twofold. First, a lower attenuation by the filter is required and so a lower total inductance can be accepted. Secondly, the 3LCs are well suited for high switching frequencies, due to their superior efficiency, and so the higher switching frequency allows for a reduced size of the output *LCL* filter.

Following the procedure illustrated in [18], several possible filter designs are evaluated in terms of weight, volume and losses at full power. The winding losses of litz (Cu) wires are analytically calculated based on the method proposed in [19], while the core losses of toroidal powder cores are calculated through the improved Generalized Steinmetz Equation (*iGSE*) [20]. Several core materials from [21] are considered, and the designs are checked for a maximum inductor temperature of 150°C. The power losses in the *LCL* capacitors are calculated according to the leakage current and the dissipation factors, derived from the manufacturers' datasheet [22], [23]. The *LCL* filter is then designed for several switching frequencies, and the Pareto fronts are displayed in Fig. 4, where the symbols differentiate between 2LC and 3LCs and the colours between the switching frequencies. As expected, it is observed that a higher power density and efficiency can be achieved with increasing switching frequency. Besides, under the same switching frequency, 3LCs offer better *LCL* filter power density and efficiency.

TABLE II
CAPACITANCE VALUES TO GUARANTEE THE REQUIRED ENERGY BUFFER AND LIMIT THE VOLTAGE RIPPLE

Ripple		Energy
2LC	3LCs	2LC - 3LCs
0.29 mF	2.93 mF	0.49 mF

V. DC-LINK DESIGN

Typically the DC-link capacitors in voltage source converters act as an energy buffer between the input and output of the converter [24]. In fact, for the three wire converters depicted in Fig. 1, without considering overmodulation, the peak AC phase voltage has to be always below half the DC-link voltage:

$$\frac{V_{\mathrm{dc,min}}}{2} - \frac{\Delta V_{\mathrm{dc,r}}}{2} \geq \hat{V}_{\mathrm{ac,max}} \tag{28}$$

Then, considering the minimum battery DC voltage, and a $\pm 10\%$ variation of the AC voltage from the nominal value, the maximum allowed voltage ripple is 55V. In this respect, the DC voltage ripple in a 2LC in case of balanced operation is driven by the high frequency components of the DC-link current and can be predicted as [25]:

$$\Delta V_{\mathrm{dc,2LC}} = \frac{3M\hat{I}_{\mathrm{ac}}\cos\varphi}{8 f_{\mathrm{s}} C_{\mathrm{dc}}}(1+M) \tag{29}$$

where C_{dc} is the DC-link capacitance value. In 3LCs, S-PWM modulated, the DC-link current shows a third harmonic component. Such low frequency harmonic dominates the higher frequencies ones and drives the DC-link voltage ripple [26]:

$$\Delta V_{\mathrm{dc,3LC}} = \frac{I_3}{3C\pi f_{\mathrm{g}}} \tag{30}$$

where the third harmonic current I_3 can be calculated as [26]:

$$I_3 = \frac{6MI_{\mathrm{pk}}}{5\pi}\left(\frac{2\cos\varphi}{3} + j\sin\varphi\right). \tag{31}$$

If the third harmonics is mitigated through space vector modulation, the DC voltage ripple is driven by the effect of the high-frequency components, as for the 2LC, and is subsequently reduced. Techniques for suppressing the low-frequency oscillation in the DC capacitors of the 3LCs have been proposed in literature [14], [27]. However, the applicability of such techniques is limited either by the power factor and/or by the modulation index [14], or by the necessity of installing additional circuitry [27]. For the case of BESSs, implementing single-stage power conversion as depicted in Fig. 1, there is no control over the modulation index, since both the DC side and AC side voltages are fixed respectively by the battery and the AC network unless a two-stage system is considered with the inclusion of a DC-DC converter. Moreover, four-quadrant operation is often required; thus, the region where the third harmonic can be cancelled out is limited [14]. In this context, the DC link is generally designed to mitigate the voltage ripple produced by the third harmonic.

Concerning the energy requirements, the DC capacitors are also designed in order to be able to sustain a load step ΔP in a time period T_{r}, allowing a maximum voltage deviation of ΔV_{dc} [28]. Then the minimum capacitance value is given by:

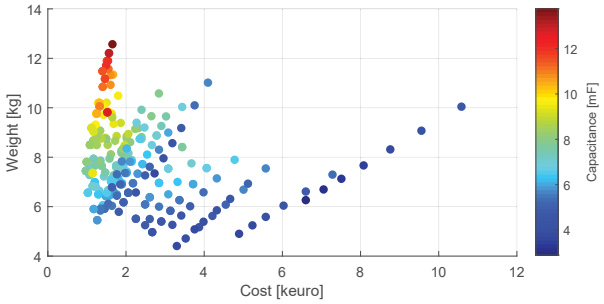

Fig. 5. Weight, costs and capacitance of the feasible DC-link capacitors designs selecting components from [22].

$$C_{\mathrm{dc,e}} \geq \frac{T_{\mathrm{r}} \cdot \Delta P}{(2 \cdot V_{\mathrm{dc}} \Delta V_{\mathrm{dc}})} \tag{32}$$

where T_{r} depends on the converter control delay and it is usually selected as 5 to 10 modulation periods [28]. Both 2LC and 3LCs are subject to this requirement.

According to the design specifications, the capacitance values that guarantee an adequate energy buffer and limit the voltage ripple are listed in Table II. As it is possible to see, the 3LCs require a much higher capacitance to limit the voltage ripple due to the third harmonic component in the DC current. Further design constraints come from the ripple current that electrolytic capacitors must withstand. The DC capacitors RMS current is equal for both 2LC and 3LCs [26], and it is analytically calculated through [29]:

$$I_{\mathrm{dc-cap}} = \hat{I}_{\mathrm{ac}}\sqrt{M\left[\frac{\sqrt{3}}{4\pi} + \left(\frac{\sqrt{3}}{\pi} - \frac{9}{16}M\right)\cos^2\varphi\right]}. \tag{33}$$

Electrolytic capacitors do not have high current capabilities, and then, their design usually leads to over-dimensioning the DC-link capacitance value in order to satisfy the current capability limitations, mainly defined by the desired minimal life-time of these components. For this reason, the DC-link design, in terms of components selections, does not present significant differences between 2LC and 3LCs. For example, considering the commercial capacitors of the $500V_{\mathrm{dc}}$ class from [22], the DC-link is designed considering parallel strings of two series capacitors. The number of parallel strings is a function of the maximum $I_{\mathrm{dc-cap}}$. The obtained designs are checked in terms of minimum capacitance, to satisfy the requirements of Table II, and minimum life-time of 20 years using the lifetime model given in [23]. The feasible solutions are plotted in Fig. 5 and it can be seen that the design with the lowest capacitance is found around 4 mF, which is higher than the minimum required capacitance shown in Table II.

VI. CONCLUSIONS AND FUTURE WORK

In this paper the design of semiconductors, *LCL* filter, and DC-link capacitors for BESS's 2L and 3L VSC have been discussed. It has been shown, that 3LCs have lower

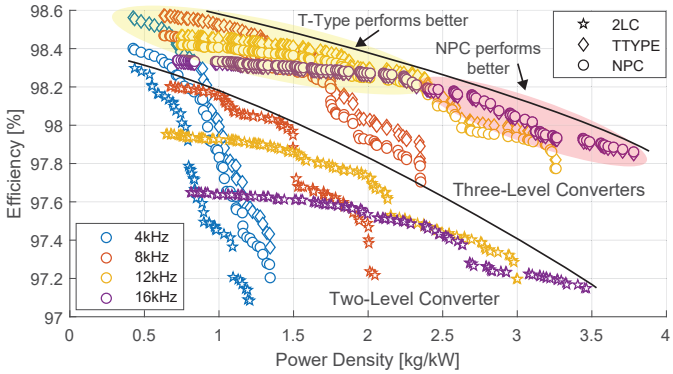

Fig. 6. System power density and efficiency at full power in inverter operation for different topologies and f_s.

semiconductor losses and that their efficiency does not decrease as much as for the 2LC for high switching frequencies. Furthermore, the analysis indicated that the T-Type topology outperforms the 3L NPC for moderate switching frequencies, i.e., $f_s \leq 12$ kHz, and at full and high partial loads. In this context, the T-Type might be the favourite for applications that require long operation at full power, while the 3L NPC is superior when operating mostly at low partial loads. Additionally, several feasible designs for the *LCL* filters and the DC-link capacitors have been shown. From Fig. 4 it is clear that increasing the switching frequency, lighter and more efficient filters can be designed. Regarding the DC-link, the procedure for its design has been illustrated, and it was shown how the poor current capability of aluminium electrolytic capacitors influences the design and leads to over-dimensioning of the DC-link in terms of capacitance value. The full system power density and efficiency at full power, considering a DC link design with a weight of 7kg, are displayed in Fig. 6. It can be seen that 3LCs perform significantly better both in terms of power density and efficiency since they do not suffer too much with the increase of switching frequency, thus resulting in higher power densities. Additionally, it is seen how the 3L T-Type circuit leads to the overall highest efficiency, while the 3L NPC at higher switching frequencies represents a good trade-off between power density and efficiency.

Future work will be focused on the experimental validation of the semiconductor and *LCL* filter models here described. Further analysis will be focused on relating the converter design with the battery storage application, introducing mission profiles in the study.

REFERENCES

[1] S. Vazquez, S. M. Lukic, E. Galvan, L. G. Franquelo, and J. M. Carrasco, "Energy storage systems for transport and grid applications," *IEEE Trans. Ind. Electron.*, 2010.

[2] K. Samir, J. I. Leon, D. Vinnikov, and L. G. Franquelo, "Grid-Connected Photovoltaic Systems," *IEEE Ind. Electron. Mag.*, 2015.

[3] M. Stecca, L. Ramirez Elizondo, T. Batista Soeiro, P. Bauer, and P. Palensky, "A Comprehensive Review of the Integration of Battery Energy Storage Systems into Distribution Networks," *IEEE Open J. Ind. Electron. Soc.*, 2020.

[4] T. B. Soeiro and J. W. Kolar, "The New High-Efficiency Hybrid Neutral-Point-Clamped Converter," *IEEE Trans. Ind. Electron.*, 2013.

[5] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative evaluation of advanced three-phase three-level inverter/converter topologies against two-level systems," *IEEE Trans. Ind. Electron.*, 2013.

[6] T. B. Soeiro, M. Schweizer, J. Linner, P. Ranstad, and J. W. Kolar, "Comparison of 2- and 3-level Active Filters with Enhanced Bridge-Leg Loss Distribution," in *8th Int. Conf. Power Electron. - ECCE Asia*, 2011.

[7] M. Schweizer and J. W. Kolar, "Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications," *IEEE Trans. Power Electron.*, 2013.

[8] IEEE Standards Association, "IEEE Std. 519-2014. IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems," 2014.

[9] CENELEC, "EN 50160 - Voltage characteristics of electricity supplied by public distribution systems," *Eur. Stand.*, 2010.

[10] C. Brivio, V. Musolino, M. Merlo, and C. Ballif, "A Physically-Based Electrical Model for Lithium-Ion Cells," *IEEE Trans. Energy Convers.*, 2019.

[11] Samsung SDI, "ESS Batteries by Samsung SDI," 2019. [Online]. Available: https://www.samsungsdi.com/ess/index.html

[12] "Semikron." [Online]. Available: https://www.semikron.com/products/product-classes/igbt-modules.html

[13] D. G. Holmes and T. A. Lipo, "Modulation of ThreePhase Voltage Source Inverters," *Pulse Width Modul. Power Convert.*, 2010.

[14] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Trans. Power Electron.*, 2000.

[15] K. Jalili and S. Bernet, "Design of LCL filters of active-front-end two-level voltage-source converters," *IEEE Trans. Ind. Electron.*, 2009.

[16] K. B. Park, R. M. Burkart, B. Agostini, and T. B. Soeiro, "Application of 1.7-kV 700-A SiC LinPak to Optimize LCL Grid-Tied Converters," *ICPE 2019 - ECCE Asia - 10th Int. Conf. Power Electron. - ECCE Asia*, 2019.

[17] Y. Wu, A. Shekhar, T. B. Soeiro, and P. Bauer, "Voltage Source Converter Control under Distorted Grid Voltage for Hybrid AC-DC Distribution Links," *IECON 2019 - 45th Annu. Conf. IEEE Ind. Electron. Soc.*, 2019.

[18] K.-b. Park, F. D. Kieferndorf, U. Drofenik, S. Pettersson, and F. Canales, "Weight Minimization of LCL Filters for High-Power Converters : Impact of PWM Method on Power Loss and Power Density," *IEEE Trans. Ind. Appl.*, 2017.

[19] J. A. Ferreira, "Improved Analytical Modeling of Conductive Losses in Magnetic Components," *IEEE Trans. Power Electron.*, 1994.

[20] J. Reinert, A. Brockmeyer, and R. W. De Doncker, "Calculation of losses in ferro- and ferrimagnetic materials based on the modified Steinmetz equation," *IEEE Trans. Ind. Appl.*, 2001.

[21] Chang Sung Powder Core Material. [Online]. Available: http://www.changsung.com/_eng/index.php

[22] Cornell Dubilier, "500C Capacitors." [Online]. Available: https://www.cde.com/capacitors/aluminum-electrolytic/screw-terminal

[23] Cornell Dublier, "Aluminum Electrolytic Capacitor Application Guide," Tech. Rep. [Online]. Available: http://www.cde.com/resources/catalogs/AEappGUIDE.pdf

[24] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters - An overview," *IEEE Trans. Ind. Appl.*, 2014.

[25] X. Pei, W. Zhou, and Y. Kang, "Analysis and Calculation of DC-Link Current and Voltage Ripples for Three-Phase Inverter With Unbalanced Load," *IEEE Trans. Power Electron.*, 2015.

[26] G. I. Orfanoudakis, M. A. Yuratich, and S. M. Sharkh, "Analysis of dc-link capacitor current in three-level neutral point clamped and cascaded H-bridge inverters," *IET Power Electron.*, 2013.

[27] J. Moia and M. L. Heldwein, "Carrier-based modulation technique to reduce low frequency ripple at the partial DC-link voltages of a three-level/-phase/-wire NPC converter applied to future DC bipolar active distribution networks," *PCIM Eur. 2016; Int. Exhib. Conf. Power Electron. Intell. Motion, Renew. Energy Energy Manag.*, 2016.

[28] L. Malesani, L. Rossetto, P. Tenti, and P. Tomasin, "AC/DC/AC PWM Converter with Reduced Energy Storage in the DC link," *IEEE Trans. Ind. Appl.*, 1995.

[29] J. W. Kolar and S. Round, "Analytical calculation of the RMS current stress on the DC-link capacitor of voltage-PWM converter systems," *IEE Proceedings-Electric Power Appl.*, 2005.