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MINIATURIZED CMOS CIRCUITS AND MEASUREMENT TECHNIQUES FOR BROADBAND DIELECTRIC SPECTROSCOPY

GERASIMOS VLACHOGIANNAKIS

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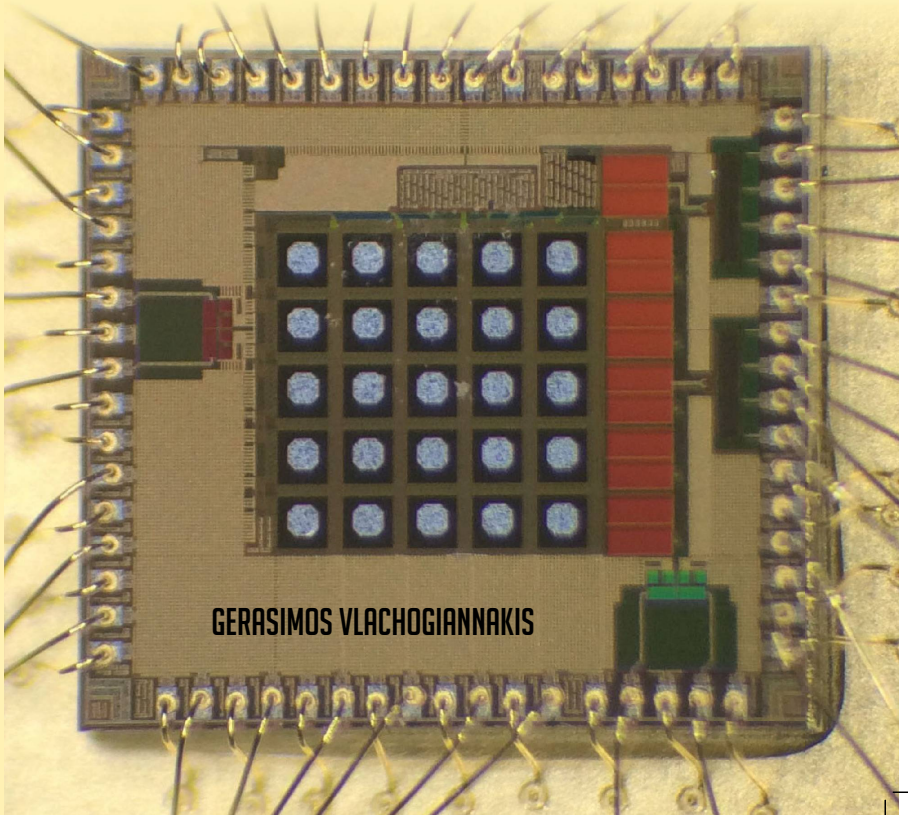

GERASIMOS VLACHOGIANNAKIS

Miniaturized CMOS Circuits and Measurement Techniques for Broadband Dielectric Spectroscopy

Miniaturized CMOS Circuits and Measurement Techniques for Broadband Dielectric Spectroscopy

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
by the authority of the Rector Magnificus Prof. dr. ir. T. H. J. J. van der Hagen,
chair of the Board for Doctorates
to be defended publicly on
Tuesday 11 January 2022 at 15:00 o'clock

by

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Keywords : Biomedical sensors, CMOS sensors, microwave sensors, bridge circuits, permittivity measurement, medical diagnostic imaging

An electronic version of this dissertation is available at
http://repository.tudelft.nl/.

To Pan.

I remember how frightened I was when, as a twelve-year-old child who'd never seen a fire, I was suddenly awakened by the very loud noise of a general fire alarm. The whole sky was ablaze and scorching hot; charred logs were flying through the air of our large provincial town; I shook feverishly. Fortunately I managed to get to the fire, taking advantage of the fact that everyone at home was in a state of great confusion. The fire was moving along the embankment.[...] The shore was piled with firewood and bast; young children my own age grabbed hold of these things and dragged them away from the burning houses. I took part too. What had become of my fear? I worked very diligently until we were told: "Enough! The danger's passed." From that time on I knew that if one is afraid of a large fire, then one must run toward it and work very hard; one will no longer be afraid. He who works has no time to be afraid or to feel revulsion or disgust.

Nikolai Chernyshevsky, 1828-1889, "What is to be done?"

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List of Abbreviations

ADC analog-to-digital converter. 37, 46, 47, 51, 53, 61, 93

AM amplitude-modulated. 35

BDS broadband dielectric spectroscopy. xi, 2–6, 8–10, 16, 18, 31, 40, 45, 46, 50, 59, 70, 73, 86, 92, 93

BEOL back end of line. 18, 78

CMOS complementary metal-oxide-semiconductor. xi, 4–6, 9, 10, 15, 17–19, 24, 31, 33, 40, 45, 46, 48, 57, 59, 73, 74, 78, 92, 93

CNC computer numberical control. 27, 30

DSB double-sideband. 35, 36

DUT device under-test. xii, 24–27, 40

FFT fast Fourier transform. 37, 50, 61

IC integrated circuit. 5, 31, 34, 83, 93

IF intermediate frequency. xiii, 45–47, 50, 52, 53, 61, 82, 93

IPN integrated phase noise. xii, 35, 36, 38–40, 52

LO local oscillator. xiii, 25–27, 46, 47, 51, 52, 60, 61, 66, 72

MoM metal-oxide-metal. 18

MUT material under-test. xi, 3, 5–9, 16–20, 47, 48, 57, 71

PCB printed circuit board. 60, 61

PLL phase-locked loop. 5, 94

PM phase-modulated. 35

SMM scanning microwave microscopy. xii, 22, 24, 28–30

SNR signal-to-noise ratio. 37

SoC system-on-chip. 53, 78

SSB single-sideband. 35, 36

TIA transimpedance amplifier. 51, 82

VNA vector network analyzer. xii, 3, 5, 6, 9, 10, 15, 17, 22, 23, 25–27, 64, 65

Summary

Abundant research reported in the literature has indicated that broadband dielectric spectroscopy (BDS), i.e., the measurement of material permittivity versus frequency, can serve a broad range of applications, including, but not limited to, biomedical, food, automotive, and agricultural industries. Adopting this technique in real-life application scenarios is directly dependent on the miniaturization of bulky measurement setups, currently in use for these (prototype) sensing systems. At the same time, a highly sensitive and precise permittivity readout is essential to distinguish between different materials or track variations in the material state composition. This work focuses on developing ultra-compact sensing elements, readout electronics, and measurement techniques to determine the localized complex permittivity with high accuracy, sensitivity, and spatial resolution at microwave operation frequencies.

Firstly, various sensing elements and high-resolution measurement setups are discussed for their compatibility with CMOS integration. Application scenarios are directed towards the characterization of low-loss materials, which often present much higher impedance than the currently 50-Ω oriented measurement setups. An I/Q-mixer-based interferometric technique is introduced to re-normalize the readout system reference impedance and improve the measurement sensitivity at high-impedance loads. Experimental results underline the potential of this technique. However, its compatibility with CMOS technology to enable small-factor systems is challenging at the intended frequencies of operation. Therefore, a double-balanced, RF-driven Wheatstone bridge with programmable branch impedance implemented in CMOS technology is proposed and analyzed for the high-resolution measurement of high-impedance loads (chapter 2).

Next, a high-sensitivity, ultra-compact BDS sensor system is introduced for localized permittivity sensing. As a sensing element, it utilizes a metal patch that performs the actual sensing by presenting permittivity-dependent admittance. This patch is best implemented on the top metallization layer of a CMOS technology such that it can directly interface with the material-under-test (MUT). High measurement sensitivity is achieved by embedding the patch in a double-balanced, RF-driven Wheatstone bridge followed by a frequency down-converting mixer. By driving the bridge with a square wave, permittivity information can be acquired at the fundamental and subsequent harmonics. This concept allows increasing the measurement speed and, at the same time, provides an extended measurement frequency range (chapter 3).

The measurement of the complex permittivity of materials is enabled by developing a dedicated calibration procedure for the patch-based BDS sensor. Measurement results of known liquids show good agreement with theoretical values in the

literature, and the relative permittivity resolution in these measurements is better than 0.3 over a 0.1–10 GHz range. The proposed sensor implementation features a measurement speed of 1 ms and occupies an active area of only 0.15×0.3 mm^2, enabling the realization of very compact sensor arrays that can facilitate (real-time) 2-D dielectric imaging of permittivity contrast (chapter 4).

Such a real-time BDS sensor array has been implemented as a 5x5 array, illustrating the scalability of the proposed patch-based BDS concept. This matrix has been demonstrated for its functionality by resolving spatial permittivity variations in the sub-mm range (chapter 5).

Last, the findings and conclusions of this dissertation, and recommendations for future work, are discussed (chapter 6).

Samenvatting

Verschillende onderzoeken in de literatuur hebben aangetoond dat breedband diëlektrische spectroscopie (BDS), d.w.z. de meting van materiaal permittiviteit versus frequentie, een breed scala aan toepassingen kan dienen, waaronder applicaties in de biomedische-, voedsel-, auto- en landbouwindustrie. De toepasbaarheid van deze techniek in (echte) gebruikersapplicaties is sterk afhankelijk van de miniaturisering van de nu nog zeer omvangrijke meetopstellingen die gebruikt worden in (prototype) detectiesystemen. Tegelijkertijd is een zeer gevoelige en nauwkeurige uitlezing van de permittiviteit vereist om goed onderscheid te kunnen maken tussen verschillende materialen of variaties in materiaal compositie. Dit proefschrift richt zich op de ontwikkeling van ultra-compacte sensoren, uitleeselektronica en meettechnieken die, d.m.v. microgolffrequenties, de karakterisatie van een materiaal voor zijn lokale complexe permittiviteit met hoge nauwkeurigheid, gevoeligheid en ruimtelijke resolutie mogelijk maken. Allereerst worden hoge resolutie detectie-elementen met hun meetopstellingen besproken m.b.t. hun geschiktheid voor CMOS-integratie. De beoogde toepassingsscenario's zijn gericht op de meting van objecten, die een zeer hoge impedantie (»50 ohm) aanbieden aan de doorgaans 50-Ω georiënteerde meetopstellingen. Dit leidt tot onnauwkeurigheden in de meetresultaten. Om dit te verhelpen wordt een op een I/Q-mixer gebaseerde interferometrische techniek geïntroduceerd die het mogelijk maakt om de referentie-impedantie van het uitleessysteem opnieuw te normaliseren. Hiermee wordt de meetgevoeligheid voor belastingen met een hoge impedantie sterk verbeterd. Meetexperimenten onderstrepen het potentieel van deze techniek. Echter de toepassing van deze techniek in CMOS-technologie, met het doel om systemen met zeer kleine afmetingen mogelijk te maken, is een uitdaging bij de beoogde meetfrequenties. Om dit probleem op te lossen wordt een dubbel gebalanceerde, RF-Wheatstone-brug met een programmeerbare takimpedantie geïntroduceerd, geanalyseerd en geïmplementeerd in CMOS-technologie (hoofdstuk 2). Vervolgens wordt een zeer gevoelig, ultracompact BDS-sensorsysteem geïntroduceerd welke geschikt is voor de detectie van de lokale diëlektrische constante over een (materiaal) oppervlak. Het detectie-element maakt gebruik van een metalen patch die een permittiviteit afhankelijke admittantie presenteert tussen zijn aansluitklemmen. Deze patch kan het best worden geïmplementeerd op de bovenste metallisatie laag van een CMOS-technologie, zodat een optimale koppeling met het te testen materiaal (MUT) bereikt kan worden. Een hoge meetgevoeligheid wordt gerealiseerd door de patch op te nemen in een dubbel gebalanceerde, RF-aangestuurde Wheatstonebrug, gevolgd door een frequentie-omlaag-converterende mixer. Door de brug met een blokgolf aan te sturen, kan de permittiviteit informatie worden verkregen op zowel de fundamentele als de daaropvolgende harmonische frequenties. Dit concept

verhoogt de meetsnelheid en het frequentiebereik (hoofdstuk 3). De meting van de complexe permittiviteit van materialen wordt mede mogelijk gemaakt door de ontwikkeling van een speciale kalibratieprocedure voor de patch-gebaseerde BDS-sensor. Meetresultaten met bekende vloeistoffen laten een goede overeenkomst zien met de theoretische waarden in de literatuur. De relatieve permittiviteit resolutie, in deze metingen, is beter dan 0,3 over een bereik van 0,1-10 GHz. De voorgestelde sensor implementatie heeft een meettijd van 1 ms en beslaat een chip oppervlakte van slechts 0,15×0,3 mm2, wat de realisatie van zeer compacte sensorarrays mogelijk maakt die "realtime" een 2-D permittiviteit contrast van een meetobject kunnen weergeven (hoofdstuk 4). Zo'n "realtime" BDS-sensorarray is geïmplementeerd als een 5x5-array, welke de schaalbaarheid van het voorgestelde patch gebaseerde BDS-concept naar grotere systemen illustreert. De functionaliteit van deze matrixsensor is gedemonstreerd door permittiviteitsvariaties op sub-mm niveau weer te geven (hoofdstuk 5). De bevindingen, conclusies en aanbevelingen voor toekomstig werk, van dit proefschrift worden besproken in hoofdstuk 6.

1

Introduction

1

1.1. Broadband dielectric spectroscopy

Broadband dielectric spectroscopy (BDS) has been identified as a valuable, non-destructive, label-free diagnostic tool for the characterization of a wide range of materials of either biomedical or industrial interest. The technique's applicability derives from the fact that each material, or a combination thereof, exhibits a unique frequency-specific dielectric response, often referred to as dielectric signature.

In the biomedical sector, many potential applications are being identified, ranging from traditional clinical and point-of-care scenarios to the emerging area of wearables. Examples include blood glucose monitoring [1] and *ex-vivo* or *in-vivo* cancer detection and assessment [2]. The latter application is motivated by measurements on bulk animal and human tissue, suggesting that the permittivity of cancer tissue can vary by up to 20% compared to healthy tissue [3, 4]. These studies – albeit conducted for cancer detection investigations – have also shown that skin hydration variations can provide measurable permittivity changes, which can be utilized as a valuable tool for hydration monitoring in the context of wearable devices – a fast-developing market.

In agriculture, the complex permittivity of fruits and vegetables is correlated to changes in temperature, water, and inorganic material content, rendering BDS a candidate for identifying faulty or stale products [5–7]. Meantime, in the automotive industry, BDS is the preferred method for oil and fuel quality inspection [8, 9].

1.2. Material permittivity

The permittivity of a dielectric material, expressed as $\epsilon^\star = \epsilon' - j\epsilon''$, is a complex-valued parameter that quantifies the degree of its polarization, i.e., the electric displacement resulting from an applied electric field. Its two components, the real part ϵ' and the imaginary part ϵ'', are indicative of the material ability to store the energy of the applied electric field (capacitive behavior) or dissipate it in the form of heat (resistive behavior), respectively [10].

Molecular and atomic phenomena manifest themselves macroscopically as inertia to abrupt field alterations and, as a result, permittivity exhibits a characteristic behavior versus frequency. Such effects referred to as relaxations or dispersions, cause abrupt permittivity variations as frequency increases. Because the molecular composition of each material is unique, so is the behavior of its permittivity versus electric field excitation frequency. It can constitute an identifier of the material and its environmental parameters, e.g., temperature and pressure.

A generic empirical model to describe the permittivity behavior versus frequency of any dielectric material containing a single relaxation is given by the Cole-Cole equation [11]:

$$\epsilon^\star(\omega) = \epsilon'(\omega) - j\epsilon''(\omega) = \epsilon_\infty + \frac{\epsilon_\infty - \epsilon_0}{1 + (j\omega\tau)^{1-\alpha}}, \tag{1.1}$$

where ω is the angular frequency of the field, ϵ_0 is the permittivity at zero frequency ($\omega = 0$), ϵ_∞ is the permittivity at an infinite frequency ($\omega \to \infty$), τ the

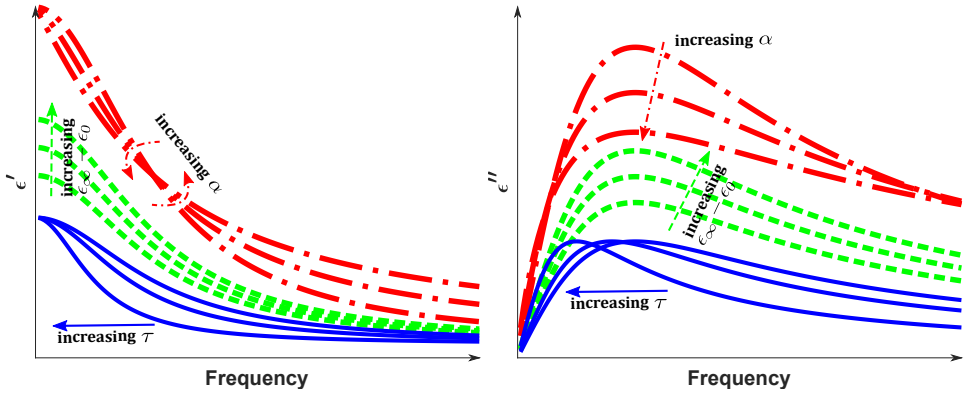

Figure 1.1: Illustrative plots of typical ϵ' and ϵ'' variation versus frequency, according to the Cole-Cole equation (1.1). It shows how individual Cole-Cole model parameters affect ϵ' and ϵ'' when all other parameters of the model are kept constant.

material-specific relaxation time parameter, and $0 \leq \alpha < 1$, a distribution parameter, which acts as a measure of the dispersion broadening, i.e., how abrupt the permittivity variation appears versus frequency. Illustrative plots of the real and the imaginary part of permittivity and how the Cole-Cole model parameters affect them are shown in Fig. 1.1. It is also known that ϵ' and ϵ'' are conjugate functions, and knowledge of each of the two can lead to the calculation of the other by using the Kramers-Kronig formulas [11, 12].

In homogenous polar materials, the parameter α of the Cole-Cole model is zero, in which case the model is also called a Debye model [13]. Fig 1.2 shows the permittivity of such well-known materials at room temperature. On the contrary, complex, non-uniform, or stratified materials can exhibit more than one relaxation and need to be modeled as a sum of Cole-Cole equations. A typical example of multi-relaxation materials is biological tissue [14]. Fig. 1.2 shows the permittivity versus frequency of a few well-characterized liquid materials extracted from their Debye model [15]. Well-characterized materials, such as those presented in fig. 1.2, are typically used as reference when evaluating the functionality and accuracy of permittivity sensors.

1.3. Miniaturization of permittivity sensors

Despite the promising potential of BDS, conventional microwave permittivity measurement techniques presented in the literature employ very costly and bulky equipment. More specifically, a coaxial probe or cavity sensor is interfaced to the material under-test (MUT) and connected to a vector network analyzer (VNA) that measures the overall reflection coefficient (Γ). The reflection coefficient is then translated to permittivity using various methods, including calibration, electromagnetic simulation, and analytical electromagnetic modeling [16, 17]. In general, these laboratory setups are not applicable in most practical application scenarios, such as outdoor,

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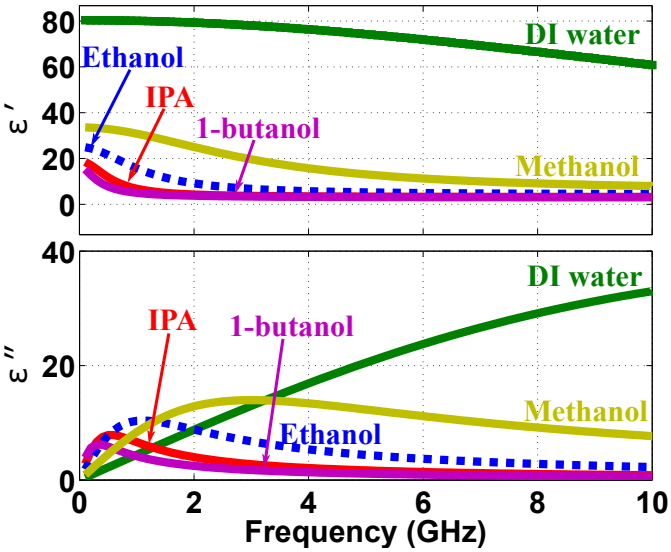


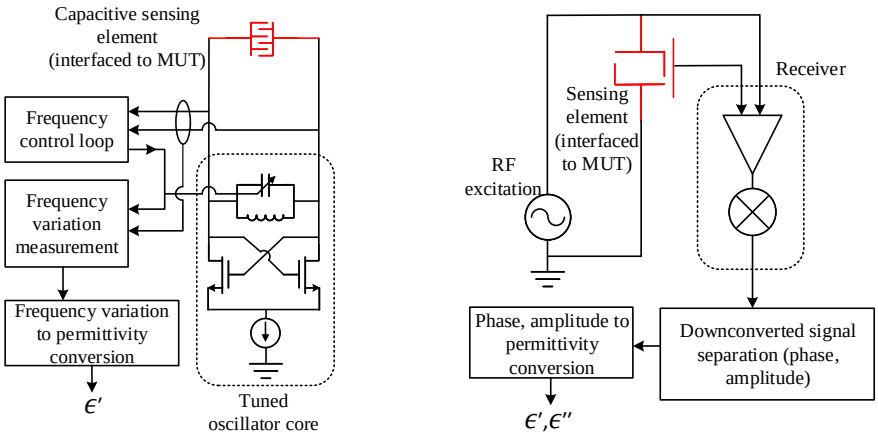
Figure 1.2: The real and imaginary part of permittivity of the materials measured, versus frequency, generated from their Debye models [15]. Ethanol (dashed line) is often used for sensor system validation as independent reference material.

remote-location measurements and point-of-care medical testing. Moreover, their high cost hinders broader adoption of these technologies, regardless of their potential benefits.

Broader adoption of permittivity sensors in biomedical, industrial, and agricultural settings can be facilitated by the large-volume production of miniaturized, low-cost, and, at the same time, precise and accurate permittivity sensors. Portability, multi-sensor integration, and high energy efficiency are essential requirements in the wearable market. At the same time, a small sensing area is significant to achieve high spatial resolution in imaging for intra-operative assisting technology. Moreover, a sensor detection range up to a few GHz will provide field penetration advantages and broadband measurement data to more accurately extract material characteristics, ultimately providing increased specificity and sensitivity of the diagnostic tools.

All the above requirements are achievable by utilizing the widespread sub-μm complementary metal-oxide-semiconductor (CMOS) technology, which offers the ultimate form-factor reduction in electronic systems and is used in the vast majority of present-day consumer electronics. CMOS advantages include multi-sensor integration, signal conditioning, and digital processing circuits on a single chip. Additionally, advanced CMOS technology nodes employ sub-μm feature sizes that can provide a functional operation up to a few GHz, to address the needs of broadband applications.

The advantages of CMOS technology in leveraging the potential of BDS have led to an abundance of fully or partially integrated CMOS systems in the literature.



(a) (b)

Figure 1.3: Categorization of CMOS integrated BDS system architectures : (a) PLL-based architecture and (b) receiver-based architecture.

These implementations can be categorized into two architectures, shown in Fig. 1.3, namely PLL-based and receiver-based.

A PLL-based dielectric spectroscopy architecture (Fig. 1.3a) [18–21] comprises a controlled LC tuned oscillator incorporated into a phase-locked loop (PLL), to control the oscillation frequency. A two-terminal capacitive sensing element is connected parallel to the LC tank and interfaced to the MUT, thus changing the effective capacitance of the sensing element and, in turn, shifting the tank tuning frequency. This effect can be captured and quantified by measuring the shift of an internal PLL control signal (e.g., the oscillator varactor control voltage), which automatically occurs in the closed-loop system so that the oscillation frequency of the oscillator is maintained. PLL-based implementations have demonstrated accurate permittivity readout, yet have two main intrinsic disadvantages: embedding of the sensing element in an LC-tuned structure typically leads to a narrow-band system, i.e., limited material characterization frequency range. Moreover, only the capacitive shift is monitored, leading to extraction of ϵ' only. Although, as mentioned, ϵ' and ϵ'' can be extracted from one another, this method will lead to increased error and noise propagation in the calculation of parameters, compared to directly measuring both. Nevertheless, a PLL-based architecture for both ϵ' and ϵ' has been demonstrated [20]. It employs an extra amplitude locking loop (ALL) which also tracks the oscillation amplitude shift caused by the variation of the quality factor of the sensing element due to ϵ'', which comes at the cost of extra complexity, integrated circuit (IC) area and power consumption.

The receiver-based architecture [22–25] mimics traditional VNA setups: an RF

source is exciting the sensing element, and the element response is downconverted using a receiver chain. Note that the receiver architecture can be either homodyne or heterodyne. As long as both the excitation and sensor element response signals are monitored, the phase and amplitude variation of the response compared to the excitation can be measured, analogous to a reflection coefficient measurement using a VNA setup. The main disadvantage of the receiver-based architecture is that it requires the (extra) generation of an RF signal, i.e., it is not a self-sustained system as the PLL-based architecture. Its main advantage is that it can directly provide both ϵ' and ϵ''. Moreover, it can offer a more broadband readout.

CMOS BDS system implementations have demonstrated the benefits of miniaturization by achieving a total die area in the order of a few mm^2. This level of miniaturization is quite impressive when compared to VNA-based lab setups. Some implementations still utilize external (off-chip) sensing elements, which is acceptable in applications requiring bulk-level measurements. Nevertheless, it is interesting to explore the possibility of miniaturizing such sensors further down to a sub-mm^2 area while including both sensing element and sensor readout electronics. These implementations will facilitate new applications that deviate from the bulk-level measurement regime, such as the unexplored area of 2-D sensor arrays for permittivity contrast measurement and visualization at microwave frequencies. Permittivity imaging functionality can be helpful in a variety of applications such as label-free, in-vivo cancer visualization as an assisting tool in removal surgery [26], food and flower quality inspection for early detection of storage disorders (e.g., browning, skin spots, etc.), evaluation of drug penetration through the skin, non-destructive film coating testing in industrial applications. At the same time, deeper miniaturization will accelerate the co-integration of BDS technology into multi-sensor systems such as wearables (e.g., activity trackers).

A differentiation should be made at this point between microwave permittivity sensors and low-frequency permittivity/impedance sensors, operating below 100 MHz. For the latter, arrayed implementations have already been implemented successfully [27, 28]. Nevertheless, motivation to move towards microwave frequency implementations (hence satisfy the term *broadband*) still exists for two main reasons:

(i) to achieve better spatial resolution in the detection of permittivity discontinuities in the MUT, and

(ii) to employ the redundancy of acquiring a frequency-dependent permittivity dataset, which provides better measurement precision [29]. Measurement precision is essential in biomedical applications as it is directly linked to increased sensitivity and specificity of diagnostic tests [30].

An additional requirement of the ultra-miniaturized, sub-mm-area sensing systems is a fast read-out with acceptable precision. These are essential properties in fast scanning imaging systems or energy-efficient battery-operated BDS devices (e.g., wearables). Previous implementations employ little or no optimization on the readout speed, resulting in potentially long measurement times or short battery life.

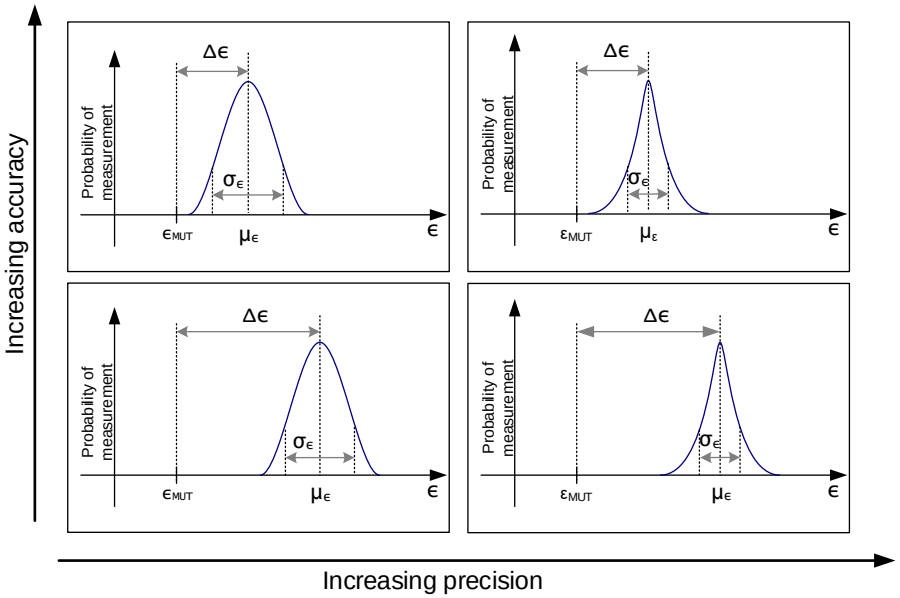


Figure 1.4: Examples demonstrating the difference between accuracy and precision: in a high accuracy system, the mean measured value is close to the actual MUT value, while a high precision system features a low variance of repeated measurements.

1.4. Sensor performance metrics

Several different performance metrics related to the permittivity sensors are mentioned in this work. This section intends to provide a clear definition for each of the individual terms and discuss their importance and how they are linked to each other.

Accuracy of the permittivity measurement is defined as the difference of the mean measured value from the *actual* permittivity of the MUT. The accuracy is of the highest interest in metrology applications. It relies upon accurate modeling of the sensing element, calibration techniques, exact knowledge of the permittivity of the calibration materials, and the measured material permittivity at the specific measurement conditions.

Precision is defined as the variance of a repeated set of measurements. It is a metric of sensor consistency, and it is not necessarily linked to its accuracy. Fig. 1.4 graphically demonstrates the difference between accuracy and precision in a material with permittivity ϵ_{MUT}. We assume that multiple measurements of the same MUT are taken and that the measured values follow a normal distribution due to the random nature of the measurement noise at the output. If σ_ϵ and $\mu\epsilon$ are the standard deviation and mean value of the measurement value probability density function, respectively, we can define accuracy as

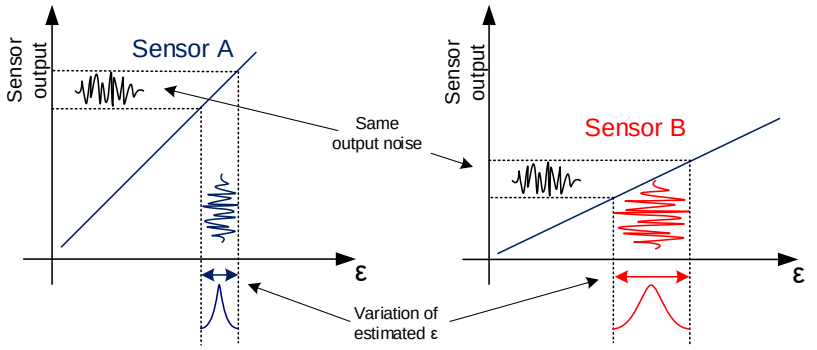


Figure 1.5: Effect of sensor sensitivity on permittivity measurement. In the example of two sensors, A and B, with the same amount of readout noise, sensor B will translate to a higher permittivity variation than sensor A because it has lower sensitivity. Therefore, the precision of sensor B is lower than that of sensor A.

$$|\Delta\epsilon| = |\mu_\epsilon - \epsilon_{MUT}|, \tag{1.2}$$

and precision simply as the standard deviation of the measurements, σ_ϵ.

It is evident that a system with low accuracy, i.e., a considerable distance of the mean measured value from the actual permittivity, can be very precise, i.e., the distribution of multiple measurements can have a very low variance. The higher the system precision, the bigger the minimum detectable permittivity difference. Moreover, high precision implies reduced measurement time because there is no need for high averaging. These features are desirable in practical applications, where permittivity differences are small and the available measurement time is restricted, e.g., in imaging systems or BDS systems targeting a low energy consumption.

Similarly, a system with high accuracy can have a low precision, which means that averaging a large number of measurements is required to ensure accurate permittivity estimation or differentiation between relatively close permittivity values. As such, measurement time will be increased. The precision is typically determined by the level of noise generated in the sensing system and its sensitivity.

Sensitivity of the sensor is the local derivative of the permittivity-to-output system transfer function. It is important because a certain amount of noise in the measured output quantity is translated to large noise in estimating the permittivity. This effect is depicted in fig. 1.5, where a linear transfer function is assumed for simplicity.

Spatial resolution refers to the minimum achievable area coverage of the sensor when interfaced to a MUT and is mainly correlated with the sensor size and geometry. Achieving high spatial resolution, i.e., minimal area coverage per single sensor is critical in imaging applications.

In the context of this work, albeit high accuracy is pursued, it is acknowledged

that there is often reduced control in achieving or even evaluating (good) system accuracy. This is mainly due to the lack of suitable, well-defined calibration standards at the specific measurement conditions. Moreover, in practice, there is often little control over the measurement conditions themselves in terms of temperature, humidity, etc. In this dissertation, the research focus is on improving two performance evaluators, which are deemed most important for practical upcoming BDS applications, namely:

- precision, achieved via maximization of system sensitivity,
- spatial resolution, achieved via minimization of the sensor area.

1.5. Thesis objectives

The objective of this thesis is to make the following original scientific contributions:

- To propose and demonstrate a measurement precision improvement for high impedance measurements using conventional VNA measurement technique (chapter 2)

For this purpose, this thesis investigates on an impedance renormalization concept to improve the system sensitivity in high-impedance measurement environments, enabling faster and more precise measurements. The developed technique applies to BDS setups comprising a traditional VNA instrument with 50 or 75 Ω reference impedance.

- To propose and demonstrate a CMOS-compatible, miniaturized reconfigurable RF Wheatstone bridge for high-precision sensing element readout, suitable for BDS (chapter 2)

We introduce a reconfigurable double-balanced RF Wheatstone bridge that provides a fully differential readout of a single-ended patch sensing element to fulfill this goal. By making the bridge reconfigurable, its impedance level can be dynamically adjusted to the ones of the MUT, yielding an improved sensitivity. This structure is fully compatible with CMOS technology and occupies minimal chip area. As such, it complies with the goal of extreme miniaturization and the ability to integrate it into a sensor array.

- To demonstrate the implementation and operation of a miniaturized, CMOS permittivity sensing pixel architecture that offers multi-frequency functionality with precise and fast readout. (chapters 3 and 4)

For this purpose, the implementation, operation, and measurement results of a CMOS permittivity sensing pixel are presented in this thesis. The sub-mm^2 area occupied by this implementation is one order of magnitude smaller than previous realizations reported in the literature. Meanwhile, it achieves comparable measurement accuracy and high energy efficiency, owing to the introduced novel high-precision

RF Wheatstone bridge concept. Moreover, the applied multi-harmonic downconversion scheme improves the measurement speed and provides new opportunities to realize energy savings. Its small area and excellent scalability position the presented architecture as an exciting candidate to implement BDS sensing pixels for permittivity imaging arrays at microwave frequencies.

- To demonstrate the implementation and operation of the first BDS imaging array to operate at microwave frequencies. (chapter 5)

A 5x5 array that uses the proposed sensor architecture and components of the preceding chapters is now demonstrated. Its implementation is the first-ever BDS sensing array to be realized. Its functionality is shown through a 2D permittivity contrast measurement of two liquids with different dielectric constants.

1.6. Thesis outline

The thesis is organized as follows:

- **Chapter 2** Discusses various permittivity sensing elements and compares differential capacitive sensing structures with single-ended ones regarding their suitability to be applied in permittivity imaging arrays. Then, it proposes and demonstrates improvements for measuring high impedance loads in conventional VNA measurement setups and within a CMOS, chip environment to acquire improved precision within a given measurement time.
- **Chapter 3** proposes an ultra-miniature CMOS permittivity sensing pixel architecture offering multi-frequency, precise and fast readout. It builds upon the introduced CMOS-compatible RF Wheatstone bridge to realize a scalable and flexible sensor readout path, suitable for integrating into imaging arrays and multiple sensor systems.
- **Chapter 4** describes the implementation and measurement results of a 40-nm CMOS compact BDS pixel for localized material characterization at microwave frequencies. This chapter elaborates on both the design procedure of the sensor as well as the calibration procedure required to convert raw measurement data into permittivity.
- **Chapter 5** describes the implementation and measurement results of a 5$\times$5 permittivity sensor array in 0.14-μm CMOS technology.
- **Chapter 6** concludes and makes recommendations for future work

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2

High-Precision Permittivity Measurement Setups

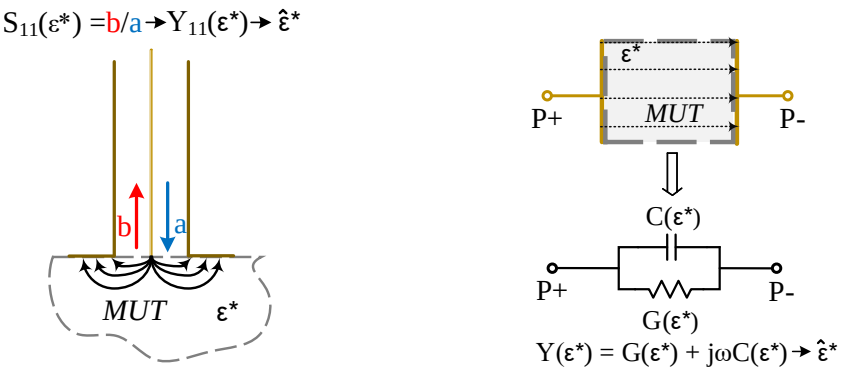
This chapter provides an in-depth description of two dielectric measurement approaches to achieve a high-precision readout. First, we discuss a critical component of a permittivity measurement setup, namely, the sensing element. Various sensing elements utilized in traditional measurement setups are presented. Their advantages, disadvantages, and suitability for miniaturization and, eventually, integration in CMOS technology are discussed. From this evaluation, a patch sensing element is favored for optimally translating permittivity to admittance. Next, we introduce an I/Q interferometric technique for impedance renormalization in a modified traditional VNA-based measurement setup. This technique aims at improving the measurement sensitivity at high-impedance loads, such as small capacitance values encountered in scanning microwave microscopy (SMM) and broadband dielectric spectroscopy (BDS). A demonstrator is developed, and the related experiments exhibit high dynamic range and resolution images, exhibiting a reduction in capacitance measurement noise of 50%, compared to the conventional approach. Last, a high-precision permittivity readout system is proposed based on a compact, double-balanced, fully-differential modification of the Wheatstone bridge, co-integrated with the patch sensing element. The proposed bridge provides a robust and stable readout in CMOS technology. By introducing re-configurable branch capacitance, the bridge impedance level can be renormalized. This concept facilitates improved measurement sensitivity for a wide range of MUT permittivity. Furthermore, its compact dimensions enable integration in BDS matrix-oriented systems.

2.1. Introduction

Given the BDS application scenarios introduced in chapter 1, this chapter addresses the need for high-precision permittivity measurements in the context of a miniaturized BDS measurement setup. As discussed in section 1.4, high-precision is seen as the primary facilitator of fast measurement speed and, as a result, system power reduction, since a smaller number of measurements need to be acquired to distinguish between different materials (permittivity values). Moreover, increased precision will lead to improved permittivity contrast detection capability for a given measurement time.

Following a discussion on permittivity sensing elements and their suitability for different applications, this chapter will propose two sensing element readout techniques to improve precision. Both methods focus on re-normalizing the impedance of the corresponding measurement instrument, i.e., the VNA and the Wheatstone bridge, to a value comparable to the impedance of the sensing element. In both cases, this improves the readout quantity's sensitivity to noise sources, as will be shown in the following sections.

2.2. Permittivity sensing elements



(a) (b)

Figure 2.1: Commonly used broadband permittivity sensing elements : (a) Coaxial probe and (b) parallel-plate capacitance.

Independent of its geometry and its specific characteristics, the sensing element of a permittivity measurement system' is used as a transducer of the complex permittivity of the MUT ($\epsilon^* = \epsilon' - j\epsilon''$) to an admittance, which can be modeled as a parallel combination of lumped conductance (G) and capacitance (C):

$$Y_s(\epsilon^*, \omega) = G(\epsilon', \epsilon'', \omega) + j\omega C(\epsilon', \epsilon'', \omega) \tag{2.1}$$

Table 2.1: Summary of sensing elements used in bulk measurement setups

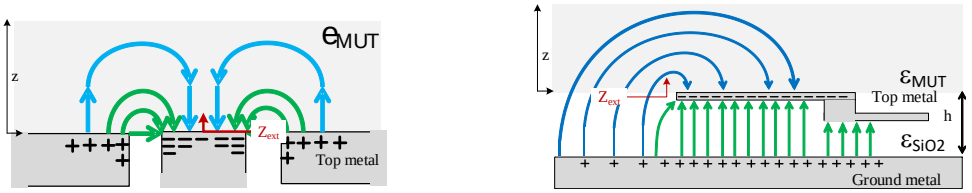
Element	Non-destructive	Broadband	Contact w/ material
Coaxial probe	Y	Y	Y
Parallel plate	N	Y	Y
Transmission line	N	Y	Y
Resonant cavity	N	N	Y
Antenna	Y	Y	N

The mapping between the element admittance Y_s and the actual permittivity of the MUT can be provided through electromagnetic simulations, analytical formulas, or a combination thereof. In principle, the real and imaginary parts of permittivity to be measured translate to a capacitance and conductance value, respectively. However, a cross-correlation typically still exists due to the element geometry and its self-conductance and capacitance.

Depending on the application requirements, variants of a sensing element can be grouped into five main categories, all of them based on the principle of translating permittivity into a measurable admittance [1], and each exhibiting its own advantages and disadvantages, as summarized in table 2.1.

Coaxial probes are the most commonly used sensing elements in material permittivity characterization. As shown in Fig. 2.1a, a coaxial probe is contacted with a MUT, and the reflection coefficient S_{11} is measured by a VNA. The reflection coefficient is eventually translated into material admittance Y_{11} and linked to the MUT complex permittivity. Interfacing a coaxial probe with a material is very convenient. It only requires access to the material surface and does not impose problematic MUT size and shape limitations. Coaxial probes can also be made very broadband, and the presented admittance-to-permittivity behavior has been rigorously analyzed [2, 3]. Due to these advantages, they have been used to acquire most of the broadband permittivity measurements available in the literature for a wide range of materials, such as in-vivo and in-vitro biological materials, solid, semi-solid, liquid biological and chemical materials [4–9].

Parallel plate elements, illustrated in Fig. 2.1b, consist of two parallel plates (electrical terminals P+ and P-) filled with the MUT. For a given geometry, an accurate permittivity-to-admittance formula can be calculated. Consequently, the permittivity can be estimated by measuring the admittance between terminals P+ and P-, through either a VNA or other techniques. Still, its conventional three-dimensional structure demands precise machining of the material sample before being physically placed between the plates. Nevertheless, with an admittance that depends on the MUT permittivity, this capacitor-based concept can be applied within an integrated circuit when adequately adjusted towards a two-dimensional geometry. Moreover, such a structure can be scaled to arbitrarily small sizes, making it appealing to CMOS implementations. Additionally, a parallel-plate sensing element can be made broadband if its self-resonance frequency, i.e., the frequency at which the capacitance is nulled by the series parasitic inductance, is pushed at a high frequency. This is typically the case in an IC environment, where device footprints



(a) (b)

Figure 2.2: Cross-sections and pictorial representation of field lines and charge distribution for two CMOS-compatible sensing element implementations : (a) Differential sensing element and (b) single-ended patch.

are miniaturized.

Transmission line-sensing elements are based on the principle that a change in the dielectric permittivity between the signal and ground of a transmission line alters its characteristic impedance Z_0 and phase velocity. Thus, for given line termination, the change in the reflection coefficient can be measured. Consequently, the related admittance and permittivity of the dielectric can be calculated. Transmission lines feature the same advantages and disadvantages as the parallel-plate capacitor sensing elements. However, since their dimensions need to be comparable to the signal wavelengths involved, their miniaturization prospects are limited for use at the frequency ranges of interest in BDS. Nevertheless, a fully integrated CMOS transmission-line-based sensing element has been demonstrated in a BDS sensor for liquids [10].

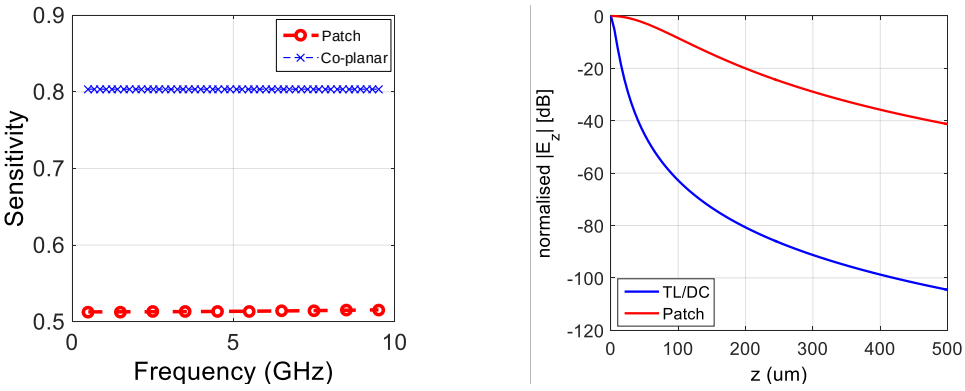
Resonant cavity sensing elements are fixtures that present a varying resonance frequency depending on the material placed inside them. The resonance frequency and quality factor are extracted from the measured impedance, which indicates the MUT permittivity. This method is very narrowband; therefore, it cannot be considered for broadband dielectric spectroscopy.

Lastly, *antennas* are a unique type of permittivity sensing element. They are used in contactless applications to measure the far-field signal in a two-antenna setup intervened by the MUT. This technique is sometimes used when there are additional constraints on the temperature of the MUT [1]. Note that the lowest meaningful measurement frequency in this far-field setup is limited by the distance of the MUT to the antennas. Therefore, this technique is not considered in the scope of this work.

2.2.1. CMOS-compatible sensing elements

Contrary to a fully custom three-dimensional sensing element, a CMOS compatible element comes with a specific set of restrictions related to its fabrication method. As described in the previous section, parallel-plate capacitors can be modified to a planar configuration to implement CMOS compatible permittivity sensing elements.

Two different sensing element styles can be considered: a co-planar structure, either in the form of a transmission line (TL) or a co-planar metal-oxide-metal (MoM)



(a) (b)

Figure 2.3: Comparison of (a) element sensitivity and (b) magnitude of the normal component of the electric field, normalized to the field intensity at the element–MUT interface between the patch and co-planar capacitive elements.

differential capacitor (DC), shown in Fig. 2.2a, or a patch element, sketched in Fig. 2.2b. To accommodate a good interface with the MUT, the sensing element is implemented on the top layer of the CMOS metal stack, called back end of line (BEOL). Additionally, a passivation layer opening is required for direct contact with the MUT, a typical process in CMOS fabrication used for bond pad generation.

Previously presented CMOS permittivity sensors typically employ differential capacitive sensing elements, similar to the one depicted in Fig. 2.2a, implemented on the top metal of the CMOS metal stack with passivation opening for direct contact to the MUT [11–15]. These element types provide convenient access to both terminals and are directly compatible with fully differential read-out chains. Additionally, they can achieve a high sensitivity on permittivity variations. We can define the sensitivity of a permittivity sensing element as a relative impedance variation at the sensor–MUT interface Z_{ext} in the presence of MUT versus a reference material ϵ_{ref} (in this case, air):

$$S = \left[\frac{Z_{ext}(\epsilon_{ref}) - Z_{ext}(\epsilon_{MUT})}{Z_{ext}(\epsilon_{ref}) + Z_{ext}(\epsilon_{MUT})} \right]. \tag{2.2}$$

A comparison of element sensitivity for two structures of the same footprint (100×100 μm) is given in Fig 2.3b. It shows that the co-planar implementation is 60% more sensitive to MUT permittivity variations.

However, this sensitivity definition refers to the element surface, and no information on the element's penetration depth capabilities is provided whatsoever. Shown in Fig 2.3b is the intensity of the normal electric field component, which is perpendicular to the element surface, normalized in amplitude to the maximum field intensity (present at the interface $z = 0$). For a patch sensor, a persistence of the field deeper in the MUT is demonstrated compared to the co-planar sensor due to the large distance of the negative/ground plane from the sensor aperture.

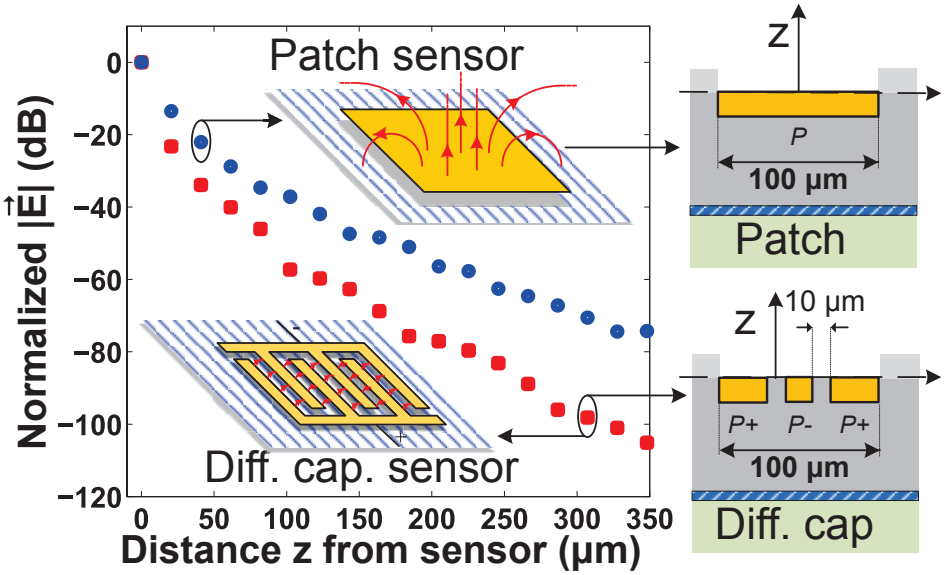
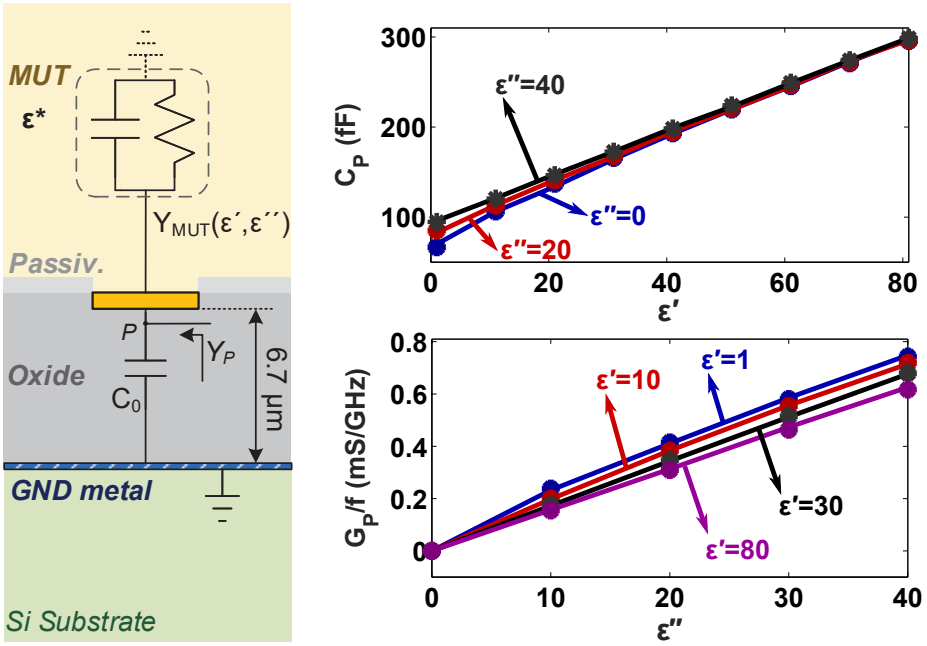


Figure 2.4: EM simulation of normalized electric field magnitude versus vertical distance from the sensor interface for two types of sensors both occupying the same 100×100 μm^2 area: a single-ended patch and a differential capacitor with 10 μm between fingers.

The electric field distribution of a patch has also been compared to a multi-finger capacitor structure. EM simulations were carried out to determine the electric field as a function of vertical distance from the element surface, using a commercial 3D EM simulation tool (Keysight EMPro). The two simulated sensors occupy an area of 100×100 μm^2, and a distance of 10 μm between the fingers was chosen for the differential sensor. A typical 40-nm CMOS metal stack was considered, and the EM simulation was carried out at 1 GHz for the worst-case scenario where the sensing element is interfaced to air ($\epsilon^\star = 1 - j0$). As seen in the simulation results of Fig. 2.4, a much steeper decay of the electric field is evident in the case of the differential sensing element. At a distance of 300 μm, the electric field magnitude is approximately 100 dB lower than the maximum strength, whereas for the patch, this reduction is in the order of 70 dB, a difference of 30 dB.

Therefore, a patch sensing element is less sensitive to potential air gaps since a smaller portion of the field is concentrated at the interface. This characteristic tolerance of the patch sensor to different MUT depths is helpful in measurement environments where air gaps might be present or permittivity differences at larger depths need to be resolved. This property is desired in solid or semi-rigid material measurements (e.g., biological tissue) in applications where a permittivity contrast measurement deeper in the MUT is targeted. Another example where a patch is preferable is a multi-sensor array setup for spatial permittivity contrast evaluation. Although the patch sensing element is expected to provide worse isolation

to neighboring pixels, it is not inherently bound to differential sensing. This allows the potential use of more advanced driving schemes where multiple patches operate together to inspect a sample. Examples of such approaches are a) the use of multi-phase patch excitation, in which selective differential sensing between different elements is applied, and b) bootstrapping of neighboring pixels, i.e., driving the patches in-phase to cancel capacitive cross-coupling [16]. Based on the above, the patch sensing element is proposed and favored in this work.



(a) (b)

Figure 2.5: (a) Cross-section of utilized patch sensing element and (b) equivalent patch capacitance and conductance from EM simulations (solid lines) and RFM model (dots) for various values of ϵ' and ϵ'' at f = 1 GHz.

Fig. 2.5a shows the cross-section of a square patch implemented on the top metal of a generic CMOS metalization stack. When the patch is in contact with air, the patch node P is loaded by the parallel-plate capacitance C_0, formed between the top metal and the ground plane. When interfaced with a MUT, the load will change depending on the MUT complex permittivity. Since permittivity relates to electric energy storage and loss (ϵ' and ϵ'' respectively), the sensing element is expected to represent a lossy capacitor of which the reactive and resistive behavior will strongly depend on the real and imaginary part of the MUT permittivity, respectively. Hence, the admittance Y_P at the patch node can be expressed as a parallel combination of a material-dependent admittance $Y_{MUT} \approx G_{MUT}(\epsilon'') + j\omega C_{MUT}(\epsilon')$ and the baseline admittance $Y_0 = j\omega C_0$, yielding $Y_P = Y_0 + Y_{MUT}$.

Table 2.2: Parameters of the linear ϵ-to-Y model

Parameter	Value
C_0	82.56 fF
α_r	2.745 fF
α_i	17.5 $\mu S \cdot GHz^{-1}$

To quantify the permittivity-to-admittance behavior of the patch, a 3D model of a $100\times100-\mu m^2$ patch on a realistic representation of the available 40-nm CMOS stack, in direct contact with a MUT, was simulated versus varying ϵ' and ϵ''. The solid lines in Fig. 2.5b show the capacitance and conductance of node P versus ϵ' and ϵ'', for different values of ϵ'' and ϵ', respectively, at a simulation frequency of 1 GHz. An explicit relation of capacitance to ϵ' and conductance to ϵ'' exists that can be linearly approximated by

$$Y_P(\epsilon', \epsilon'', \omega) \approx \alpha_i \cdot \omega \cdot \epsilon'' + j\omega \cdot (C_0 + \alpha_r \epsilon'), \tag{2.3}$$

where α_r and α_i are real parameters. Note that the ω contribution in the real part of the admittance results from the fact that conductivity of the material is given by $\sigma = \omega\epsilon''$ [17]. Table 2.2 summarizes the model parameters in (2.3) extracted after least square fitting with the EM-simulated curves.

Although the linear model is simple, intuitive, and valuable for preliminary analysis or applications that do not require increased accuracy, it is clear from the simulated results of Fig. 2.5b that C_{MUT} and G_{MUT} also vary with ϵ'' and ϵ', respectively. This effect cannot be captured by (2.3). For calibration purposes, a rational function model (RFM), fitted from EM simulations, can be used to arrive at an analytical model, a methodology widely used in permittivity measurements performed with open-ended coaxial probes [2, 3, 18]:

$$Y_P(\epsilon^\star, \omega) \approx j\omega C_0 + \frac{\sum_{n=1}^{N}\sum_{p=1}^{P} \alpha_{np} \left(\sqrt{\epsilon^\star}\right)^p (j\omega a)^n}{1 + \sum_{m=1}^{M}\sum_{q=1}^{Q} \beta_{mq} \left(\sqrt{\epsilon^\star}\right)^q (j\omega a)^m}, \tag{2.4}$$

where a is a scaling parameter, set equal to the patch dimension, and α_{np}, β_{mq} are $N \times P$ and $M \times Q$ real model parameters, respectively. To find the parameters, (2.4) is fitted with parametric EM simulations across ϵ', ϵ'' and frequency. A fitted model with $N = P = M = Q = 4$ is deemed sufficient since it already achieves a 1% maximum deviation from simulations over a 0.1-10 GHz frequency range.

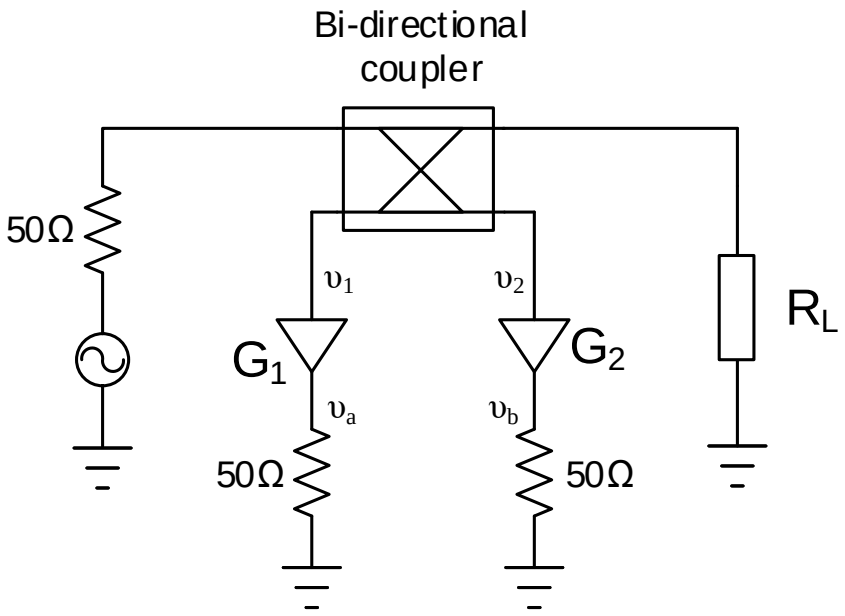


Figure 2.6: Principle schematic for the measurement of a reflection coefficient.

2.3. High-Precision permittivity measurements using I/Q mixer-steering interferometric

This section introduces an all-electronic, I/Q-mixer-based interferometric technique to reduce measurement noise in the characterization of extreme impedances. The proposed method employs a standard VNA, an arbitrary waveform generator, and an I/Q-mixer chain to generate a very stable cancellation signal that enhances the precision of a high-impedance/high-reflection measurement. This hardware implementation enables frequency scalability, due to the large commercial availability of the utilized components and high stability, speed, and repeatability, due to its fully electronic approach. The proposed technique is embedded in an scanning microwave microscopy (SMM) setup to demonstrate a more than 50% measurement noise reduction in the characterization of dielectric materials.[1]

2.3.1. Precision of high impedance load measurements

Let us consider the schematic of a VNA in Fig 2.6. It outlines the most widely used principle for measuring a reflection coefficient. The incident and reflected voltage

[1]Parts of this section were previously published in [19].

waves are coupled through a bi-directional coupler, presenting two voltages v_1 and v_2 at the coupled outputs, before being amplified and measured as v_b and v_a. If the incident and reflected measurement paths have gains G_1 and G_2, respectively, the measured value of the reflection coefficient Γ_{meas}, before calibration, is given by

$$\Gamma_{meas} = \frac{v_b}{v_a} = \frac{G_2 v_2}{G_1 v_1}. \tag{2.5}$$

To formulate the measurement variance, we define the gain path standard deviations σ_{G1} and σ_{G2}, which are uncorrelated with each other. We can also assume some measurement uncertainty in the measured voltage quantities, σ_{v2}, σ_{v2}, due to additional noise sources along the measurement path. The variance of the measured reflection coefficient can be calculated through the propagation of uncertainty:

$$\sigma^2_{\Gamma_{meas}} = \left(\frac{G_2 v_2}{G_1^2 v_1}\right)^2 \sigma^2_{G1} + \left(\frac{G_2 v_2}{G_1 v_1^2}\right)^2 \sigma^2_{v1} + \left(\frac{v_2}{G_1 v_1}\right)^2 \sigma^2_{G2} + \left(\frac{G_2}{G_1 v_1}\right)^2 \sigma^2_{v2}. \tag{2.6}$$

Substituting (2.5) into (2.6):

$$\sigma^2_{\Gamma_{meas}} = \Gamma^2_{meas} \left(\frac{1}{G_1^2}\sigma^2_{G1} + \frac{1}{v_1^2}\sigma^2_{v1}\frac{1}{G_2^2}\sigma^2_{G2} + \frac{1}{v_2^2}\sigma^2_{v2}\right). \tag{2.7}$$

From (2.7), it can be concluded that the standard deviation of the reflection coefficient measurement is proportional to the measured reflection coefficient itself, which suggests that reflection coefficients close to zero have a better readout precision as far as stochastic measurement errors are concerned. Additionally, as the gain G_1, G_2 of the coupled signals increases, for a constant deviation, the measurement precision improves.

So far, we discussed only the deviation of measuring the amplitude of the reflection coefficient. Assuming also deviations $\sigma_{\varphi 1}$ and $\sigma_{\varphi 2}$ in the phase of each path then, by the propagation of uncertainty from 2.5, it will appear in the measured phase as

$$\sigma^2_{\angle\Gamma_{meas}} = \sigma^2_{\varphi 1} + \sigma^2_{\varphi 2}. \tag{2.8}$$

Therefore, the measurement phase error is constant for any load and does not depend on the reflection coefficient amplitude or phase. However, it should be noted that (2.8) holds only where the phase is well defined and not when the reflection coefficient is zero (or very close to zero). In those regions of vague phase definition, the linear relations do not hold anymore, and an excessive error in the measurement result of the phase will exist.

2.3.2. Precision improvement techniques

Based on the above analysis of measurement noise versus load impedance, accurate high-frequency measurement of extreme impedances (referenced to the system

impedance) has always been a very challenging task. When dealing with a highly reflective device under-test (DUT), this effect is due to the reduced sensitivity, leading to increased measurement noise of the Γ-to-impedance transformation [20]. Recently, the need to characterize ultra-small devices (i.e., ultra-scaled CMOS, carbon nanotubes, nanofets, etc.) and the advancement of near-field SMM has spawned an increased interest in extreme temperatures impedance measurements. For example, ultra-small device characterization requires the accurate measurement of very small capacitances (i.e., below 20 fF). At the same time, SMM techniques are based on a nanometer probe illuminating a surface with a high-frequency signal to resolve small resistivity and permittivity differences over a high-impedance offset [21, 22].

Several techniques have been proposed to achieve better sensitivity in determining the actual impedance value of a high-Γ device. These can be grouped into two main categories, namely matching techniques and interferometric techniques. Both methods attempt to re-normalize the VNA reference impedance (50Ω) to a value closer to the targeted DUT, yielding a lower magnitude of the (re-normalized) reflection coefficient, which places it in the high-sensitivity region of the measurement setup. *Matching techniques* employ high-Q resonant networks [22], providing the proper impedance transformation only at a fixed, limited number of frequency points, yielding little (frequency) flexibility for a given characterization setup. *Interferometric techniques* create, by various means, a signal $\mathbf{b_{inj}}$ such that, by destructive interference, the wave scattered by the DUT (b) is canceled out. This approach results effectively in a measurement of Γ equal (or very close) to zero, since $\mathbf{b} = -\mathbf{b_{inj}}$, and $\Gamma = (\mathbf{b}+\mathbf{b_{inj}})/\mathbf{a}$ where $\mathbf{a}$ is the incident wave [23–26]. Moreover, a two-port technique has also been proposed and improves the stability and accuracy of Γ measurement [27].

2.3.3. An active I/Q-mixer-based interferometric technique

Fig. 2.7 gives the simplified block scheme of the proposed technique. The VNA source power is split to drive the local oscillator (LO) input of a passive I/Q mixer, which is phase-coherent to the incident wave $\mathbf{a}'$. The second branch of the splitter loops back to the R-channel jumper. A low-noise amplifier optimizes the LO drive level for the passive I/Q mixer. The I and Q ports of the mixer are controlled by DC values, allowing the adjustment of the signal phase and amplitude without any frequency conversion. After being "steered" in the I/Q plane, the signal is injected into port 3 of a directional coupler towards port 1 (see Fig. 2.7). When no signal injection is applied at port 3, the reflected wave $\mathbf{b}'$ at port 1 is a phase-shifted and attenuated version of the wave reflected from the load due to the presence of the coupler. However, if a signal is injected at port 3 ($\mathbf{b_{inj}}$), the resulting wave $\mathbf{b}'$ exiting port 1 is given by

$$\mathbf{b}' = 10^{-\frac{C}{20}} \cdot e^{j\varphi_C} \cdot \mathbf{b_{inj}} + 10^{-\frac{L}{20}} \cdot e^{j\varphi_T} \cdot \mathbf{b}, \tag{2.9}$$

where φ_C and φ_{T} are the phase shifts of the coupling and through paths, and C, L the coupling factor and insertion loss in dB, respectively. We can, therefore,

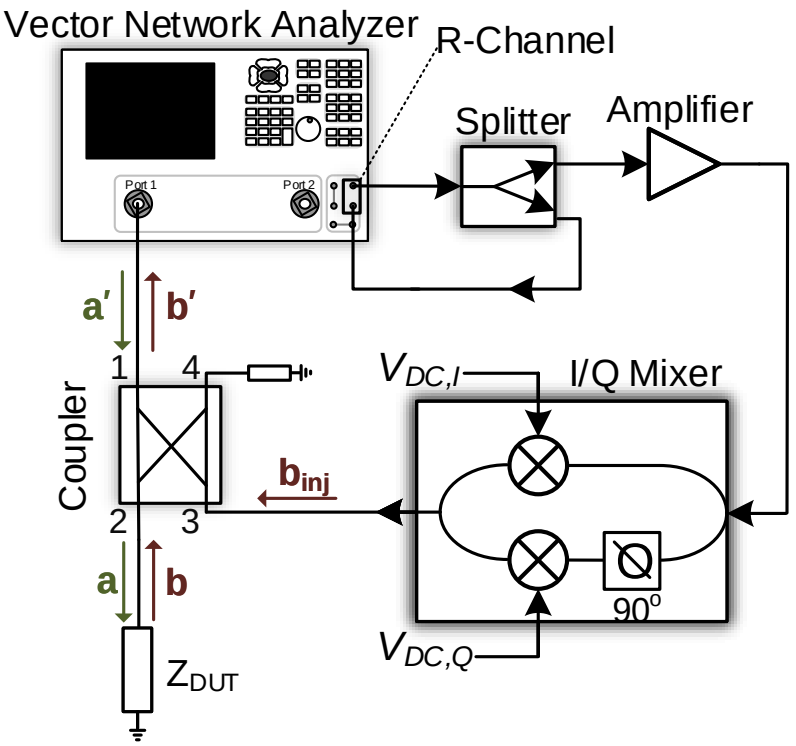


Figure 2.7: Simplified block scheme of the proposed I/Q-steering interferometric technique.

calculate that the injected signal needed to nullify the reflected signal to the VNA, namely, $\mathbf{b}' = 0$:

$$\mathbf{b_{inj}} = 10^{\frac{C-L}{20}} \cdot e^{j\varphi_T - \varphi_C + \pi} \cdot \mathbf{b} \tag{2.10}$$

Equation (2.10) provides the $\mathbf{b_{inj}}$ that cancels the reflected wave and, thus, drastically lowers the coefficient measured by the VNA. We can compare the proposed setup to other state-of-the-art implementations by evaluating the following statements:

- The cancellation signal should be injected close to the DUT. The section of the transmission line extending from the cancellation plane to the DUT acts as a resonator with a Q factor that increases with transmission line length. A very high Q (narrowband) cancellation will be affected by any disturbance in the measurement system and its environment (e.g., phase/amplitude variation due to cable flexing, temperature variations). Compared with traditional solutions, the proposed setup reduces from two couplers between the cancellation plane and the DUT [5] to only one, thus reducing the Q of the cancellation.

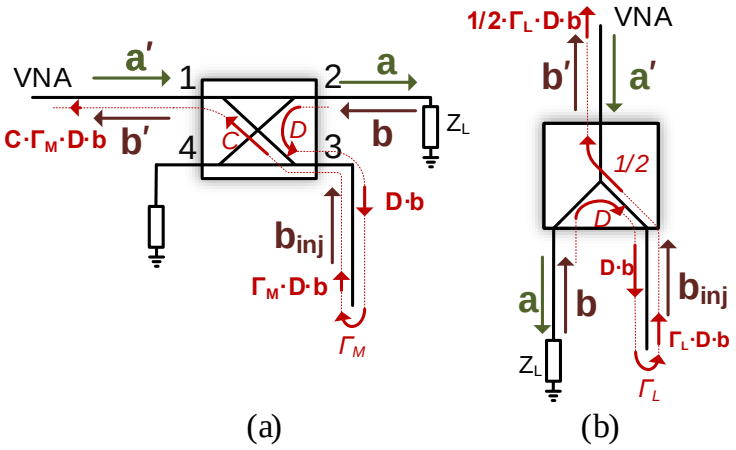


Figure 2.8: Flow analysis of the indirect wave contribution (denoted as $\mathbf{b}'$) to the cancellation due to the DUT reflection: (a) interferometric technique using power divider and a passive tuner and (b) proposed interferometric technique using a directional coupler and an active signal injection. The red dashed line indicates the unwanted (indirect) path to the injected signal and its effect on the reflected wave back to the VNA. Assuming $\Gamma_M = 0.1$, $\Gamma_L = 0.9$, $C = -10\ dB$ and $I = -40\ dB$, more than 50 dB reduction on $\mathbf{b}'$ can be acquired with the proposed technique.

- The cancellation point should be stable and independent of load variation. In [24–26], also shown in Fig. 2.8.a, the indirect, unwanted contribution ($\mathbf{b}'$) of DUT reflection ($\mathbf{b}$) to the direct, wanted reflected wave to VNA ($\mathbf{b}'$) is a version of the signal $\mathbf{b}$, attenuated by the isolation I of the splitter and the reflection coefficient Γ_L of the load, which in this case is close to unity, for proper operation of the technique. This also holds when a hybrid coupler is utilized as a power splitting element with a passive load providing the cancellation [27]. In the proposed setup, $\mathbf{b}$ is additionally attenuated by the coupling C, as well as the reflection coefficient of the mixer Γ_M, which is a constant low value (i.e., in the order -10dB) that can also be further minimized by a circulator.

2.3.4. SMM experimental setup and measurement results

The proposed interferometric technique was employed in a near-field scanning microwave microscopy setup (see Fig. 2.9). An open-ended coaxial probe with 20 μm diameter at the tip end is placed a few μm above the wafer to scan a DUT area of few mm^2 (see inset Fig. 3). A computer numberical control (CNC) machine with μm displacement accuracy (Colinbus Laboflex-30) is used to mount the probe along with the coupler and I/Q mixer and perform 2-D scanning. A VNA (HP 8753D) is used to perform the Γ measurements. A double-balanced I/Q mixer (Marki IQ1545MMP) outputs the injection signal into a coupled-line coupler (Krytar 2611). The LO drive signal is amplified using two low noise amplifiers (Mini-Circuits ZRL-3500 and ZFL-

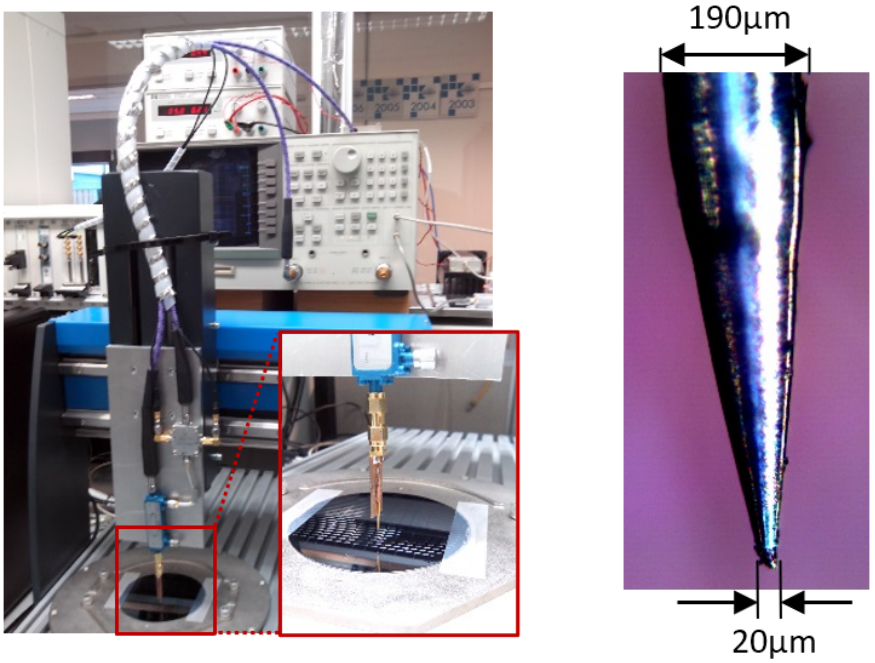


Figure 2.9: Photo of the experimental setup with zoom-in of the probe and the wafer (left) and probe microphotograph and dimensions (right).

2500). The DC values of the I and Q ports are set by two arbitrary waveform generators (AWG) controlled by a PC (NI PXI-5422).

All instruments are controlled by a MATLAB environment. A search algorithm is implemented to identify the I and Q values ($V_{DC,I}$ and $V_{DC,Q}$ in Fig. 2.7 providing the correct $\mathbf{b_{inj}}$ (as suggested by eq. 2.10) when the probe is placed over an initialization region of the wafer. The resulting I and Q values are then held constant during the entire scanning. For comparison purposes, we have also measured each measurement point without interferometric technique by applying the I and Q values that minimize the LO feed-through of the mixer, resulting in no signal injection to the coupler. The VNA frequency was set to 2 GHz, with a bandwidth of 10 Hz for all measurements.

Fig 2.10 shows the image of a die that contains silicon trenches and cavities embedded in SiO_2, which was used for experiments with SMM. No differentiation of the two materials is possible from an optical image, except for the outlines of the structure, indicating a height difference. Moreover, because the probe impedance is mainly capacitive, the reconstructed image from the raw Γ amplitude is too noisy, with no observable difference. In contrast, the image of the raw Γ phase can still provide a meaningful image.

By using the interferometric technique to normalize the system impedance to the one of the SiO_2, the same SMM image information is transferred to amplitude

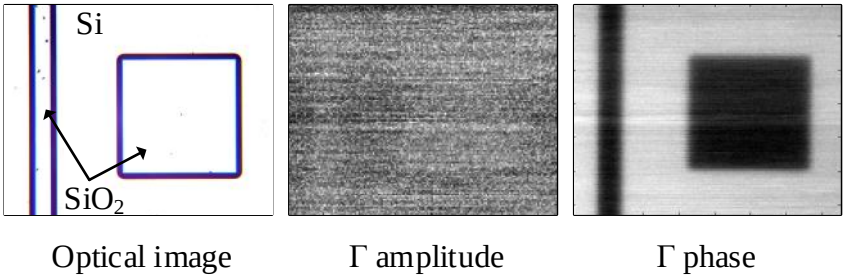


Figure 2.10: Optical image and reconstructed images of raw Γ amplitude and phase (without interferometric technique). Due to excessive noise, no information can be extracted from the Γ amplitude. Instead, all information is located in the phase of Γ.

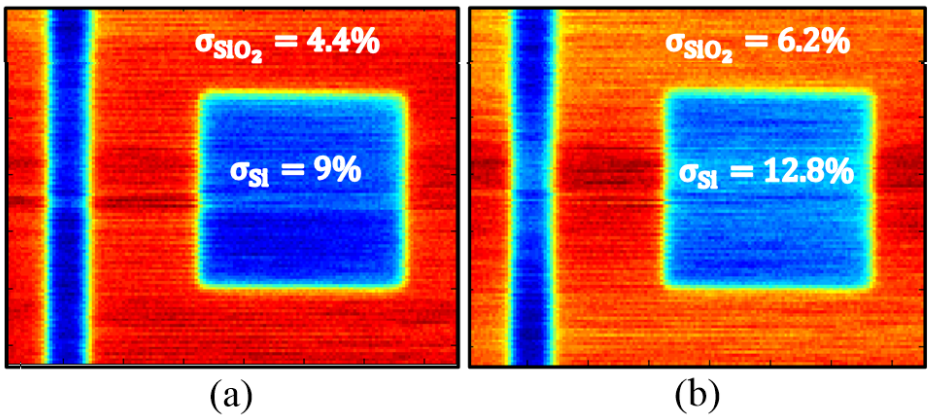


Figure 2.11: Two-dimensional images of a $3 \times 2.4mm^2$ extract of the wafer (scanning step of 20µm). (a) Image acquired from measured Γ amplitude with interferometric technique and (b) image acquired from measured Γ phase without the interferometric technique. The standard deviation of measurement of all measurement points that fall within the same material is annotated (SiO_2 – red and Si – blue).

and, as discussed in section 2.3.3, the phase is not well defined at $\Gamma = 0$. Therefore, the phase image bears excessive noise, and the amplitude is considered the only meaningful quantity. Fig. 2.11 shows the reconstructed 2-D images of the measured Γ. The image constructed using Γ amplitude with interferometric technique reduces the image noise by more than 40% compared to the image constructed using the Γ phase without interferometric technique (fig. 2.10).

To extract the impedance information at the probe connection point, a short-open-load one-port calibration procedure is carried out at port 2 of the coupler (see

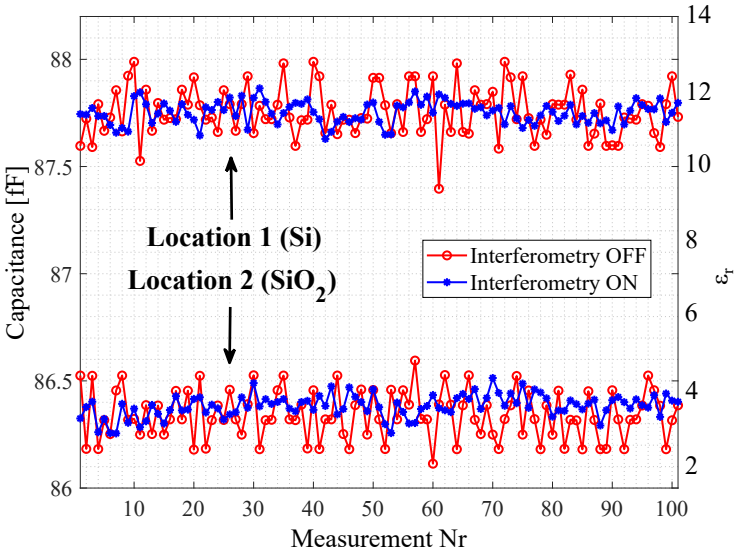


Figure 2.12: Measurement traces (100 points) of two locations of the wafer with different materials (SiO_2 and Si respectively), with and without the interferometric technique (blue asterisk and red circle trace, respectively).

Fig 2.7), with and without the cancellation, respectively. The probe impedance at the point where the cancellation is performed is used as the load standard for cancellation signal injection. De-embedding of the probe was done by fitting the measurements to a realistic 3-D EM model of the structure to acquire the equivalent capacitance of the probe, resulting from the air gap between the probe and the wafer and the scanned material properties.

Fig. 2.12 shows the measured capacitance and permittivity measurement traces at two wafer locations (Location 1 – Si and location 2 – SiO_2). The measurement's standard deviation (σ) was consistently improved by more than 50% when the interferometric technique was enabled (0.32 fF versus 0.7 fF at location 1 and 0.27 fF versus 0.56 fF at location 2).

Additional measurements, including other test wafers, were performed to assess the precision improvement of the proposed setup. Four dies of the same size and height were placed aside, as shown in Fig. 2.13, and the CNC machine was used to place the probe tip above each one of them. Different materials have been developed on the surface of the used wafers, namely, Si, Si_3N_4, SiO_2, and SiC. The Si_3N_4 die is used for impedance renormalization point for the interferometric technique. Fig. 2.14 compares the measured permittivity traces when the interferometric technique is switched on and off. Using the interferometric technique provides measurement noise improvement of -9% in Si, -78% in Si_3N_4, -54% in SiO_2, and -57% in SiC.

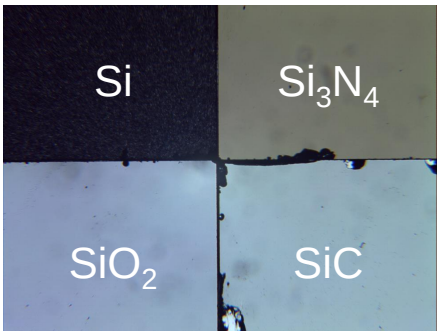


Figure 2.13: Multi-die structure comprising Si, Si_3N_4, SiO_2, and SiC dies placed aside for permittivity measurement with the proposed SMM setup .

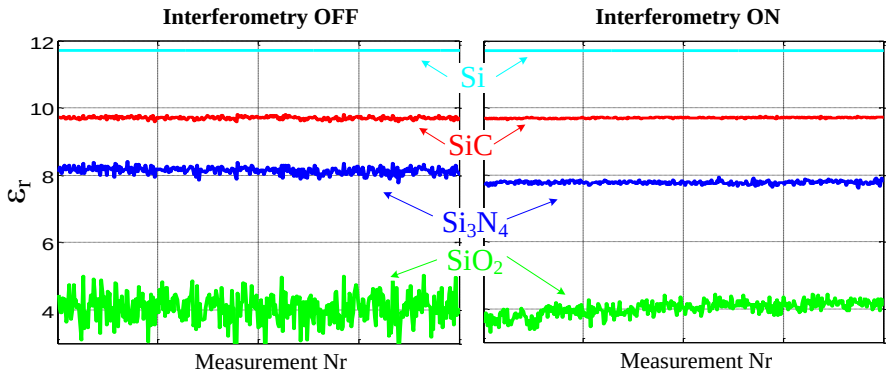


Figure 2.14: Permittivity measurement of the four materials in the multi-die structure of fig. 2.13, when the proposed active interferometric technique is OFF (left) or ON (right)).

2.4. CMOS integrable Wheatstone bridge

The focus of this work is to implement a high-resolution high-impedance measurement BDS front-end/system as an IC in CMOS technology. Despite the effectiveness of the interferometric technique proposed in section 2.3, straightforward integration would require the inclusion of area-consuming passive RF couplers on-chip, severely limiting the aimed miniaturization of the BDS system for the intended applications. This limitation becomes even more evident at lower frequencies since the required passive RF coupler area would be comparable to the wavelength of operation.

The Wheatstone bridge [28, 29] is a widely adopted method of measuring or sensing electrical impedance. It quantifies impedance variation relative to a con-

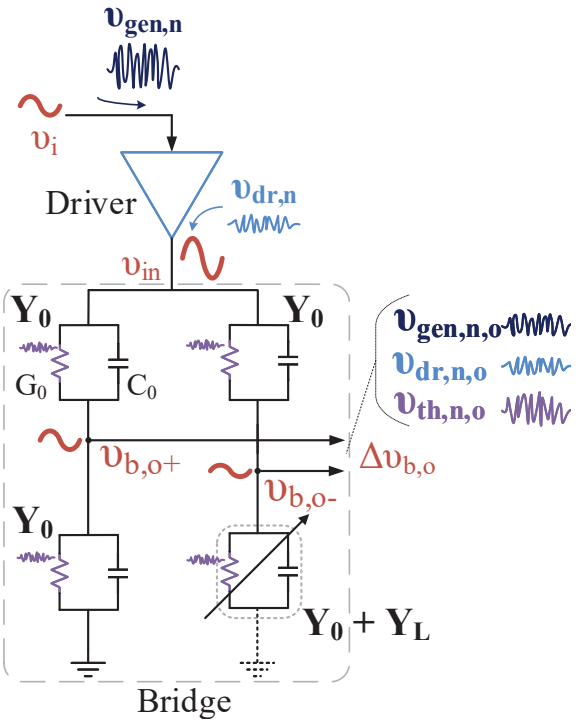


Figure 2.15: Balanced impedance bridge, driven at RF frequency by a driver, with annotated signals and noise sources contributing to the total noise at the output of the bridge.

stant baseline value, such as C_0 in the patch sensor. Additionally, it lends itself to a compact integration in CMOS technology since it consists of routinely available resistors and capacitors of a small footprint. At RF frequencies, impedance bridges have been widely used in broadband vector network analysis as directional detection elements, as an alternative or complementary to bi-directional couplers [30].

In this subsection, an alternative analysis of the AC-driven Wheatstone bridge with complex branch loads is presented. Mathematical manipulation of the bridge equation is performed to extract the necessary information for calibrating a sensing element within the bridge. This analysis is later verified by measurements of various known RF impedances in a probed measurement environment. Moreover, the bridge output noise is calculated to extract information about its minimum detection limit.

2.4.1. Bridge analysis

Consider the RF impedance bridge shown in Fig. 2.15 with branch admittances Y_0 and the load to be measured Y_L, defined as the deviation from the baseline admittance Y_0. The bridge is excited at a given frequency ω with a signal of amplitude v_{in}, through a bridge driver that amplifies a signal v_i of the same frequency. The differential output voltage of the bridge can be found after straightforward circuit analysis:

$$\Delta v_{b,o} = v_{b,o+} - v_{b,o-} = v_{in} \cdot \frac{Y_L}{4Y_0 + 2Y_L}, \tag{2.11}$$

where $Y_L = G_L + jB_L$ and $Y_0 = G_0 + jB_0$ are the complex representation of the admittances. A common approximation is that, for small variations of the measured load admittance, i.e. $G_L << G_0$ and $B_L << B_0$, equation (2.11) denotes that the output varies linearly with the measured load admittance:

$$\Delta v_{b,o} \approx v_{in} \cdot \frac{Y_L}{4Y_0} \tag{2.12}$$

This approximation, however, can result in significant errors in the estimation of Y_L. Logically, the more generic result that accounts for any measured load value can also be used. Eq. (2.11) is valid irrespective of how the loading unbalances the bridge and does not require approximations. Assuming that $Y_L \neq 0$, inverting (2.11) results in

$$\frac{1}{\Delta v_{b,o}} = \frac{1}{v_{in}} \left(2 + \frac{4Y_0}{Y_L}\right). \tag{2.13}$$

Substituting for Y_0 and Y_L yields

$$\Re\left\{\frac{1}{\Delta v_{b,o}}\right\} = \frac{1}{v_{in}} \left(2 + 4G_0 \cdot G_{Lw} + 4B_0 \cdot B_{Lw}\right) \tag{2.14}$$

and

$$\Im\left\{\frac{1}{\Delta v_{b,o}}\right\} = \frac{4}{v_{in}} \left(B_0 \cdot G_{Lw} - G_0 \cdot B_{Lw}\right), \tag{2.15}$$

where $G_{Lw} := G_L/|Y_L|^2$ and $B_{Lw} := B_L/|Y_L|^2$ are defined as the *weighted load conductance* and *weighted load susceptance* values, respectively.

From this analysis, it becomes evident that, irrespective of the deviation of Y_L from Y_0, the real and imaginary parts of the inverse bridge differential output are linear combinations of the weighted load conductance and susceptance. The advantage of formulating the bridge behavior as in (2.14) and (2.15) is that they present a linear relationship between the output quantity (inverse of voltage output) to the input quantity (the weighted conductance and susceptance). In this manner, an intuitive calibration procedure can be obtained that is both linear and theoretically bound to the bridge operation instead of using high-order polynomial fitting [10, 13, 14]. The calibration procedure will be described in detail in section 4.3.

[2] Parts of this section were previously published in [31].

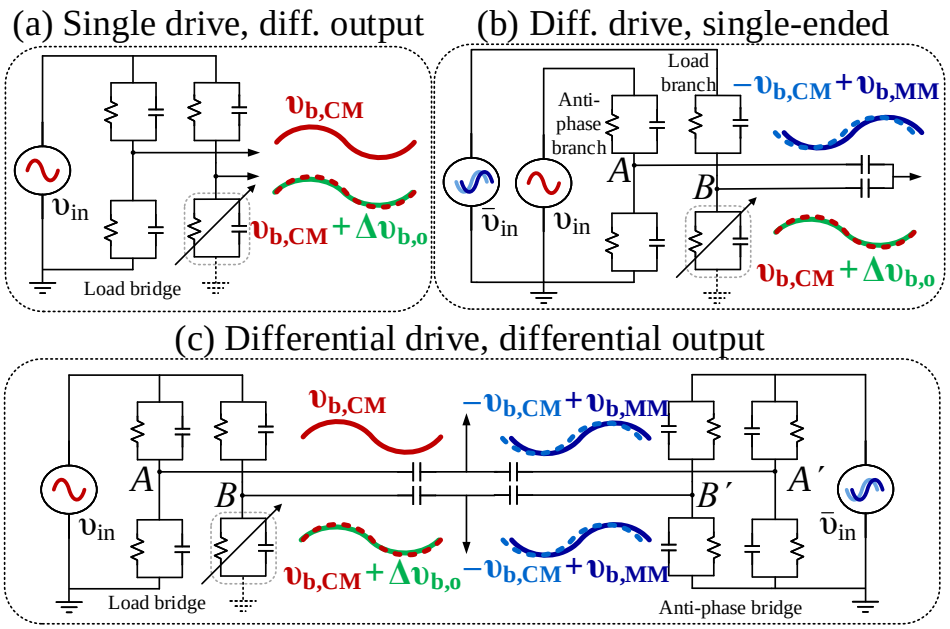


Figure 2.16: Evolution of single-driven, single-ended impedance bridge towards a fully differential, double-balanced topology. $v_{b,CM}$ denotes for common-mode signal, while $v_{b,MM}$ is the signal caused by the phase mismatch between the two out-of-phase driving sinusoids.

2.4.2. Double-balanced, fully differential bridge

The RF impedance bridge of Fig. 2.15, analyzed until now, suffers from a large common-mode signal at its output. To achieve the highest sensitivity to load changes, equation (2.11) suggests that the drive amplitude voltage $|v_{in}|$ should be maximized. In a CMOS implementation, where the bridge is actively driven by MOS transistors, this maximum amplitude is in the order of the nominal supply (VDD). Moreover, the highest sensitivity is achieved when all nominal branch admittances are equal (Y_0). Under these assumptions, the worst-case common mode-signal $v_{b,CM}$ at the differential output of the bridge is half the supply voltage (peak-to-peak). This common-mode signal is superimposed on top of the useful differential signal of interest, namely $\Delta v_{b,o}$, which will be orders of magnitude smaller, as graphically illustrated in the single-driven topology of Fig. 2.16. Such a large common-mode voltage poses a stringent requirement to the common-mode rejection ratio (CMRR) of the read-out chain and compromises the linearity of the active circuitry following the bridge.

An anti-phase drive of each branch of the bridge (solution 2 in Fig. 2.16), can mitigate this problem since the baseline signals, having a phase difference of 180^o, will cancel out when combined at the output of the bridge. The latter is done preferably capacitively to achieve DC blocking. However, this results in a single-ended bridge output, and the benefits of a fully differential read-out chain cannot

be employed. Moreover, if the two drive signals are not exactly 180^o out-of-phase, a phase mismatch signal ($v_{b,MM}$) will appear in the output of the bridge. This mismatch signal cannot be treated as a constant offset since it will be load-dependent due to the non-zero output impedance of the bridge driver.

A double-balanced configuration, solution 3 in Fig. 2.16, uses an anti-phase-driven copy of the bridge (without the load connection). Capacitively combining the four bridge nodes (A to A′ and B to B′, respectively) results in a differential output. Additionally, any signal caused by phase mismatch of the bridge drive turns into a common-mode signal, which is much smaller than $VDD/2$ and can easily be rejected in a fully differential chain. Nevertheless, using a double-balanced bridge configuration instead of a single one comes at the price of doubling the required IC area and the noise power. It also requires more energy to drive the bridge(s) for the same output signals.

2.4.3. Bridge noise

To calculate the noise at the output of the bridge, we can break it down into three uncorrelated components, as shown in Fig. 2.15: thermal noise generated by the resistive bridge elements ($v_{th,n}$), flicker, shot, and thermal noise generated by the active devices driving the bridge ($v_{dr,n}$), and input noise to the bridge driver originating from the RF signal generator, either external or internal ($v_{gen,n}$). By applying superposition, the contribution of each component to the output noise can be analyzed. The total noise is thus the mean-square sum of these three components: $\overline{v_{n,o}{}^2} = \overline{v_{th,n,bo}^2} + \overline{v_{dr,n,o}^2} + \overline{v_{gen,n,o}^2}$.

The thermal noise power at the differential output of the bridge is given by

$$\overline{v_{th,n,o}^2} = 4kT \int_{\omega-\Delta\omega/2}^{\omega+\Delta\omega/2} \Re\left(\frac{1}{4Y_0 + Y_L}\right) \cdot d\omega \tag{2.16}$$

$$= 4kT \int_{\omega-\Delta\omega/2}^{\omega+\Delta\omega/2} \frac{4G_0 + G_L}{(4G_0 + G_L)^2 + (4B_0 + B_L)^2} \cdot d\omega, \tag{2.17}$$

where $\Delta\omega$ is the observation bandwidth, which is tied to the inverse of the measurement time t_{meas} through the relation

$$\Delta\omega = \frac{2\pi}{t_{meas}}. \tag{2.18}$$

Since the complex permittivity is translated to conductance and capacitance, the resulting bridge susceptance will essentially represent a capacitance, i.e., $B = \omega C$. In addition, the observation bandwidth is typically much smaller than the frequency of interest ($\Delta\omega << \omega$), and thus, we can safely neglect the frequency variation of the integrated quantity:

$$\overline{v_{th,n,o}^2} \approx 4kT \left(\frac{4G_0 + G_L}{(4G_0 + G_L)^2 + \omega^2(4C_0 + C_L)^2}\right) \Delta\omega. \tag{2.19}$$

We will show in section 3.3.3 that a clipping buffer providing a square-wave excitation can be used as the bridge driver. Assuming a quiet power supply, the contribution of noise from this bridge driver is in the form of cyclo-stationary phase-modulated (PM) noise that results from up-conversion of thermal and flicker noise to the frequency of operation [32]. This noise will be scaled by the bridge similar to the bridge drive signal v_{in} and can, therefore, be expressed as a function of the single-sideband (SSB) phase noise of the driver, L_{dr}, and the differential output ($\Delta v_{b,o}$) of the bridge:

$$\overline{v_{dr,n,o}^2} = 2\int_0^{\Delta\omega} 10^{L_{dr}(\omega)/10} \cdot \Delta v_{b,o}^2 \cdot d\omega = IPN_{dr} \cdot \Delta v_{b,o}^2, \tag{2.20}$$

where IPN_{dr} is the double-sideband (DSB) integrated phase noise (IPN) of the driver up to the measurement bandwidth $\Delta\omega$. Similarly for the external generator noise, any amplitude-modulated (AM) component is suppressed by the buffer. However, the PM noise will be propagated to the bridge through its phase noise transfer of unity, since any timing variation in the input of the switching buffer will be transferred directly to its output. Consequently, the contribution of the generator noise to the output of the bridge can be expressed, identically to (2.20), as

$$\overline{v_{gen,n,o}^2} = IPN_{gen} \cdot \Delta v_{b,o}^2, \tag{2.21}$$

where IPN_{gen} is the DSB IPN of the generator within the measurement bandwidth $\Delta\omega$.

Notice from (2.20) and (2.21) that the noise components related to the bridge driver are proportional to the output power of the bridge, which suggests that the more balanced the bridge is, the lower the external noise contribution to the output. These contributions can be grouped into what we can call *external noise contributions*. Fig. 2.17 shows how the two noise contributions, namely the thermal contribution of the bridge itself and the external noise contributions, will vary versus the bridge output voltage. The total noise power, being the mean-square sum of the two, is dominated by the external sources when the bridge is unbalanced and is limited by the thermal noise level when the bridge is close to its balanced state. The transition point between the two dominant noise regimes is denoted as $\Delta v_{b,o,t}$ in Fig. 2.17 and is closer to the balanced state for an external source with higher IPN.

In practice, the total noise is in many cases dominated by external sources since the phase noise levels of buffers and generators are much higher than the thermal noise level of the bridge, even for small bridge output voltages. As an example, consider a realistic loading scenario of the RF bridge as in Fig. 2.15, with $G = 1\ mS$, $C = 100\ fF$, $G_L = 0.01\ mS$ and $C_L = 1\ fF$ (1% imbalance), driven at 1 GHz with an amplitude of $v_{in} = 1\ V$ and read out at an observation time of 1 ms According to (2.11) and (2.19), the signal output of the bridge is $\Delta v_{b,o} = 2.5\ mV$ and the thermal noise power at the output is $v_{th,n,o}^2 = 1.489 \cdot 10^{-15}\ V^2$. For an external source (driver or generator) to contribute the same noise level at the bridge output, a required IPN of $-85.2\ dBc$ is calculated from (2.20) or (2.21), which

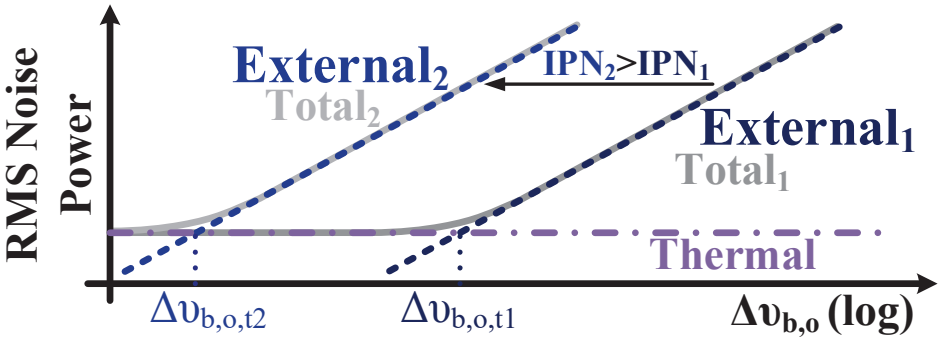


Figure 2.17: Thermal and external noise contributions to the bridge output noise versus bridge differential output voltage, $\Delta v_{b,o,t}$) for two different levels of IPN of the external source, showing the reduced noise contribution of a balanced bridge.

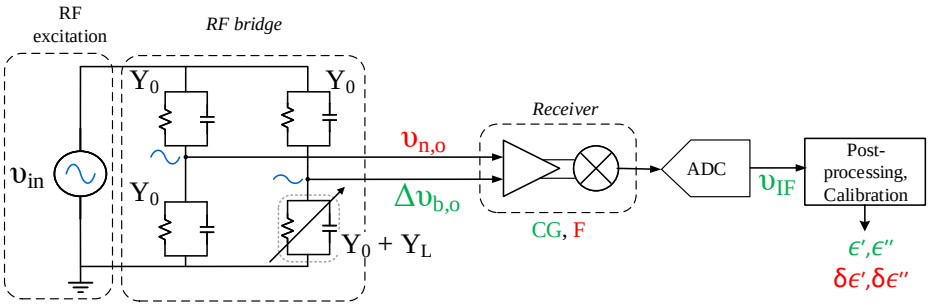


Figure 2.18: Generic receiver-based readout system, including the RF bridge.

corresponds roughly to an SSB phase noise of $-118\ dBc/Hz$ at frequency offsets below 1 kHz. This performance is at the boundary of what is achievable by state-of-the-art frequency synthesizers at this frequency of operation [33, 34].

2.4.4. Permittivity readout precision

Knowing the noise introduced at the output of the bridge, we can proceed with determining the (best) achievable permittivity precision concerning a given noise level. As discussed in section 1.3, a receiver-based readout is preferred for broadband readout. A block diagram of such a readout system including an RF bridge front-end, a down-conversion receiver chain with conversion gain CG, and noise factor F an analog-to-digital converter (ADC) is depicted in fig. 2.18.

Let $v_{IF} = |v_{IF}| \cdot e^{-j\phi_{IF}}$ be the single-ended, amplified voltage output of the ADC. Also, assume that the A/D conversion quantization noise is far below the signal noise, as is the good design practice in all readout systems. We can relate the minimum variance bound of the amplitude and phase at the desired frequency of

operation, acquired by the fast Fourier transform (FFT) of v_{IF}, to its signal-to-noise ratio (SNR), through the Cramér-Rao bound [35]:

$$var\left\{|\hat{v}_{IF}|\right\} \geq \overline{v_{n,IF}^2}, \tag{2.22}$$

$$var\left\{\hat{\phi}_{IF}\right\} \geq \frac{2\pi}{SNR_{IF}}, \tag{2.23}$$

where $v_{n,IF}^2$ is the noise at the system output. Using the definitions for SNR, $SNR_{IF} = \Delta v_{b,o}^2/(F \cdot \overline{v_{n,bo}^2})$, and the conversion gain $CG = v_{IF}/\Delta v_{b,o}$, and using, as explained in 2.4.3, that $\overline{v_{n,bo}^2} = IPN \cdot \Delta v_{b,o}^2 + \overline{v_{th,n,o}^2}$, we acquire

$$var\left\{|\hat{v}_{IF}|\right\} \geq IPN \cdot F \cdot v_{IF}^2 + CG \cdot F \cdot \overline{v_{th,n,o}^2}, \tag{2.24}$$

$$var\left\{\frac{\hat{\phi}_{IF}}{2\pi}\right\} \geq IPN \cdot F + \frac{\overline{v_{th,n,o}^2}}{\Delta v_{b,o}^2} \approx IPN \cdot F, \tag{2.25}$$

where $F = 10^{NF/10}$ the system noise factor, and NF the noise figure. Note that a ratiometric measurement can be carried out by dividing the two chip output voltages (the output due to the measured load and the fixed capacitor output) for better sensitivity to the actual supply voltage and phase referencing. In that case, we can calculate, by the propagation of uncertainty, that the variance of the measured ratio signal $out = v_{IF}/v_{ref}$ is

$$var\left\{|\hat{out}|\right\} \geq 2 \cdot IPN \cdot F \cdot out^2 + 2 \cdot CG \cdot F \cdot \overline{v_{th,n,o}^2}, \tag{2.26}$$

$$var\left\{\frac{\hat{\phi}_{out}}{2\pi}\right\} \geq 2 \cdot IPN \cdot F. \tag{2.27}$$

As expected, a higher external IPN and system noise factor incurs a more noisy readout of both amplitude and phase. Moreover, an unbalanced bridge negatively affects only the variance of the signal amplitude. At the same time, the phase information stays unaffected to a first-order approximation and only depends on the input noise and the noise performance of the read-out circuitry.

The variance of the measured amplitude and phase propagates to the real and imaginary part and, through (2.14)-(2.15) and (2.3), to a variance of the load (G and C) and permittivity, respectively. Thus, we can conclude that the optimal precision of the real and imaginary part of the permittivity occurs when the bridge is perfectly balanced to the measured admittance. Indeed, as derived in (2.11) and (2.12), a balanced bridge has the highest Y_L-to-output sensitivity (equal to $4Y_0/v_{in}$). Moreover, the measured output variance is minimized to the thermal noise level at balance, as predicted from (2.26).

We can observe the effect of a balanced bridge and evaluate the permittivity resolution by performing a perturbation analysis on the equations that govern a permittivity readout system with the proposed bridge, i.e., eq. (2.11) multiplied by

the system gain. A CMOS readout system is designed in 40nm CMOS technology and simulated parameters for conversion gain and noise figure. A complex permittivity sweep is performed, and the calculated output amplitude and phase of the chip are superimposed by the random noise predicted by (2.26) and (2.27), respectively. Then, in a numerical analysis environment, the system of equations 2.3, 2.14, and 2.15 is solved for the permittivity, and the standard deviation, hence, precision, of the calculated permittivity is extracted. The resulting surfaces of this procedure are shown in fig. 2.19 for the simulated precision of the real and imaginary part of permittivity.

For a simulated bridge branch of $260\ fF$ parallel to $42\mu S$, and at the frequency of $f = 1\ GHz$, there is a specific complex permittivity value that balances the bridge, thus offering the best precision. As such, the complex permittivity precision contains local minima at $\epsilon' \approx 20.5$ and $\epsilon'' \approx 19.5$.

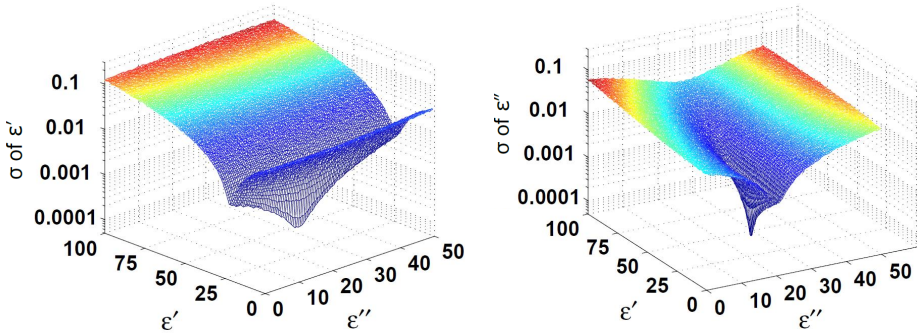


Figure 2.19: Simulated ϵ' and ϵ'' precision versus permittivity for the chip model for $f = 1\ GHz$, $b = 2$, $\Delta f = 1\ kHz$, $IPN = -90\ dBc$, $NF = 7.5\ dB$, $CG = 30\ dB$ (off-chip amplification included).

The circuit also implements a re-configurable bridge branch impedance Y_0 using switched capacitance circuits (step of $100\ fF$) controlled by a digital controlled word b. Fig. 2.20 shows the related simulated permittivity precision versus MUT permittivity for various values of the branch capacitance setting b at 1 GHz. The best precision is expected at this frequency since the noise figure, and external IPN of the used RF generator (Keysight E8257D) are at their minimum. By choosing the proper control value b, an absolute permittivity precision of < 0.05 can always be achieved. However, the deterioration of noise figure at lower frequencies (see Fig. 3.5), and the IPN at higher frequencies (due to external generator [33]) is expected to deteriorate the precision accordingly. In fact, if we assume a linear $\epsilon - to - Y_L$ model as well as a linearized bridge operation, the permittivity resolution deteriorates 10 times for every 10 dB increase of IPN or the noise figure, when the external bridge driver noise is dominating the overall measured noise (unbalanced bridge), as is practically the case.

It is demonstrated that a controllable bridge capacitance is a valuable technique

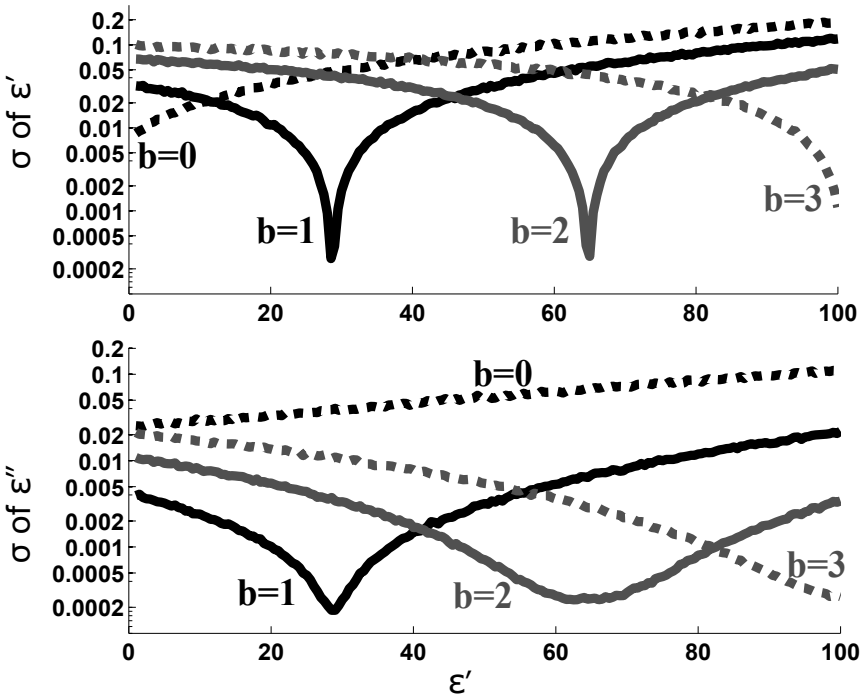


Figure 2.20: Simulated (a) ϵ' (top) and (b) ϵ'' (bottom) precision versus real part of permittivity, at different bridge capacitance settings for $f = 1\ GHz$, $\Delta f = 1\ kHz$, $IPN = -90\ dBc$, $NF = 7.5\ dB$, $CG = 30\ dB$ (off-chip amplification included).

for improving readout precision for the intended permittivity range. This concept resembles the interferometric technique presented in section 2.3, in that a reference impedance renormalization is effectively taking place by changing the branch impedance of the bridge. Designing a switchable impedance is very straightforward in CMOS technology, offering excellent switch functionality at a small area footprint and low cost.

The designed system has been fabricated in CMOS technology. The specific details of the implementation, calibration procedures and experimental results confirming the theoretical equations and simulations will be elaborated in the following chapters.

2.5. Conclusion

In this chapter, several commonly used permittivity sensing elements were discussed. A capacitive patch element was proposed and selected for its advantages towards implemented CMOS miniaturized application-oriented BDS systems. An interferometric technique for permittivity readout resolution improvement was proposed and tested. It is based on changing the system reference impedance to a

value similar to the high levels of the DUT. Although this interferometric technique is not directly implementable in CMOS, an RF bridge with analogous impedance renormalization through balancing is proposed. The bridge transfer function, noise, and achievable precision are analyzed and used, together with the simulation results of a realistic BDS system, as a showcase for the improved precision in a reconfigurable, double-balanced bridge topology. These topologies are compatible with CMOS technology and can be relatively easily implemented in a compact and cost-efficient way. The findings of this chapter provide the basis for the CMOS BDS systems realizations described in the following chapters.

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3

CMOS Permittivity-sensing Architecture and Circuits for Broadband Dielectric Spectroscopy

A compact, scalable, and broadband architecture is presented for complex microwave permittivity sensors in CMOS technology. It consists of a patch sensing element embedded in a (programmable) reconfigurable, double-balanced, differential RF bridge, which has been introduced in chapter 2. The bridge is driven by a clipping buffer that provides a multi-harmonic excitation of the sensing element. A dedicated intermediate frequency (IF) down-conversion scheme utilizes the excitation to allow fast multi-frequency permittivity characterization at the fundamental, third and fifth harmonics. The proposed configuration can act as the fundamental building block for BDS systems implementations that serve a wide span of industrial and biomedical applications, ranging from wearables to permittivity imaging. The BDS architecture has been implemented in CMOS technology to enable experimental verification.

Parts of this chapter were previously published in [1].

3.1. Introduction

Implementing a BDS sensing system in low-cost, high-yield CMOS technology is essential to the mass adoption of such a technique in commercially available products. Additional to the need for compatibility with CMOS technology, the proposed architecture can offer improved reliability and suitability for a variety of applications if it adheres to an additional set of requirements:

- Broadband operation allowing flexibility in the operating frequency,
- Complex material permittivity characterization, i.e., the ability to detect both real and imaginary parts of the permittivity,
- Scalability, i.e., suitability for embedding in a 2-D array for permittivity contrast imaging
- Low power consumption for battery-operated systems

The following sections elaborate on implementing such a compact, multi-purpose permittivity sensor architecture suitable for broadband permittivity sensing of liquid and semi-rigid materials. The proposed architecture provides a fast, multi-harmonic frequency readout that satisfies the real-time requirements at low energy consumption. Moreover, since both real and imaginary parts of permittivity are acquired, the accuracy of material characterization is significantly increased even when only a few frequency points are measured in the case of time or energy consumption constraints.

This chapter's architecture and CMOS circuits considerations have resulted in two demonstrator chips, i.e., a standalone ultra-compact BDS sensor system and a 5x5 sensor array for permittivity difference imaging. The experimental results of these demonstrators will be presented in chapters 4 and 5, respectively.

3.2. Multi-harmonic downconversion architecture

As discussed in chapter 1, a receiver-based architecture is favored for a broadband permittivity measurement system. Additionally, a double-balanced, fully differential bridge has been introduced and analyzed in section 2.4.2 to provide a high-precision readout on admittance changes of a sensing element in a CMOS-compatible setting. The downconversion architecture, including an LNA and downconversion mixer stage, has already been briefly presented in 2.18.

To effectively digitize and process the permittivity readout, the RF output of the bridge needs to be down-converted from the characterization frequency f_{RF} to a convenient intermediate frequency (IF), f_{IF} to enable straightforward digitization using an ADC. For this purpose, the bridge is connected to a downconversion mixer, as shown in Fig. 3.1, in which the output signal of the bridge is mixed with an LO signal at f_{LO}, generating an output signal Δv_{IF}, which is a replica of $\Delta v_{b,o}$ at $f_{IF} = f_{RF} - f_{LO}$, assuming a perfectly linear mixing operation.

A switching mixer with a square-wave LO drive is preferred to achieve a higher conversion efficiency than its small-signal equivalent [2, 3]. As a result, the LO

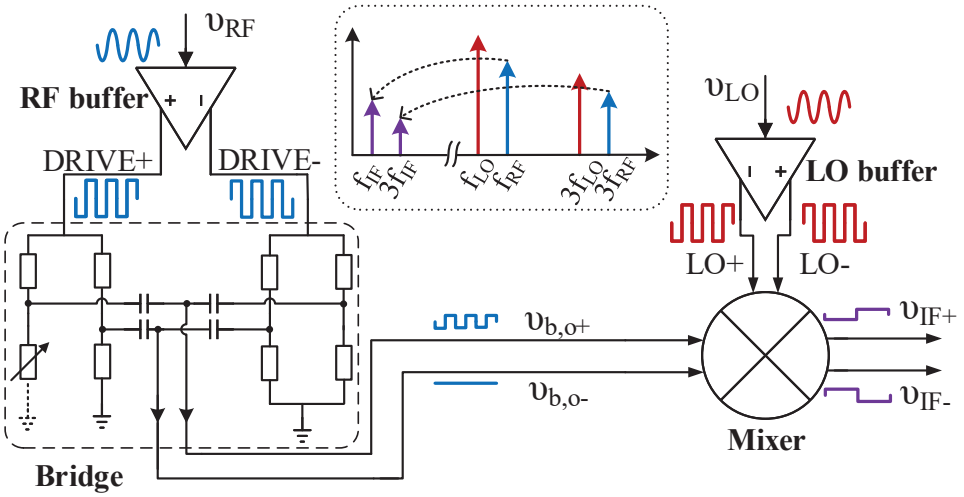

Figure 3.1: Block-level diagram of the multi-harmonic IF downconversion architecture with annotated signals and their frequency-domain representation (insert).

signal will also contain the odd higher-order harmonics of the fundamental f_{LO}. At the same time, it is also convenient to apply a square wave to the bridge to maximize the effective drive of the signals DRIVE+ and DRIVE- in Fig. 3.1. Indeed, a square wave provides $4/\pi$ higher amplitude than when using a sine-wave excitation. In addition, the square wave also excites the bridge sensor with its higher order-odd harmonics. Mixing the resulting bridge output signal with the square-wave LO signal will yield an IF signal that contains the down-converted spectral components of these signals, which are $2 \times f_{IF}$ apart (fig. 3.1.). With a properly chosen frequency offset, these can be easily acquired by an ADC allowing simultaneous characterization of the MUT at the fundamental measurement frequency and its odd harmonics. This approach reduces the measurement time and the required system power consumption per frequency point measurement.

Since the amplitude of the higher-order odd harmonics in the square wave reduces by at least $1/n$ compared to the fundamental, where n is the harmonic, a reduced measurement sensitivity is expected for higher harmonics. Nevertheless, due to the high dynamic range of the bridge concept when operating close to its balancing point, valuable information can still be acquired over an extended frequency range. Moreover, in addition to the baseband products of the mixing process, cross-mixing can create spectral content close to the even harmonics of f_{RF} (e.g., $3f_{RF} - f_{LO}$). Careful design of the mixer and a clean LO signal is required to avoid self-mixing with the odd harmonics of LO, which will fall within the frequency band of interest. Given this, a fully differential chain with layout matching techniques can minimize second-order harmonic signal content and non-linearities.

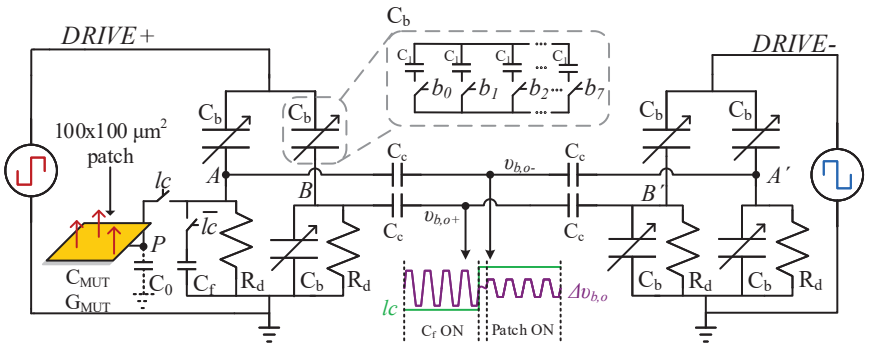

Figure 3.2: Schematic of the fully differential, double-balanced bridge with its sensing patch, implemented on the top metals of the 40-nm CMOS technology.

3.3. Circuit building blocks

This section discusses the integrated circuit design of the permittivity sensor based on the architecture above. Its circuit blocks compromise the sensor, the RF bridge, the downconversion mixer, and the drivers needed for the mixer and bridge that provide the square waves for the multi-harmonic operation.

3.3.1. Patch sensing element readout bridge

Fig. 3.2 shows the schematic of a bridge implemented in CMOS technology in which a square 100×100 μm^2-patch sensor patch is embedded. It is the actual implementation of the fully differential, double-balanced architecture discussed in 2.4.2. As demonstrated in sections 2.4.3 through 2.4.4, the value of branch impedances of the bridge affects the resulting readout precision for a given MUT permittivity since operation close to the bridge balancing point minimizes the injected measurement noise. A programmable branch impedance can provide the option to match the bridge to the MUT permittivity dynamically.

Shown in Fig. 3.2 is the implementation of the bridge in 40-nm CMOS technology. The dominant part of the branch admittance is the capacitor C_b. To accommodate large capacitive load variations and investigate the behavior of the bridge at various imbalanced states, C_b is implemented as a parallel combination of eight switchable capacitors. Each comprises a capacitor C_1 of roughly $100\ fF$, in series with a $10\ \mu m/40\ nm$ CMOS switch. This capacitor bank is controlled by a unitary weighted 8-bit digital signal b, resulting in a maximum branch capacitance of $\approx 800\ fF$.

The finite quality factor of the capacitor and the equivalent on/off resistances of the switch can be modeled by an equivalent conductance in parallel with a capacitance, whose values vary versus frequency. Although the switched-capacitor is physically a series R-C combination, the parallel equivalent model is extracted for compatibility with the MUT model (parallel G_{MUT}, C_{MUT} combination) and for consistency with the admittance-based analysis of the bridge in the previous chapters. Similarly, because the patch conductance is proportional to the frequency of

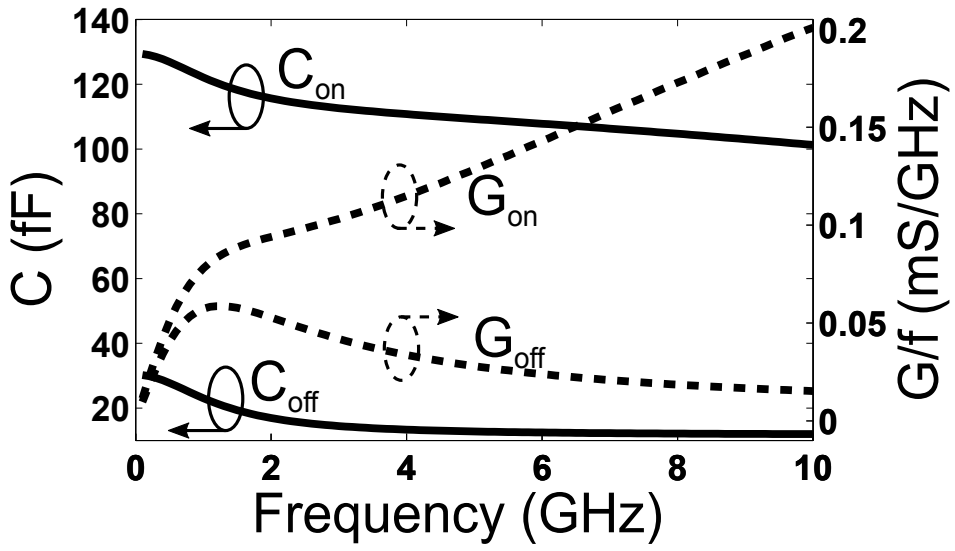

Figure 3.3: Equivalent parallel capacitance and normalized conductance of switched-capacitor at on and off stage.

operation (see eq. 2.3), the normalized conductance of the switched capacitor is extracted, i.e., the conductance divided by the frequency. Fig. 3.3 shows the simulated on/off parallel normalized conductance and capacitance versus frequency for the switched capacitor, estimated after a post-layout extraction of parasitics. The simulated on-capacitance and normalized conductance vary versus frequency from $130\ fF$ to $100\ fF$ and from $0.01\ mS/GHz$ to $0.2\ mS/GHz$, respectively, while the off-capacitance and normalized conductance are between $30\ fF$ to $12\ fF$ and $0.01\ mS/GHz$ to $0.06\ mS/GHz$, respectively. At each frequency, the total branch capacitance and admittance depend on the number of activated capacitors, determined by the value of b as: $Y_b = b \times Y_{on} + (8-b) \times Y_{off}$. A proper value of b can be used to bring the bridge branch admittance to a value such that the bridge comes close to its balanced state for the measured load. For example, for the permittivity range of simulations in Fig. 2.5b, we expect a load variation of $60 - 300\ fF$ and $0 - 0.8\ ms/GHz$ for patch capacitance and conductance, respectively. A value of b between 0 and 3 can fall within this range.

A 1.2-kΩ discharge resistor R_d is placed between the bridge center nodes (A, A', B, B') and the ground to ensure a DC discharge path for the proper operation of the NMOS switches. The value of the resistor is a trade-off between resistor size and additional voltage drop due to this extra bridge loading. Similarly, the four 25-fF combining capacitors C_c are of the same order of magnitude as the input capacitance of the following downconversion mixer for optimum voltage division.

As suggested by (2.11), the output voltage of the bridge is proportional to the amplitude of the drive signal v_{in}. Since its value depends on the supply voltage,

it is desirable to decouple the system output from the bridge drive amplitude. In addition, to gain information on both capacitance and conductance, we need to acquire both the real and imaginary parts of the bridge output. Therefore, both an amplitude and phase measurement of the bridge output is required. For the phase measurement to be consistent, a reference phase needs to be measured in addition. This is required to determine the relative phase variation at the output of the bridge, caused only by the patch load variation.

In a single sensing-element implementation, contrary to a sensor array, relative amplitude and phase measurement can be achieved without the introduction of any additional active circuitry by disconnecting the bridge from the patch and by connecting it to a fixed on-chip capacitance $C_f \approx 100\ fF$. This can be done during a continuous-time measurement, through a series NMOS switch, as shown in Fig. 3.2. This switch operates in its linear region because the discharge resistor R_d sets its DC bias to zero. The maximum voltage swing across the switch (350 mV in the presence of resistor R_d and parasitics to ground) is well below the simulated 1-dB compression point of 760 mV. A digital signal (lc) (see Fig. 3.2) controls the bridge's connection to the patch sensor or the fixed capacitor C_f. It is used to acquire a continuous measurement trace containing the bridge outputs during these two load cases. The acquired signal is down-converted and digitized, and the load cases are isolated in the digital domain by synchronization to the control signal lc. FFT is applied to the resulting signals to obtain the relative phase difference and amplitude ratio, which now only depend on relative differences between the fixed and the measured load.

Note, however, that such a time-division solution for a reference measurement does not eliminate fast variations of the bridge drive voltage, which can occur independently during the measurement of these two load-connection cases, as these variations will be uncorrelated to each other. If a BDS array is implemented, adding a dedicated sensor readout path for the reference measurement might be considered since it will only yield a small area overhead to the total system. In this work, the time-division technique will be adopted in the single sensor demonstrator (chapter 4), while an extra dedicated sensor readout will be used in the array implementation (chapter 5).

3.3.2. Downconversion mixer

Fig. 3.4 shows the schematic of the downconversion mixer connected to the bridge to perform the frequency translation of the RF bridge output signal to IF. This topology implements a current-mode switching mixer that achieves low 1/f noise operation and high linearity [4]. The transistors Q_1 and Q_2, along with resistors R_L, form a differential transconductance (g_m) stage. If the value of R_L is large enough, most of the drain current of the transistors will be transferred to the output, converting the bridge output voltage (v_{RF+}, v_{RF-}) to a differential current (i_{RF+}, i_{RF-}). The transistor Q_s sets the bias current, which is generally limited by two main factors: a) the large resistor value limits the headroom of Q_1 and Q_2, which is required for good linearity and b) Q_s needs to be small to minimize its parasitic drain capacitance that deteriorates the common-mode rejection ratio and second-order

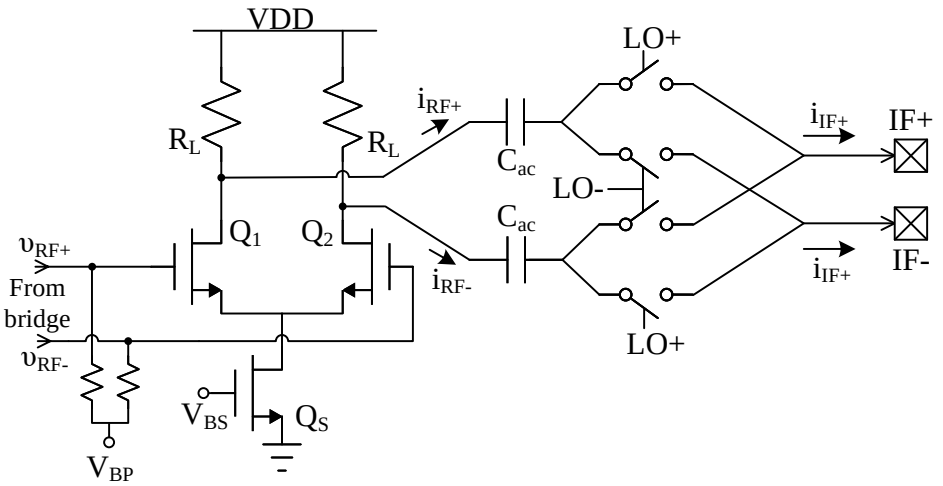

Figure 3.4: Current-mode downconversion mixer schematic consisting of a transconductance stage and a current-mode switch quad.

non-linearity. On the contrary, a higher bias current results in a larger amplification and, hence, a better noise performance. As a trade-off, a bias current of 700 μA was chosen to achieve a transistor g_m of 5 mA/V.

The output current of the g_m stage is fed to a CMOS switching quad that performs the mixing action. Capacitive coupling prevents DC from flowing through the CMOS switches to avoid flicker noise and improve non-linearity [4]. An optimum switch size exists since a large transistor size reduces the on-switch resistance (and thus the insertion loss) but increases the parasitic capacitance to the ground and the loading of the LO driver. A transimpedance amplifier (TIA) converts the down-converted current back to voltage, and an ADC digitizes the waveforms.

Fig. 3.5 shows the simulated conversion gain and noise figure of a CMOS mixer designed in 40-nm technology when terminated with an external 10-$k\Omega$ TIA and driven by an input port with an impedance equal to that of the bridge. Given the multi-harmonic operation, the gain and noise performance at the third and fifth harmonic operation are also simulated. Due to the $1/n$ reduction in the LO amplitude, the third and fifth harmonic conversion gain is expected to be 9.5 dB and 14 dB lower than the first harmonic, respectively. This trend is seen at frequencies above 1 GHz, while for lower frequencies, the first and third harmonics experience a more loss in the RF path due to the capacitive coupling at the bridge-mixer and g_m-quad connections. A 20-dB/dec gain roll-off is observed above 1 GHz. The noise figure is 7.5 dB at 2 GHz and stays below 10 dB in the 1-5 GHz range. Below that, it increases rapidly to 22 dB due to the signal loss at the bridge output capacitor C_c. As expected, the noise figure of the third and fifth harmonic downconversion process deteriorates by at least as much as the conversion gain deterioration.

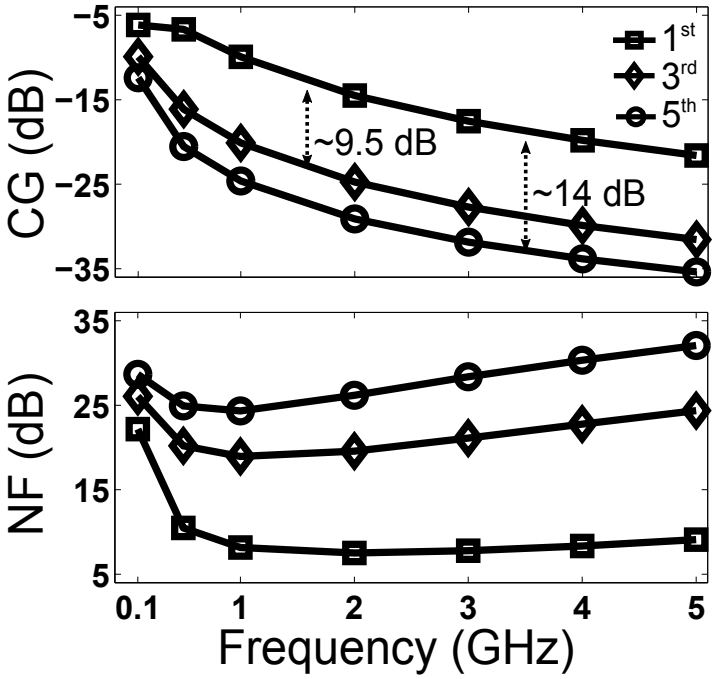

Figure 3.5: Simulated conversion gain (top) and noise figure (bottom) of the downconversion mixer versus fundamental RF frequency f_{RF}, at the first, third, and fifth operation harmonic. An IF frequency of 150 kHz is used.

3.3.3. Square-wave drivers

The bridge and LO drivers share the same topology, utilizing inverter amplifiers to achieve a square-wave rail-to-rail output. As shown in Fig. 3.6, the driver consists of a self-biased inverter that sets the DC voltage of the input waveform to the desired mid-rail value by proper choice of the NMOS and PMOS size. Two complementary copies of the input are created. A series of increasingly larger cross-coupled inverters further amplifies the signal and ensures rise-fall edge alignment, thus minimizing phase imbalance. Optimization of the inverters' transistor size ratio allows minimizing rise-fall mismatch that creates a common-common mode voltage at the output of the bridge. In general, steeper edges (i.e., larger-sized transistors and higher power consumption) minimize rise-fall mismatch across PVT variations. In fact, the simulated typical common-mode output on the bridge, caused by the driver at a 1.1-V supply, is 5 mV, while the worst-case (fast-n/slow-p, VDD=1V) was simulated to be 20 mV, which poses no significant risk for the linearity of the g_m stage, as would be the case with a large common-mode signal component when using a single sensing element readout bridge. Finally, the driver's simulated IPN, which contributes to the bridge output noise, is between -92 dBc at 1 GHz and -81 dBc at 5 GHz, for an integration bandwidth of 0.01-1 kHz.

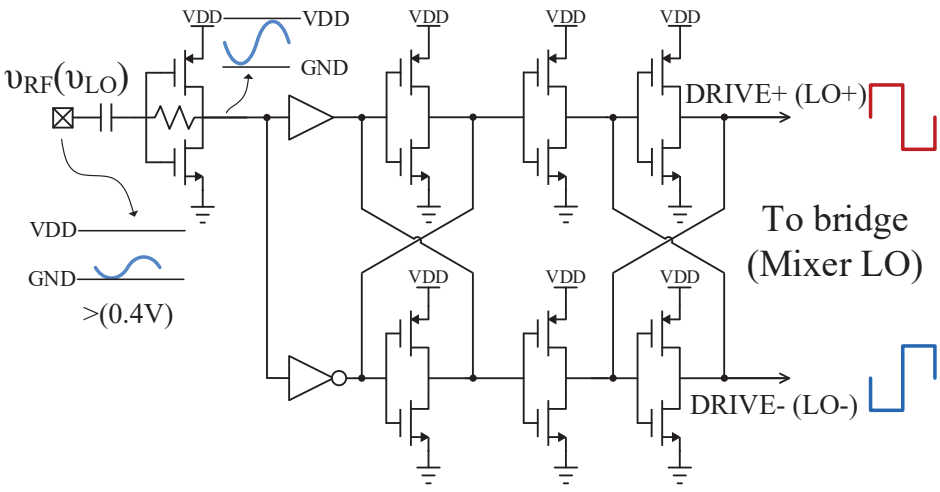

Figure 3.6: Schematic of the bridge and mixer drivers.

3.4. Scalable array concept

The architecture presented in section 3.2, implemented using the circuits described in section 3.3 can also be used in array configurations of microwave permittivity sensors for imaging or reconfigurable sensing platforms with varying sensing areas. As discussed in chapter 1, permittivity sensing arrays can be applied in applications in which the local differentiation between material is required or cases that require an average permittivity measurement over a large effective area that a larger patch cannot cover due to excessive capacitance.

Permittivity sensing arrays can be applied in applications where permittivity differentiation between materials in a lateral direction is required or applications requiring a permittivity measurement over a larger area or depth. In both cases, a single large patch might not be possible due to related excessive capacitance of the sensor patch involved. Fig. 3.7 shows a top-level diagram of exemplary array implementation, incorporating N rows and M columns of permittivity sensing pixels. Each pixel in the array core comprises a sensing element and its associated bridge with programmable admittance. The output of each pixel is converted to current so that pixel outputs of each row can be connected and directed to row-level down-conversion mixers. Similarly, row-level buffers are used to distribute the RF driving signal to the pixels. In this diagram, the IF output of the pixels is directed out of the chip to be digitized. However, in a system-on-chip (SoC) approach, the ADC can be placed on-chip and be shared among various sensing platforms.

In the schematic of Fig. ,3.7 each pixel can be driven and read out independently. Consequently, each pixel can be adjusted for its phase and read even without being driven and vice versa. For this purpose, a polarity switch in their driving paths can alternate each pixel drive or readout phase between 0 and 180 degrees. These features provide new possibilities for shaping the imposed electric field, enabling

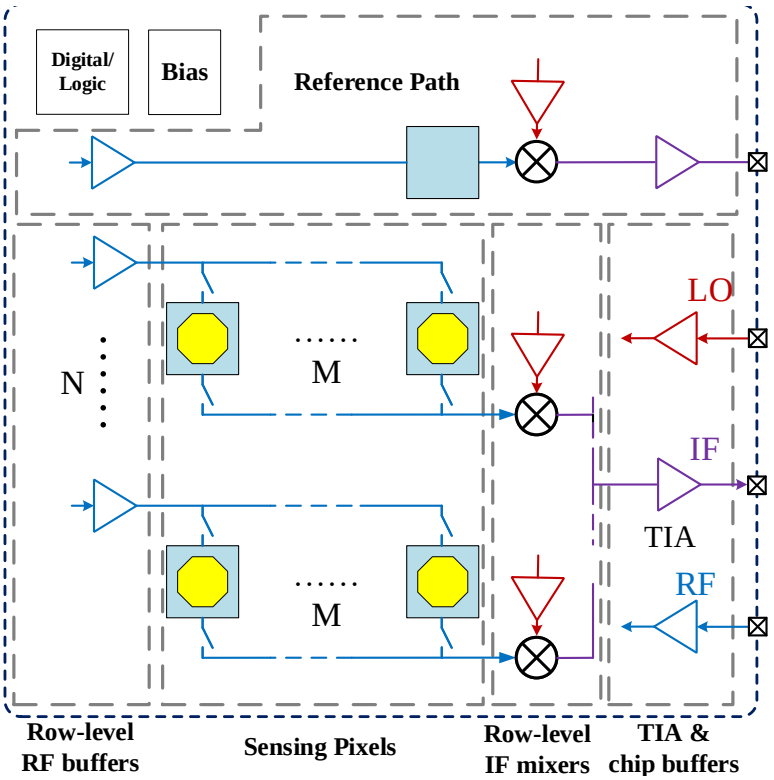

Figure 3.7: Conceptual top-level block diagram of a N×M permittivity sensing array.

us to trade-off field penetration, direction, and spatial resolution. Features that are enabled by utilizing the excellent switching capabilities of CMOS technology.

3.5. Conclusion

An architecture for the implementation of a CMOS-compatible complex broadband permittivity (pixel) sensing element was presented. The proposed architecture allows low form factor integration and is energy efficient, making it suitable for biomedical applications that demand real-time fast dielectric measurements or permittivity imaging. The circuit blocks presented can be used to implement this pixel architecture in various application scenarios. Indeed, this dissertation will present two related implementations, a single sensing element readout system and a 5×5 array, discussed in chapters 4 and 5, respectively.

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4

A Compact CMOS Permittivity Sensor for Broadband Dielectric Spectroscopy and Imaging

A compact sensing pixel to determine the localized complex permittivity at microwave frequencies has been fabricated in 40-nm CMOS technology. Its implementation showcases the proposed techniques, architecture, and circuits introduced in chapters 2 and 3. As such, it utilizes a square patch, interfaced to the MUT sample, embedded in a double-balanced RF Wheatstone bridge to provide a permittivity-dependent admittance. The bridge is cascaded by a linear, low-IF switching downconversion mixer and is driven by a square wave that allows simultaneous characterization at multiple harmonic frequencies. For the developed sensor hardware, a calibration procedure has been developed. Measurement results of liquids show good agreement with the theoretical values. The measurement precision of the relative permittivity is better than 0.4 over a 0.1–10 GHz range. The proposed implementation features a measurement speed of 1 ms and occupies an active area of 0.15×0.3 mm^2. This ultra-compact area facilitates multi-sensor arrays that enable 2-D dielectric imaging based on permittivity contrast. Moreover, the measurements demonstrate noise reduction through bridge balancing.

Parts of this chapter were previously published in [1, 2].

Lastly, the realized hardware provides Debye model parameter estimation of an independent material within a 1.6% error margin, using a full span frequency dataset and a 5.3% error margin when operating in energy-saving mode.

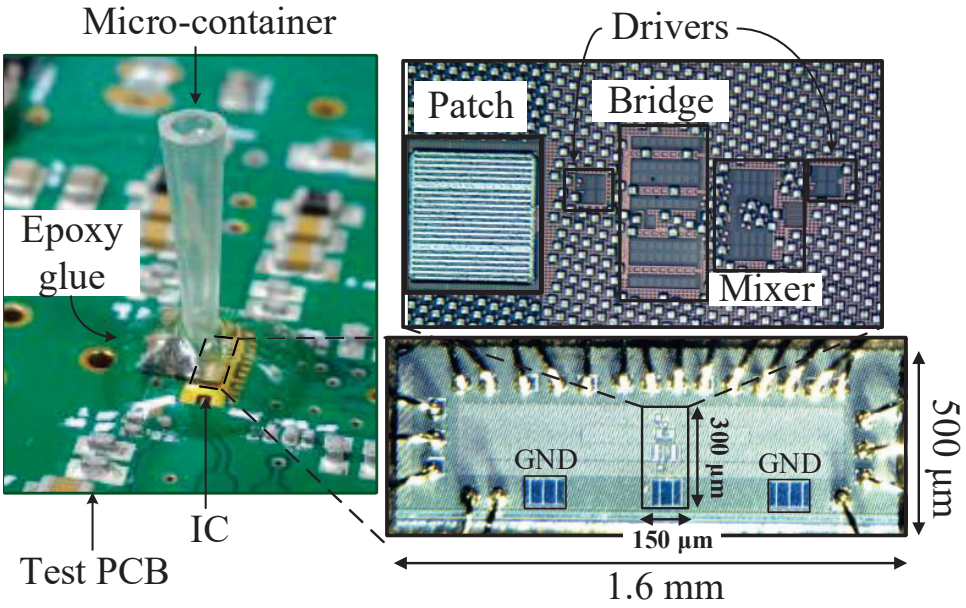


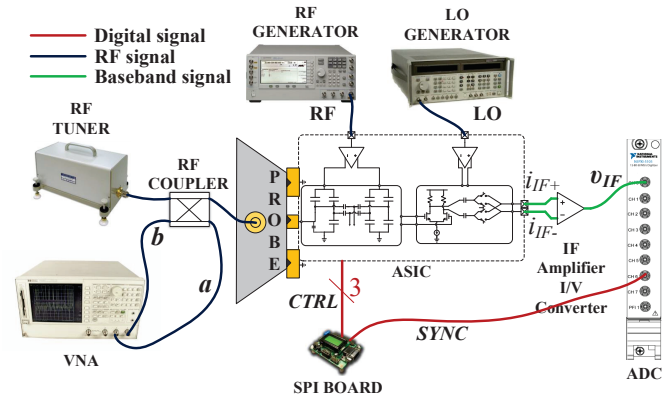
Figure 4.1: Photographs of the fabricated prototype chip and its PCB packaging to measure the complex permittivity of liquid materials.

4.1. Introduction

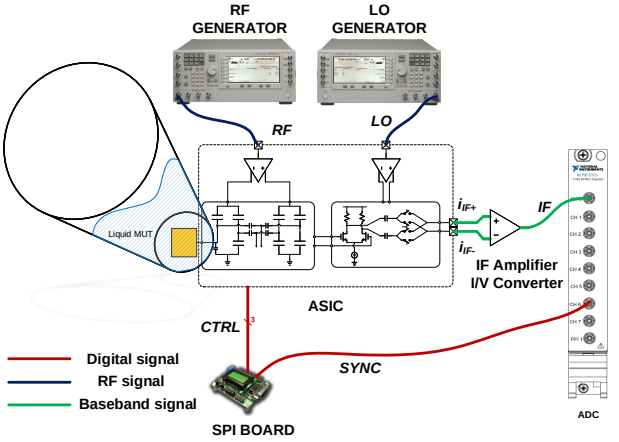
The following sections detail an integrated complex permittivity sensor, prototyped in 40-nm CMOS, which occupies only a sub-mm^2 area, providing fast data acquisition. The proposed sensor features a single-ended patch sensing element embedded in a fully differential double-balanced RF-driven impedance bridge. A multi-harmonic measurement scheme is employed to extend the frequency range and increase the effective measurement speed. In this chapter, we propose a calibration procedure based on the RF bridge analysis presented earlier. Moreover, the noise sources that contribute to the system precision limit are identified, and their contribution is quantified. Independent measurements with the sensing pixel loaded by a probe offering a known termination are used to validate the bridge transfer characteristic. Furthermore, statistical data of material measurements have been collected to evaluate the permittivity precision of the sensor when using the fundamental, third and fifth harmonic to acquire the data.

4.2. Fabricated prototype and experimental setup

The BDS sensor has been fabricated in a 7-metal, 40-nm CMOS process featuring an ultra-thick top metal option, which was utilized to implement the patch sensing element. Such an advanced technology node allows an extensive frequency range. Still, it does not offer any significant area savings over older CMOS nodes due to



(a)



(b)

Figure 4.2: Block diagram of chip measurement setups; (a) setup used to verify the bridge operation with an RF tuner as load and (b) setup for the measurement of liquid MUTs. The RF, LO, and read-out circuitry control is the same in both the tuner and the liquid material measurement.

the extensive usage of analog circuitry and passive elements. The chip micrograph, the test printed circuit board (PCB), and the packaging used to measure liquids are shown in fig. 4.1. The chip area is $1.6 \times 0.5\ mm^2$ while the active pixel area is $0.15 \times 0.3\ mm^2$, thus suitable for embedding in a sub-mm spatial resolution array. As seen in the zoomed-in micrograph, the active circuitry size is similar to that of the patch, allowing a circuit-under-pad (CUP) approach in follow-up operations. The trade-off of such an approach will be the higher parasitic capacitance of the patch since the ground plane will shift to a higher metal level. The latter approach has been adopted in the array implementation described in chapter 5.

To verify the bridge operation, the sensor pixel can be loaded by a known tunable

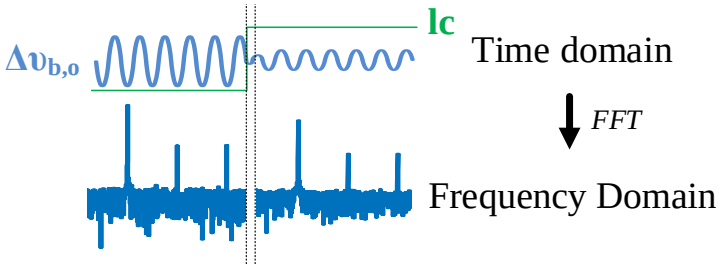


Figure 4.3: Measurement of amplitude and phase from lc signal synchronization.

admittance. For this purpose, two additional ground pads are included in the design so that the engine patch is embedded in a G-S-G configuration and can be interfaced with by a probe.

The chip was mounted and wire-bonded on a test PCB. Characterization of liquid materials is enabled by placing a 15-nL micro-container with a 500-μm bottom opening on top of the chip so that it encloses the patch. The rest of the chip was covered by epoxy glue to protect the bondwires (see fig. 4.1). Cross-contamination among experiments was avoided by washing the container with ethanol and drying with pressurized air between every measurement. To prevent the formation of air bubbles, the liquid MUT was injected slowly into the micro-container by pointing a micro-needle towards the container walls. For the same purpose, the liquid was slightly stirred, and the needle was carefully removed.

Fig. 4.2 shows the two measurement setups for the characterization of the chip: Load measurements for bridge verification in Fig. 4.2a and liquid material permittivity measurement in Fig. 4.2b. In both setups, external generators provide the RF (Agilent E8257D) and LO (HP 8657A) signals. Since the RF generator's close-in noise is critical in achieving low noise at the permittivity sensor readout, the highest quality generator available is used for the RF signal. An intermediate frequency of 150 kHz was deemed high enough to stay above the 1/f corner frequency of the mixer. A high-precision IF transimpedance amplifier (AD 624ADZ), with a gain of 10 kΩ, converts the output differential current ($i_{IF+} - i_{IF-}$) to a single-ended voltage (v_{IF}). An external 12-bit, 60MS/s ADC (NI-5105) with an adjustable conversion gain of 0–40 dB digitizes the voltage output. The ADC quantization noise does not contribute significantly to the overall measured noise. An external controller, implemented on a PCB, provides the required digital controls to the chip, i.e., the branch capacitance setting b and the lc bit control for ratio-metric measurement. The lc signal is also used for the synchronization of the ADC.

The readout signal acquisition procedure is depicted in fig. 4.3; A trace of 1 ms is acquired at each measurement, corresponding to a frequency resolution bandwidth (Δf) of 1 kHz. The digitized data are transferred to a PC, where the FFT is performed, the corresponding amplitude and phase at IF are calculated, and the calibration procedure is carried out.

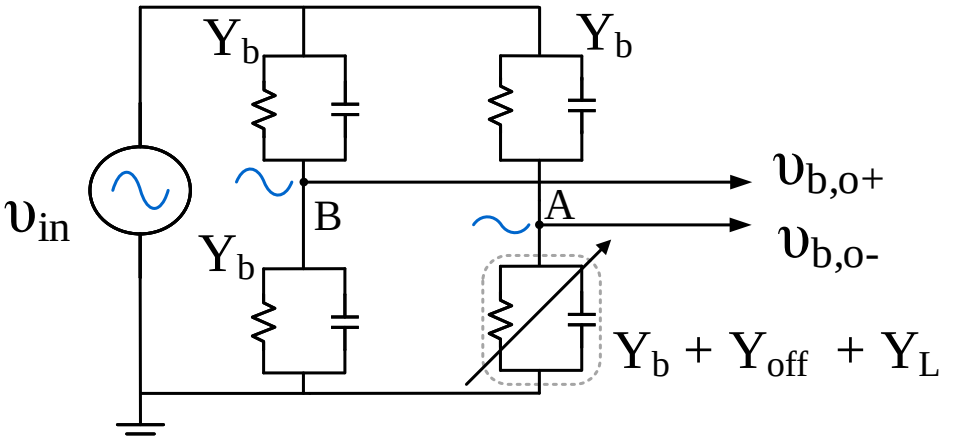


Figure 4.4: RF bridge equivalent schematic for calibration.

4.3. System calibration

As discussed in section 2.4.1 and formulated in the bridge equations (2.14) and (2.15), the real and imaginary parts of the inverse bridge differential output are linear combinations of the weighted load conductance and susceptance. This result allows us to perform a *linear fitting* procedure for calibration. The benefit of such an approach is that it theoretically requires a minimum number of only two known loads, assuming that no systematic or random errors are induced by the calibration materials or measurement noise. In practice, however, more calibration points will help to average out such errors. In any case, a linear output expression alleviates errors induced by approximating (2.11) to a Taylor polynomial expansion of a particular order, bounded by the available number of calibration materials.

Equations (2.14) and (2.15) hold under the assumption that the bridge is perfectly balanced to the baseline load admittance, i.e., in the middle of the measured load range. In practice, however, due to the asymmetric nature of the patch node (A in fig. 4.4) to the rest of the bridge and the finite quality factor of the switched branch capacitors, it is impractical to ensure such a condition. Assuming that Y_A is the admittance of node A to ground, a generic approach would be to assume that $Y_A = Y_b + Y_{off} + Y_L$, where $Y_{off} = G_{off} + j\omega C_{off}$ indicates how much load should be added at the patch node so that the bridge is balanced to the baseline load admittance. Being a fictional admittance, Y_{off} can assume both positive and negative values. The unbalance of the bridge can be defined as $\Delta Y = Y_{off} + Y_L$. Assuming a linear behavior of the circuitry following the bridge, we can use the result of (2.14) and (2.15) and formulate the calibration equations about the measured chip output quantity out:

$$\Re\left\{\frac{1}{out}\right\} = K_R + K_{GR} \cdot \Delta G_w + K_{CR} \cdot \Delta C_w \tag{4.1}$$

and

$$\Im\left\{\frac{1}{out}\right\} = K_I + K_{GI}\cdot\Delta G_w + K_{CI}\cdot\Delta C_w \tag{4.2}$$

where $\Delta G_w = \Delta G/|\Delta Y|^2$, $\Delta C_w = \Delta C/|\Delta Y|^2$ are the imbalance weighted loads and K_R, K_{GR}, K_{CR}, K_I, K_{GI}, K_{CI} are real-valued numbers, further referred to as the K coefficients. A calibration operation would estimate these coefficients as well as Y_{off}. Provided they are available, the sensor load Y_L can be estimated by observing the respective chip output out_m. More specifically, by solving the system of (4.1) and (4.2) the measured weighted load values are acquired:

$$\Delta G_{w,m} = \frac{\hat{K}_{CI}\left(\Re\left\{1/out_m\right\} - \hat{K}_R\right) - \hat{K}_{CR}\left(\Im\left\{1/out_m\right\} - \hat{K}_I\right)}{\hat{K}_{CI}\hat{K}_{GR} - \hat{K}_{CR}\hat{K}_{GI}} \tag{4.3}$$

$$\Delta G_{w,m} = \frac{\hat{K}_{GI}\left(\Re\left\{1/out_m\right\} - \hat{K}_R\right) - \hat{K}_{GR}\left(\Im\left\{1/out_m\right\} - \hat{K}_I\right)}{\hat{K}_{CI}\hat{K}_{GR} - \hat{K}_{CR}\hat{K}_{GI}} \tag{4.4}$$

From the definition of the weighted loads, we get

$$\Delta G_m = \frac{\Delta G_{w,m}}{\Delta G_{w,m}^2 + \omega^2\Delta C_{w,m}^2} \tag{4.5}$$

and

$$\Delta C_m = \frac{\Delta C_{w,m}}{\Delta G_{w,m}^2 + \omega^2\Delta C_{w,m}^2}. \tag{4.6}$$

from which, the measured load is calculated as $\hat{Y}_{L,m} = \Delta Y_m - \hat{Y}_{off}$.

Although approximate values of Y_{off} and the K coefficients can be estimated during the design process, their exact value remains unknown due to fabrication tolerances and modeling or simulation inaccuracies. To determine these values, a calibration procedure can be defined as follows:

- Measure the sensor output at a set of known load values $\mathbf{Y_{L,cal}}$
- Search for the combination of K coefficients and Y_{off} that achieve the best linear fit of $\Delta C_{L,m}$ and $\Delta G_{L,m}$ versus inverse output, according to (4.1) and (4.2), using the adjusted R^2 as a goodness-of-fit figure of merit.
- Store the combination of Y_{off} and K coefficients as the corresponding calibration parameters of the chip.

Note that the calibration coefficients are frequency specific since both Y and Y_{off} are frequency-dependent (see fig. 3.3). Moreover, even with the presence of mismatch among the branch admittances of the bridge, the calibration procedure still holds because there always exists a Y_{off} such that linear equations (4.1) and (4.2) still hold. Therefore, minimizing mismatch during the design procedure is not a strict requirement if Y_{off} is found through a search algorithm. An analysis of the bridge behavior in the presence of mismatch and proof that the mismatch effect is absorbed by the calibration procedure is provided in appendix A.

4.4. Experimental results

4.4.1. Load measurements

For a more dedicated verification of the bridge operation and the calibration procedure described in sections 2.4 and 4.3, respectively, the patch was contacted by a probe (Cascade Z40-V-GSG-500) to a digitally-controlled RF tuner (Maury MT982E), such that any loading of the bridge with various RF admittances is possible. As shown in the experimental setup diagram of fig. 4.2a, the patch is interfaced to the tuner by directly probing the former and connecting the probe to the tuner through the forward path of a low-loss bi-directional RF coupler (Mini-circuits GDC35-93HP+). The coupling ports of the coupler are connected to a VNA (HP 8753D) for on-the-fly measurement of the forward (a) and reflected wave (b) to allow for simultaneous measurement of the actual load admittance by the reference instrument. Calibration of the VNA is performed using an SOL wafer calibration kit of the probe while the source is driving the termination port of the RF tuner. The VNA power is turned off during measurement, and only the a and b waves are measured. Inverting the measured reflection coefficient ($\Gamma = b/a$) provides the calibrated Γ of the measured load; therefore, its admittance Y_L can be calculated and expressed as a parallel combination of a capacitance C_L and a resistance R_L. This procedure is identical to the one used in load- and source-pull measurement systems to measure the load or source admittance [3]. The RF measurement frequency of this experiment was 1 GHz.

At 960 discrete tuner position settings, the bridge load was varied between 53.5 fF and 920.2 fF and the resistance between 540 Ω (1.85 mS) and 988 Ω (1.01 mS). Therefore, the baseline admittance value of the bridge is a 486.7-fF capacitor in parallel to a 764-Ω resistance (1.31 mS conductance). These loading conditions are similar to what is expected for the permittivity of interest. The calibration coefficients are calculated as described in 4.3, for the two bridge settings of $b = 1$ and $b = 8$. Fig. 4.5 shows the calibration surfaces, as defined by (4.1) and (4.2), for these two bridge settings, with the annotated measurement points. The measured data are fitted to the calibration surface with an adjusted R^2 always better than 99.97% and an rms error less than 0.94%.

As already mentioned, apart from the K coefficients of the calibration surfaces, an offset admittance Y_{off} is always associated with the calibration procedure to denote the deviation of the load baseline value from the bridge balance. The offset admittance that maximizes the calibration surface fit (adjusted R^2) to the materials is $27.3\ fF||0.15\ mS$ for $b = 1$ and $752\ fF||-1.35\ mS$ for $b = 8$. The difference of offset capacitance between these two settings is $724.7\ fF$, which agrees well with the simulated branch capacitance difference of $693.5\ fF$ from the simulations (see section 2.4). On the other hand, the conductance difference is $1.5\ mS$, as opposed to the simulated value of $0.14mS$, which indicates an inaccurate model of the switched capacitor losses at this frequency. Nevertheless, the low offset values for $b = 1$ indicate that the bridge can be close to the balanced state for the range of loads used.

The inverse calibration procedure is followed to extract the load capacitance

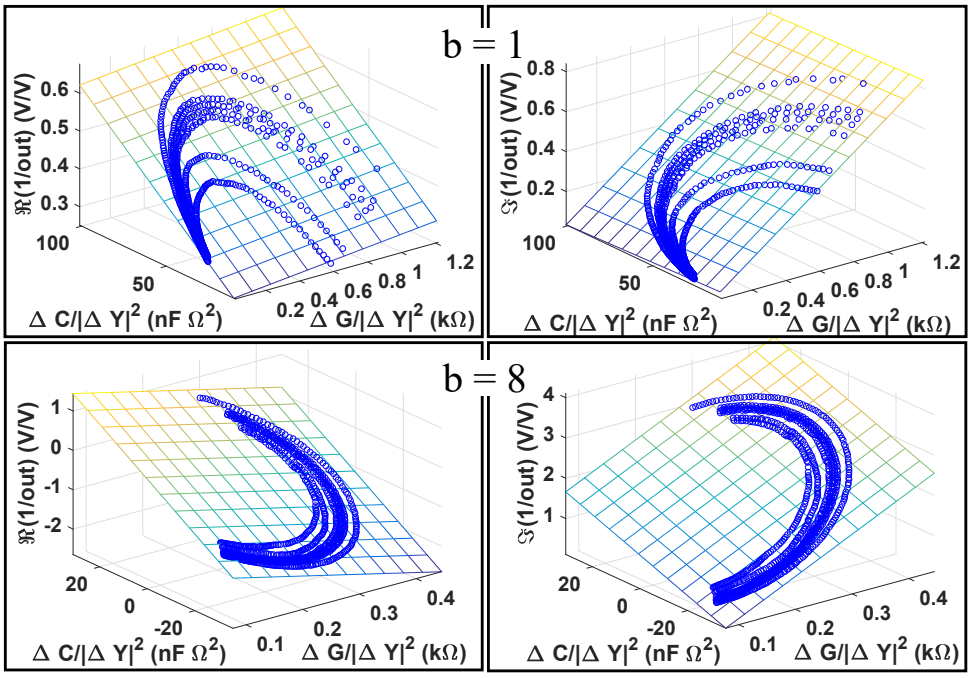


Figure 4.5: Calibration surfaces acquired from all admittance measurements, showing a linear dependence of the real and imaginary part of the inverse output to the normalized admittance and conductance, as suggested by eq. 2.14 and 2.15.

and resistance measured by the chip to validate the calibration. fig. 4.6 shows the capacitance and resistance values measured by the chip and the VNA for $b = 1$. A good agreement between the load calculation from the chip and the VNA is generally observed, with the resistance calculation from the chip being noisier than the capacitance calculation. This is an expected result since the system is more optimized for capacitive, low-loss loads compared to the ones presented by the tuner. The rms capacitance error between the VNA and chip measurements is $1.63\ fF$ while the resistance error is 20.7 Ω. For $b = 8$, the errors are 2.24 fF and 10 Ω, respectively.

4.4.2. Material permittivity measurements

Six liquid materials were available for permittivity measurement: de-ionized water, methanol, ethanol, 2-propanol (IPA), 1-butanol, and air. Except for air, which we assume to be a lossless dielectric with a unity relative permittivity at all frequencies, all other materials exhibit a frequency-dependent permittivity, described by their unique Debye model parameters [4]. Fig. 1.2 shows the permittivity profile versus the frequency of the utilized materials. All materials except ethanol are used for the calibration of the chip. Ethanol was chosen as the independent measurement material because its permittivity is in-between all the available material permittivities

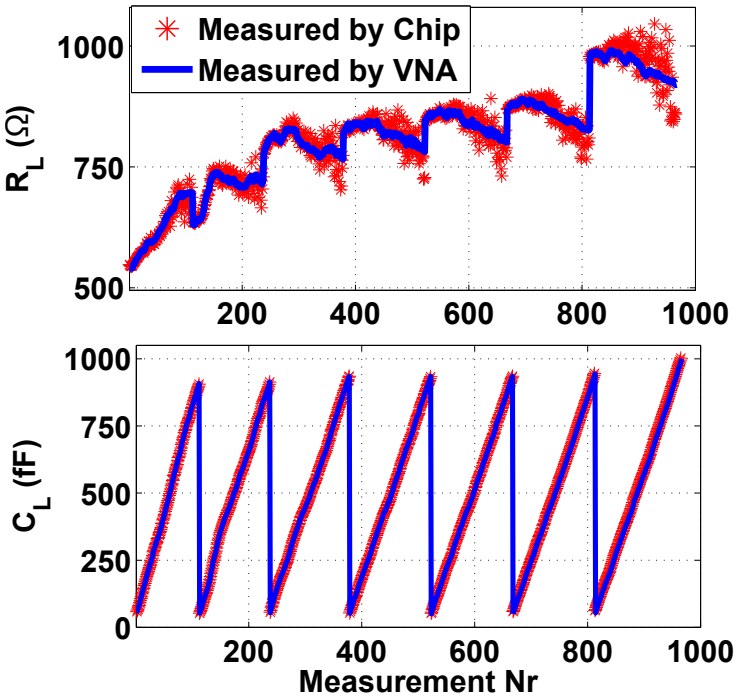


Figure 4.6: Measured load shunt capacitance and resistance for 960 different tuner settings at $b = 1$.

for most of the frequency range.

For all available materials, 100 measurements, each with a duration of 1-ms, are acquired, for every available value of b (from 0 to 8), at different RF fundamental frequencies, covering 0.1-5 GHz. The third and fifth harmonic could also be measured, as described in 3.2, achieving a meaningful signal at an overall frequency range of 0.1-10 GHz. The chip power consumption from a 1.1-V supply was measured between 1.2 mW at 0.1 GHz and 24 mW at 5 GHz. This increase is caused due to the inverter-based topology of the bridge and LO driver. As such, their power consumption varies linearly with frequency.

Translation from a permittivity to an admittance value and vice-versa is performed using the rational function model for the patch, introduced in 2.4 of section 2.2. Subsequently, the established calibration procedure is followed at each frequency and b setting. An average of all 100 measurements is used for the calibration to reduce the random statistical variation of the measurements. Fig. 4.7 shows the calibration material measurements at 1 GHz, located on the calibration surfaces.

Since white Gaussian random noise sources generate the permittivity read-out noise, we can also assume a Gaussian distribution of the permittivity measurement variation. Therefore, to assess the permittivity precision of the independent material (ethanol), the standard deviation (σ) of 100 consecutive permittivity mea-

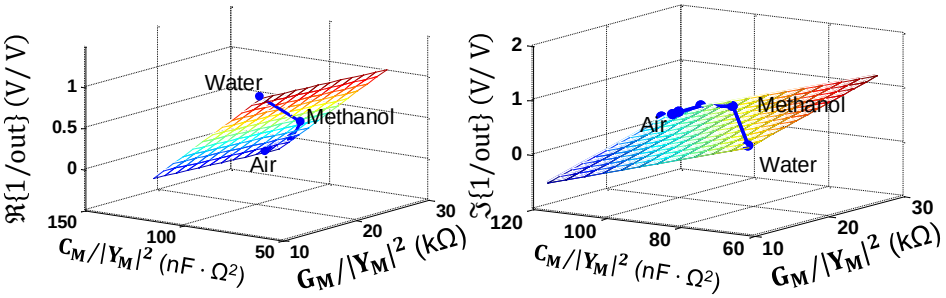


Figure 4.7: Calibration surfaces acquired from the measurements of different liquids, showing a linear dependence of the inverse output real and imaginary part to the normalized admittance and conductance.

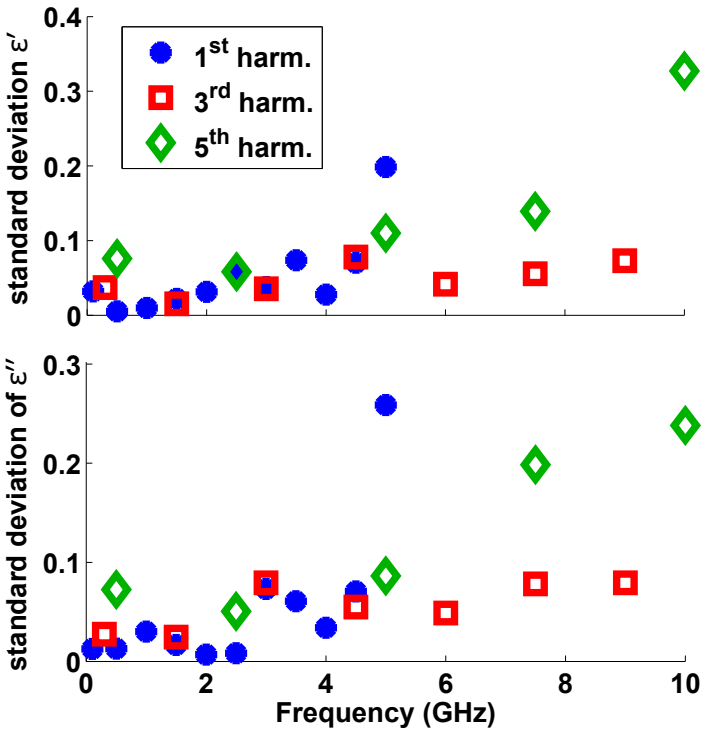
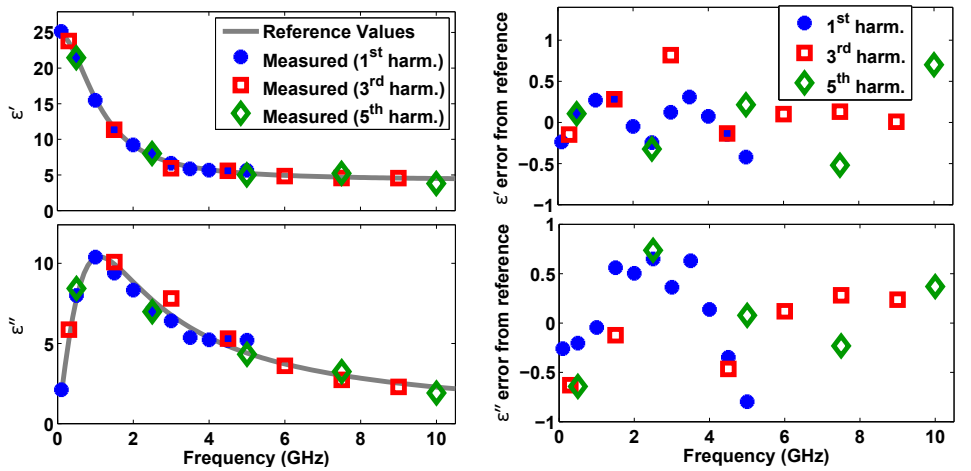


Figure 4.8: Measured permittivity precision of ethanol using first, third, and fifth frequency harmonics.

surements is examined. This value is a metric of the system precision and indicates the minimum resolvable permittivity difference at the resolution bandwidth that corresponds to each of the individual 1-ms measurements.



(a) (b)

Figure 4.9: (a) Independent measurement of ethanol permittivity versus frequency. The Debye model of ethanol is shown as a reference value. (b) Error between the measured permittivity of ethanol and the values corresponding to its Debye model.

Measurement Noise

The variance of the measured amplitude and phase versus chip output at 1 GHz is shown in Fig. 4.10. In the same plot, the predicted Cramér-Rao measurement bounds of (2.26) and (2.27), analyzed in section 2.4.3 , are annotated. It is observed that the measurement variances are concentrated on or above the bound. An excellent agreement between prediction and measurement is seen in the output phase, which, as predicted by (2.27), does not depend on the bridge imbalance. On the contrary, a larger bridge imbalance affects the amplitude variance, as expected by (2.26). The discrepancy of some measurement points from their lower bound is likely due to the sensitivity of the measurement amplitude to short-term variations of supply voltage or other measurement conditions that happen within the measurement time of 1 ms.

Calibrated permittivity accuracy and precision

Fig. 4.11 shows how permittivity precision varies with the bridge controllable capacitance setting b when measuring ethanol at 1 GHz. As expected from the analysis of section 2.4.3, and the simulations of section 2.4.4, the precision worsens when the bridge is unbalanced and improves when it is close to the balanced state. An excellent agreement is also observed between the measured and theoretical precision corresponding to the Cramér-Rao bound, which was extracted by passing the measurement values through a system model including the simulated chip parameters, as presented in section 2.4.4. This limit is shown as a dashed line in fig. 4.11.

The improvement of precision when the bridge is in its most optimal state is

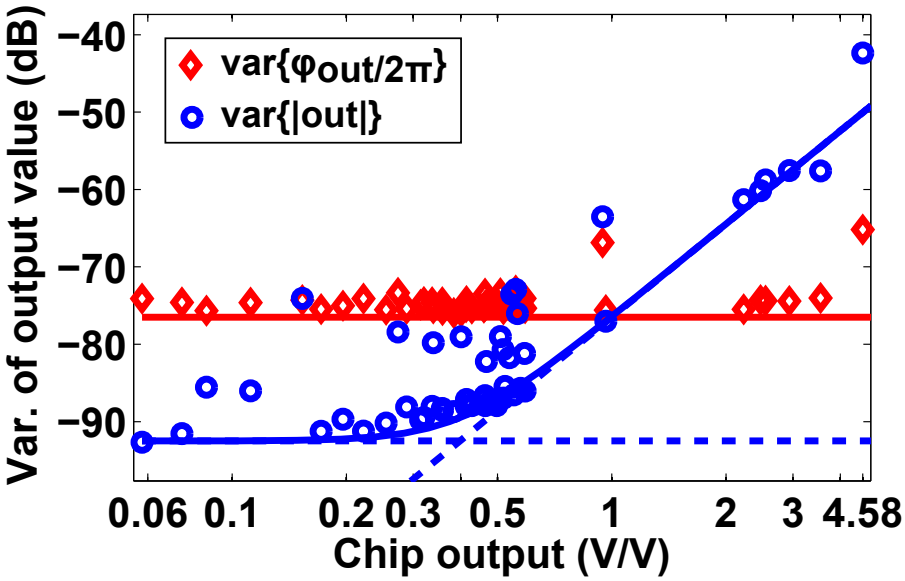


Figure 4.10: Output phase and amplitude variance versus chip ratiometric output value for all measured materials and all bridge capacitance settings (varying bridge imbalance) at 1GHz, with annotated expected Cramér-Rao measurement bounds of (2.26) and (2.27). $\Delta f = 1\ kHz$, $IPN = -90\ dBc$, $NF = 7.5\ dB$, $CG = 30\ dB$ (off-chip amplification included).

demonstrated in fig. 4.12, where 100 repeated measurements are performed for a totally unbalanced versus a balanced bridge (i.e., bridge admittance closely matches material equivalent admittance) at 1 GHz. It is observed that the real part measurement standard deviation is improved by 70% (0.014 versus 0.054) and the imaginary part by 95% (0.0013 versus 0.034), highlighting the importance of balancing the bridge to perform a highly repeatable and sensitive measurement. A practical example of this feature in real-life scenarios would be to balance the bridge on background tissue before initiating tumor mapping.

It was found that the bridge balances best for ethanol at $b = 2$ below 5 GHz and at $b = 1$ above that frequency. Fig. 4.8 shows the measured permittivity precision of ethanol for these capacitance settings versus frequency, demonstrating measurements at the first, third, and fifth harmonic. Owing to the worse noise figure at the higher harmonics, the precision at the first harmonic point of each measurement is always better than that at the third harmonic, which, in turn, is always better than that at the fifth. The measured precision also follows the generator's integrated phase noise profile versus frequency; therefore, it worsens at higher frequencies. Over the frequency range of 0.1–10 GHz, the permittivity precision always stays below 0.4 and 0.3 for the real and imaginary parts, respectively.

As has been discussed, the achieved permittivity precision is bounded by external phase noise sources and short-term supply variations that cannot be correlated

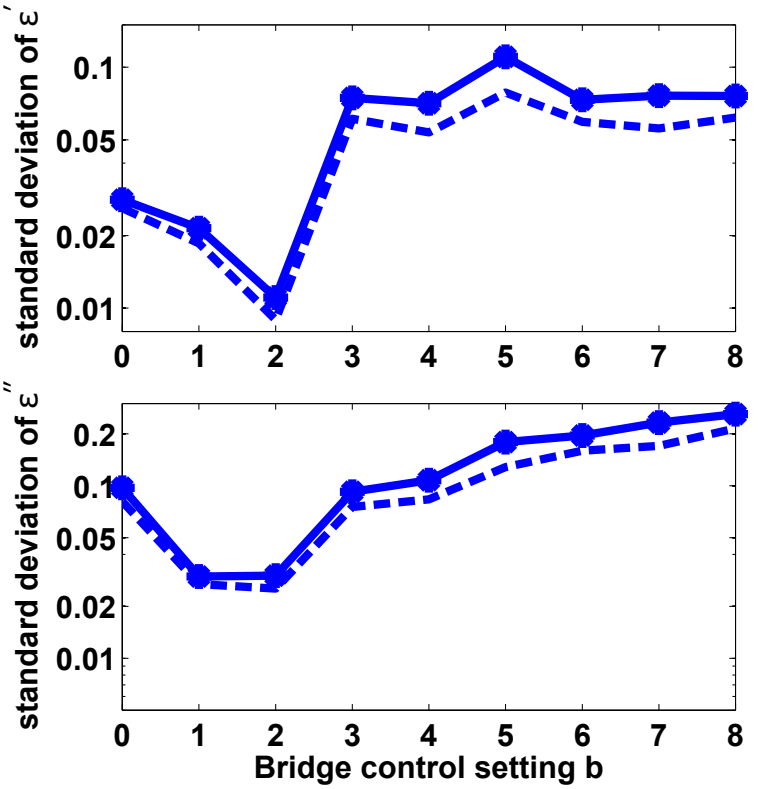


Figure 4.11: Permittivity precision versus bridge control setting b, for ethanol measurement at 1 GHz (solid line). The dashed line corresponds to the expected precision if the phase and amplitude variance were equal to the Cramér-Rao bound.

due to the time-division measurement of the reference load. These effects can be mitigated in a future pixel array implementation by including a reference pixel to be read out simultaneously with the pixel of interest in a parallel measurement path (see chapter 5). Thus, global external noise sources and supply variations can be canceled out by the ratio-metric measurement. This modification appears desirable but might not yield the desired performance improvement for the intended final BDS system implementation, namely, a fully integrated solution that includes on-chip RF generators. The latter is expected to suffer from a much worse phase noise than a BDS system featuring high-end external synthesizers, limiting the achievable precision.

Using bridge settings that minimized the bridge imbalance, ethanol's average measured permittivity values were acquired and plotted versus frequency in fig. 4.9a. The error between measurement and reference numbers, indicated in fig. 4.9b, stays below 1, with an rms value of 0.32 and 0.48 for the real and imaginary parts, respectively. The random distribution of the error versus frequency or harmonic re-

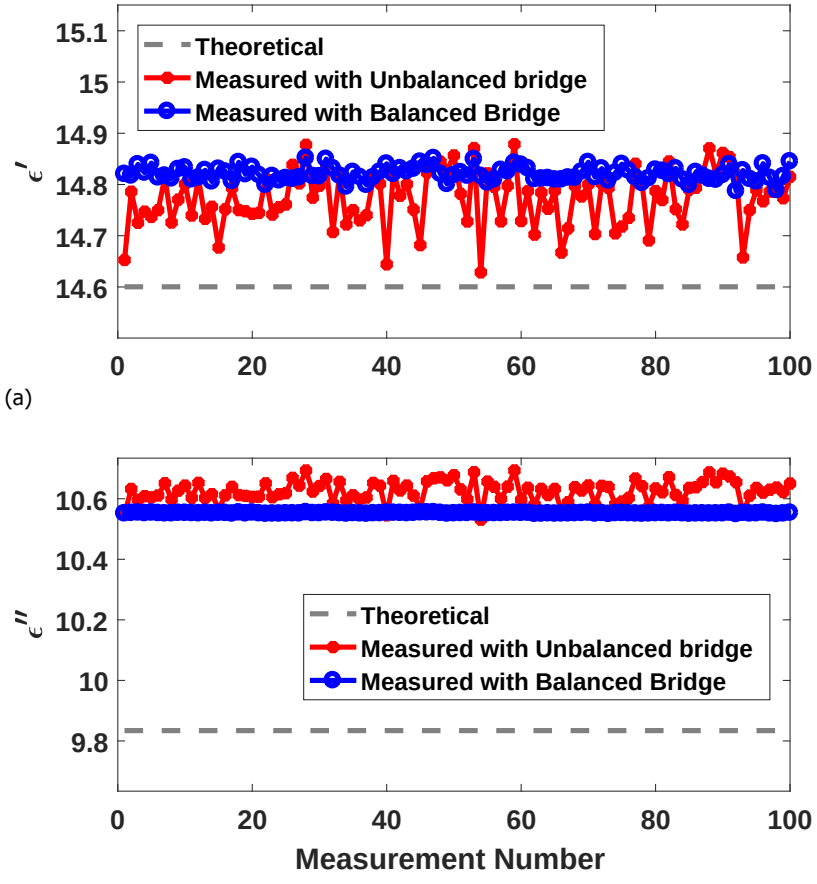


Figure 4.12: Repeated measurements of Ethanol at 1 GHz, showing the reduced readout variation for the balanced bridge case (blue trace) versus an imbalanced case (red trace, for both real and imaginary permittivity values.

sults in cases where the third and fifth harmonic measurement has lower error than the first. This indicates that the accuracy errors are rather due to inaccuracy of the calibration materials, the patch model, and the calibration fitting than a statistical error associated with noise, as is the case for the measured precision.

Debye Model Estimation

To demonstrate the effectiveness of the permittivity sensor in characterizing the MUT and highlight the benefits of a wide measurement bandwidth and complex permittivity readout capability, a nonlinear fitting is performed on the measured data to extract the parameters of ethanol's Debye model:

Table 4.1: Comparison of debye model parameter estimation accuracy for different sensor measurement cases

	Measurement case	ϵ_0	ϵ_0 error	ϵ_∞	ϵ_∞ error	λ	λ error	Meas. time	Meas. energy
1	Full frequency dataset, only ϵ'	4.2179	*0.99%*	25.2227	*0.61%*	0.2745	***1.6%***	24.2 ms	300 μJ
2	Full frequency dataset, both ϵ' and ϵ''	4.3613	*1.32%*	25.251	*0.72%*	0.2829	***4.7%***		
3	First harmonic, only ϵ'	4.4775	***5.1%***	25.2827	*0.63%*	0.2823	*4.48%*		
4	First harmonic, both ϵ' and ϵ''	4.5193	***6.09%***	25.211	*0.56%*	0.2827	*4.62%*		
5	Single meas. (1,3,5 GHz), only ϵ'	4.4888	*5.4%*	63.9	***155%***	0.6293	*133%*	2.2 ms	11.8 μJ
6	Single meas. (1,3,5 GHz), both ϵ' and ϵ''	4.0368	***5.24%***	24.918	*0.61%*	0.2814	*4.15%*		

$$\epsilon = \epsilon' - i\epsilon'' = \epsilon_0 + \frac{\epsilon_\infty - \epsilon_0}{1 + (i\lambda f/c)}, \tag{4.7}$$

where ϵ_∞, ϵ_0, and λ are the Debye model parameters, f the measurement frequency, and c the speed of light in vacuum [4].

Table 4.1 presents the estimated parameters and the related estimation error in several test cases. Fundamental frequency varies from 0.1 GHz to 5 GHz, with 0.5 GHz step between 0.5 GHz and 5 GHz (11 points in total). All measurements are performed at a speed of 2.2 ms per measurement, producing three frequency points for fundamental frequencies below 2 GHz and two frequency points below 3 GHz. The measured power consumption of the chip is between 1.2 mW at 0.1 GHz and 24 mW at 5 GHz, owning to the hard-clipping multi-harmonic design of the RF and LO buffers that increase power consumption linearly with frequency. The energy per measurement can be calculated by combining the consumption information with the measurement time for each scenario. It can be seen that using the full frequency range and only the real part of permittivity (case 1) provides the lowest possible error of estimated parameters, even significantly lower than using both real and imaginary parts of permittivity for estimation (case 2). This observation could mistakenly lead to the conclusion that imaginary part estimation is more erroneous and even unnecessary, given the fact that a material can be only estimated from ϵ', and that ϵ'' can be extracted therefrom [5, 6]. The same trend holds when using only the first harmonic, thus a reduced frequency dataset, although the error difference between cases 3 and 4 of Table 4.1 is not very significant. Moreover, it is clear that using third and fifth harmonics leads to improved estimation for the same measurement time and energy (cases 1 versus 3).

However, the importance of utilizing both ϵ' and ϵ'' for material estimation, rather than only the former, is becoming significant in a scenario that requires fast or ultra-low energy readout (e.g., in real-time 2D scanning or wearables). In these cases, only one measurement can be acquired at 1 GHz, resulting in permittivity measurement at three frequency points (1, 3, and 5 GHz) owning to the multi-harmonic down-conversion scheme. Using here only ϵ' yields a failure in estimating the material characteristics (errors more than 100% observed in case 5), while also utilizing the information of ϵ'' brings the accuracy to much more acceptable levels, highlighting the practical importance of complex permittivity sensing architectures in real-life biomedical devices.

Table 4.2: Comparison of implemented sensing pixel with state-of-the-art cmos integrated permittivity sensors

	CMOS node	Sensing element	Architecture	Operating frequency (GHz)	Permittivity range	Permittivity accuracy	Permittivity precision (σ)	Mes. time	Power (mW)	Area [Active] (mm^2)
This work	40 nm	Single-ended patch	Multi-harm. IF down-conversion	0.1–10	ϵ': 1 – 80 ϵ'': 0 – 40	$\epsilon' < 1$ $\epsilon'' < 1$	$\epsilon' < 0.4$ $\epsilon'' < 0.3$	1 ms	1.2–24	1.6×0.5 [0.15×0.3]
[7] JSSCC'12	90 nm	Differential capacitor	LC VCO	7–9	ϵ': 2.4 – 20.2	N/A	$\epsilon' <1^*$ (@8 GHz)	N/A	16.5	2.5×2.5 [1.5×2.2]†
[8] IMS'13	65 nm	CPW t-line	IF down-conversion	1–50	ϵ': 4 – 5 ϵ'': 1 – 4	N/A	$\lvert\epsilon\rvert$: 0.0445* (@20 GHz)	20 ms	114	N/A [0.6×2]
[9] T-MTT'13	90 nm	Differential capacitor	LC Frac-N PLL	10.4	ϵ': 1 – 8	$\epsilon' <0.1^*$	N/A	N/A	22	1.7×1.3 [0.9×0.9]†
[10] JSSCC'14	0.35 μm	Off-chip μ-strip line	Super-heterodyne	0.05–3	ϵ': 1 – 48	$\epsilon' <0.6^*$	N/A	1 ms	4–9	3×3 [0.9×2.5]†
[11] T-MTT'14	0.18 μm	Differential capacitor	Zero-IF	0.62–10	ϵ': 1 – 40 ϵ'': 0 – 20	$\epsilon' <0.7^\ddagger$ $\epsilon'' <0.1^\ddagger$	N/A	>10 ms	65–72	3×3 [0.9×2.3]†
[12] TCAS-I'15	0.18 μm	Differential capacitor	RO Int.-N PLL & ALL	0.7–6	ϵ': 1 – 80 ϵ'': 0 – 40	$\epsilon' <1.75^*$ $\epsilon'' <0.7^*$	N/A	1 s	69–140	2.5×2.5 [0.9×1.3]†
[13] T-BioCAS'15	0.35 μm	Off-chip 3D capacitor	Zero-IF	0.009-2.4	ϵ': 1 – 94 ϵ'': 0 – 465	$\epsilon' <0.5^*$ $\epsilon'' <1^*$	N/A	N/A	61–94	3.3×3.3 [2.5×2.5]†
[14] JSSC'16	65 nm	Differential capacitor	Injection-locked VCOs	6.5/11/ 17.5/30	ϵ': 1 – 60	N/A	$\epsilon' <0.008^\S$	0.01 ms	65	1.5×1.2†

*Extracted from the reported maximum percentage error and ϵ value at that error

†Estimated from the chip micrograph

‡Estimated from the provided graph

§Extracted from the reported minimum detectable capacitance change and EM-simulated sensor sensitivity versus ϵ'

4.4.3. Comparison with the state of the art

Having presented the implemented sensor characterization results, we can compare them with state-of-the-art CMOS integrated sensors. Table 4.2 summarizes the achieved performance of the sensor along with the results of previously published state-of-the-art implementations. To the best of the authors' knowledge, this work features the smallest active area while achieving fast and precise operation over two decades of bandwidth. Moreover, it measures both real and imaginary parts with the highlighted advantages over spotted-frequency counterparts and implementations measuring only the real part [7, 9, 14].

Compared to previous works, this contribution quantifies both the accuracy and precision of measured permittivity over the operating frequency range. A single-ended patch sensing element approach is followed, which facilitates better EM interfacing with the MUT, as discussed in chapter 2. These properties, along with its compact size, fast readout, and broadband architecture, make it a suitable pixel element for 2-D permittivity-based imaging sensors in biomedical and industrial applications.

4.5. Conclusion

This chapter presented the experimental results of an ultra-compact BDS sensing pixel realized in 40-nm CMOS technology. It is based on the proposed architecture of chapter 3. First, a calibration procedure has been defined, and the experimental setup has been explained. Next, the measurement results have been discussed. The chip functionality was demonstrated by loading the Wheatstone bridge with a

known adjustable load using an RF tuner. Measurements with known liquids were performed to quantify the permittivity accuracy and precision. Measurement noise minimization has been demonstrated by controlling the bridge branch impedance such that a balanced state occurs for the material of interest. Material identification through the extraction of the material Debye parameters is fast and accurate, owing to the system's multi-harmonic downconversion ability and the extraction of both real and imaginary parts of permittivity. The sensor core features record low area with higher measurement speed while offering comparable accuracy to other CMOS permittivity sensors. The proposed architecture's demonstrated capabilities underline its suitability for usage in multi-modal sensing systems such as wearables or to act as a basis for implementing permittivity sensing imaging arrays.

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5

A 5x5 CMOS Permittivity Imaging Array

A 0.14-μm CMOS 2-D permittivity imaging array prototype operating at microwave frequencies is presented. It comprises 25 permittivity-sensing pixels, each consisting of a sensing patch connected to a dedicated RF bridge. A transconductance stage converts the imbalance voltage to a current signal, subsequently downconverted to an intermediate frequency and sampled. The implemented permittivity sensing array shows precise permittivity measurements over a range of 0.1-10 GHz and successfully demonstrates 2-D permittivity contrast imaging with a precision of 0.1 - 2.4 in a frequency range from 0.1 to 10 GHz, when the sensing array is interfaced with various dielectrics. The realized array provides sub-mm spatial resolution, enabling the quick and accurate detection of material transitions.

Parts of this chapter were previously published in [1, 2].

5.1. Introduction

This chapter demonstrates a 5x5 permittivity sensing 2-D array comprising the sensing pixel architecture introduced in chapter 3, whose functionality was evaluated in chapter 4. To the best of the author's knowledge, this demonstrator is the first CMOS microwave permittivity sensing array for the localized detection of permittivity variations in a material. Although various standalone permittivity sensor implementations in CMOS technology have shown accurate permittivity detection at GHz frequencies, existing permittivity sensing arrays have only been demonstrated at frequencies below 100 MHz [3, 4]. Despite the difficulties inherent to a microwave array design, the incentive to move to high-frequency broadband implementations derives from the desire to select the frequency with the highest dielectric contrast, and the improved sensitivity due to the availability of redundant wideband data.

The chapter is organized as follows: First, the array architecture is presented, addressing the compact integration of each pixel, its local readout bridge, and the interconnection of the pixels for readout using a single analog interface. Moreover, flexible array readout options such as phase inversion, pixel addition, and pixel isolation are discussed. Last, experimental results of the implemented demonstrator are presented, and conclusions are drawn.

5.2. System Architecture and Implementation

The permittivity imaging demonstrator was implemented in a low-cost 6-metal CMOS BEOL stack of a 140-nm minimum gate length technology (NXP C14). This technology offers one ultra-thick, low-resistive top metal layer (M6) and five thin metal layers (M1, M2, M3, M4, M5). Although it is challenging to implement high-frequency analog circuits within such a digital-oriented metal stack, it was chosen to demonstrate that the sensor array co-integration with a digital backend and other digitally-intensive systems in SoC configurations without increasing the total cost per area of the die.

Fig. 5.1 shows the floorplan of the implemented imaging array. Patch sensing elements are preferred for the intended permittivity sensing, based on their advantages discussed earlier in section 2.2.1. Two-dimensional (2-D) permittivity imaging is enabled by arranging the sensing elements as image pixels in a 5×5 square matrix.

The active circuits used for the readout of the patch sensing elements are divided into three hierarchical levels, graphically depicted using different colors in Fig. 5.1, namely: the *pixel-level circuitry*, dedicated to one specific patch sensing element, *row-level circuitry*, shared among a five-pixel row or column, and *chip-level circuitry*, representing global, single placement circuits. Note that, for compactness and scalability of the imager, it is essential that the pixel-level circuitry is placed underneath the patch sensing elements. Fig. 5.2 summarizes the circuit-level array architecture with its hierarchical levels, detailed in the following sub-sections.

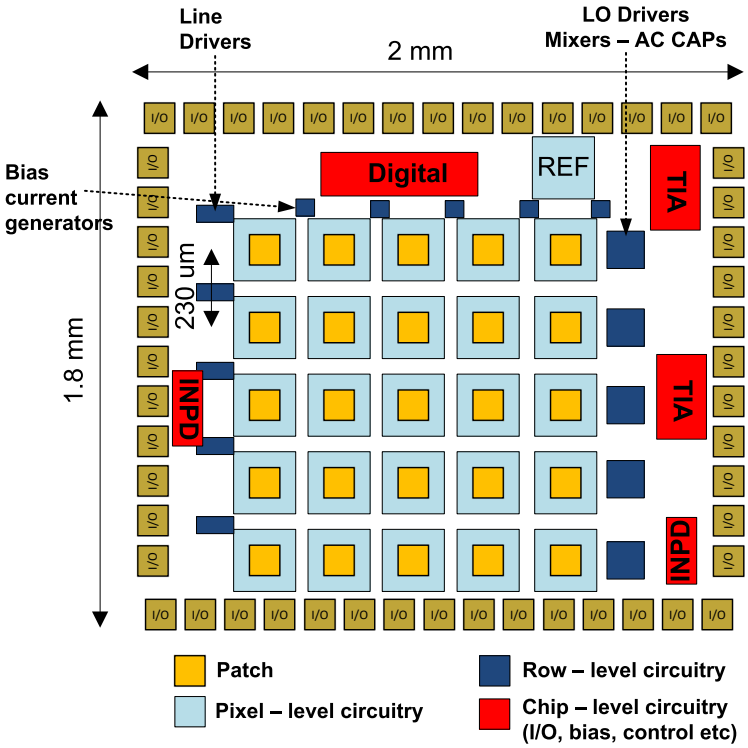


Figure 5.1: Floorplan of the implemented 5×5 permittivity imaging array, depicting the physical placement of individual building blocks and the hierarchical levels.

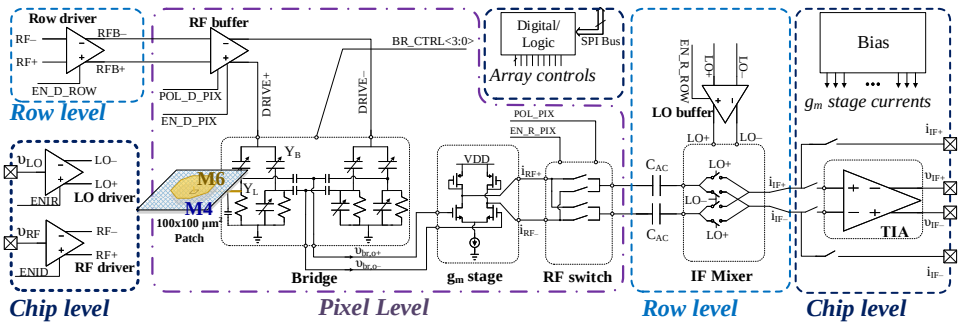


Figure 5.2: Permittivity imager circuit-level architecture.

5.2.1. Patch sensing element

The permittivity-sensing function is carried out by the patch sensing elements placed on the ultra-thick, top metal layer of the CMOS stack (M6). Passivation openings are created above the patches to allow direct contact with the MUT. As discussed

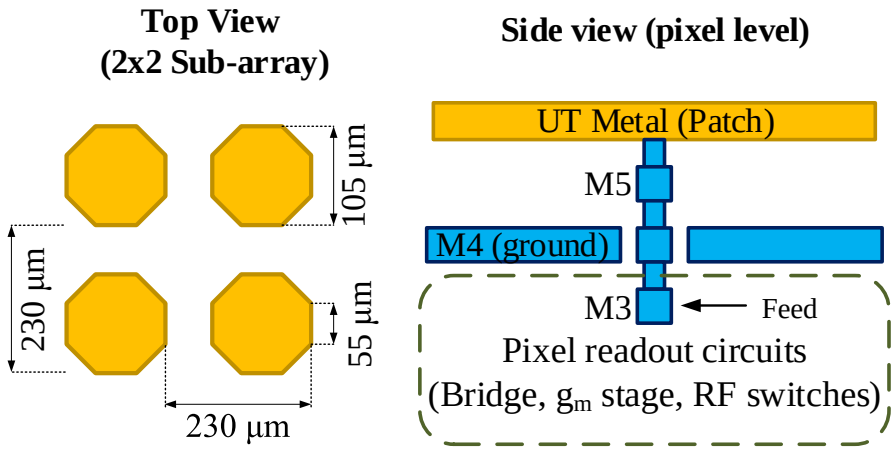


Figure 5.3: Side and top view of the patch within the implemented matrix.

in section 2.2, the patch sensing element presents a permittivity-dependent load admittance Y_L. In a first-order approximation, the real and imaginary parts of admittance depend on the real and imaginary part of the permittivity ($\varepsilon^* = \varepsilon' - j\varepsilon''$). The underlying relation is extracted from EM simulations using Keysight EM Pro. The implementation details of the patch sensing element and their arrangement in the 5x5 matrix are shown in Fig. 5.3. During the design phase of this array implementation, it has been discovered that if it has a circular shape and its feed point is connected at the center of the patch, it will be convenient to model the patch as a patch-loaded coaxial probe using Green's functions [5, 6]. Therefore, contrary to the standalone implementation, the array patches have been implemented as octagons to approximate a circular shape within the technology design rules. Additionally, the octagonal-shape patch has stacked vias to connect it to its feed point in M3, which provides access to the active drive and read circuits. A 230-μm pitch is achieved, set by the dimension of the underlying pixel circuitry and their local supply decoupling capacitors. The patch dimension is 105 μm, which was deemed optimal in terms of offset capacitance, the driving capability of the bridge associated with the patch, the area of coverage, and the minimization of cross-coupling with the neighboring patches.

To allow the placement of active pixel-level circuitry beneath the patch and provide sufficient isolation, M4 is used as a ground plane. The selection of the metal layer used for the ground plane was based on the trade-off between the patch baseline offset capacitance, C_0, and the number of available layers to implement the pixel-level circuitry. Indeed, the baseline capacitance of the patch, when loaded with $\epsilon^\star = 1 - j0$ is $C_0 = 192\ fF$, which is approximately two times higher than using the M1 layer as ground and about 3 times lower compared to using the M5 layer as the ground plane. The slope of the permittivity-to-capacitance translation (see eq. 2.3) is $2\ fF$, which, along with the conductivity of the patch, remains relatively

unchanged with the selection of the ground layer due to the low loss of the oxide used between the metal layers.

5.2.2. Pixel-level circuits

The pixel-level circuits comprise the same architecture detailed in chapter 3 and demonstrated in the standalone pixel of chapter 4: Each patch sensing element is connected to a double-balanced Wheatstone bridge, with a local clipping RF driver buffer to provide the fundamental and higher harmonic content at the bridge drive input. Differential readout is performed employing a dummy bridge to cancel the common-mode signal. As a result, the bridge output voltage is directly linked to the permittivity of the material interfaced with the patch. The bridge branches feature a reconfigurable admittance Y_B, in the form of 4-bit binary-weighted switched-capacitor, providing a 230 fF range with 15 fF steps (140% of the simulated patch range) to allow dynamic tuning of the bridge to the patch admittances ($Y_L \approx Y_B$). Under this condition, the bridge achieves the highest sensitivity to its load, hence permittivity variations. This flexibility allows adjusting the high-sensitivity point of the bridge depending on the MUT's properties.

Moreover, a transconductance (g_m) converts the bridge output voltage signal to an output current. A cascode current source is used to reduce the imbalance of the differential output signal down to 0.6%. The g_m stage provides a transconductance of 7 mA/V when drawing 1 mA of supply current. Its 1 dB compression point is located at an input differential voltage of 320 mV for a 1.8V supply, offering a 24 dB margin from the maximum expected bridge output of 20 mV.

Two additional challenges arise within the array concept. First, it is essential that the pixel-level circuits are placed underneath the patch and made as compact as possible, as their occupied area determines the patch pitch and thus spatial resolution of the imaging array. Even though only three metal layers were available for laying out these circuits, as already demonstrated from chapter 3, the proposed architecture can be made ultra-compact due to the absence of area-consuming passive elements, such as inductors and transformers.

A second challenge is related to the individual readout of each pixel without cross-contamination by signals from other pixels. For this purpose, an RF switch is added to each pixel to select its output current during scanning. Owning to the current-mode output, a simple NMOS switch is sufficient to maintain the path linearity. The NMOS switch ON to OFF resistance ratio (R_{ON}/R_{OFF}) and the g_m stage output impedance allow the simultaneous summation of 5 pixel output currents to reduce readout time. Nevertheless, due to the finite impedance levels involved, switching 5 pixels on simultaneously yields 35% signal loss in simulation compared to a sequential readout, namely, reading out each pixel and adding the signal using post-processing.

Polarity switching is also implemented to steer the pixel signal to an in-phase or inverted-phase version (0 or 180 degrees). This feature adds the functionality of differential readout between individual array pixels. Along with the enable function, polarity control is also implemented in the RF driver of the bridge (Fig. 5.4). This functionality allows experimenting with different field distributions across the

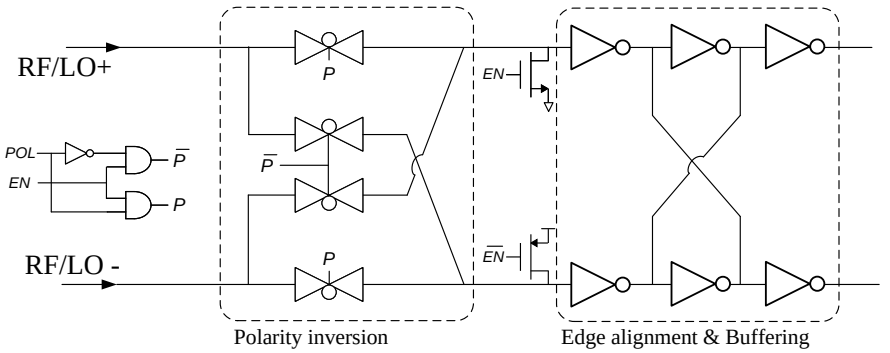


Figure 5.4: RF/LO buffer with enable and polarity option.

patches. During pixel scanning, the buffer of the neighboring pixels can be completely turned off to isolate them from the active pixel. An edge aligner is used at the end of the driver chain to correct for any phase mismatch and apply a high-quality differential signal to the bridge. Even though the adaptive bridge structure can suppress any signal caused by a mismatch in the differential bridge drive (section 2.4.2), minimizing the phase mismatch helps avoid any unwanted large signal excursions at the output of the bridge that would challenge the linearity of the subsequent g_m stage.

5.2.3. Row-level circuits

Each pixel provides an RF output current signal, which is selectively gated through the RF switch within the pixel. The outputs of the pixel belonging in the same row are combined and delivered to a shared current-mode passive IF mixer. Each row mixer has a dedicated LO buffer of the same architecture depicted in Fig. 5.4 to ensure a square-wave drive level that maximizes the conversion gain of the fundamental and subsequent odd harmonics. A row-level driver is also used to drive the drive signal to the five individual pixel RF buffers.

5.2.4. Chip-level circuits and considerations

Since the mixers also output a current signal, the row mixer outputs are time-multiplexed to the overall chip output via an on-chip TIA that converts the IF current to voltage. Note that it is unnecessary to implement extra switches after the row mixers to multiplex their outputs, as the mixer output itself can be set to a high-impedance mode when turned off. A current-mode output option that bypasses the TIA is also selectable for testing purposes.

Because most off-the-shelf instruments or available components for RF signal generation are single-ended, and it was desired to avoid external baluns that increase the BoM, the global RF and LO signals are fed as single-ended inputs to the

chip. The differential RF and LO signals are generated on-chip using active input single-to-differential converters (INPD) instead of passive baluns to save chip area.

The input single-to-differential converters provide the differential rail-to-rail RF and LO signals fed to row-level RF and LO drivers. The RF bridge drive signal is carefully routed to each row driver to minimize phase differences across the pixels since it can limit the array's ability to group sensing elements into coherent driving or differential driving schemes. The maximum phase imbalance of the RF bridge drive signal among pixels of the array was simulated using an EM simulation tool and was found to be: 2.5^o and 13.8^o at 1 GHz and 5 GHz, respectively while, for neighboring pixels, these values are 0.55^o and 3.2^o, respectively.

A reference pixel was added to the array to remove amplitude fluctuations and acquire both the real and imaginary parts of the output voltage. This reference pixel is connected to a fixed load instead of a patch and has its own dedicated readout path while using an identical excitation. In contrast to the standalone implementation of chapter 4, where the same bridge was connected to a fixed load using a time division scheme, in this matrix, the solution of a simultaneously available reference pixel readout was selected to suppress any short-term variations of global chip supply and other noise sources.

An SPI interface is used to communicate to the chip, while digital logic allows independent access to the matrix elements. The pixel control is made such that excitation and readout of pixels can be independently enabled to allow for various reading and driving schemes during material characterization experiments. At the same time, a fast scanning synchronous engine is implemented using the SPI clock to achieve fast sequential pixel readout without the limitations of the SPI interface.

5.3. Experimental results

A 5×5 demonstrator IC, shown in Fig. 5.5 was fabricated in 0.14 μm technology. The chip occupies a total area of 5.75 mm^2 (2.5 $mm \times$ 2.3 mm), with the effective sensor area of 1.15×1.15 mm^2. Together with a small container, the chip was mounted on a PCB for liquid measurements (see Fig. 5.5), while the bonding wires were covered by epoxy glue to isolate them from the MUT. During scanning at 900 MHz operation frequency, the chip draws 153 mW from a 1.8 V supply. Note that this power consumption is quite increased compared to the 6.5 mW/pixel of the standalone 40-nm demonstrator due to a higher supply and slower technology node that required increasing the RF driving buffers size. Moreover, additional buffering is used within the array (chip-level circuitry), and two pixels (active and reference pixel) are activated simultaneously during scanning.

5.3.1. System raw output and calibration

For the initial sensor array functionality evaluation, the uncalibrated system output is first observed. Fig. 5.6 shows the output voltage amplitude of the middle array pixel, normalized to the reference pixel, for all bridge capacitance settings (Y_B) and various materials. As expected, the bridge programmability can provide bridge

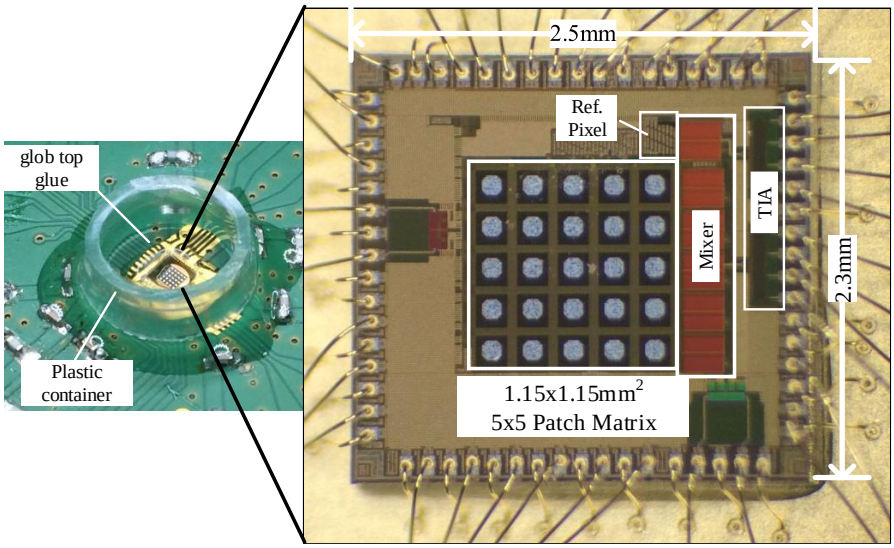


Figure 5.5: Photograph of prototype chip assembly and chip micrograph.

balancing for all materials with a permittivity range from 1 (air) to 80 (water). When air is used on top of the patch, the bridge is balanced for a capacitor setting of 2 ($\approx 190\ fF$), and when water is used, the bridge is balanced with a capacitor setting of 14 ($\approx 380\ fF$). At the same time, we observe that the capacitor setting for which the minimum standard deviation is achieved coincides with the setting for which the bridge is balanced. This result is consistent with the outcomes of the analysis in section 2.4.3.

The system calibration procedure is repeated per pixel, as described in section 4.3, employing air, butanol, 2-propanol, and methanol, and de-ionized water as calibration materials, while ethanol is kept as independent material for accuracy and precision evaluation. Fig. 5.7a shows the raw voltage output, normalized to the reference pixel, versus pixel number when the bridge is normalized to the water permittivity. It is clear that the array pixel location-related artifacts, such as signal, supply, and ground routing resistances, are such that the uncalibrated output cannot be used for imaging purposes. Fig. 5.7b shows that the artifacts are minimized after calibration when ethanol is the independent material. It is seen that calibration allows a consistent readout level for each pixel for the same material.

5.3.2. Material permittivity measurement

The accuracy and precision of the permittivity sensing array for BDS are evaluated by measuring the permittivity versus frequency of ethanol. The averaged measured result across all pixels for 100-measurements, when the bridge is balanced for the

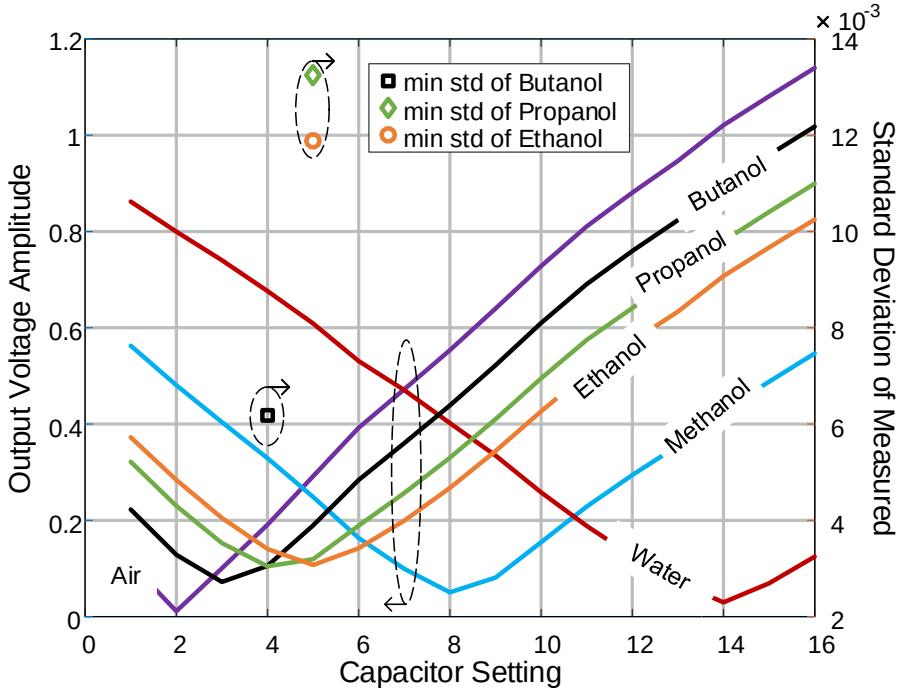
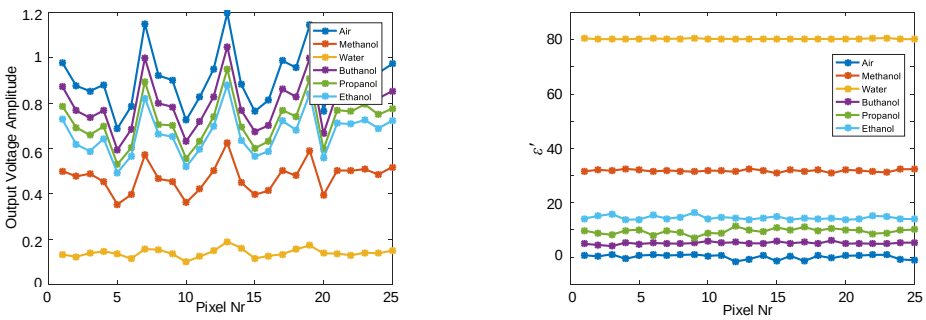


Figure 5.6: Normalized output voltage amplitude of center Pixel (pixel 13) versus capacitor setting for 6 materials at 900 MHz, and the corresponding lowest standard deviation (σ) of chosen independent material.



(a) (b)

Figure 5.7: (a) Raw output voltage amplitude and (b) calibrated ϵ' versus array pixel. Ethanol is used as an independent material, with all the others as calibration materials. Pixel numbering starts from top left. Measurements are performed at 900 MHz.

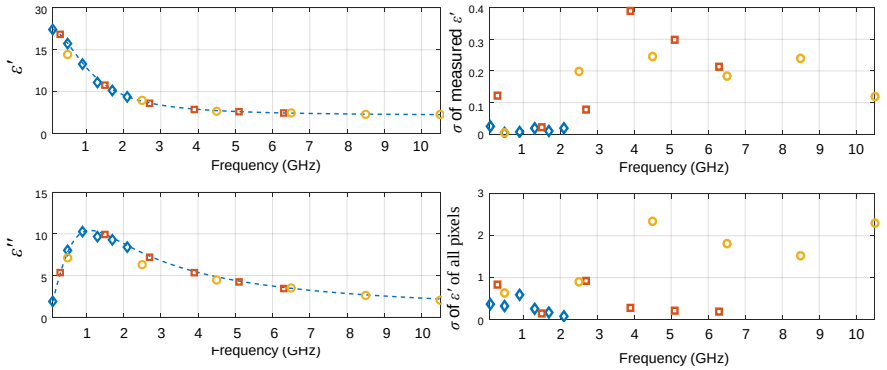


Figure 5.8: Measured ethanol real (ϵ') and imaginary (ϵ'') versus frequency, as a result of averaging of all 25 pixels and associated measured standard deviations among individual array pixels. Blue diamond: first harmonic, orange square: third harmonic, yellow circle: fifth harmonic.

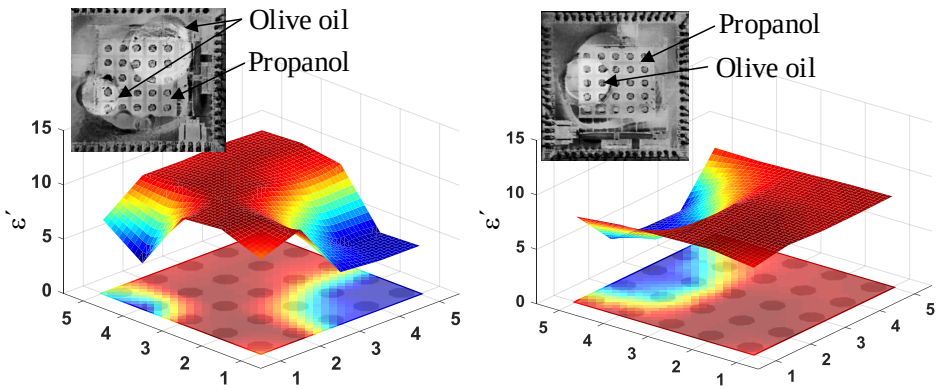


Figure 5.9: 3D permittivity plots and projected images captured by the sensing array chip using drops of olive oil in a base liquid consisting of 2-propanol.

permittivity of ethanol, is shown in Fig. 5.8. The measured ε' stays below 0.02 for the first harmonic, i.e., 0.1 - 2.1 GHz, and below 0.4 across all operation frequencies, i.e., third and fifth harmonics up to 10.5 GHz. A metric that provides an indication of the achievable permittivity imaging contrast is the standard deviation σ of all the ε' measurements across all pixels. This is shown in Fig. 5.8 to be as low as 0.1 and lower than 2.4 . The first harmonic features worst-case standard deviation of 0.4, which is, a more than 4 times better precision than that of the fifth.

Table 5.1: Comparison of implemented sensing pixel array with other works

	This [1]	[7]	Chapter 4 [8]	[3]	[4]
CMOS node [nm]	140	180	40	350	130
Frequency	0.1-10 GHz	0.62-10 GHz	0.1-10 GHz	10-50 MHz	0.5-4 MHz
Parameter	ϵ',ϵ''	ϵ',ϵ''	ϵ',ϵ''	R, C	|Z|
Power [mW]	156 @ 900 MHz	65-72	1-24	85	N/A
Size [mm^2]	2.5x2.3	3×3	0.15×0.3	2×2	2.2×2
Array	5×5	No	No	10×10	12×12
Accuracy	σ<0.4	rms error<1%	σ<0.4	N/A	N/A

5.3.3. Permittivity imaging

5.3.4. Comparison with the state of the art

The permittivity imaging demonstrator is compared with other published works in table 5.1. The implemented 5x5 permittivity sensing array is the first and only permittivity imager operating at frequencies above 100 MHz. Owning to the ultra-compact size of the standalone sensing pixel of chapter 4 [8], the 5x5 array has a smaller dimensions than other state-of-the art implementations operating in this frequency range [7]. Moreover, compared with other arrayed implementations, this work features a much higher operation frequency, which provides the advantage of higher flexibility in selecting the operating frequency for optimal permittivity contrast. The support of higher operation frequencies comes at the cost of increased IC area, i.e., smaller spatial resolution than low-frequency counterparts and increased power consumption.

5.4. Conclusion

This chapter presented the implementation of a 5×5 0.14-μm CMOS 2-D permittivity imaging array prototype operating at microwave frequencies. The pixel design and readout follow the architecture presented in previous chapters of this thesis. The implemented permittivity sensing array shows, like its standalone counterpart, precise permittivity measurements over a range of 0.1-10 GHz. Additionally, it successfully resolves sub-mm permittivity transitions in a 2-D plane.

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6

Conclusions

This dissertation has focused on developing miniaturized CMOS circuits for BDS and implementing measurement techniques that minimize readout noise, leading to improved precision of the complex permittivity measurement in a material. This chapter concludes the thesis with a summary of the original contributions and the research outcomes. Finally, this thesis culminates with recommendations for future work.

6.1. Original contributions

The original scientific contributions made in this thesis are summarized as follows:

- Proposed, analyzed, and verified an I/Q-mixer-based interferometric technique for the reference impedance renormalization of a VNA to improve the sensitivity of high impedance load measurement (chapter 2).
- Proposed, analyzed, and verified the operation of a CMOS compatible, programmable, double-balanced, fully differential RF Wheatstone bridge to minimize the common-mode rejection ratio in RF impedance measurement (chapters 2 and 4).
- Proposed and demonstrated a compact multi-harmonic down-conversion scheme in CMOS technology for the fast, energy-efficient readout of a permittivity sensing element (chapters 3 and 4).
- Proposed and demonstrated a first 2-D imager for detecting material transitions based on permittivity contrast at microwave frequencies (chapter 5).

6.2. Thesis outcomes

Several applications of BDS require the miniaturization of bulky laboratory setups currently in use to measure the complex permittivity of materials. CMOS technology is the most suitable platform to implement ultra-compact BDS sensors due to its wide usage and small form factor. At the same time, the improvement of measurement precision is important for fast readout and energy efficiency. These are both required in battery-operated devices and applications performing imaging based on permittivity contrast.

In chapter 2, permittivity sensing elements have been investigated, and a patch sensing element is favored for its flexibility and its optimal translation of permittivity to admittance for the intended applications. We introduce an active interferometric technique based on I/Q mixer steering, which aims at improving the measurement precision at high-impedance loads, such as small capacitances of BDS sensing elements. Although the technique's effectiveness has been successfully demonstrated, it is recognized that implementing it in CMOS technology would consume a large chip area. A CMOS-compatible, high-precision double-balanced, fully differential modification of the Wheatstone bridge is proposed instead, dynamically matching the branch impedance to that of the patch, thus achieving high precision.

In chapter 3, we have presented a compact, scalable, and broadband architecture for complex microwave permittivity sensing in CMOS technology. It implements a square-wave drive of the double-balanced, fully-differential Wheatstone bridge and a multi-harmonic bridge IF down-conversion scheme. Thus, multi-frequency permittivity characterization at the first, third, and fifth harmonics is possible with a single measurement.

Chapter 4 has detailed the implementation of an ultra-compact BDS sensing pixel in 40-nm CMOS technology, based on the proposed Wheatstone bridge architecture and multi-harmonic IF down-conversion scheme. Extensive characterization of the IC has demonstrated successful bridge operation and high-precision, energy-efficient complex permittivity measurement of liquid materials.

In chapter 5, the compact and scalable pixel architecture has been utilized to implement a 0.14-μm CMOS 2-D permittivity imaging array prototype, operating at microwave frequency. It comprises 25 permittivity-sensing pixels arranged in a 5x5 matrix. The implemented permittivity sensing array shows precise permittivity measurements and successfully demonstrates 2-D permittivity contrast imaging when the sensing array is interfaced with various dielectrics. The realized array provides sub-mm spatial resolution, enabling the quick and accurate detection of material transitions.

6.3. Recommendations for future work

The contributions made in this thesis have laid the ground for several fascinating research paths that have so far remained unexplored. Some recommendations for future developments follow.

The permittivity-to-admittance transfer function used in this work is based on matching 3D electromagnetic simulations of the structure to a linear or a rational function model. Although a rigorous analytical tool for the modeling of the patch sensing element has already been implemented [1], the results presented in this dissertation did not make use of this work. Introducing an analytical method in the calibration procedure could provide useful feedback on the possible sources of measurement inaccuracy. A combination of analytical and EM simulation methods can yield an improved accuracy, provided that all other sources of possible error (e.g., environmental factors) are well controlled.

Due to the focus on the development and characterization of the sensor core, the implemented prototypes presented in this work have resorted to external, high-performance equipment for data digitization, post-processing, and frequency generation. Having validated the core permittivity sensing architecture in a standalone sensor and a 2-D imaging array, the next step would be the co-integration of these functions into a single IC, where necessary for the intended application. Although an external 12-bit, 60 MS/s ADC was used in this work, the actual integrated ADC requirement is much more relaxed. Indeed, based on the highest IF frequency of 500 kHz (the fifth harmonic of the 100 kHz IF) and the required dynamic range of 75 dB at a 1 kHz resolution bandwidth (1 ms sample size), a 2 Ms/s with 8-bit resolution would suffice. Cautious design to ensure good ADC linearity is impor-

tant because the nonlinear harmonics will fall at the odd harmonics used for the multi-harmonic down-conversion scheme.

Similarly, PLLs can be integrated on the same IC for frequency generation. However, even state-of-the-art on-chip CMOS PLLs cannot achieve the unparalleled performance of external equipment or dedicated on-board IC parts. This means that increased noise is expected to be injected into an unbalanced bridge, making the need for a constantly balanced bridge more imperative. Advanced bridge balancing schemes should be developed for the automatic balancing of the bridge using digital assistance.

It has become clear that a commercial BDS system will require large data storage and post-processing. A random-access memory (RAM) will be required either on-chip or on the product PCB, given the low sample rate of the required ADC. Data processing, such as FFT, and averaging can be handled by on-board microcontroller units (MCUs) and digital signal processors (DSPs). Nevertheless, depending on the application, certain data processing tasks can be distributed, as is the case with wearables, where a common practie is to store and process the data on the cloud.

As discussed in section 2.2.1 of this thesis, one of the reasons that the patch sensing element was selected is the prospect of using advanced patch driving schemes, e.g., differential patch excitation, patch combination, etc. Options for individual pixel phase inversion in the bridge driver or the readout path was implemented in the imaging chip. These options have been left unexplored in the experiments performed so far, pending the definition of a successful verification setup.

Apart from the advanced patch driving options, further experiments from the perspective of potential technology users are required. As an example, for the application of skin hydration monitoring, relevant medical tests can be conducted. This direction requires interdisciplinary cooperation and research, which is sometimes challenging to coordinate. However, it is necessary to expedite the adoption of BDS in real-life application scenarios.

Scientific interaction with potential technology users will also allow determining whether it is needed to achieve a better spatial resolution than the 230 μm achieved in the demonstrated imager. In the current discussion, it is believed that this spatial resolution will be sufficient for the considered applications, e.g., Mohs' surgery procedure [2]. Nevertheless, it is worth investigating the limiting factors in spatial resolution improvement if such a requirement arises. Assuming that we can decrease the patch to the minimum possible allowed by the technology design rules, the pixel size is limited by the area of the circuitry placed underneath, i.e., the bridge, the bridge driver, the decoupling capacitors, and the gm stage. Generally, decreasing the patch size will decrease its capacitance. This, in turn, will reduce the required bridge branch capacitance and the bridge driver size. Since the driver's size decreases, so does its current consumption, decreasing the local decoupling capacitor size. Nevertheless, it is expected that the g_m stage size cannot easily be reduced, as its size is linked to its noise performance.

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A

Bridge transfer function in the presence of mismatch

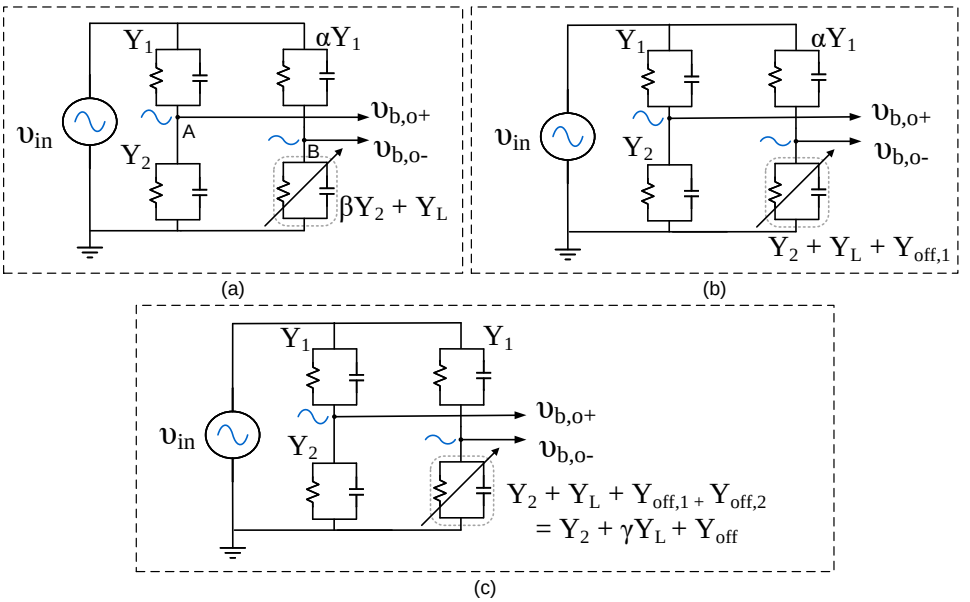

Figure A.1: Bridge analysis in the presence of mismatch between the branches.

Mismatch is unavoidable between the bridge elements, even if typical precautions are taken to minimize it, such as identical switched capacitance elements, large width resistors and as symmetrical layout as possible.

Consider the single-branch bridge of fig. A.1(a), where separate values of branch admittance occur. Without loss of generality, we can assign the top-left branch with an admittance of Y_1, and the bottom-left branch with an Y_2. These two can be quite close but also completely different. In a typical bridge implementation, the admittance Y_2 will embed all parasitic capacitance of node A to ground. We also assume that, despite the effort that the top-right branch be equal to Y_1 it differs from it by an unknown, random factor α. Similarly, the bottom-right branch differs from Y_2 by an, also unknown, factor β.

At a given frequency of operation, we can transform the bridge to its equivalent form of fig. A.1(b), where βY_2 has been replaced by an equivalent $Y_2 + Y_{off,1}$, where $Y_{off,1} = (\beta - 1)\, Y_2$. Next, we can replace the upper-right admittance αY_1 by Y_1, provided that offset admittance $Y_{off,2}$ is added in parallel to the variable admittance Y_L. This offset admittance needs to satisfy the following condition for equivalence of the output voltage $\upsilon_{b,o-}$:

$$\upsilon_{in} \cdot \frac{\alpha Y_1}{\alpha Y_1 + Y_2 + Y_L + Y_{off,1}} = \upsilon_{in} \cdot \frac{Y_1}{Y_1 + Y_2 + \ Y_L + Y_{off,1} + \ Y_{off,2}} \tag{A.1}$$

Solving A.1 for $Y_{off,2}$ yields

$$Y_{off,2} = \frac{1 - \alpha^2}{\alpha} \left(Y_2 + Y_L + Y_{off,1} \right). \tag{A.2}$$

We can rewrite the total admittance of the bottom-right branch as $Y_2 + \gamma Y_L + Y_{off}$, as, shown in fig. A.1(c), where

$$Y_{off} = \frac{1-\alpha^2}{\alpha}\, Y_2 + \beta \cdot \frac{1-\alpha^2}{\alpha}\, Y_2 \tag{A.3}$$

and

$$\gamma = \frac{\alpha + 1 - \alpha^2}{\alpha} \tag{A.4}$$

We have shown that any mismatch across the bridge can be transformed into the generic case of fig. A.1(c) where the upper-left and upper-right admittances are equal (Y_1), similarly to the nominal lower-left and lower-right admittances (Y_2) All mismatch is grouped to an offset admittance parallel to the load. The load variation undergoes a constant multiplication by a factor γ, dependent on the mismatch between the lower branch admittances α.

Through straightforward analysis we can show that the inverse output of the bridge in fig. A.1(c) varies linearly to the inverse of the quantity $Y'_L = \gamma Y_L + Y_{off}$:

$$\frac{1}{\Delta v_{b,o}} = \frac{1}{v_{in}} \left(1 + \frac{Y_2}{Y_1} + \frac{(Y_1 + Y_2)^2}{Y_1} \cdot \frac{1}{Y'_L} \right), \tag{A.5}$$

which reduces to (2.13) of chapter 2 for $Y_{off} = 0$ and $Y_1 = Y_2 = Y_0$. The above equation falls within the calibration equations described in section 4.3, since the linear coefficients of the loads and the offset admittance are found through a search algorithm, and is not assumed by the designed nominal values. Thus, mismatch between the bridge components does not affect the calibration procedure and, as a result, the accuracy of the system since there always exists an offset admittance Y_{off} such that linear equations (4.1) and (4.2) hold true. Instead, the main accuracy bottleneck lies on the actual permittivity values of the materials used for calibration and the accuracy of the ϵ-to-Y transfer characteristic of the patch sensor.

Acknowledgements

It goes without saying that working towards a Ph.D. is quite a solitary endeavor. Nevertheless, there is a handful of people without whom these pages and the brain matter imprinted in them would have been even more painstaking or, I should admit, would not have existed at all.

My Ph.D. journey was an unusual one, given that I worked remotely for a large part of it. This was not the result of the unprecedented COVID-19 situation but started in 2017 before working off-grounds was considered necessary or even cool. When I was in the third year of my research at the TU Delft, I felt compelled to -again- change things in my life and was quite comfortable with the idea of never defending a Ph.D. Yet, I had not accounted for my supervisor and promotor, Marco Spirito, and his commitment to keeping me busy.

From the time we first spoke about the INFORMER project, Marco has gently driven me towards continuing this line of research up to a level that could be considered complete for a Ph.D. thesis, at least to the minimum definition of the term. Marco, you have been very supportive during these years. I have always valued your excitement levels when talking about your students' research (including mine). Your input in my research dilemmas, agonies, and deadends has always steered me to a clear path ahead.

I was fortunate to also have Leo de Vreede as my promotor because he has always been very involved in my work and has always been committed to participating in meetings and providing great insight. His willingness to keep up with my scientific output and tirelessly provide feedback has been a great educational experience. Leo, thank you for all the time you have spent with me. Also, thank you for providing me with your typical Dutch directness when I actually needed it in my life.

As if my luck was not enough, I was also privileged to have more than two supervisors in my project, which is quite an unusual trait. Michiel Pertijs is the person to complete the great committee of the INFORMER project. Michiel's experience on imagers and top-level integration has been a precious addition to this work.

I owe a lot to the colleagues I worked together with on the INFORMER project: Harshitha Thippur Shivamurthy and Zhebin Hu. Their contribution was highly significant, and the technical discussions with them were always enjoyable.

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Curriculum Vitæ

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Work

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List of Publications

Journal Papers

J1 H. T. Shivamurthy, Z. Hu, **G. Vlachogiannakis**, M. Spirito and A. Neto, *Equivalent Circuit Modeling of a Single-Ended Patch Sensing Element in Integrated Technology*, IEEE Transactions on Microwave Theory and Techniques, vol. 68, no. 1, pp. 17-26, Jan. 2020.

J2 **G. Vlachogiannakis**, Z. Hu, H.T. Shivamurthy, A. Neto, M.A.P Pertijs, L.C.N de Vreede, M. Spirito, *Miniaturized broadband microwave permittivity sensing for biomedical applications*, IEEE Journal of Electromagnetics, RF and Microwaves in Medicine and Biology, vol. 3, no. 1, pp. 48-55, March 2019.

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C1 **G. Vlachogiannakis**, Z. Hu, H. Thippur Shivamurthy, A. Neto, M.A.P. Pertijs, L.C.N. de Vreede, M. Spirito, *A compact energy efficient CMOS permittivity sensor based on multiharmonic downconversion and tunable impedance bridge*, 2018 IEEE International Microwave Biomedical Conference (IMBioC), Philadelphia, PA, 2018.

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