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Technology platform for advanced neurostimulation implants
The “chip-in-tip” DBS probe

Kluba, M.M.

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Technology Platform for Advanced Neurostimulation Implants

The "Chip-in-Tip" DBS Probe

Marta Maria Kluba

Technology Platform for Advanced Neurostimulation Implants

The "Chip-in-Tip" DBS Probe

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
by the authority of the Rector Magnificus Prof.dr.ir. T.H.J.J. van der Hagen
Chair of the Board for Doctorates
to be defended publicly on
Monday, 31st January 2022 at 10:00 o'clock

by

Marta Maria KLUBA

Master of Science in Biomedical Engineering (double degree)
RWTH Aachen University, Germany
RUG University of Groningen, The Netherlands
and
Master of Science in Chemical Technology
AGH University of Science and Technology, Kraków, Poland
born in Oświęcim, Poland.

This dissertation has been approved by the promotor:

Promotor: Prof. dr. ir. R. Dekker

Composition of the doctoral committee:

Rector Magnificus,	chairperson
Prof. dr. ir. R. Dekker	Delft University of Technology, promotor

Independent members:

Prof. dr. ir. P.M. Sarro	Delft University of Technology
Prof. dr. P.J. French	Delft University of Technology
Prof. dr. ir. J. Vanfleteren	Ghent University, Belgium
Dr. V. Giagka	Delft University of Technology
Dr. G. Pandraud	Ommatidia LIDAR, The Netherlands
Dr. V.A. Henneken	Philips Research, The Netherlands

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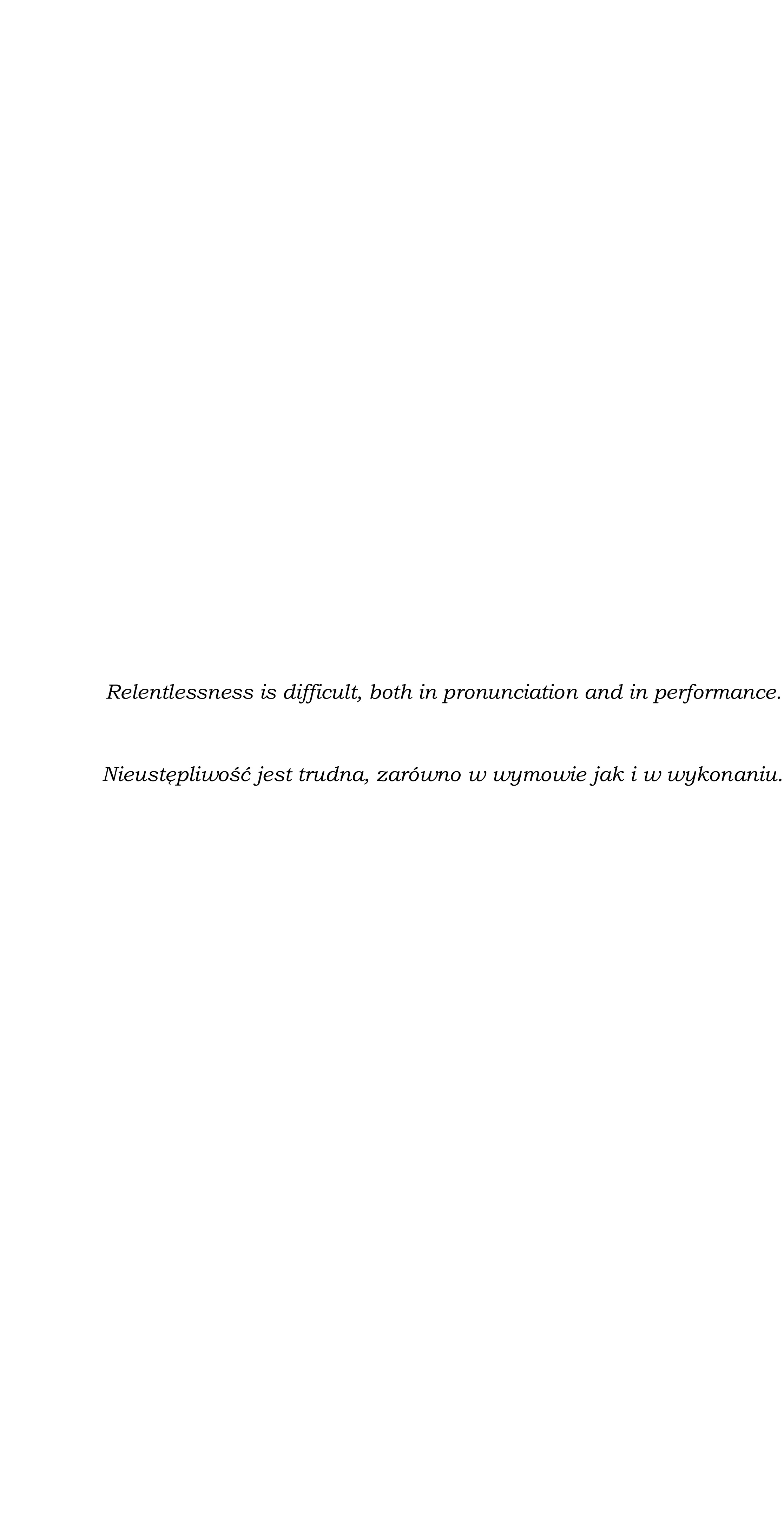
[1] Author email: klubam@gmail.com



Relentlessness is difficult, both in pronunciation and in performance.

Nieustępliwość jest trudna, zarówno w wymowie jak i w wykonaniu.

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PREFACE

This thesis was realized within the EU ECSEL JU project InForMed, grant number 2014-2-662155. The main goal of this project was innovation of tools and technologies for medical device fabrication and assembly, and to establish an integrated pilot line for their manufacturing and testing. To bridge the gap between research and industry production, cooperation between a number of international partners was started to bring together the knowledge and experience from both worlds.

Participating in the InForMed project had multiple implications for this thesis that is focused on the development of a highly integrated deep brain stimulation (DBS) probe. The choices made while designing the DBS probe, the selection of materials and fabrication methods, and the development of test protocols were carefully evaluated with the whole team. The initial goal of the project was to design, fabricate and test the directional DBS device that would need to fulfill all the requirements for implantable medical devices. However, after the end-user and leader of the DBS work package, Medtronic, had withdrawn from the project, many activities connected with device packaging and the final system assembly and testing were dropped. At that point the focus of the PhD project shifted towards the development of the necessary enabling technology modules, and the evaluation of their feasibility.

The manufacturing process should be easily scalable and transferable to the pilot line and finally to the industrial manufacturer. The alignment of the designed structures and the used fabrication and packaging methods and techniques was crucial since several manufacturing steps were performed at different fabrication sites. For this reason, only a limited number of technologies and materials could be considered for further investigation in this thesis. Moreover, the focus of the thesis was directed from quantitative research, including investigation of design variations and different materials and methods, towards a more qualitative evaluation of the jointly selected options, chosen based on the experience of the partners.

This work is a result of a collaboration with the following InForMed partners:

- CEA Leti, France;
- Comelec, Switzerland;
- Delft University of Technology (TU Delft), The Netherlands;
- Fraunhofer IZM (FIZM), Germany;
- ICSense, Belgium;
- Medtronic (MEDC), The Netherlands (2015-2016);
- Murata, France (former IPDiA);
- Okmetic, Finland;
- Philips Innovation Services (PInS), The Netherlands;
- Philips Research, The Netherlands;
- Picosun, Finland;
- Salvia BioElectronics, The Netherlands (2017-2018).

The majority of the design and processing work was performed at the Delft University of Technology (TU Delft) in the Else Kooi Laboratory (EKL). Therefore, to fabricate some proof of concepts devices and test devices in a coherent way, locally applicable rules regarding, for example, contamination had to be take into consideration. In some cases, a material of choice (e.g., platinum used for metallization) had to be replaced with the closest available substitute.

1

INTRODUCTION

1.1 NEUROSTIMULATION

In 46 AD Scribonius Largus discovered the therapeutic properties of electrical stimulation when he used the torpedo fish (electric ray) to treat headaches [1]. Since then, not much research was carried out in the electrical stimulation of the body until the discovery of electricity around the 16th and 17th centuries. Consequently, a series of experiments carried out throughout the 18th and the 19th century demonstrated that electrical stimulation of nerves or the brain could induce twitching movement in a dead animal's limb [2][3]. Such a bodily response like limb movement was induced by applying current directly to the corresponding nerve or the region in the brain responsible for sending signals to that part of the body. The current activates the neural network, the signal travels down to the limb, and the muscle is activated [4].

Since the 19th century, the field of neurostimulation – the intentional modification of the nervous system activity through targeted delivery of electrical stimuli - has changed enormously. Nowadays, nervous system stimulation is applied to induce or suppress not only a mechanical response, but it can also influence hearing, vision, immune system response, pain perception, and even mental state. The targeted neurostimulation therapy can compete with, or even outperform, the traditional chemical treatment [5][6]. The well-targeted electrical neuromodulation can help to reduce the whole-body side effects typical for traditional medications therapies. Furthermore, modern neurostimulation devices can precisely target very specific nerve bundles or regions in the brain. Also, they can be implanted in the body to aid easy delivery of the stimuli for an extended period (Figure 1.1).

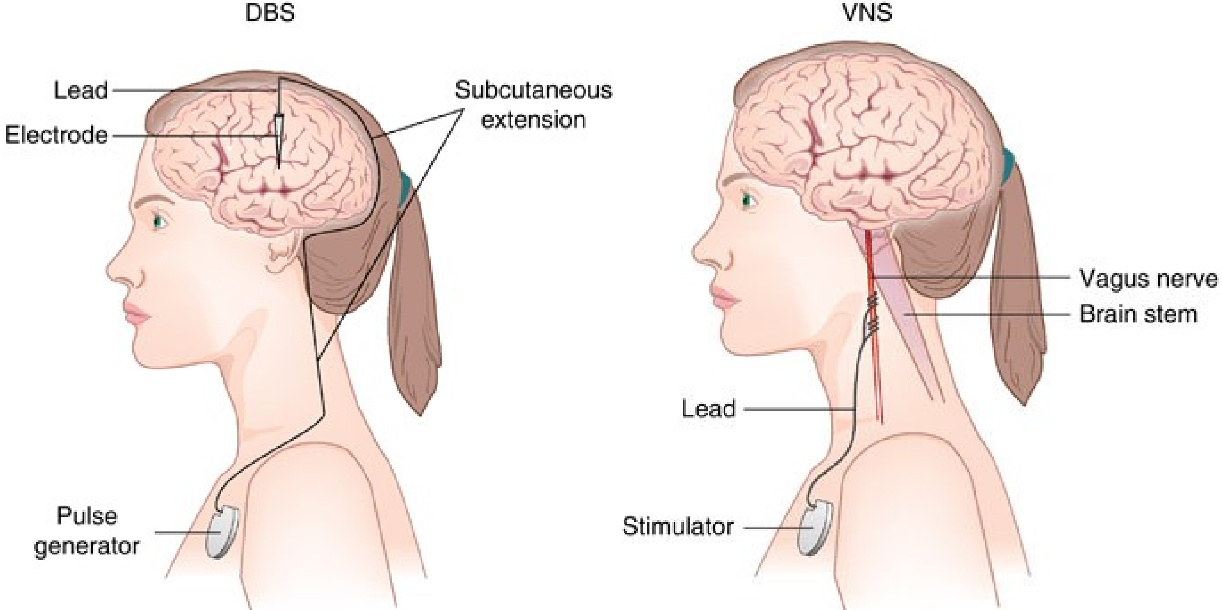

Figure 1.1: Schematics of the implanted deep brain stimulator (DBS) and vagus nerve stimulator (VNS) [7].

Many of the current implantable neurostimulation devices are commercially available on the market, and some are even recognized as an official medical treatment for specific conditions. Some examples of implantable biomedical devices are: cardiac stimulators to treat various types of heart arrhythmias; cochlear implants to restore hearing or retina implants to restore vision; spinal cord stimulators to treat chronic pain; vagus nerve stimulators to treat epilepsy and depression; and deep brain stimulators to treat Parkinson's disease, essential tremor, dystonia [8][9]. Examples of implantable bioelectronics are shown in Figure 1.2.

Figure 1.2: Examples of chronically implantable neurostimulation devices available on the market. (a) Cardiac implant (pacemaker) from Medtronic [10]. (b) Cochlear implant from Oticon Medical [11]. (c) Spinal cord stimulator from Boston Scientific [13]. (d) Retinal prosthesis system (Argus II) from Second Sight Medical Products [12]. (e) Vagus nerve stimulator from Cybertonics [14]. (f) Deep brain stimulator (DBS) from Medtronic [15].

1.2 STATE OF THE ART

Traditional neurostimulation devices, such as an implantable deep brain stimulator (DBS), are composed of an implantable pulse generator (IPG), extension cord, and stimulation leads with electrodes on their distal end. The IPG is usually implanted underneath the skin in the patient's chest (Figure 1.3a,b). It contains a battery pack, telemetry coil, and circuitry for steering, sensing, diagnostic and communication management [16]. All these elements are enclosed in a rigid casing, usually made from titanium that is often additionally coated with a parylene layer. The case is hermetically closed to protect the implant from bodily fluids and protect the body from harmful substances that can be released from the implant.

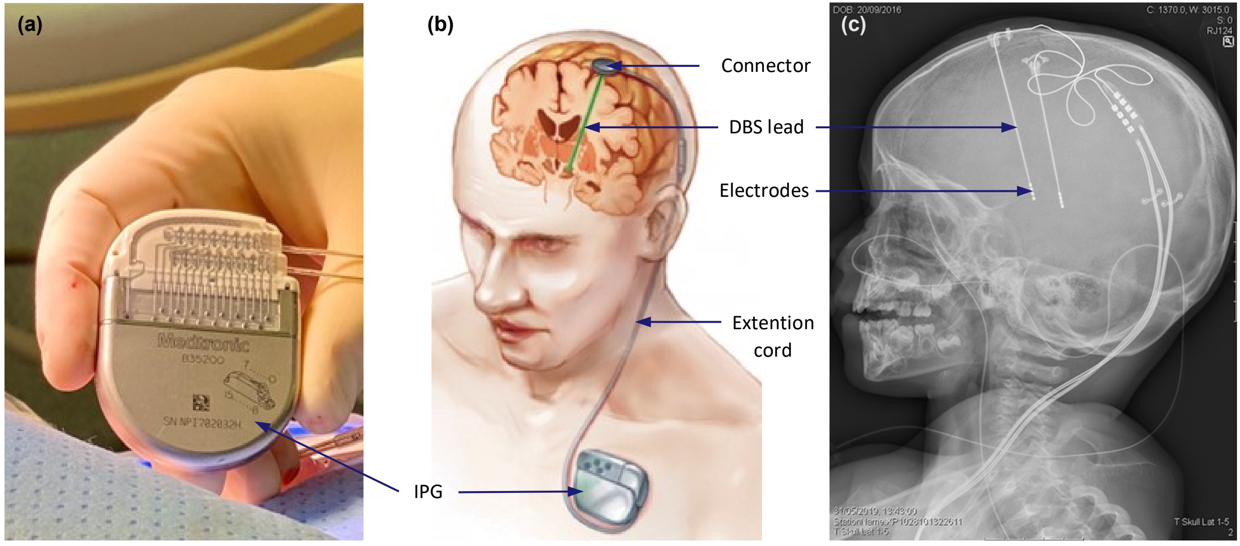

Figure 1.3: Deep brain stimulation (DBS) device. (a) Implantable pulse generator (IPG) with two extension cords for operating two DBS leads [17]. (b) Schematic of the implanted one-lead DBS device composed of the IPG, extension cords with connectors, and the DBS lead [18]. (c) A two-year-old boy with implanted two-lead DBS device [19].

The multi-wired flexible extension cord is attached to the pulse generator through a series of connectors located on the titanium casing. The cord is composed of a coiled conductor (e.g., platinum-iridium wire) filled with silicone rubber (e.g., PDMS) and insulated with a polymer such as a polycarbonate urethane [20]. In the case of the DBS device, the extension cord runs from the IPG implanted in the chest, underneath the skin, to the skull. On the skull, the cord connects with the DBS leads and passes the signal from the pulse generator to the stimulation electrodes. To ease the implantation of up to 45 cm long extension cord [21][22], it is often split into two or three parts and reconnected again on the skull using connectors (Figure 1.3b).

The stimulation lead (usually 2 in the case of DBS) is implanted through the skull deep into the brain (Figure 1.3b,c). The lead is composed of a coiled conductor that transports the signal to the stimulation electrodes located on the tip of the DBS lead. The DBS lead and the electrodes are made from biostable and biocompatible platinum or platinum-iridium alloy located on a polymer-based (polyurethane) tip (Figure 1.4). The exposed electrodes are in direct contact with the tissue to form a neural interface with the brain and enable its stimulation.

Figure 1.4: Tip of the DBS lead with coiled conductor and four cylindrical electrodes located at the tip [23].

1.3 BEYOND THE STATE OF THE ART

The advancements in the field of neurostimulation are impressive both from a technical and from a therapeutic point of view. The number of medical conditions that can be treated using existing or completely novel neurostimulation devices continues to grow. Unfortunately, some aspects of implantable bioelectronics devices have not changed for decades, even though they call for improvement.

1.3.1 Packaging vs. aesthetics and invasiveness

For example, the golden standard for encapsulating the implantable pulse generator (IPG) module remains a bulky titanium case that accommodates all the electronic components (Figure 1.5). Besides aesthetical aspects, implanting such a case involves rather invasive surgery, especially for implants where the targeted stimulation site is located far from the pulse generator unit (e.g., deep brain stimulator). Much research is currently going on in the field of soft encapsulation of long-term biomedical devices, which might not only allow for the miniaturization of the pulse generator unit but also bring it closer to the stimulation site [24]. The miniaturization process can be further improved by applying highly efficient or even rechargeable energy sources, energy-saving stimulation algorithms, reducing the size of the electronic components (e.g., employing high-capacity trench capacitors), or more space-efficient electronic components integration (e.g., flip-chip) [25].

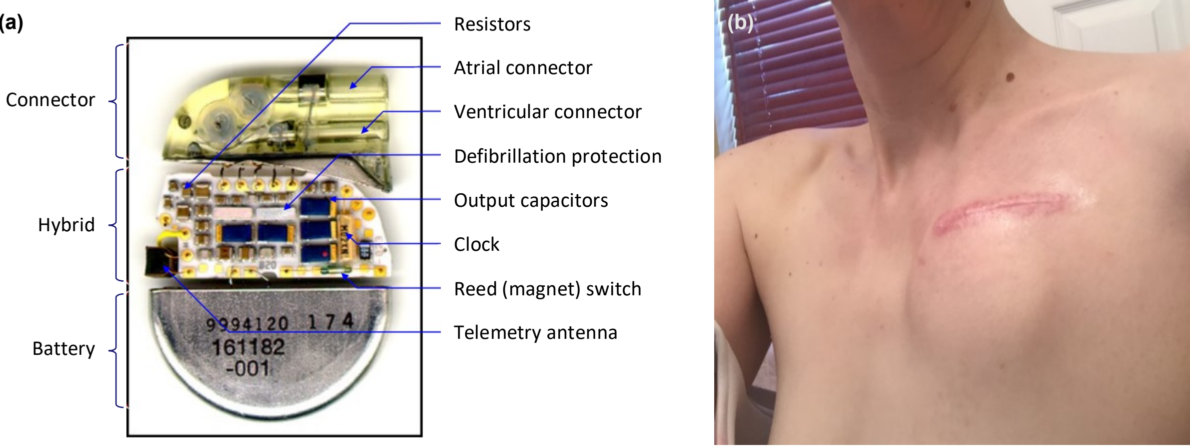

Figure 1.5: (a) The anatomy of the cardiac pulse generator (pacemaker) [26]. (b) DBS pulse generator implanted under the skin on the chest [27].

1.3.2 Manufacturing vs. resolution

Another area for improvement concerns the labor-intensive manufacturing process. Techniques like soft lithography are commonly used to fabricate flexible stimulation leads with electrodes. They not only come at a high cost due to low throughput, but because of the low process resolution, they also limit the size, number, and distribution pattern of the electrodes that can be integrated at the tip of the lead. As a result, the most advanced stimulation leads available on the market contain only eight electrodes, even though in some cases, such as for DBS, the advantages of directional stimulation with a multitude of smaller electrodes (Figure 1.6) has been repeatedly proven [25][28][29][30]. The number and the design freedom of the electrodes located at the tip of the DBS lead can be improved by fabricating flexible structures on a flat silicon carrier using standard integrated circuit (IC) microfabrication techniques and consequent folding and rolling of such a device into the round shape of the DBS. In response to the resolution issue, Sapiens SBS has developed a wafer-based process allowing for the fabrication of DBS leads with up to 64 individual electrodes [31][32].

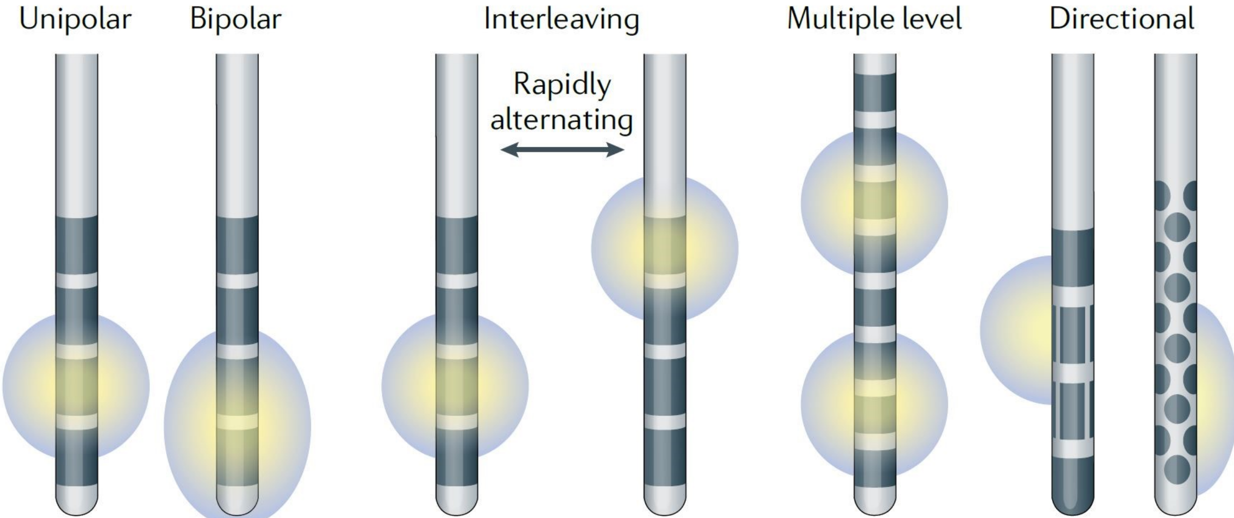

Figure 1.6: Various DBS probe designs and stimulation patterns. Examples of standard, cylindrical electrodes (first five) and segmented electrodes (last two) that enable directional brain stimulation [25].

The fabrication of the lead designed by Sapiens with dozens of individually activated electrodes, and consequent trial implantations, allowed to show the benefits of directional stimulation. It can reduce the side effects of surrounding tissue overstimulation and enable the stimulation of new, smaller regions in the brain. Nevertheless, the lead has never been further developed and used for chronic stimulation because the number of contacts (one for each electrode) that had to be made during the surgical procedure was extremely challenging. Moreover, the wafer transfer technique and the consequent manual release of the flexible film with the electrodes are not scalable, somewhat cumbersome, and do not tend to have a high yield.

1.3.3 Highly integrated silicon-based devices

To reach beyond state of the art in the implantable neurostimulation field, it seems essential to focus on further miniaturization of the implant and improvement of the stimulation resolution by increasing the number of electrodes. Looking at these challenges from the manufacturing point of view, it only seems logical to investigate IC-compatible microfabrication technologies, such as Flex-to-Rigid (F2R) [33]. The Flex-to-Rigid can tackle both of the objectives simultaneously by allowing for high-level components integration and further device miniaturization.

1.4 FLEX-TO-RIGID (F2R) PLATFORM

Flex-to-Rigid (F2R) is a generic platform that enables miniaturization of medical devices by permitting monolithic component integration into a semi-flexible device structure [33]. The technology is compatible with integrated circuit (IC) microfabrication techniques. Thanks to this, advanced electronic components can be fabricated on individual silicon islands and subsequently connected with flexible polyimide-aluminum-based interconnects. The device, such as the smart catheter equipped with MEMS ultrasound transducers (CMUTs), is fabricated on a silicon wafer, where it remains suspended using flexible tabs (Figure 1.7a). After it is released from the wafer (Figure 1.7b), the device can be folded or, like in the case of the smart catheter, wrapped around a shape (Figure 1.7c).

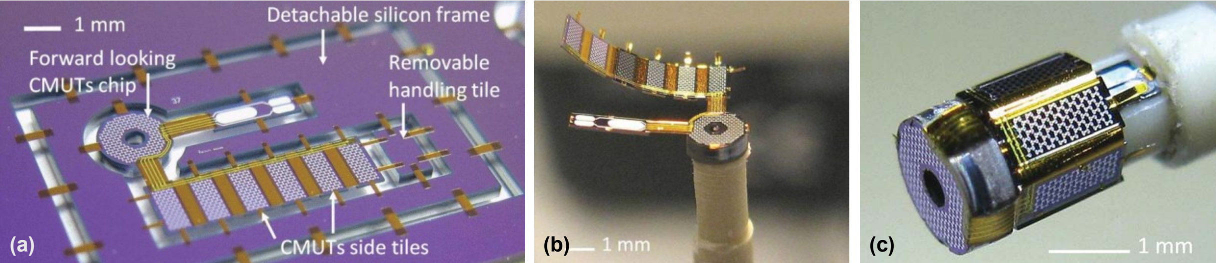

Figure 1.7: Semi-flexible demonstrator device fabricated in the Flex-to-Rigid technology comprising ultrasounds transducers (CMUTs) [33]. (a) The device suspended in the silicon frame using polymer-based tabs. (b) Mounting of the device released from the wafer. (c) The device mounted at the tip of the catheter.

Additionally, the F2R technology uses standard IC-compatible tools and techniques, making the fabrication process fully scalable, reducing the costs of bioelectronics device manufacturing, thereby making treatment more affordable and accessible.

1.5 HIGH-LEVEL COMPONENTS INTEGRATION

The F2R platform enables a high level of integration of components into the semi-flexible device structure. Integrating electronic components such as application-specific integrated circuits (ASICs) or capacitors directly in/on the silicon allows for the fabrication of a high-resolution stimulation device with a large number of electrodes without the need for complex leads and extension cords. For example, integrating signal multiplexing components at the tip of the deep brain stimulator (DBS) lead can ensure high stimulation resolution by enabling individual activation of multitude of electrodes, but at the same time significantly reduce the number of signal and power wires running down to the pulse generator (Figure 1.8). In this case, the flexible interconnects enable the folding of the integrated device into the desired, miniaturized shape. They can also make the bioelectronics device more flexible and thus more compatible with the human body (e.g., spinal cord stimulator, deep brain stimulator) or enable wrapping the implant around, for example, a nerve bundle (e.g., vagus nerve stimulator) [28].

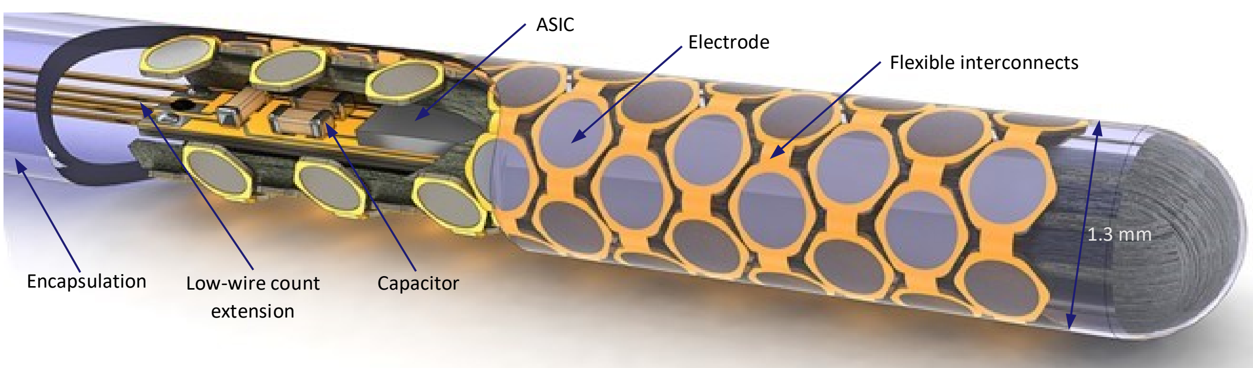

Figure 1.8: Impression of the highly-integrated directional deep brain stimulation probe with ASIC and safety capacitors integrated inside the tip of the probe. Source: InForMed.

Furthermore, direct integration of components into the stimulation part of the implant enables not only its miniaturization or improving mechanical compatibility with the human body. Moving components out of the implantable pulse generator (IPG) can significantly decrease its dimensions, making the treatment less invasive, and in the future, the IPG may even become obsolete.

The current F2R platform uses polyimide and aluminum as base materials for the flexible interconnects. These materials are not suitable for long-term implantable neurostimulation devices. Aluminum is not a noble material, and as such, it might react with bodily fluids [24]. Polyimide is not an FDA-certified material for long-term use in the human body. Besides, polyimide manufacturers refuse to supply the material when it is intended to be used for implantable devices. Therefore, the Flex-to-Rigid technology needs to be developed into a platform containing only biocompatible and biostable flexible interconnects.

1.6 RESEARCH OBJECTIVES

The research presented in this thesis was partially carried out within the EU ECSEL Joint Undertaking project InForMed. One of the objectives of this project was to develop a guideline for crossing the valley of death between academia and industry in the field of medical device microfabrication. Following that guideline, several technologies enabling the fabrication of innovative medical devices were developed, and the transfer of these processes from the laboratory to the pilot line or foundry was executed. Multidisciplinary teams were formed within the project involving academia, silicon wafer and electronic component manufacturers, packaging and coating specialists, and contractors. The project objectives and collected specialists created a perfect ground for tackling the challenges that are slowing down the development of current neurostimulation devices, such as deep brain stimulators (DBS). The interdisciplinary approach and the condition of process scalability and transferability to industry resulted in continuous balancing between the academic laboratory capabilities and industrial requirements, which strongly impacted the research done in this thesis.

The goal of the research presented in this thesis was to develop a set of enabling technologies that will turn the Flex-to-Rigid technology into a platform for the fabrication of highly integrated implantable medical devices. To achieve this, several critical aspects of this goal have been investigated, such as monolithic wafer-based component integration, biocompatible flip-chip on the semi-flexible Flex-to-Rigid devices, packaging and soft encapsulation for implantable devices, parylene processing in a microfabrication cleanroom, and the flexible implantable interconnect fabrication process itself. These topics have been investigated using a 40-electrode DBS device design as a demonstrator. The scope of this work is not to fabricate a fully functioning device but rather to develop the building blocks that will enable large-scale fabrication of implantable electronic devices that are compatible with industrial manufacturing.

1.7 OUTLINE OF THIS THESIS

In this thesis, a number of technologies have been developed to enable electronic component integration into long-them neurostimulation implants. Several aspects of design, fabrication, integration, and packaging of a highly integrated directional deep brain stimulation (DBS) probe have been investigated.

In Chapter 2, the parylene-based Chip-in-Tip DBS design is introduced. It allows for placing the steering ASICs (chips) and the necessary decoupling capacitors inside the tip of the DBS probe. This approach enables directional stimulation using forty independent electrodes and, at the same time, simplifies the implantation procedure by limiting the number of connections between the probe and pulse generator. The requirements are defined, and corresponding technologies and materials necessary to realize the design, fabrication, component integration, and packaging are investigated.

Chapter 3 focuses on the biocompatible flip-chip process for ASICs integration directly onto the DBS structure. The developed enabling technologies such as platinum-based stud bumping, platinum to platinum bonding, and biocompatible underfill are presented. The processes are verified using specially prepared test devices, representing the Chip-in-Tip DBS design.

Chapter 4 presents the developed technologies enabling integration of high-density trench capacitors directly into an SOI substrate, further used to fabricate the semi-flexible DBS probe structure in the Flex-to-Rigid process. Two technologies are developed for the precise separation of capacitor structures. The first one employs sealable microchannels (trenches) embedded in silicon. The second one is based on the custom-developed SOI wafer with a patterned BOX layer – cavity-BOX. Next, the design and the fabrication process alignment strategy are established, and the feasibility of the inter-facility capacitors integration process is shown using a demonstrator device.

In Chapter 5, some aspects of the Chip-in-Tip DBS device packaging are investigated. First, a tool for wrapping the semi-flexible 2D structure into a cylindrical 3D DBS probe is developed. Thanks to applying a set of metal strips to mount the device, there is no need for inserting additional mechanical support inside the device. Next, the device filling method and material are selected and tested using parylene-silicon-based mock-up DBS structures.

Chapter 6 concentrates on various aspects of processing wafers containing parylene in the EKL microfabrication cleanroom environment. Special attention is drawn to the fabrication of parylene-platinum-based flexible interconnects. First, the adhesion between the parylene and platinum is studied in various configurations. The influence of the standard microfabrication processes on the adhesion in the stacks is evaluated. Next, the processing aspects such as contamination prevention and cleaning of the wafers containing parylene and parylene patterning methods are investigated. Finally, the procedures for platinum processing on top of parylene are presented.

In Chapter 7 and Chapter 8, the technologies developed for parylene processing in a microfabrication cleanroom are applied to fabricate devices with parylene-based flexible interconnects. For that, a test device comprising flexible internets, comb-meanders structure, and a set of electrodes is designed, fabricated, and evaluated. In Chapter 7, the interconnects are fabricated by encapsulating platinum tracks in two layers of parylene deposited underneath and on top of the metallization using the "Top stack" approach. In Chapter 8, the titanium nitride (TiN) interconnects are encapsulated in parylene and a stack of additional ceramic layers SiO_2 and Si_3N_4. In this process, the interconnects are first encapsulated in ceramics, and at the very end of the fabrication, the parylene encapsulation is deposited using the "Parylene Last" approach.

The general conclusions of this thesis, contributions to the field of microfabrication, and recommendations for future research are collected in Chapter 9.

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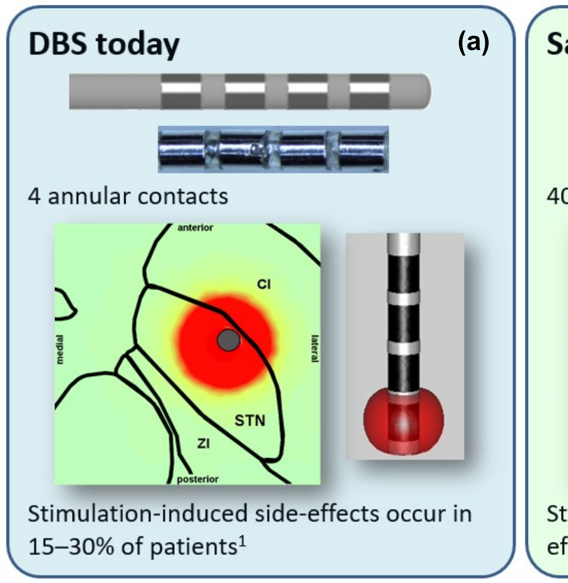
2

CHIP-IN-TIP: HIGHLY INTEGRATED DBS PROBE

2.1 INTRODUCTION

The application range for deep brain stimulation (DBS) devices is continuously widening. Neurologists worldwide are investigating the use of DBS for the treatment of new conditions going beyond physical impairments, such as Parkinson's disease or dystonia, to psychological diseases such as obesity, depression, or obsessive-compulsive disorder (OCD) [1]. The search for new applications is happening regardless of the fact that even the most advanced DBS leads available on the market are not yet able to precisely stimulate the targeted region in the brain without overstimulation of the surrounding tissue (Figure 2.1). Tissue overstimulation can lead to treatment failure and can cause serious side effects [2].



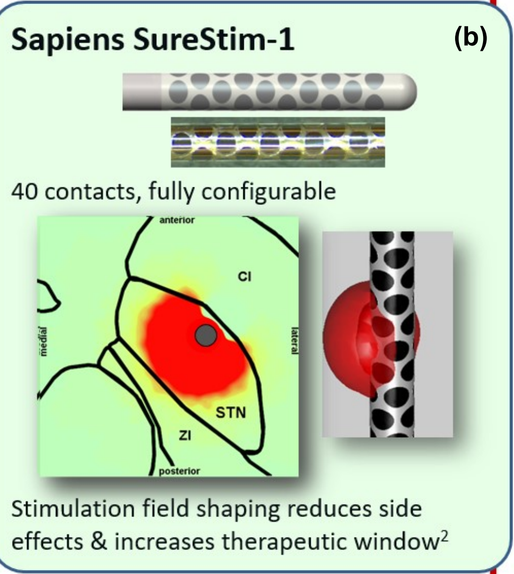


Figure 2.1: Brain stimulation patterns using DBS probe [3]. (a) Standard 4-contact DBS with cylindrical electrodes. Overstimulation of the internal capsule (CI) region in the brain is shown. (b) Directional 40-contact DBS with segmented oval electrodes precisely targeting the subthalamic nucleus (STN).

2.2 STEERABLE BRAIN STIMULATOR (SBS) - DIRECTIONAL DBS

As a response to the omnipresent brain overstimulation with standard DBS devices, Sapiens has developed a high-resolution steerable brain stimulator (SBS) lead. It allows for adding directionality to the stimulation pattern of standard DBS devices (Figure 2.1). The SBS device incorporates up to 64 stimulation electrodes evenly distributed around the tip of the lead, a lead extension with forty coiled wires, an implantable module with electronics (multiplexing integrated circuit and capacitors), and an extension cord connecting the implantable module with an implantable pulse generator. Each circular electrode in the SBS device can be activated individually or in groups to achieve the best stimulation result [4]. Figure 2.2 illustrates several elements of the SBS device developed by Sapiens.

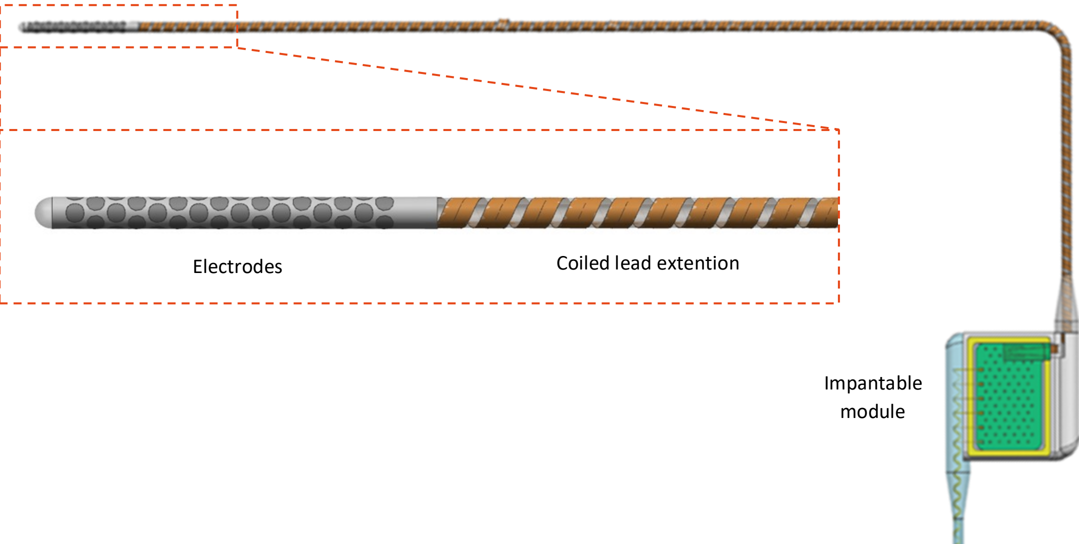


Figure 2.2: Directional Steerable Brain Stimulator (SBS) device with 64 individual electrodes, integrated coiled lead extension, and implantable module containing decoupling capacitors and multiplexing ASIC. Source: InForMed.

2.2.1 Fabrication process

The current SBS lead is fabricated in a specially developed flat-film technology. The parylene-platinum-based flexible foil, later forming the lead, is fabricated on a silicon wafer using mostly techniques compatible with the standard IC microfabrication. A wafer transfer technique in combination with applying a sacrificial layer is used during the process to encapsulate the platinum-based metallization in parylene from both sides [3]. The finished wafer contains several leads attached to it using a sacrificial layer. Each lead comprises an approximately 50 cm long flexible foil with interconnects and 40 electrodes at its distal end (Figure 2.3a). At the end of the fabrication process, the leads are released from the wafer by dissolving the sacrificial layer in a suitable solvent (Figure 2.3b,c). Finally, the released lead is coiled and assembled into a long, round lead with a diameter of approximately 1.3 mm.

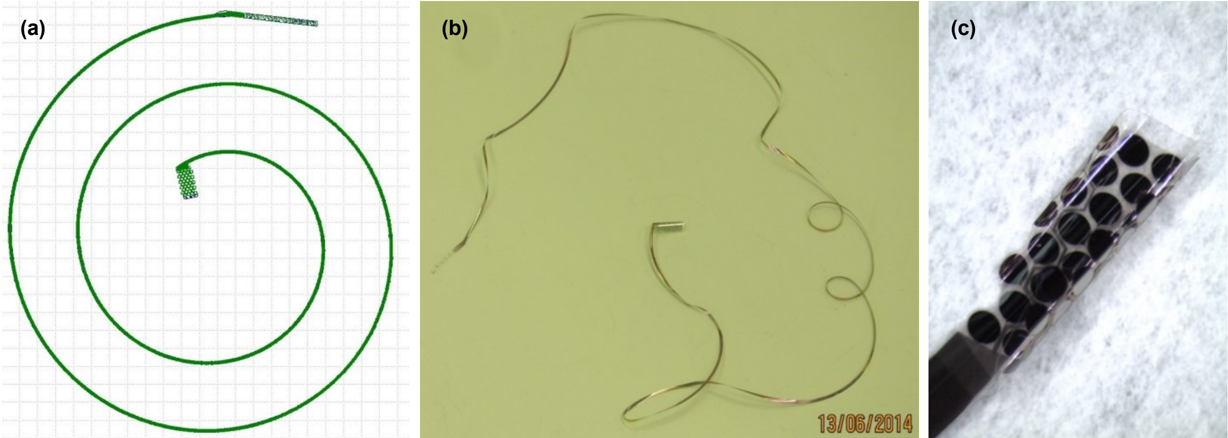


Figure 2.3: SBS lead composed of 40-electrodes and an integrated lead extension. (a) Device design and placement on a 6-inch silicon wafer. (b) Fabricated flexible device after release from the wafer. (c) Close up on the SBS tip containing 40-circular electrodes. Source: InForMed.

2.2.2 Specifications

The SBS flat film technology enables fabrication and subsequent trial implantation of the high-resolution DBS lead. The therapeutic advances of directional stimulation, such as reducing side effects while maintaining the benefits of neurostimulation therapy, are

evident. However, the SBS implant was never brought to the market due to the difficulties associated with connecting the 40-wire proximal end of the lead to the implantable module placed in the skull during surgery [5].

The thin-film fabrication process involves a rather costly and cumbersome wafer-transfer technique and a manual flexible foil release from the wafer. These methods reduce the yield of the manufacturing process. They are also not compatible with IC-microfabrication techniques, which prevents scaling-up of the production. Furthermore, besides a high resistance, the densely packed 40-track metallization compacted on a 1 mm wide and 50 cm long flexible foil makes the SBS lead fragile and prone to damage both during the assembly and during the implantation procedure.

2.3 CHIP-IN-TIP

The issues associated with the multi-wire lead can be largely resolved by moving the electronics from the implantable module to the distal end of the lead – the *Chip-in-Tip* approach (Figure 2.4). After integrating the electronic components, such as multiplexing ASICs and decoupling capacitors on the tip of the SBS lead, the implantable module becomes redundant, and the 40-wire lead can be replaced with a simple, low wire count extension of the standard lead of the pulse generator.

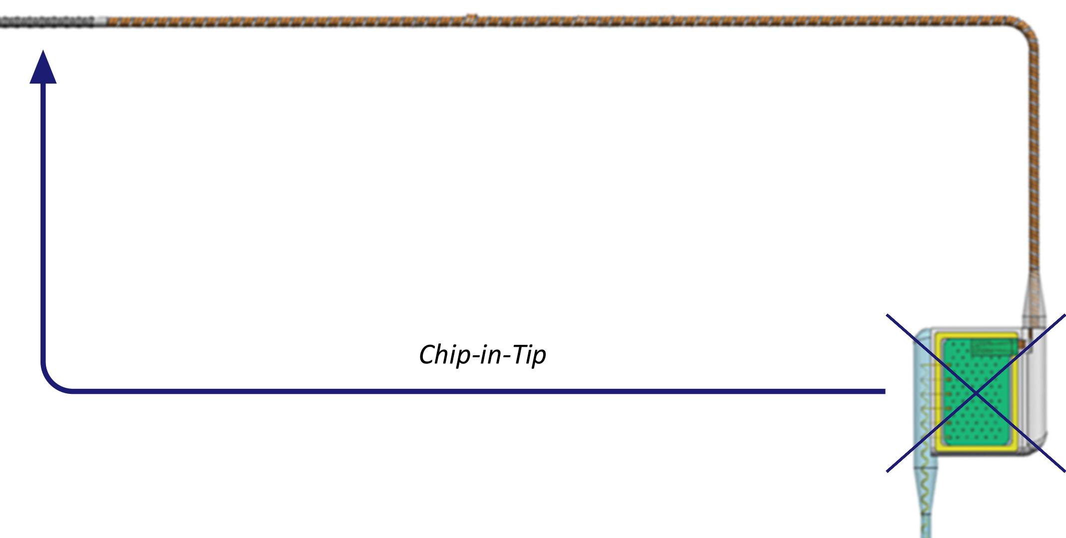


Figure 2.4: Illustration of the Chip-in-Tip approach where electronic components such as multiplexing ASICs and blocking capacitors are moved from the implantable module to the tip of the DBS lead. The implantable module becomes redundant.

2.3.1 Requirements

The Chip-in-Tip deep brain stimulation lead design must comply with a series of requirements set for the whole family of DBS devices. Like the standard DBS leads available on the market, it must have a round and stiff needle-like construction with a diameter of approximately 1.3 mm [6]. This will enable precise and possibly low invasive implantation using surgical tools already available on the market.

Next, the exterior part of the lead that is in contact with the human body must be made of biocompatible and biostable materials that are approved by the Food and Drug Administration (FDA) for use in long-term implantable medical devices [7]. It is highly recommended to only use biocompatible and biostable materials inside the implant to protect the body against harmful substances if the soft encapsulation layer fails.

Furthermore, the safety of the brain tissue stimulation must be secured. Each stimulation electrode is equipped with a blocking capacitor placed in series, usually between the electrode and the multiplexing ASIC. The decoupling capacitor blocks any potentially harmful DC voltage from reaching the brain tissue but allows the AC signal with a specific frequency and voltage (approximately 60-80 Hz and 3 V) to stimulate the brain [8].

On top of the requirements set for the standard DBS device, the Chip-in-Tip design must also meet the needs of directional DBS devices such as the SBS lead. Stimulation directionality must be ensured by incorporating a multitude of electrodes at the approximately 1 cm long distal end (tip) of the lead [9]. The 1 cm long tip of the lead ensures proper implantation into the targeted subthalamic nucleus (STN) with a maximum dimension of approximately 8.5 mm [10]. The electrodes, usually circular or oval, should be distributed evenly around the circumference of the lead. Besides fulfilling the manufacturing requirements, the difficulties connected with the multi-wire extension lead should also be addressed by replacing the complex lead extension with a simpler one with a low wire count (below ten wires).

Finally, the method selected for lead manufacturing should be scalable and compatible with high-yield production. Techniques such as the manual release of devices using dissolvable release layers should be avoided and replaced by scalable manufacturing methods.

2.3.2 Concept

In the Chip-in-Tip concept, *the chip* (ASIC) is integrated directly into *the tip* of the DBS lead. As a result, the number of interconnects in the lead extension can be limited to a few power and signal wires, regardless of the number of integrated electrodes. A consequence of moving the chip to the tip is that now also the DC blocking capacitors, placed between the ASIC and the electrodes, have to be integrated into the tip.

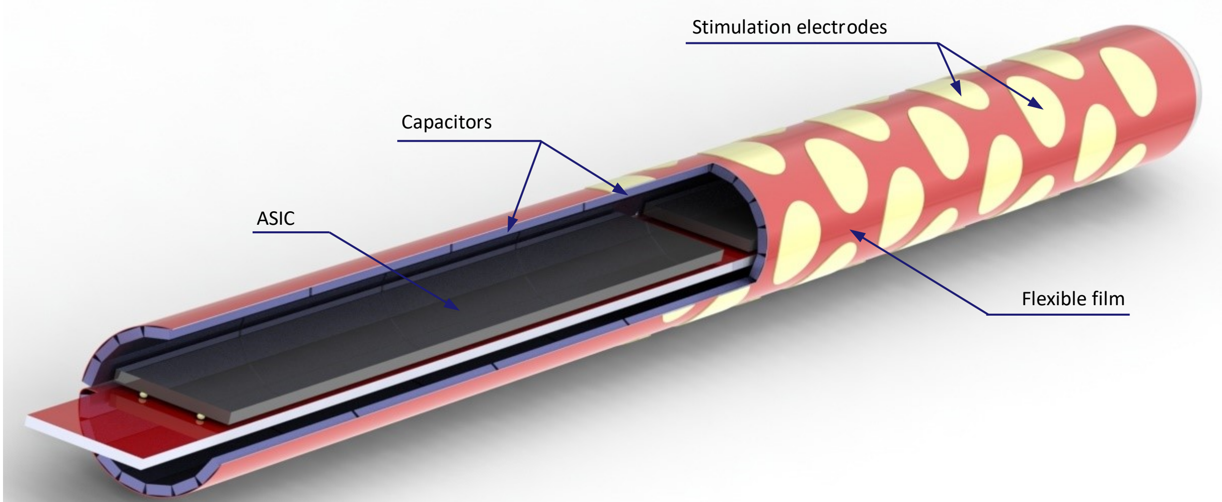


Figure 2.5: A 3D model of the Chip-in-Tip concept incorporating two ASICs (chips) and eighty blocking capacitors inside the tip of the 40-electrode DBS probe.

In the Chip-in-Tip approach, the Flex-to-Rigid (F2R) platform is employed to fabricate a semi-flexible structure into or onto which electronic components can be integrated using monolithic processes [11]. The F2R is a wafer-based, IC-compatible microfabrication process that allows for the fabrication of structures composed of silicon islands connected with flexible interconnects. The starting silicon wafer can already include

structures, such as high-density trench-based PICS3 capacitors [12] that are prefabricated in designated areas of the wafer. The stimulation electrodes can be integrated with the flexible interconnects forming the top layer of the device. After device fabrication, additional electronic components, such as the thinned-down ASICs, can be assembled onto the silicon islands, for example, by using flip-chip. The device with integrated electronics can then be folded into the needle-like shape of the DBS probe and filled with biocompatible silicone to form the DBS lead with 40 electrodes, distributed around its circumference (Figure 2.5).

In order to realize the Chip-in-Tip DBS concept, additional research of the presented technologies and methods is needed. The following topics are investigated in the subsequent sections of this chapter:

- The semi-flexible F2R structure design that enables accommodation of the ASICs and blocking capacitors in the DBS tip (Section 2.4).
- The biocompatible materials, suitable for implantable electronics that can replace the polyimide and aluminum-based interconnects used in the current F2R process (Section 2.5).
- The biocompatible ASIC mounting method (flip-chip) that can be performed on a substrate containing polymer-based interconnects and does not use potentially toxic or degrading materials for stud bumps (e.g., solder or gold) or as underfill (Section 2.6.1).
- The methodology for pre-integration of the blocking capacitors in the silicon starting substrate and the subsequent separation of the silicon islands containing the components using the F2R process with improved resolution (Section 2.6.2).
- The wrapping of the assembled device into a needle-like cylinder and its subsequent filling and encapsulation using biocompatible materials suitable for long-term implants (Section 2.7).

2.4 DIRECTIONAL DBS – THE CHIP-IN-TIP DESIGN

During the F2R-based design of the Chip-in-Tip DBS lead, both the 2D wafer architecture and the 3D shape of the lead after rolling had to be simultaneously taken into account from an early stage of the development. For each design feature, such as the distribution of the electrodes, the number and shape of the capacitor islands, the fabrication-related 2D design aspects, and the performance-related 3D design aspect were carefully evaluated.

In this section, first, the Chip-in-Tip DBS design process is described. Special attention is paid to the placement of the components on the 2D structure. Next, the potential fabrication flow is presented.

2.4.1 Electrode placement and distribution

The developed DBS concept was modeled on the 40-electrode SBS device. The incorporated 40 round electrodes, each with a diameter of 0.7 mm, have a surface area of approximately 0.4 mm^2 following the design optimized by Sapiens. They are distributed evenly over the 5 mm wide and 10 mm long area that is later forming the 1.3 mm diameter probe (Figure 2.6a,b). To enhance the stimulation directionality, the electrodes are organized in a diagonal checkerboard pattern with ten rows, each containing four electrodes. After wrapping the device around the tip, the four electrodes will be evenly distributed around the circumference of the probe (Figure 2.6c).

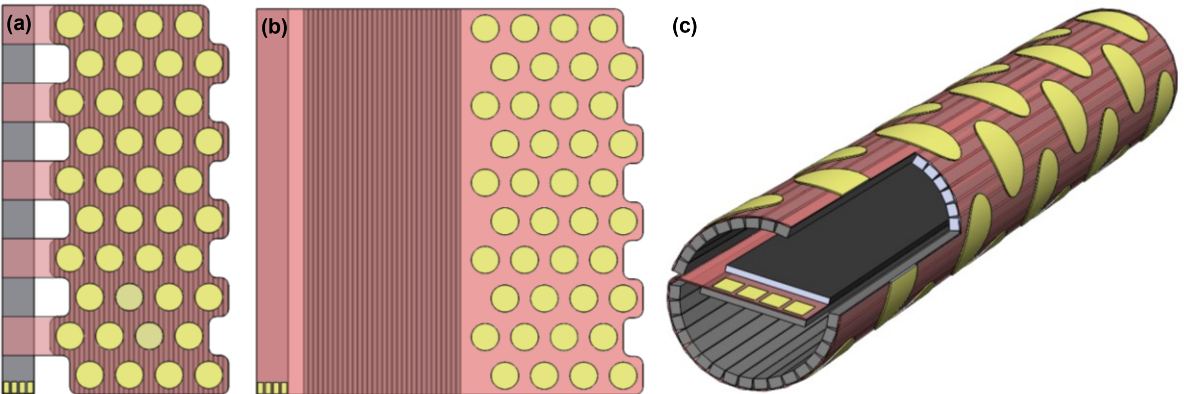


Figure 2.6: The Chip-in-Tip DBS device showing the placement and distribution of the forty stimulation electrodes. (a) In a single-wrap DBS concept. (b) In a double-wrap DBS concept. (c) In a rolled-up state.

Single-wrap design

In the early stage of the design, the electrodes were placed directly above the segmented capacitor islands. The round shape of the probe was achieved in a single wrap, and it exploited the interlocking design of the capacitors (Figure 2.6a). However, during the single-wrap design detailing, several issues and concerns were identified:

- Placement of the electrodes directly on top of the capacitors limits their curvature in the final, wrapped state. The surface of the electrodes will follow the bends determined by the number of capacitor islands distributed around the circumference of the probe.
- The interlocking capacitor island design hinders the placement of capacitors in all the designated areas of the silicon wafer, especially in the small islands at the seam of the probe. Moreover, the presence of rigid silicon islands at the seam makes it difficult to precisely fold the device in a closed cylindrical shape without the risk of forming an approximately 80 μm gap reflecting the device layer thickness.
- The single-wrap design requires a complex design of the metallization running from the capacitors to the electrodes. Interconnects meander between the electrodes that occupy most of the available area. Therefore, their width and pitch are limited, resulting in a high interconnect resistivity.

Double-wrap design

To mitigate the issues mentioned above, the double-wrap design was developed (Figure 2.6b). In this approach, the electrodes are placed on a flexible film area extending to the right from the area with capacitor islands. The device is assembled into a cylindrical shape by wrapping the semi-flexible structure twice around the 1.3 mm circumference of the probe. During the first wrap, capacitors are evenly distributed around the circumference of the probe. During the second wrap, the electrodes are distributed over the capacitors. The separation of electrodes from the capacitors in the double-wrap design enables:

- Rounder surface of the electrodes and thus the whole probe.
- More straightforward capacitor islands design and distribution, which maximizes usage of the available surface area.
- Easier and more robust assembly, which eliminates the risk of gap forming at the seam of the probe.
- More relaxed metallization design with wider and thus more reliable and easier to manufacture interconnects.

Additionally, the double-wrap design makes it much easier to modify the shape and size of the electrodes or even enables the adding of extra electrodes for sensing purposes in the flexible area. Moreover, the relaxed metallization design permits using a single metallization layer to form the electrodes and interconnects.

2.4.2 ASIC integration

The most important element of the Chip-in-Tip design is the ASIC integration. The chip must be flip-chipped onto the designated silicon island of the F2R-structure using platinum bond pads with a diameter of 75 µm. The island with the mounted chip must be folded inside the DBS probe cylinder (Figure 2.5), so the width of the silicon island holding the ASIC is limited to a maximum of 1 mm, and the ASIC thickness must not exceed 100 µm. The silicon island with mounted ASIC is folded to the inside the tip at the bending radius of approximately 55 µm.

After the discussion with project partner Medtronic and ASIC manufacturer ICSense, it was concluded that two ASICs with a length of approximately 8 mm and a width of 1 mm are needed to be able to operate all the electrodes individually. Chips with these dimensions can still be thinned down to 100 µm while maintaining sufficient mechanical strength for handling.

2.4.3 Capacitors spatial distribution

One of the first 3D-design considerations was the distribution of the silicon islands for the decoupling capacitors. On the one hand, increasing the number of islands around the circumference makes the probe rounder and more friendly for tissues (Figure 2.7). On the other hand, the design of the capacitors in PICS3 technology requires specific island dimensions. First, a silicon island thickness of 80 µm was chosen based on the selected trench capacitor technology requirements. Next, the length and width of the islands were determined to ensure adequate offset from the edge of the island, ensuring high-yield fabrication and sufficient mechanical strength [13].

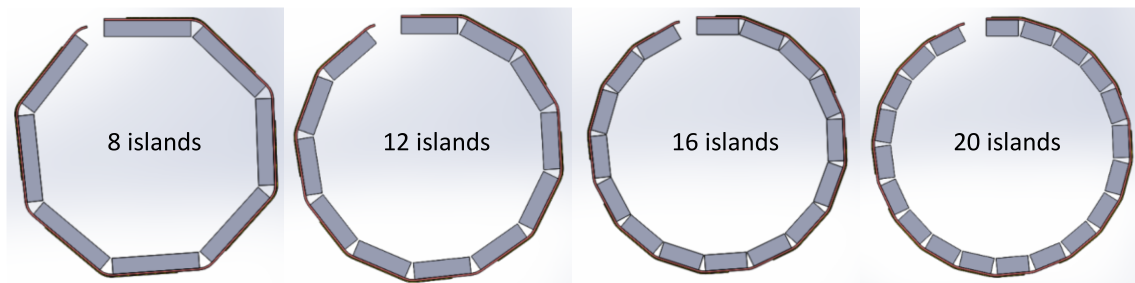


Figure 2.7: Selected designs of capacitor islands number and their distribution around the DBS probe influencing the device roundness.

The most optimal distribution of the capacitor islands, resulting in the best compromise between the PICS3 design restrictions and the roundness of the probe, was achieved by using 16 islands. The individual islands have a width of 210 µm, and they are physically isolated with 40 µm wide trenches. The width of the trench ensures that the capacitors do not touch each other after the device wrapping into the 1.3 mm diameter probe. The physical separation is more space-efficient than isolating the capacitors using junction isolation. The number of islands around the circumference is limited to multiples of four to comply with the number of electrodes per row. In the Chip-in-Tip DBS design, the length of the islands is matched with the length of two rows of electrodes (2070 µm). Two capacitors, connected in parallel, are assigned to each of the eight electrodes. This allows for a simple metallization pattern with relatively short interconnects.

2.4.4 Final design

The final Chip-in-Tip DBS design is shown in Figure 2.8. The length of the DBS structure is 18 mm to be able to accommodate the two ASICs. The design comprises one large silicon island, 128 small silicon islands, and a flexible film area.

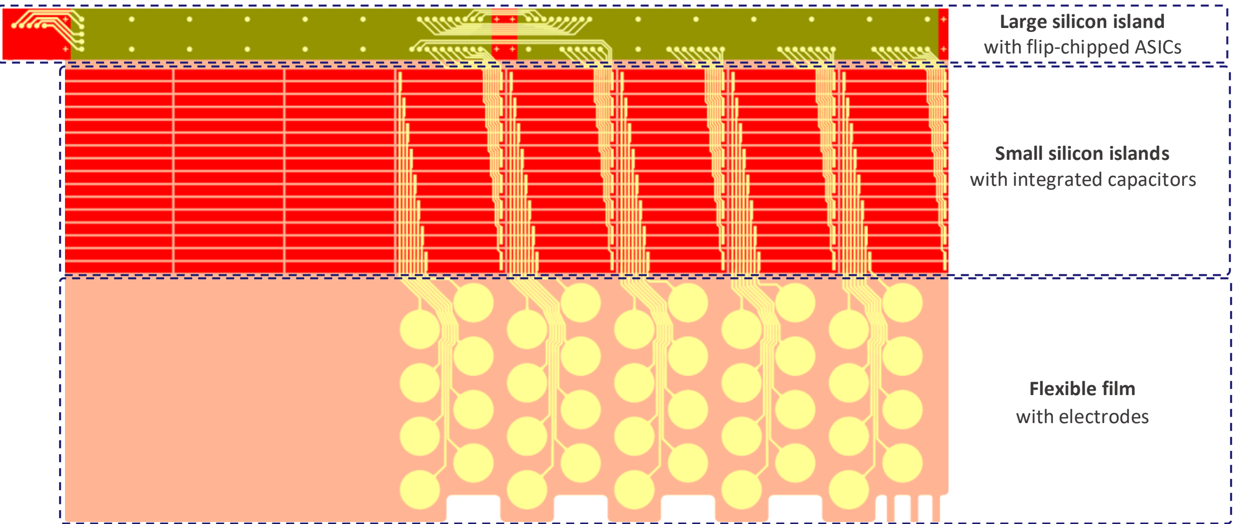


Figure 2.8: The 2D representation of the 40-electrode DBS design with integrated electronic components. The large silicon island (18 mm x 1 mm) contains the flip-chipped ASICs (green). The small silicon islands (210 µm x 2070 µm) are separated with 40 µm wide trenches and accommodate prefabricated decoupling capacitors (red). The flexible film (17 mm x 5 mm) contains 40 flexible electrodes (yellow).

The ASICs are mounted onto the large (1 mm x 18 mm) silicon island. The island extends beyond the semi-flexible structure. On the extended part, bond pads are placed that will be used to connect to the lead extension after the device assembly into a cylinder-shaped probe.

The middle part of the DBS structure is filled with 128 small silicon islands separated by 40 µm wide trenches. The islands are organized in 8 rows of 16 structures. The first five rows (80 islands) are meant for accommodating blocking capacitors. The last three rows of small silicon islands have been added to ensure the conformal shape of the rolled-up probe over its entire length.

The flexible film area contains 40 embedded stimulation electrodes with a diameter of 0.7 mm. The electrodes are distributed in a checkerboard pattern over ten rows, each one containing four electrodes. The end of the flexible film is patterned so that it does not cover any of the electrodes.

All the structures are connected with the flexible interconnects embedded in the flexible film. The individual interconnects run from the large silicon island, through the small silicon island, down to the electrodes. A set of bond pads and interconnects is also designed on the large silicon island to provide an assembly location for the lead extension and the ASICs, and to ensure communication between the chips.

The entire Chip-in-Tip structure, including bond pads, electrodes, and interconnects, is realized using a single metallization layer.

2.4.5 Fabrication flowchart

The F2R-based fabrication flow for manufacturing the final Chip-in-Tip DBS device is shown in Figure 2.9. A uniform thickness of all the silicon structures is ensured by using SOI substrates with an 80 µm thick device layer.

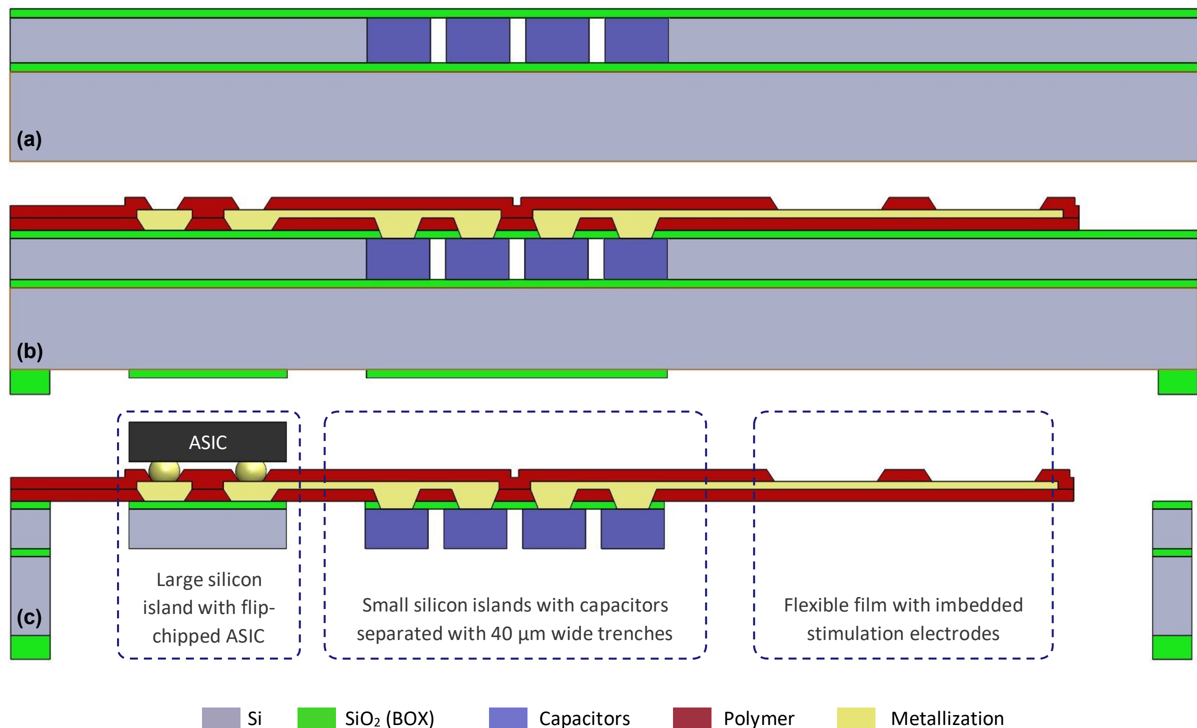


Figure 2.9: The simplified manufacturing process of the Chip-in-Tip DBS probe. (a) Fabrication of the trench capacitors on an SOI substrate with an 80 μm thick device layer. In this flow, the structures are separated using sealable trenches. (b) Fabrication of the flexible film containing 40-stimulation electrodes, flexible interconnects, and a series of bond pads for ASIC attachment. (c) Device thinning and release using the F2R-based backside-DRIE process.

Capacitor prefabrication

The fabrication starts at the foundry of InForMed partner Murata by manufacturing the trench capacitors in the designated area of the device layer. Next, the substrates with prefabricated components are transferred to the EKL cleanroom, where the capacitors are isolated with 40 μm wide and 80 μm deep trenches (Figure 2.9a).

Capacitor separation

In this flowchart, the structures are separated in a front-side DRIE process, during which trenches are etched through a meshed SiO_2 mask [14]. The trenches are subsequently sealed with a PECVD SiO_2 layer to allow for further wafer-scale processing.

Flexible film fabrication

Next, a flexible film (approximately 10 μm thick) with embedded interconnects and electrodes is fabricated (Figure 2.9b). It is composed of two equally thick layers of parylene sandwiching metallization pattern in the stress-neutral plane.

Device thinning and release

Next, the semi-flexible DBS device is thinned down, and the flexible film is released (Figure 2.9c) in a two-step backside DRIE process [14]. After etching, the finished devices remain suspended in the wafer by means of flexible tabs. Thanks to this, the ASICs can be flip-chipped onto the designated silicon island in a wafer-based process. During flip-chip, the risk related to individual device handling can be minimized by automated pick-and-place equipment. Subsequently, the assembled DBS device can be removed from the wafer by laser cutting the flexible tabs.

2.5 BIO-COMPATIBLE MATERIALS FOR IMPLANTABLE DEVICES

The Chip-in-Tip DBS device and its fabrication flow were designed using the Flex-to-Rigid (F2R) technology. Hoverer, the current F2R platform is built on aluminum-polyimide-based flexible interconnects. Neither aluminum, which is prone to corrosion, nor polyimide are recommended for usage in implantable devices by the Food and Drug Administration (FDA). In order to realize the Chip-in-Tip design, the materials used to fabricate the flexible interconnects must be replaced with ones that are biocompatible, biostable, and certified for use in long-term neural implants.

2.5.1 Flexible film

There is a number of polymers that are considered suitable for minimally invasive neural implant interfaces. The most common are polydimethylsiloxane (PDMS) and polymonochloro-p-xylene (parylene C) [15]. In this work, parylene C, further called parylene, was selected as the most suitable flexible film material. It is currently one of the most commonly used polymers to produce and encapsulate minimally invasive biomedical devices. Parylene is also commercially available, and it has the FDA approval with UPS Class VI biocompatibility [15][16][17][18].

Parylene properties

Parylene has excellent electrical and moisture barrier properties, and it is chemically and biologically inert. It also shows significantly lower permeability to gas and water compared to alternative biocompatible polymers such as PDMS [19]. Additionally, it has a low moisture absorption percentage below 1%. Furthermore, polymer-based implant soft-encapsulation is less stiff than the traditional metal-based casing, which improves the structural biocompatibility of the implant by reducing the mechanical mismatch between the device and tissue [15]. Some properties of parylene are listed in Table 2.1.

Table 2.1: Selected properties of parylene C.

Material Properties	**Parylene C**
Tensile strength (MPa)	69 [1,2]
Elongation at break (%)	200 [1,2]
Moisture absorption (%)	0.06-0.6 [3]
Young's Modulus (GPa)	3.2 [4]
Dielectric coefficient at 1kHz	3.1 [1,2]
Resistivity (Ω*cm)	$6\text{-}8.8 \cdot 10^{16}$ [1,2]
Refractive index	1.639 [1,2]
Melting point (°C)	290 [1,2]
Glass transition temperature (°C)	80-100 [2]

[1]Specialty Coating Systems, Parylene C [20]; [2]PCT Parylene Properties [21]; [3]Jeong, 2012 [22]; [4]Noh, 2004 [23]

In the deposition chamber, all the exposed surfaces are coated with a layer of parylene with a uniform thickness. The final layer thickness is determined by the amount of used substrate (dimer) and the exposed surface in the deposition chamber. The process and tool can be tuned to achieve layer thicknesses ranging from several microns to hundreds of microns in a single deposition. The layer is highly conformal with excellent step coverage, and it is pinhole-free and stress-free [16][24].

Parylene deposition

Parylene is deposited using a chemical vapor deposition (CVD) process. First, a dimer substrate (para-xylene) is sublimated in a vaporizer at 150°C in close to vacuum conditions. The dimer gas flows into a pyrolysis furnace set between 690°C, where the dimer structure is turned into vapor saturated with monomer. Next, the vapor passes to the deposition chamber, where the polymerization occurs at room temperature and at a pressure of 30-50 mTorr [25][26].

Parylene in microfabrication cleanroom

Even though parylene is commonly applied in bioelectronics, it is still a relatively new material in a microfabrication cleanroom. Most applications use parylene as an encapsulation layer deposited at post-processing stages, which does not require further device processing in the cleanroom. The layer itself can be introduced in the cleanroom facility without major issues as it does not generate particles nor leaves residues in the tools [17].

However, particles can be generated during the tool preparation for the deposition process and when using standard surface masking techniques (such as masking tapes) to locally prevent parylene deposition. Therefore, the masking techniques must be replaced by cleanroom-friendly methods for selective parylene deposition, and, for the time being, the deposition must occur in an isolated, cleanroom-like space. In the future, a cleanroom-compatible parylene deposition tool should be considered [27].

The next step after introducing the parylene into a microfabrication cleanroom is the development of parylene compatible processes. For the monolithic fabrication of the parylene-platinum-based flexible interconnects that are present in the DBS design, several processing steps (discussed in detail in Chapter 6) must be optimized or developed from scratch:

- A local (one-side) parylene deposition technique,
- A selective and controlled parylene pattering method,
- Cleaning procedures suitable for wafers containing parylene layer,
- Parylene-compatible processing (e.g., <100°C) of the other layers present in the device (e.g., deposition of platinum on top of the parylene and its further patterning),
- Excellent adhesion between the layers of the parylene-based stack.

2.5.2 Metallization

The Chip-in-Tip DBS design assumes a single metallization used for the fabrication of the electrodes, interconnects, and bond pads. Therefore, the selected metallization material and properties must comply with the requirements set for all of these components.

Electrodes

The electrodes are in direct contact with tissue and can significantly influence the performance of the device. Therefore, the selection of the electrode material is mainly driven by the requirements set for the stimulation electrodes. The stimulation electrodes must be biocompatible, biostable, and inert to the surrounding conditions in order to ensure safe and reliable stimulation. Besides, the electrodes must have good electrical and electrochemical properties such as high conductivity, good interface impedance, and charge delivery capacity to be able to deliver appropriate current to the stimulation side [5].

Currently, platinum is the most common material used for stimulation electrodes that make direct contact with tissue. This is mainly because of its high nobility, which makes the material biologically inert due to low reactivity and corrosiveness [28][29][30]. Platinum is also capable of constantly transferring stimulation charges to the tissue over an extended period [31]. Sometimes, a small fraction of iridium is added to the platinum alloy to improve the electrical properties of the metallization, such as charge storage capacity [32].

In this work, pure platinum is selected for the flexible interconnects and the electrodes. It can be straightforwardly deposited in contrast to the platinum-iridium alloys that require a highly optimized deposition process. Physical vapor deposition (PVD), also called sputter deposition, is used in this thesis to deposit a conformal platinum layer and to ensure a good metallization step coverage [33].

Interconnects

The most common materials for flexible interconnects used in implantable devices are gold and platinum or a combination stack composed of these materials [3][34]. In the combination stack, a micron-thick layer of gold (resistivity 2.44 μΩ·cm [35]) serves as the main conductor, and a nanometer-thick layer of platinum (resistivity 10.5 μΩ·cm [35]) serves as a biocompatible capping layer and to form the electrodes. This thesis explores a single-metallization approach. Therefore, only platinum is considered as metallization for the interconnects as well as the electrodes.

The resistivity of platinum is about five times higher than the resistivity of gold or aluminum (2.65 μΩ·cm [35]). To compensate for the relatively low conductivity of the material, the width and thickness of the metal tracks should be maximized. The width is determined by design. The thickness of the interconnects is limited mainly by the flexibility of platinum, which has a relatively high Young's Modulus of 147 GPa [36] compared to aluminum with Young's Modulus of 69 GPa [36], which is used in the standard Flex-to-Rigid process.

Bond pads

The bond pads are located on the large silicon island, and they are formed in the same step as the other elements of the metallization (electrodes and interconnects). The bond pads are designed to enable flip-chip of the ASIC directly onto the semi-flexible DBS structure. The bond pads metallization must be thick enough to ensure good results during the bumping process [37].

In order to ensure the necessary flexibility and conductivity of the platinum-based flexible interconnects and sufficient thickness of the bond pads, the thickness of the platinum layer used in this thesis is limited to 600 nm. This thickness is also in line with the parylene-platinum-based interconnects used previously in the directional SBS device designed by Sapiens [3].

2.6 COMPONENT INTEGRATION

Two types of components have to be integrated into the tip of the DBS probe. These are the two multiplexing ASICs and eighty DC blocking capacitors. The integration processes are proposed in this subsection.

2.6.1 ASICs integration

The two 1 mm wide, 8 mm long, and 100 µm thick ASICs are flip-chipped onto a dedicated silicon island that contains an array of 600 nm thick platinum bond pads with a diameter of 75 µm. For biocompatible flip-chipping, a platinum-based stud bumping process was developed, replacing the common solder or golden stud bumps.

The platinum-based flip-chip approach involves some challenging steps. For example, handling of the exceptionally thin and long ASICs and their attachment to the semi-flexible DBS structure requires practice and excellent manual skills. To ease the process, the flip-chip can be performed on a wafer level with the devices still attached to the wafer by means of the release tabs. A handle wafer with mirrored topography can be used to eliminate the height differences of the DBS structures.

Furthermore, some technological development of the flip-chip method itself is required. First of all, the temperature needed to perform stud bumping or chip bonding might exceed the temperature budget set for the parylene-containing substrate. Secondly, platinum is not a common material for flip-chip bumping. Therefore, a process for making well-adhering platinum stud bumps on platinum bond pads must be developed. Finally, extra attention must be paid to the chip underfill process. The underfill material must be fully biocompatible, and the process itself must be compatible with the parylene-based device.

The technological challenges and development points, such as fully platinum-based flip-chip or biocompatible underfill, have been investigated together with a project partner, Fraunhofer IZM. The results are discussed in Chapter 3.

2.6.2 Capacitor integration

As mentioned before, the decoupling capacitors are fabricated by InForMed partner Murata in their PICS3 deep trench capacitor process. The wafers with capacitors are further processed in the DBS fabrication facility, EKL. The first challenge is the inter-facility processing of the substrate. For this, a mutual design, a common alignment strategy, and compatible processing methods must be established. The strategy for a common product and process design and following feasibility study are discussed in detail in Section 4.5.

The next challenge is a precise separation of the prefabricated capacitors into islands (L x W x D: 2070 µm x 210 µm x 80 µm) by means of 40 µm wide and 80 µm deep trenches. In the standard F2R process, the islands are separated by 350 µm wide trenches, etched from the backside of the wafer, that are only 50 µm deep [11]. Two technologies have been developed to enable the capacitor integration process with the required narrow and deep trenches.

One method, described in Section 4.3, exploits a sealable trenches technology (Section 4.2) to define the silicon islands from the front side of the wafer and continue the wafer-level fabrication of the DBS structures after the trenches have been sealed. The other method employs a novel cavity-BOX SOI substrate. It allows for high-resolution device layer patterning during the backside DRIE process by using a pre-patterned hardmask formed in the buried oxide layer. The development of the cavity-BOX substrate and its application to the F2R process is presented in Section 4.4.

2.7 PACKAGING

After fabrication, the flat DBS structure containing the integrated blocking capacitors and ASICs is suspended in a wafer frame. The structure still needs to be wrapped into a 1.3 mm diameter cylinder and packaged to form the final DBS lead. The following aspects of packaging are considered in this section:

- Device wrapping into a needle-like probe and consequent filling of the cylinder,
- Attachment of the lead extension to the microfabricated DBS tip,
- Final encapsulation of the DBS probe.

The device assembly into a complete system is not within the scope of this project. Instead, the focus is on the development of the device wrapping and filling technique. These topics are briefly introduced in this section and discussed in detail in the corresponding sections of Chapter 5. The other aspects of the packaging specific for the Chip-in-Tip DBS design, namely the lead extension attachment and final device encapsulation, are only briefly considered.

2.7.1 Wrapping

The first stage of the packaging process is wrapping the DBS structure, with integrated capacitors and flip-chipped ASICs, into a probe with a diameter of 1.3 mm. In the case of rolled/wrapped devices such as the DBS probe, the most common practice is to use a thin titanium rod to which the device is attached and wrapped around it. The rod stays inside the device, and it becomes its structural element. The rod also ensures the stiffness of the device, which in the case of DBS probes, is crucial for proper device implantation.

In the Chip-in-Tip design, the inside of the DBS device is occupied with the silicon island holding the ASICs. This implies that using a solid rod to wrap the device around it is not possible. Therefore, a custom tool has been designed to enable the wrapping of the device into a cylindrical shape (Figure 2.10). The tool enables fixing of the DBS device between two metal strips placed under tension, and wrapping of the device. Then, the tension is released, and the metal stripes are removed from the inside of the wrapped device. The tool and wrapping procedure are described in detail in Section 5.2.

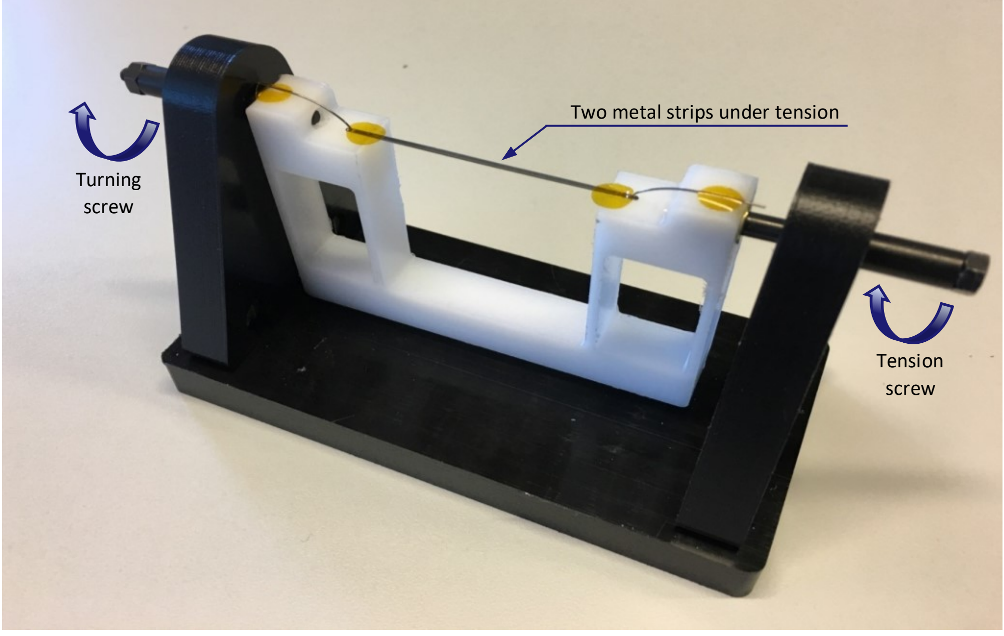


Figure 2.10: Custom-designed tool for wrapping the DBS device into a cylinder-shaped probe. Source: PInS.

In this method, there are no additional elements needed to wrap the DBS device into its needle-like shape. The two flexible layers of the double-wrap design are glued together using a thin film of biocompatible adhesive. The required stiffness of the DBS probe is ensured by the silicon islands distributed around its circumference and the cylinder filling material.

In general, the Chip-in-Tip DBS probe was designed so that the structures are self-aligning around the circumference during the double wrapping procedure. Several parameters of this manual process must be optimized in order to achieve the required shape and dimensions of the probe. For example, the transversal force applied to the device itself must be carefully adjusted not to cause damage to the device and yet to enable wrapping of the device into a closed cylinder with a properly closed ring of capacitors without overlapping the electrodes. The specific solutions and results for this procedure are presented in Section 5.2.

2.7.2 Filling

After wrapping, the DBS device is hollow with a silicon island, holding the ASICs, floating inside the cylinder. The next step in the packaging process is filling the cylinder with a biocompatible material. From the construction point of view, the filler has to ensure the required device stiffness and mechanical strength by filling the cylinder and fixing all the loose elements. On top of that, the filling material must be biocompatible and suitable for application in long-term implantable devices. Finally, the filler must be thin enough to flow into all the voids inside the cylinder, also the hard-to-reach spaces between the capacitor islands.

Currently, the most common biocompatible filler used in DBS probes is silicone rubber (PDMS) [38]. To properly fill the DBS device, a relatively thin filler must be applied, possibly in combination with modern filling methods, such as injection molding or a vacuum centrifuge process. Silicon rubber tends to be too viscous (e.g., medical-grade silicon rubber 115 Pa·s [39]) to be able to fill the narrow spaces, such as the <40 µm gaps between the capacitors. Therefore, in Section 5.3, a medical-grade epoxy (viscosity from 0.1 to 0.2 Pa·s [40]) is tested as an alternative filling material for the DBS devices.

2.7.3 Lead extension attachment

Another aspect of packaging that has to be considered is the attachment of the lead extension to the DBS probe. In conventional DBS systems, the lead extension is an integral part of the lead and does not need to be separately attached to the probe (tip). The flexible device with electrodes and extension wires is fabricated as one thin film structure and is consequently rolled to form the complete DBS lead [3][41].

In the case of the Chip-in-Tip design, the F2R-based semi-flexible DBS probe includes the integrated components, electrodes, and a series of bond pads located on an extended part of the inner silicon island. These bond pads are designated for the attachment of the lead extension (Figure 2.11). The flat lead extension can be fabricated separately using, for example, thin-film technology developed by Medtronic. It can be attached to the DBS probe using a biocompatible bonding technique, such as platinum-based wire bonding and wrapper to form a coiled led extension. Subsequently, the connection site and the lead extension can be filled with silicone rubber or medical-grade epoxy to form one uniform DBS lead.

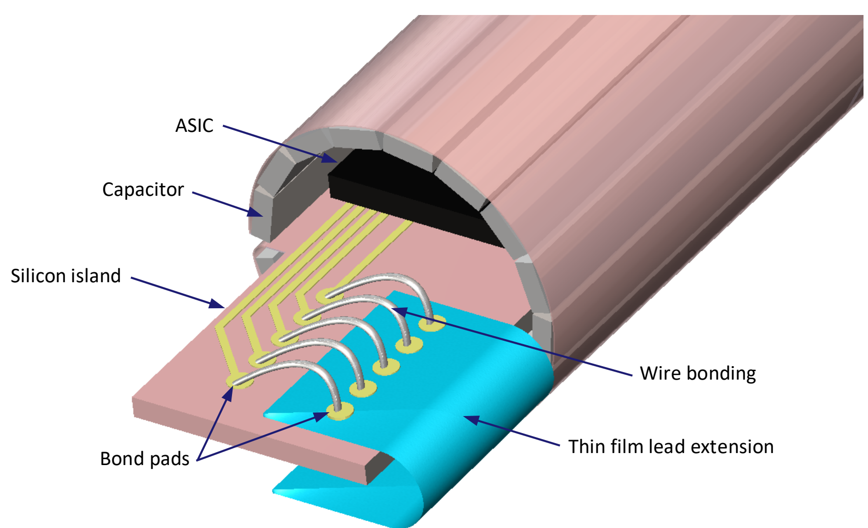


Figure 2.11: Attachment of the flexible lead extension directly onto the DBS structure using optimized platinum-based wire bonding technique.

In order to successfully realize this approach, a method for attaching the flexible, polymer-based lead extension to the 80 µm thin DBS probe must be developed. Here, aspects like temperature budget or bonding pressure must be considered [37]. Another difficulty might arise from the relatively thin bond pads formed from only 600 nm thick platinum. These topics are not within the scope of this thesis.

2.7.4 Encapsulation

The final packaging stage of almost any bioelectronics device is encapsulation. Encapsulation applied to long-term implantable devices must be biocompatible, biostable, and have good barrier properties [42]. The purpose of the encapsulation layer is to protect the device from moisture and harsh bodily conditions and protect the patient from the release of potentially harmful substances present in the implant or formed as a result of corrosion [43].

Soft implants with electrodes, such as spinal cord stimulators, must remain flexible to perform under constant mechanic stress in the moving body. Furthermore, biomedical devices implanted in soft tissue, such as the DBS probe, need to have a soft encapsulation layer to ensure good structural biocompatibility (mechanical match) with the surrounding tissue [15][24]. These devices can be encapsulated with polymers such as silicon rubber (PDMS) or parylene [15][44].

Polymer-based soft encapsulation, often called non-hermetic encapsulation, allows for water to saturate the layer. However, if good adhesion is ensured, the moist will not condensate on the surface of the device, causing the device to fail [43]. Depending on the polymer and the underlying surface, various adhesion enhancing treatments such as O_2 plasma or a monolayer of an adhesion promoter (e.g., A-174 for parylene on SiO_2) can be applied [15][44][45][46]. Furthermore, the barrier properties and adhesion of the soft encapsulation can be improved by applying additional nanometer-thin layers of ceramics such as alumina, SiO_2, and Si_3N_4 [24][47][48].

The FDA approved parylene is the most common material used for biomedical applications due to its low permeability and water absorption, reasonable compatibility with microfabrication cleanroom environment, and the ability to form thin, conformal, stress-free, and pinhole-free layers [15][16][19][49].

A thin film of parylene is also considered as a final encapsulation layer for the assembled Chip-in-Tip DBS lead. The platinum electrodes would have to be reopened after the conformal parylene deposition process is complete. For this purpose, a 3D lithography technique can be developed involving, for example, laser ablation of a rotating rod, or directional plasma etching through a physical shielding mask or dome with orifices aligned with the electrodes. The required development and optimization of such a custom lithography process performed on a round DBS device are not within the scope of this thesis.

2.8 CONCLUSIONS

In this chapter, the Chip-in-Tip design for realizing a directional, 40-electrode DBS probe with high stimulation resolution has been developed. The design allows for the integration of multiplexing ASICs (chips) and DC blocking capacitors directly onto/into the tip of the DBS probe. As a result, a more robust DBS lead extension with a low wire count can be used. The Chip-in-Tip design facilitates an easier implantation procedure and ensures overall implant miniaturization.

Next, monolithic DBS device fabrication and capacitors integration processes have been developed based on the Flex-to-Rigid (F2R) platform. In order to realize the design, technology modules such as inter-facility design and process alignment (capacitors integration), high-resolution silicon islands separation (sealable trenches and cavity-BOX SOI), and a scalable process for the fabrication of biocompatible parylene-platinum-based interconnects have been proposed. Consequently, the biocompatible mounting of strip-shaped ASICs (1 mm wide, 8 mm long, and 100 µm thick) onto the F2R base DBS structure, such as platinum-based flip-chip, has been explored. Finally, the possible packaging techniques for wrapping the device into a 1.3 mm diameter cylinder, voidless filling of the cylinder, attaching the flexible lead extension to the DBS structure, and complete device encapsulation with a non-hermetic layer have been discussed.

The design, fabrication, and packaging strategies presented in this chapter will enable the miniaturization and scalable fabrication of a variety of medical microelectronic devices. Moreover, by using biocompatible materials, the developed techniques are also suitable for implantable devices, such as neurostimulators, intended for long-term use in the human body. The established integration process permits for the use of high-quality components and achieving exceptional device resolution (e.g., by increasing the number of stimulation electrodes) without compromising the robustness or increasing the complexity of the device. Moreover, the scalable fabrication process can reduce production costs and make the devices more accessible, which in the case of bioelectronics means more affordable treatment.

This thesis concentrates on developing the enabling technologies necessary to realize the directional DBS Chip-in-Tip device, including demonstrating the feasibility of the developed methods using non-functional test structures.

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3

ASIC INTEGRATION – BIOCOMPATIBLE FLIP-CHIP

3.1 INTRODUCTION

The Chip-in-Tip deep brain stimulator (DBS) integrates two ASICs flip-chipped directly onto a 1 mm wide silicon island that is located in the center of the DBS tip with a diameter of 1.3 mm (Figure 3.1).

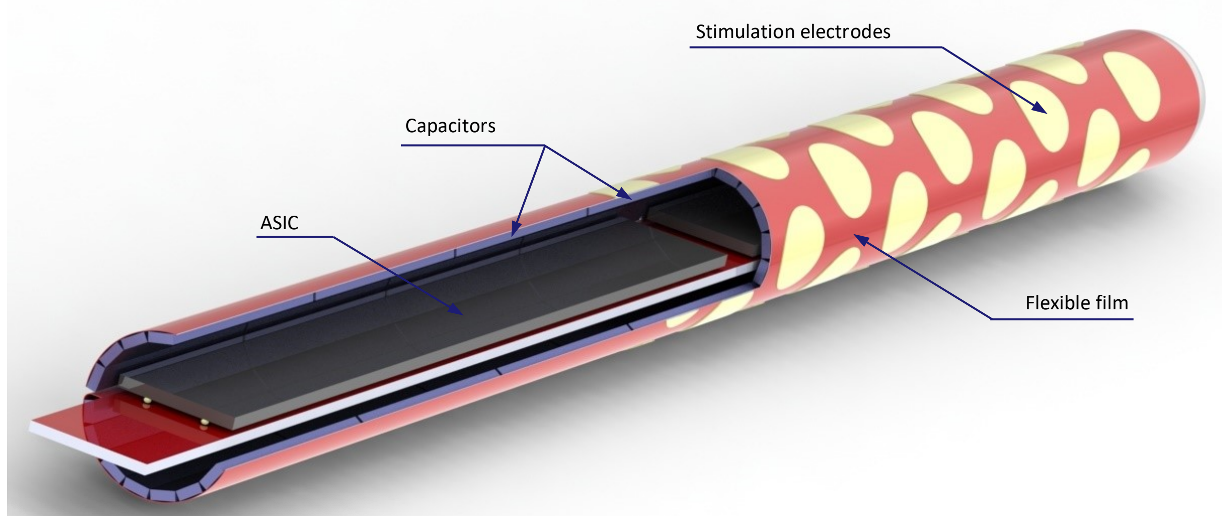

Figure 3.1: 3D model of the Chip-in-Tip concept incorporating two ASICs (chips) and eighty blocking capacitors inside the tip of the 40-electrode DBS probe.

Flip-chip minimizes the necessary area for the chip integration by bonding the chips directly above the substrate using stud bumps. Stud bumps are small „balls" of conductive material deposited directly onto the bond pad of the substrate (Figure 3.2a). Subsequently, the ASIC is flip-chipped onto the bumped substrate in a bonding process (Figure 3.2b). Finally, the bumping area between the substrate and the ASIC is underfilled with a polymer (Figure 3.2c).

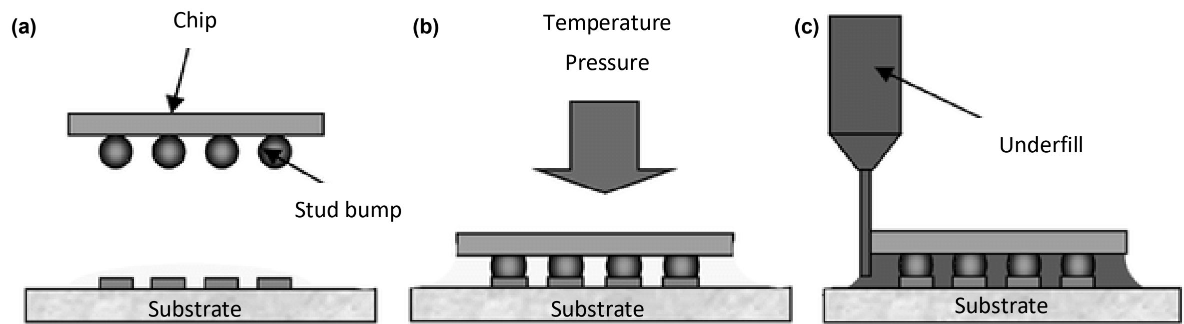

Figure 3.2: The steps of the flip-chip process. (a) Chip bumping. (b) Bonding of the structures. (c) Underfill. Source: Adopted form Zhang, 2004 [1].

3.1.1 Bump material

The most popular materials used for stud bumping are gold and, less often, copper. Next to being environment-friendly, gold stud bumps are reliable, and they can be made at a pitch as small as 50 µm [2].

The bond pad metallization must be compatible with the bump metallization. For example, gold stud bumps require gold or aluminum bond pads to ensure good adhesion and make the bonding possible. If the original bond pad metallization is not compatible with the stud bump material, an additional under bump metallization layer can be deposited on the original bond pads.

3.1.2 Bonding

After the bumping process, the ASIC is flipped and aligned directly above the substrate with the stud bumps. This can be done manually or by employing an automatized pick-and-place technique. Next, the ASIC and the substrate are bonded together using pressure and heat (thermocompression bonding) or pressure, heat, and ultrasonic energy (thermosonic bonding) [2]. The bonding conditions vary depending on the bond-pad and stud bump materials. For example, gold-gold bonding requires temperature of approximately 300°C and pressure of 40 kN, while aluminum or copper to gold bonding requires approximately 400°C and 70-80 kN [3]. In the thermosonic process, the pressure and temperature can be significantly reduced by adding ultrasonic energy. For example, using thermosonic gold-gold bumping requires only 100-160°C and 0.2-0.5 N/bump [4].

3.1.3 Underfill

The last step of the flip-chip process is filling the empty space between the substrate and the chip with a suitable underfill material. This provides mechanical strength to the connection, ensures electrical isolation between not-bonded areas of the chip and substrate, and equalizes the thermal expansion mismatch between the bonded elements. Conventional underfills are non-conductive, thermoset polymers based on, for example, liquid silicone rubber [5] or bisphenol A [6]. They often contain the addition of silicon oxide particles to increase the stiffness of the underfill. The curing (thermosetting) process takes from a quarter up to a couple of hours and is performed at approximately 150°C [7], depending on the underfill composition. Some special application epoxies can be cured at room temperature, which can take up to several days [8].

3.2 TEST STRUCTURES

Dedicated test structures were designed to aid the development of the biocompatible flip-chip technology module. These structures mimic the layout and the layers present in the final DBS design (see Section 2.4). The structures were developed and fabricated by the TU Delft at the EKL cleanroom facility.

3.2.1 Design

Each test structure is composed of two silicon islands (Figure 3.3). The smaller island (1 mm x 8 mm), further called chip, mimics the ASIC, and the larger island (3.5 mm x 9.5 mm), further called substrate, mimics the substrate. The chip contains 75 µm diameter bond pads for flip-chip testing. The substrate contains a corresponding but mirrored layout of 75 µm diameter bond pads located in the center of the island. Additionally, 600 µm and 800 µm diameter bond pads are included to evaluate the

electrical connections after bonding. The larger bond pads are located at the edges of the substrate, and they remain accessible after the flip-chip.

On the chip, as well as on the substrate, the bond pads are connected with 40 µm wide metal tracks forming a daisy chain pattern. After flip-chip, the combined metallization of the two bonded structures (the chip and the substrate) forms closed circuits. These circuits can be used for evaluating the bonding process.

Two types of metallization materials are used to fabricate test structures for the flip-chip experiments: aluminum and platinum. The aluminum-based device can be fabricated faster due to already established processing methods. The aluminum-based devices were used to pave the way towards the platinum-based flip-chip experiments.

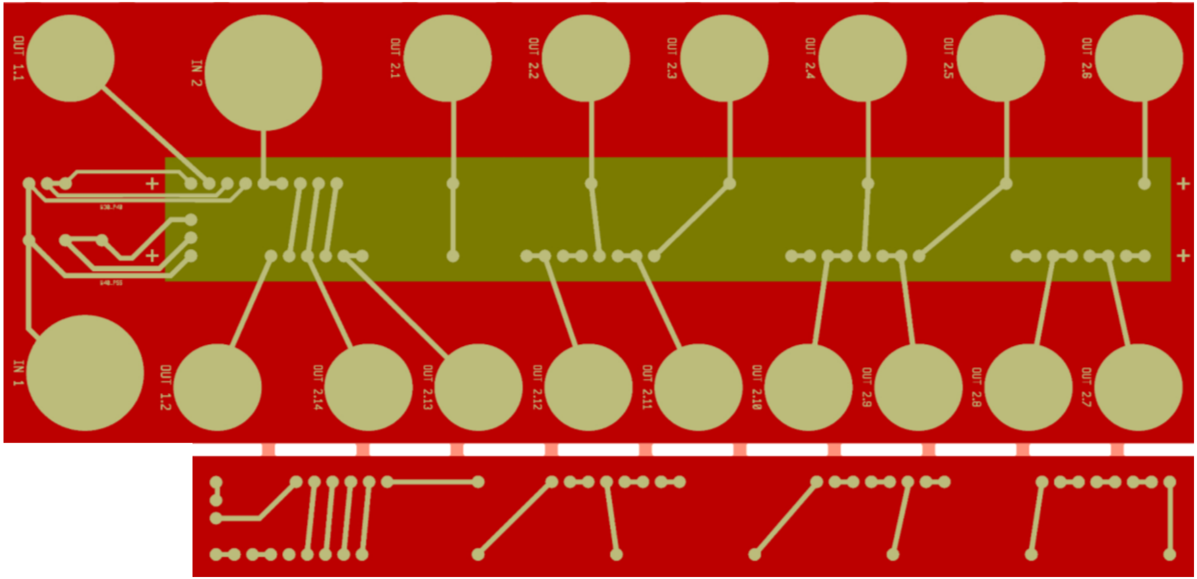

Figure 3.3: Two-element parylene-based test structure for biocompatible flip-chip development. Top structure (substrate): larger silicon island mimicking the DBS device. Bottom structure (chip): small silicon island mimicking the ASIC.

3.2.2 Fabrication

The test structures are fabricated on 525 µm thick 4-inch silicon substrates. A 2 µm thick PECVD SiO_2 layer is first deposited as an insulator and a structural layer during the process. Next, a 5 µm thick layer of parylene is deposited and patterned at the location of the bond pads using an O_2-based directional plasma. Next, the metallization is deposited and patterned. The sputter-deposited aluminum metallization is 2 µm thick, and it is patterned using chlorine-based plasma. The sputter-deposited platinum metallization is 600 nm thick, and it is patterned by argon-based ion-milling using a photoresist mask. After removing the photoresist mask, a second 5 µm thick layer of parylene is deposited and patterned to reopen the bond pads. The cross-section of the test structure is shown in Figure 3.4.

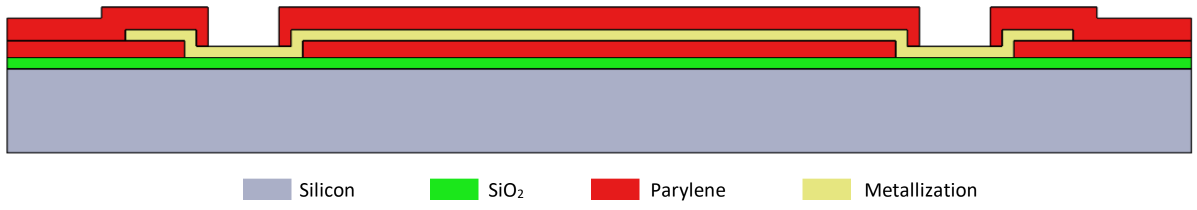

Figure 3.4: Cross-section of the test structure (chip) with bond pads and parylene-based metallization.

In the final device, the metallization of the bond pads is fabricated directly on the rigid silicon dioxide layer. It permits reliable stud bumping and bonding processes, both of which use compression and a raised temperature, which cannot be performed on a soft parylene layer. The metallization of the interconnects is sandwiched between two layers of parylene, mimicking the flexible interconnect stack. The example of fabricated test structure is shown in Figure 3.5.

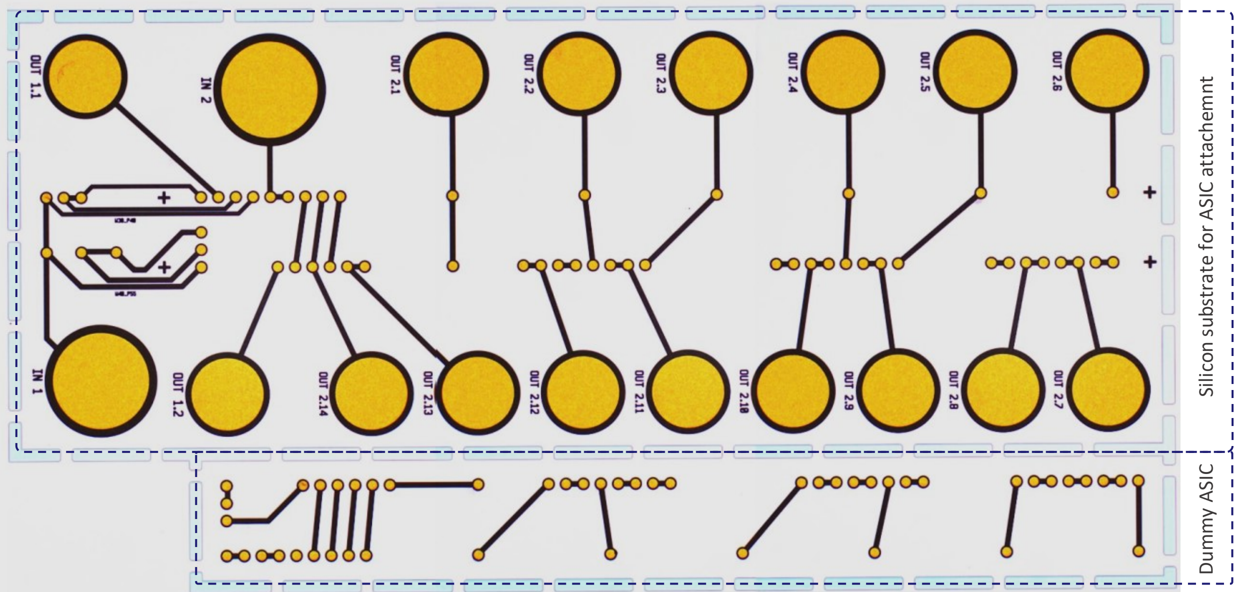

Figure 3.5: Top-view image of the fabricated aluminum-based test structures for flip-chip experiments.

3.3 ENABLING TECHNOLOGIES

Standard flip-chip processes or materials are not always biocompatible, and thus they might not be suitable for long-term implants. Moreover, this technique has not been designed to integrate thin chips (100 μm thick) onto a substrate containing a temperature-sensitive polymer (parylene). In this section, several enabling technologies are investigated that are necessary for the development of a biocompatible flip-chip process suitable for bonding substrates containing a parylene-based flexible film:

- Biocompatible platinum stud bumping on a brittle silicon substrate,
- Platinum-based bonding compatible with silicon-parylene-based structures,
- Biocompatible underfill of an area of 1 mm by 8 mm with a narrow clearance of approximately 30 μm.

The experiments were conducted in collaboration with flip-chip specialists from Fraunhofer IZM (FIZM), Berlin. The samples were designed and fabricated at the EKL facility in Delft, while the majority of the flip-chip processes were perfumed at FIZM.

3.3.1 Platinum bumping

The first step of the flip-chip process is the deposition of small platinum stud bumps on top of the bond pads of one of the elements to be bonded (chip or substrate), a process commonly referred to as "bumping." For this, the Kulicke&Soffa (K&S) IConn ProCu bumper/bonder tool was used. Platinum is a rather unusual material for stud bumping. Because it is much harder than gold, which is commonly used for stud bumping (Young's modulus of 147 GPa for platinum [9] versus 74 GPa for gold [9]), it is more challenging to create platinum stud bumps.

In the experiments, the bumping parameters were optimized to ensure good platinum ball adhesion, and at the same time, avoid substrate damage such as cratering. The optimized parameters for stud bumping using a 25 µm thick platinum wire are listed in Table 3.1.

Table 3.1: Optimized parameters for platinum stud bumping.

Parameter	Value
Wire thickness	25 µm
Temperature	160°C (Al substrate) 120°C (Pt substrate)
US current	115 mA
Force	0.6 N
Time	150 ms
Atmosphere	Nitrogen

In the case of the devices with the 2 µm thick aluminum bond pads, the wafer was diced into single 525 µm thick devices before bumping, and the platinum bumps were placed on the substrate at 160°C. In the case of the devices with 600 nm thick platinum metallization, the bumping was performed at 120°C on wafer quarters, and the bumps were placed on the chip. The platinum-based wafer quarters were diced after the bumping process was completed.

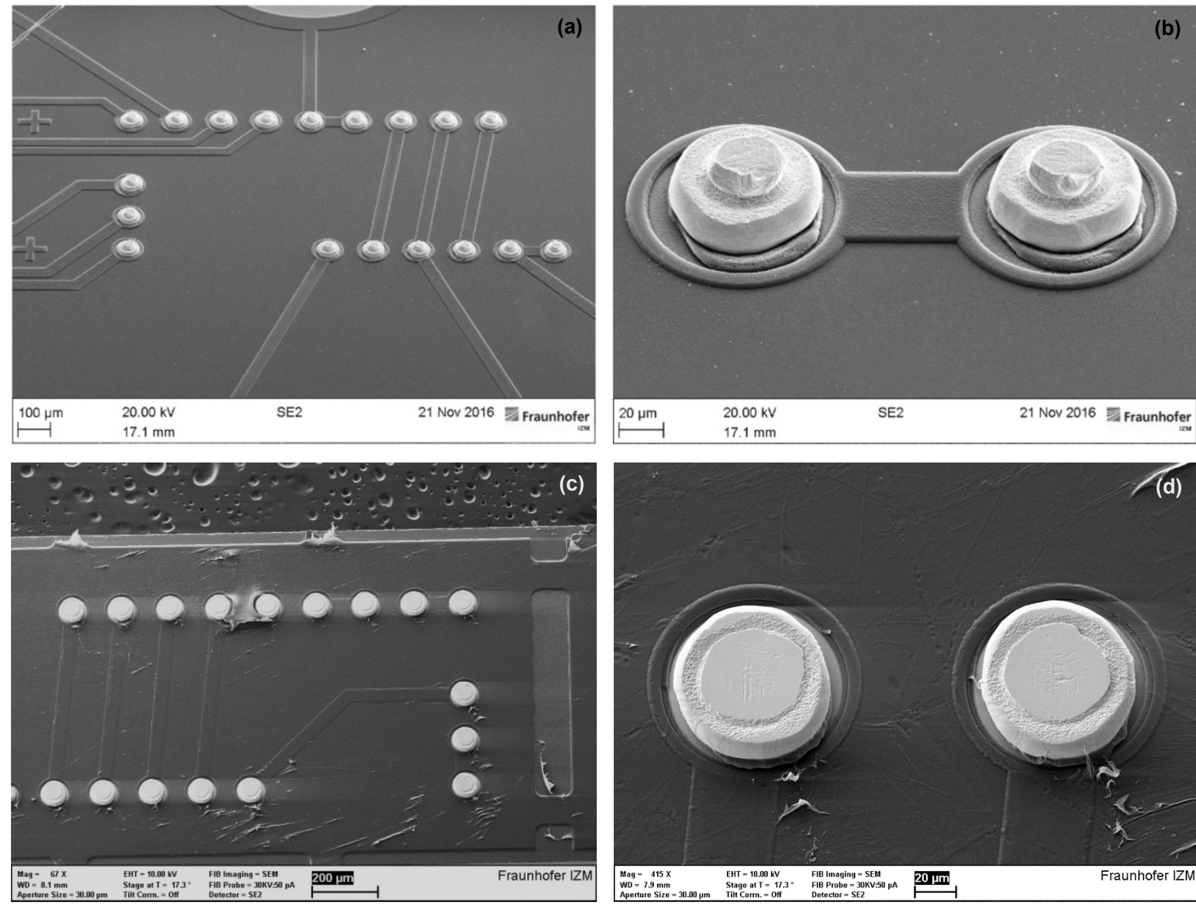

Figure 3.6: SEM image of the platinum stud bumps on the 75 µm diameter bond pads. (a-b) Stud bumps located on the substrate part of the test device with 2 µm thick aluminum bond pads. Deformation of the aluminum bond pads metallization due to applied pressure is visible. (c-d) Stud bumps located on the substrate part of the test device with 600 nm thick platinum bond pads. Source: FIZM.

After optimizing the bumping parameters, the platinum stud bumps were properly attached to the 75 µm diameter bond pads with 2 µm thick aluminum (Figure 3.6a,b) and to the bond pads with 600 nm thick platinum (Figure 3.6c,d). The average single bump shear stress of 84 MPa, measured using the Nordson DAGE 4000Plus shear test equipment, indicates good bum adhesion to the substrate [10]. Furthermore, no damage to the substrate or the parylene layer was observed after the bumping process.

3.3.2 Bonding

The bonding process was performed on the samples previously bumped with platinum. During bonding, the SET FC150 Die/Flip Chip Bonder was used [11]. The parameters of the bonding process were optimized first for the aluminum-based samples and next for the platinum-based samples. The monitored parameters were: deformation of the bond, adhesion between the bonded structures, and devices damage.

Platinum bonding of devices with aluminum bond pads

The devices with the aluminum bond pads were flip-chipped using thermocompression bonding performed in an inert atmosphere. The optimal bonding parameters are collected in Table 3.2. Before the bonding process, the samples were preheated to 100°C to reduce the bonding time. After the bonding, an extended cooling down to 100°C was performed to slowly release stresses accumulated in the joins during the bonding.

Table 3.2: Optimized parameters for thermocompression bonding of the samples with 2 µm thick aluminum bond pads and platinum stud bumps.

Parameter	Value
Substrate temperature	220°C
Chip temperature	220°C
Force	4.5 kg
Time	30 sec
Atmosphere	Nitrogen

Figure 3.7 depicts a top-view X-ray and CT image of the optimized aluminum-platinum bonded structures, and Figure 3.8 depicts the cross-section SEM images. Both the X-ray and the CT images confirm proper alignment and do not show any damage to the bonded structures.

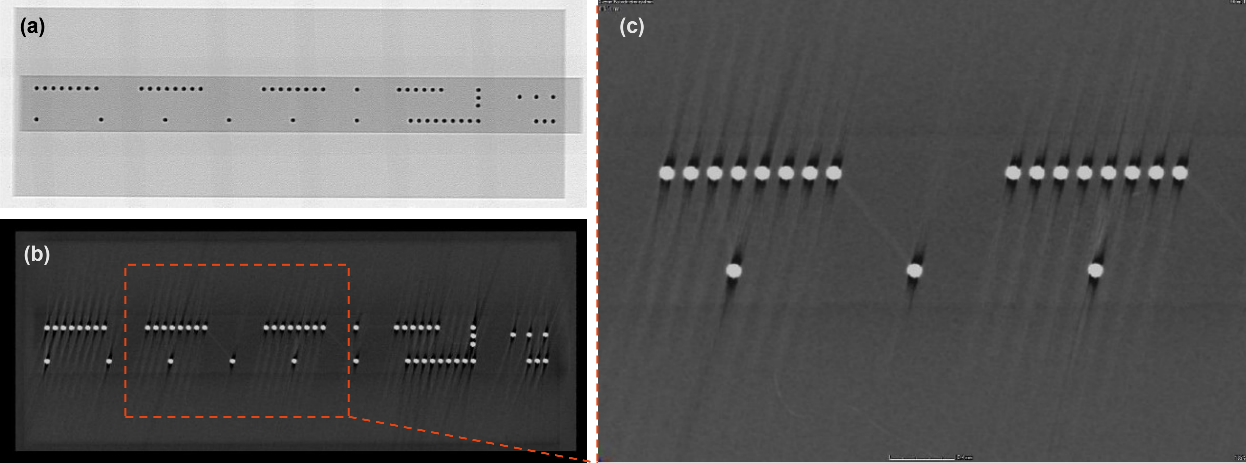

Figure 3.7: Top-view of the flip-chipped structures with aluminum bond pads and platinum stud bumps. (a) X-ray image. (b) CT image. (c) Close-up of the CT images. The diagonal artifacts on the CT images are due to the high contrast of the platinum bumps. Source: FIZM.

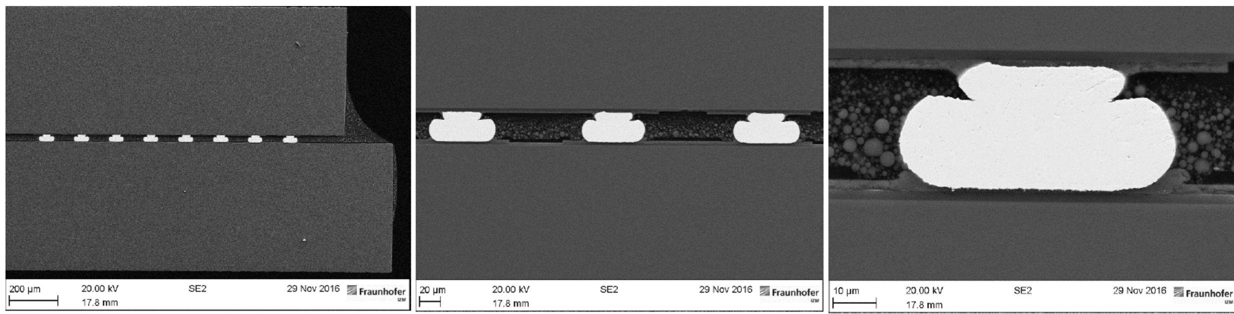

Figure 3.8: Cross-section SEM images and their close-ups of the bonded 525 µm thick devices with aluminum metallization and platinum stud bump. The structure is underfilled with polymer for examination purposes. Source: FIZM.

In Figure 3.8, the structures are underfilled with a polymer to be able to make a cross-section. The stud bump deformation is good. The bonding surfaces are conformal and without voids ensuring a proper connection between the structures. The platinum stud bump height after bonding is approximately 30 µm. The bonded structures are properly adhering to each other, and an electrical connection has been established. The resistance of the circuit measured between inlet IN1 and outlet OUT1.2 (see Figure 3.9) is 5.4 Ω, which is within the expected range (calculated resistance is 4.9 Ω). No defects, cracking, or cratering of the devices were observed.

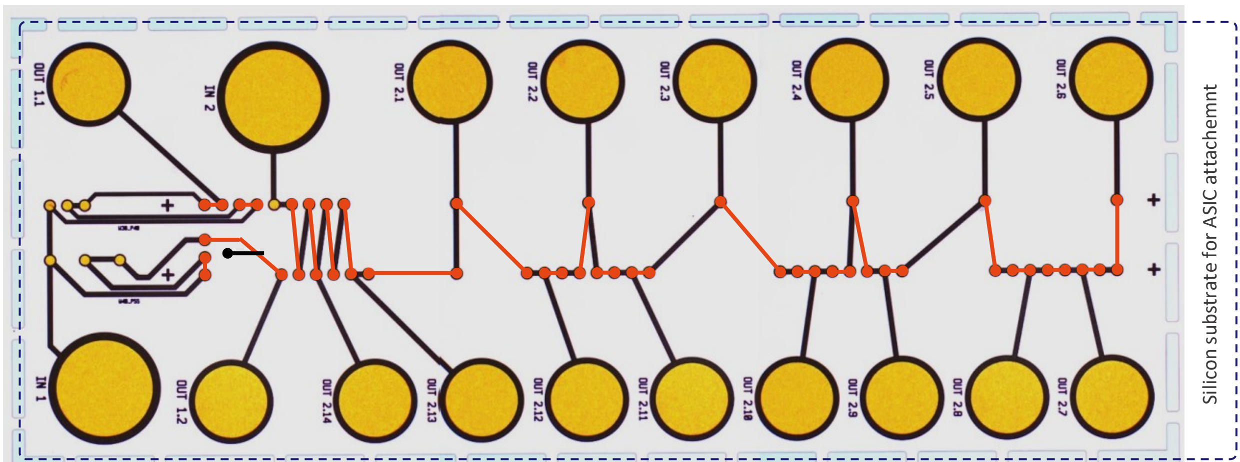

Figure 3.9: The original substrate image with an overlayer (drawn in orange) representing the chip metallization after the flip-chip process. The combined two metallization patterns form a closed daisy chain circuit.

Platinum bonding of devices with platinum bond pads

Before bonding, the wafer quarter containing the previously bumped with platinum devices with the 600 nm thick platinum bond pads were thinned down to 100 µm using a grinding and polishing process. Subsequently, the quarters were diced. The test structures were thinned down to mimic the dimensions of the final device and allow for practicing handling of the fragile chips.

Similar to the aluminum-based devices, flip-chip bonding was performed using thermocompression bonding performed in an inert atmosphere. The samples were preheated to 100°C before bonding and slowly cooled down to 100°C after bonding. The initial bonding was performed using the bonding parameters optimized for the aluminum-based devices (see Table 3.2).

During the first trial, it was not possible to achieve sufficient adhesion between the bumped chip and the substrate. Even when varying bonding parameters such as temperature and force, no improvement was observed. Because no platinum-platinum adhesion issues were observed during the bumping process, the lack of adhesion during bonding might be related to substrate surface modification during the thinning and dicing process. Unfortunately, the adhesion was not improved even after cleaning the devices with available parylene-compatible methods such as acetone, IPA, or an O_2 plasma flash.

In order to rule out the substrate-related reasons for the bad bonding results, the platinum-platinum-based bonding experiment was repeated. The thinned substrates were replaced with a silicon wafer with a 200 nm thick layer of platinum. This resulted in successful bonding using the optimized bonding conditions listed in Table 3.3.

Table 3.3. Optimized parameters for thermocompression bonding of the samples with 600 nm thick platinum bond pads and platinum stud bumps.

Parameter	Value
Substrate temperature	300°C
Chip temperature	300°C
Force	8.0 kg
Time	30 sec
Atmosphere	Nitrogen

The cross-section of the chip bonded to the wafer with platinum metallization is shown in Figure 3.10. The structure is underfilled to enable the cross-section cut. The stud bump deformation is excellent, with maximized contact between the two bonded structures. The adhesion is good and ensures a proper connection between the structures. The platinum stud bump height after bonding is approximately 20 µm. No defects such as cracking or cratering of the devices were observed.

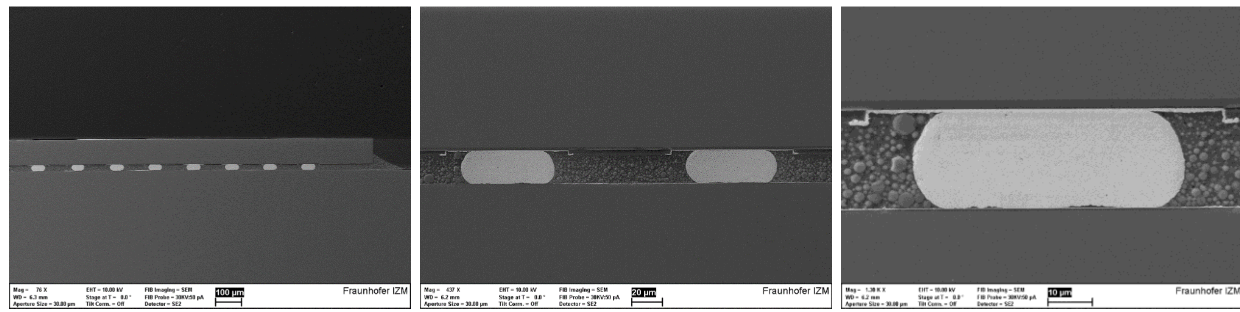

Figure 3.10: Cross-section SEM images and their close-ups of the platinum-bumped chip with platinum bond pads bonded to the wafers with a 200 nm thick layer of platinum. The chip is thinned down to 100 µm. The structure is underfilled with polymer for examination purposes. Source: FIZM.

3.3.3 Underfill

The final step of the flip-chip process is the underfilling of the gap between the bonded structures with a non-conductive material. In the case of flip-chip designated for medical implants, the underfill must be biocompatible. Moreover, it must adhere properly to all exposed surfaces and should not form voids that can potentially lead to moisture condensation and subsequent device failure.

In this section, medical-grade silicone rubber and parylene C are investigated as underfill. During the underfilling experiments, the aluminum-based test structures with a gap of approximately 30 µm were used (Figure 3.11).

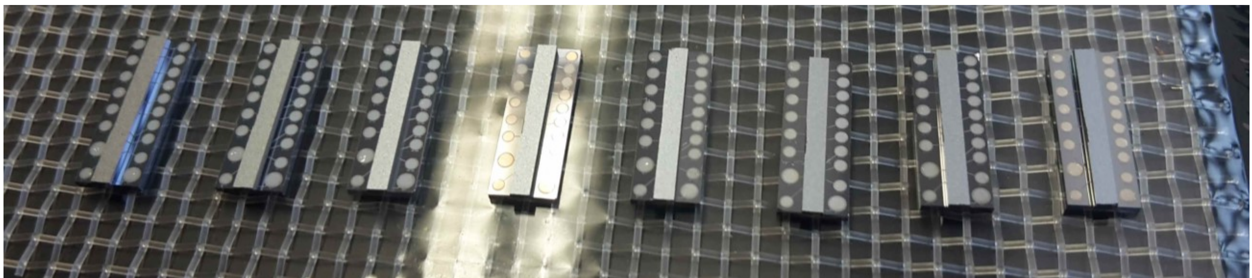

Figure 3.11: Bonded aluminum-based devices used for underfilling experiments. The individual devices have a thickness of 525 µm. The gap between bonded structures is approximately 30 µm high.

The focus of these experiments is to determine whether the selected biocompatible materials are suitable for chip underfill and if they can form a conformal, voidless layer. In this study, the devices are completely encapsulated with the underfill material to allow for fast and efficient evaluation.

Biomedical grade silicone rubber

Silastic MDX4-4210 is medical-grade silicone rubber [12]. The material is approved for use in implantable devices, and it qualifies for the United States Pharmacopeia (USP) Class VI certificate. The devices were placed individually in a PMMA mold (Figure 3.12a), and the silicone rubber was dispensed into the mold. After curing for 24 hours at room temperature, the underfilled devices were removed from the mold (Figure 3.12b).

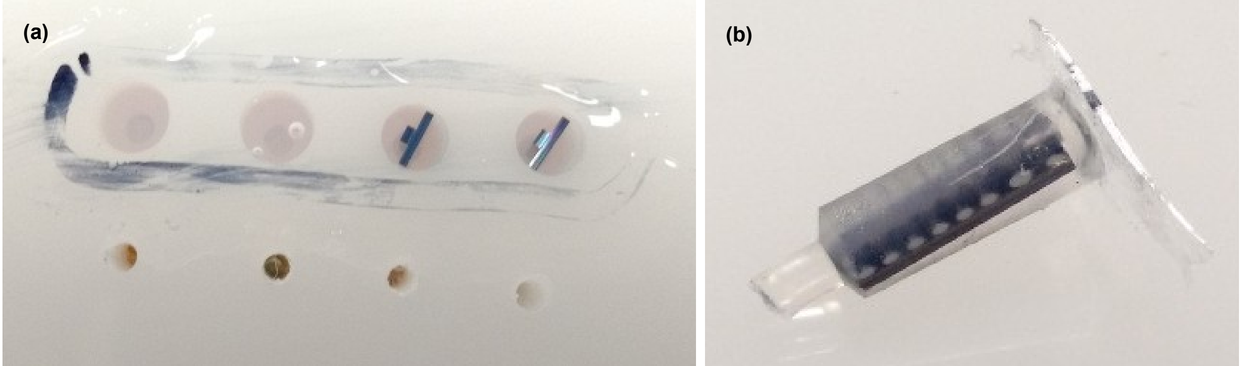

Figure 3.12: (a) The PMMA mold with devices underfilled with silicone rubber. (b) A single device released from the mold. Source: FIZM.

The underfilled deceives were examined using CT and X-ray microscopy to inspect the underfilled area between the two silicon chips. In the X-ray image (Figure 3.13a), no signs of voids or filling defects were observed. However, this can be related to tool-specific limitations such as resolution or selectivity to distinguish voids in the polymer. In the CT images, a sponge-like structure was observed (Figure 3.13b,c). This may indicate a non-complete filling of the gap or adhesion issues induced during the underfilling process.

Cross-section images of the underfilled structures have not been taken. Cutting through the soft silicone can cause deformation of the polymer layer that is under investigation.

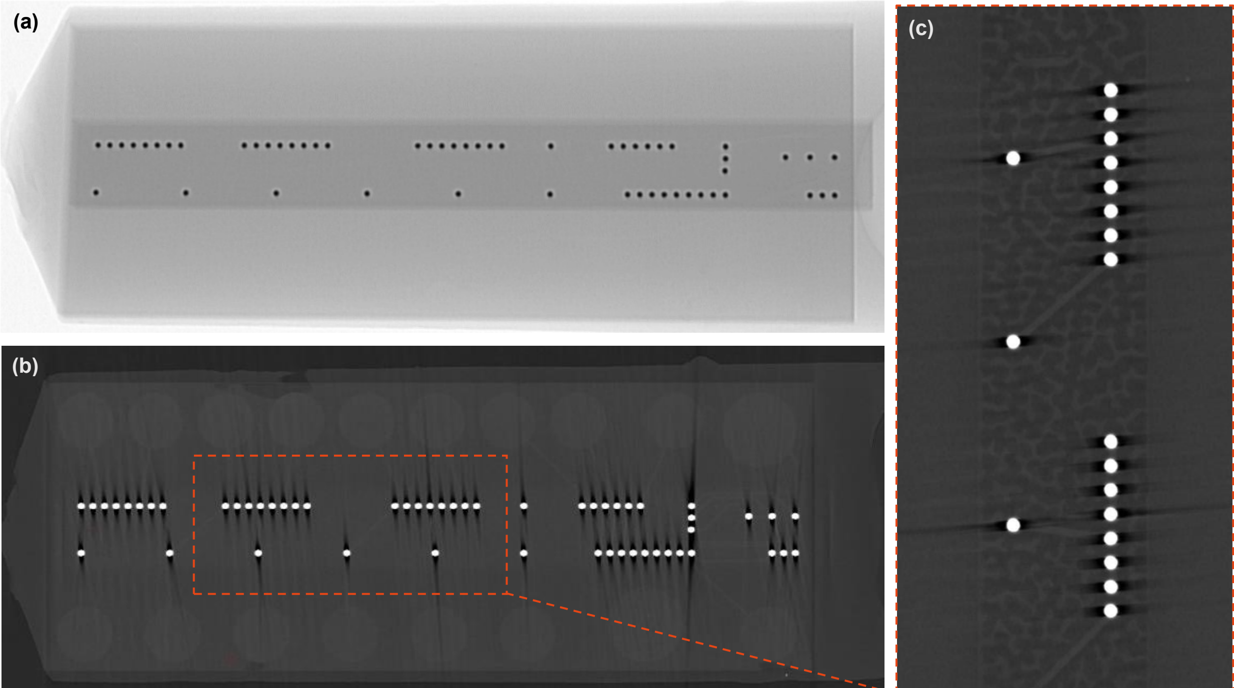

Figure 3.13: Top view of the bonded structures after underfilling with silicone rubber. (a) X-ray image of the complete device. (b) CT image of the complete device. (c) Close-up of the CT image. Source: FIZM.

Parylene

Parylene C is biocompatible and approved by the FDA for use in implantable devices. It is also known to form highly conformal layers. However, the deposition method (CVD) involves the risk of closing the edges of the bonded structures before the gap is filled, resulting in voids.

In this experiment, parylene was deposited at two different partial pressures of the monomer in the deposition chamber: at 28 mTorr, which is the pressure optimized by the manufacturer for parylene deposition, and at 10 mTorr, which is the lower pressure limit of the coating tool. By lowering the partial pressure of the monomer, the degree of coating conformity, especially in narrow spaces such as trenches, can be significantly improved [13]. Before the deposition, all the samples were cleaned using a low-power 60 W O_2 plasma. During the deposition, A-174 adhesion promoter was applied in situ.

First, a 16.5 µm thick layer of parylene was deposited at 28 mTorr. The acquired SEM images show that the layer did not completely underfill the gap between the chips (Figure 3.14). It suggests that the amount of used parylene substrate (dimer), and the resulting layer thickness, was insufficient to form a fully sealed layer around the device.

The samples were analyzed using CT imaging to evaluate how well the deposited layer of parylene closed the gap (Figure 3.15a). In the image, the approximately 15 µm thick layer of parylene can be seen. The layer seems to be uniformly deposited around the whole sample, including the edge of the gap between the chip and the substrate. However, the area underneath the chip does seem a little darker when compared to the rest of the parylene layer. This might suggest the presence of a large void and thus incomplete underfilling. Unfortunately, due to the nature of the sample and the limitations of the CT scanner, it was not possible to capture an unambiguous image of the underfilled area.

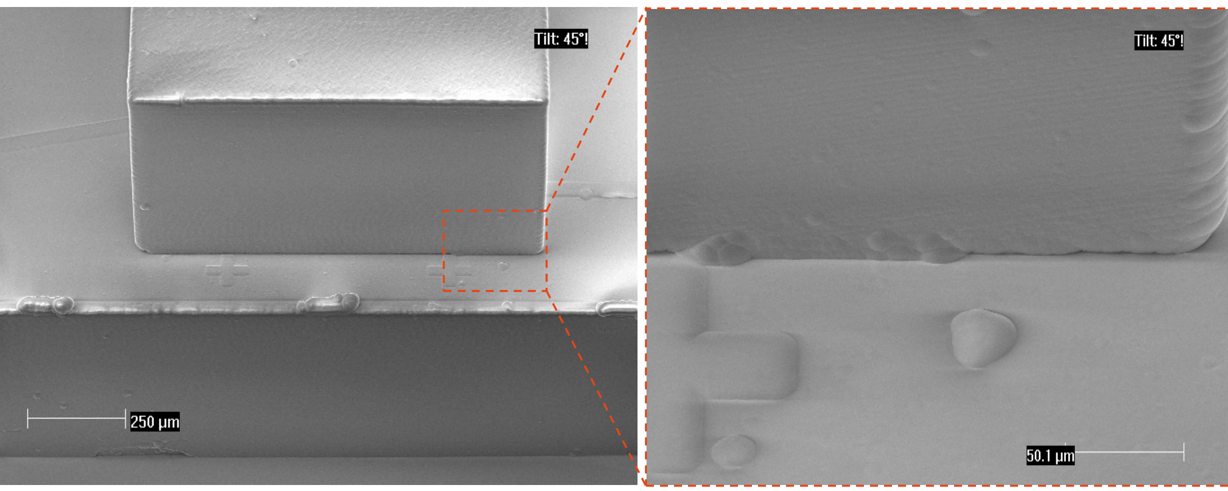

Figure 3.14: SEM images of bonded structures underfilled with 16.4 µm of parylene deposited at 28 mTorr.

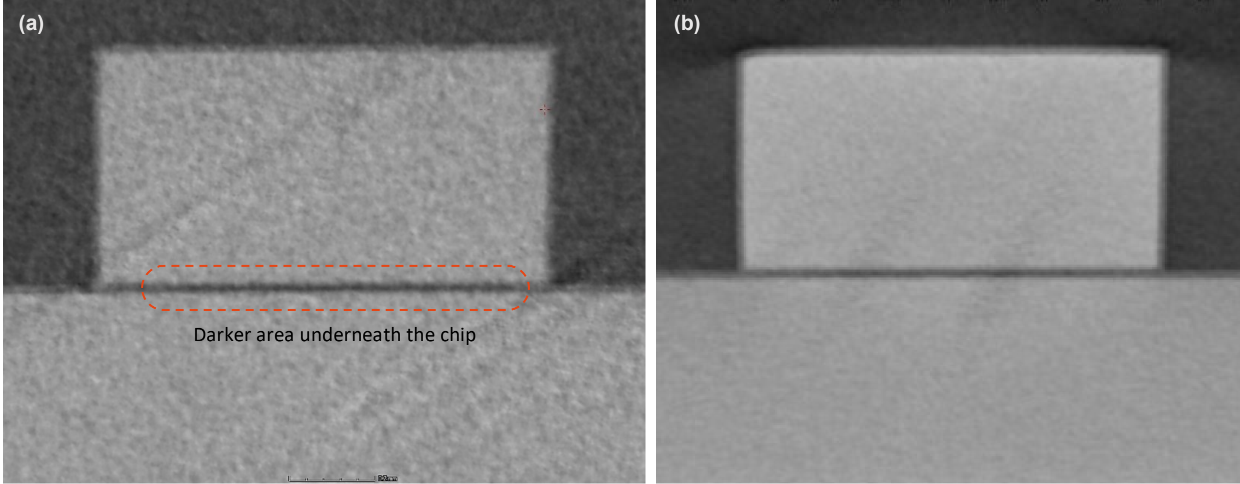

Figure 3.15: Side-view CT image of the underfilled structures. (a) Sample underfilled with 16.4 µm of parylene deposited at 28 mTorr. (b) Sample underfilled with 20 µm of parylene deposited at 10 mTorr. Source: FIZM.

Next, a 20 µm layer of parylene was deposited at almost three times lower pressure of 10 mTorr. This time, more parylene substrate was used to ensure good device encapsulation. The 20 µm thick parylene can be clearly seen in the CT image (Figure 3.15b). The layer seems more uniform than the layer deposited at 28 mTorr, especially in the area underneath the bonded chip. The top-view CT image of the sample underfilled with parylene at 10 mTorr also does not indicate the presence of voids or the occurrence of delamination (Figure 3.16).

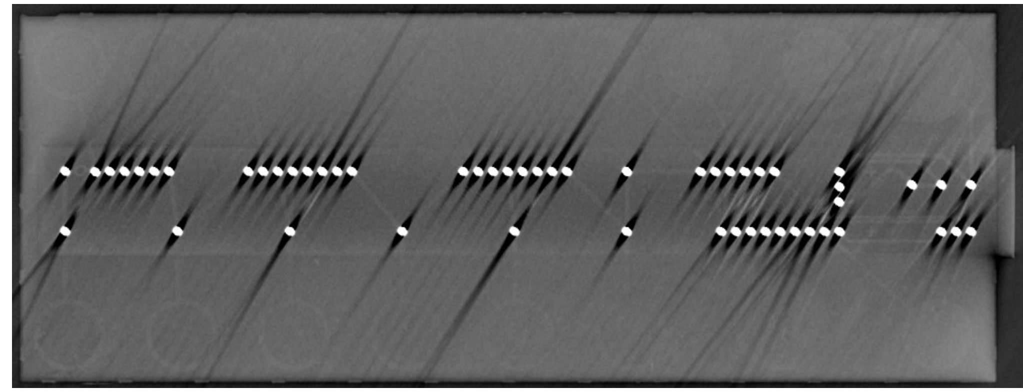

Figure 3.16: Top-view CT image of the structure underfilled with 20 µm of parylene deposited at 10 mTorr. The dark diagonal artifacts are due to the high contrast of the platinum bumps (bright spots). Source: FIZM.

3.4 DISCUSSION AND CONCLUSIONS

The goal of this chapter was to develop enabling technologies allowing for biocompatible flip-chip. The challenges were rising from the fact of using platinum as a bumping material, and handling of chips that have an arbitrary shape, 1 mm wide, and 8 mm long, and only 100 µm thick, and that already contain parylene structures sensitive to damage due to high temperature or mechanical force. The work focused on developing a platinum-based stud bumping and bonding process and investigating the biocompatible underfill.

The experiments were performed on specially developed and fabricated test structures. The dimensions of the test chips are identical to those of the final ASIC to enable practicing the handling of the devices. The silicon-parylene-based stack is similar to the one present in the final Chip-in-Tip DBS device.

Bumping

Platinum stud bumps were successfully placed on 525 µm thick devices with 2 µm thick aluminum and 600 nm thick platinum bond pads with a diameter of 75 µm. Good bump adhesion was achieved for optimized bumping parameters, and no damage to the samples, such as cracking or cratering, was observed. The bumping was performed in an inert, nitrogen atmosphere at temperatures up to 160°C. In these conditions, no visible changes to the parylene layer were observed. The 1 mm wide and 8 mm long chips were handled and bumped without major difficulties.

Bonding

The full-thickness (525 µm thick) aluminum-based structures with platinum stud bumps were successfully bonded using a thermocompression bonding technique. The process parameters were optimized to provide good adhesion and stud bumps deformation. The alignment of the structures was good, and an electrical connection between the chip and the substrate was established. The samples showed no visible damage such as cracking, cratering, or modifications to the parylene layer. The bonding was performed in a nitrogen atmosphere at a temperature of 220°C using a force of 4.5 kg for 30 seconds.

The thinned down (100 µm thick) platinum-based samples (chips) were successfully bonded to a wafer with a 200 nm thick layer of platinum. The bonding was performed in a nitrogen atmosphere at temperatures of 300°C using a force of 8 kg for 30 seconds. No damage to the samples was observed. The samples could not be bonded to the designated substrate due to bond pad damage and contamination induced during the wafer thinning processes. As a result, the alignment, the electrical connectivity, and the parylene layer status could not be evaluated. Based on the results achieved for the aluminum-based samples, the alignment and electrical connectivity should not be an issue. However, the higher temperature of 300°C can potentially modify the parylene layer. If that is the case, a thermosonic bonding process that allows for bonding at lower temperatures can be used instead of thermocompression bonding.

Underfill

The medical-grade silicone rubber and the parylene C were investigated as alternative materials for the biocompatible underfill of the 30 µm gap between the bonded structures (chip + substrate).

In the case of the samples underfilled with silicone rubber, the preliminary results show the formation of a sponge-like structure underneath the chip. This may indicate voids

or poor adhesion. Unfortunately, the exact cause could not be determined because of the nature of the samples and the lack of suitable measurement equipment. To evaluate the adhesion of the silicone rubber to the materials present at the interface, a separate study is recommended, including an investigation of adhesion enhancing methods. If voids turn out to be an issue, a thinner medical grade silicone rubber can be used in combination with a vacuum-centrifuge filling method.

The parylene underfill was performed at two different partial pressures: 28 mTorr and 10 mTorr. The preliminary results indicate that the underfilling at 10 mTorr was, as expected, more successful. The layer deposited at 10 mTorr appears more uniform. There are no indications of the presence of voids underneath the chip. However, the capabilities of the testing equipment, in combination with the nature of the sample, make it difficult to determine if the gap was underfilled without voids and if the parylene layer remained intact. It is recommended to repeat the experiment using, for example, dedicated test structures such as trenches mimicking the gap underneath the chip or a transparent substrate that will allow for a better assessment of the underfilling process.

For both the silicone rubber as well as the parylene underfill, the complete devices were encapsulated instead of just the gap between the chip and the substrate. Nevertheless, the experiment allowed to preliminary asses the suitability of the selected materials as candidates for a biocompatible alternative to standard underfills. However, in the final Chip-in-Tip DBS flow, only the space under the chip must be filled. Therefore, further research is needed regarding the underfilling method and possible ways of protecting the areas that should not be coated. Alternatively, the chip underfill can be performed later in the assembly process, after attaching the lead extension, and it can be partially combined with the device encapsulation process.

General

The enabling technologies for biocompatible flip-chip, developed in this chapter, are compatible with the DBS process, or they can be adjusted to be so. The application of a noble material for the stud bumps and bond pads, and the use of biocompatible underfills, make the process potentially suitable for a wide range of medical devices, especially those designed for permanent implantation. The development of a biocompatible flip-chip process can significantly contribute to the miniaturization of advanced, highly integrated implantable electronics.

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4

INTEGRATING HIGH-DENSITY CAPACITORS

4.1 INTRODUCTION

The goal of this chapter is to develop a set of enabling technologies for the Flex-to-Rigid (F2R) platform that will allow for monolithic integration of high-density capacitors directly into the semi-flexible structure. The deep brain stimulator (DBS) design (see Chapter 2) highlights the necessary modifications of the current F2R technology and demonstrates how the technologies developed in this chapter can enable the integration of the components.

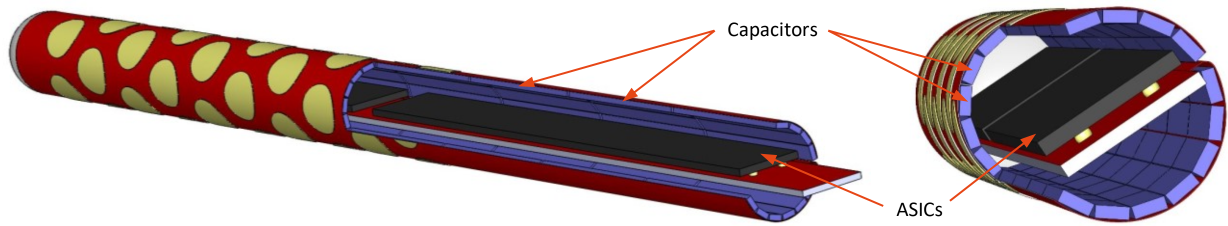

Figure 4.1: The 18 mm long wrapped DBS model with a diameter of 1.3 mm. The two ASICs are integrated inside the cylinder shape while the sixteen capacitors are distributed around the device circumference.

4.1.1 Design requirements

The developed in this thesis DBS device was designed in F2R technology to enable 40-electrode stimulation and, at the same time, simplify the multi-wired lead extension by moving the multiplexing chip into the tip of the DBS lead – Chip-in-Tip approach (Figure 4.1). To realize this approach, the DC blocking capacitors have to be integrated into the tip of the DBS lead. Based on the given pulse generator parameters, provided by project partner Medtronic, the minimum capacitance per electrode should be around 75 nF to prevent direct current from reaching the brain tissue.

To ensure the optimal shape (as round as possible) and diameter (1.3 mm) of the folded DBS probe, the area designated for the capacitors is composed of 80 silicon islands separated with 40 µm wide trenches and connected with flexible interconnects. The 210 µm wide and 2070 µm long islands are organized in five rows, each containing 16 islands distributed around the circumference of the tip (Figure 4.1). Each electrode is assigned two islands for capacitors integration.

Given the number of electrodes and the available silicon area, the capacitors with approximately 100 nF/mm^2 are needed to fulfill the DBS requirements. The only available on the market capacitors that could match these requirements are the high-density trench capacitors fabricated in a PICS3 technology developed by Murata [1]. The PICS3 technology allows for customizable capacitors design, and like F2R, it uses an IC-compatible process, which permits monolithic integration of the PICS3 capacitors directly into the F2R-based DBS structure. The thickness of the silicon island was adjusted to 80 µm to facilitate the integration by matching with the thickness of the capacitor.

4.1.2 Enabling technologies

The DBS device, designed in the F2R technology, can allow for monolithic integration of high-density capacitors by prefabricating them directly into the designated area of the silicon substrate and separating them with trenches to form a foldable F2R-based structure. However, the current Flex-to-Rigid was designed to produce much thinner devices, up to 50 µm thick, with a minimum spacing between the silicon islands of approximately 350 µm [2]. Therefore several modifications to the current F2R technology are needed in order to fabricate DBS devices with 80 µm thick silicon islands separated with only 40 µm wide trenches.

Two technological solutions were developed and are described further in this chapter to facilitate the precise separation of the silicon islands that contain prefabricated structures. The first solution employs sealable high-aspect-ratio (HAR) microchannels (trenches) embedded in silicon (see Section 4.2) [3]. At the early stage of the fabrication, the trenches are etched in the device layer to separate the capacitors. Subsequently, the trenches are sealed to enable further component integration (see Section 4.3) [4]. The second solution exploits a patterned buried oxide (cavity-BOX) layer in customized SOI substrates (see Section 4.4) [5]. The enabling technologies developed to integrate high-density capacitors into the F2R-based structure are validated using a DBS demonstrator that does not include metallization, and it is therefore not a functioning device.

Sections 4.2, 4.3, and 4.4 are based on publications. Some of them are included one-to-one, and therefore repetitions are unavoidable. Section 4.2 was written from the perspective of microfluidics.

4.1.3 Process alignment

Besides the device architecture, the fabrication processes themselves had to be aligned to enable monolithic integration of the capacitors into the F2R structure. In Section 4.5, the design and the fabrication process alignment strategy are established, followed by the inter-facility fabrication of a working demonstrator.

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4.2 MICROCHANNELS EMBEDDED IN SILICON[1]

***Abstract**: This paper presents a new method for the CMOS compatible fabrication of microchannels integrated into a silicon substrate. In a single-step DRIE process (Deep Reactive Ion Etching), a network of microchannels with a High Aspect Ratio (HAR) of up to 10 can be etched in a silicon substrate through a mesh mask. In the same single etching step, multidimensional microchannels with various dimensions (width, length, and depth) can be obtained by tuning the process and design parameters. These fully embedded structures enable further wafer processing and integrating electronic components like sensors and actuators in wafers with microchannels.*

4.2.1 Introduction

The field of microfluidics is rapidly expanding, and as a result also the need for advanced microchannel fabrication technologies. The majority of the silicon-based microfluidic devices, especially those with wide and/or deep microchannels, such as devices for cooling or gas chromatography, are still sealed with wafer bonding techniques [1][2]. This cumbersome method limits miniaturization and further system integration possibilities.

Previous studies have already shown that it is possible to fabricate CMOS-compatible microchannels that allow for the addition of actuators/sensors [3][4]. Furthermore, a recently proposed method for a two-step fabrication of sealable microchannels through a mesh mask with about 1 µm wide slits facilitates the development of silicon-based platforms like Lab-on-Chip (LOC) or Organ-on-Chip (OOC). These high-resolution silicon-based microfluidic devices enable miniaturization and allow for further wafer processing and thus integration of actuators or sensors for in-situ stimulation or measurement. However, the major drawback of this method is the limited depth of the microfluidic channel. For example, the 10 µm wide sealable trenches could reach a maximum depth of 40 µm (aspect ratio of 4). The saturation in the DRIE process limited the depth during the first etching step of the 1 µm wide, deep trenches [5].

This paper introduces a new CMOS compatible method for the fabrication of fully embedded multidimensional microchannels with a high aspect ratio (HAR) in a single DRIE step.

4.2.2 Materials and Methods

The fabrication starts with the depositions of a 2 µm thick layer of low-stress PECVD SiO_2 on silicon substrates (Figure 4.2a). At the location of test channels, rows of parallel arrays with 56 different combinations of sub-micron size rectangular slits (Table 4.1) are dry-etched in the silicon dioxide using a standard photoresist mask (Figure 4.2b).

Table 4.1: The 56 different slits sizes are compiled from the dimensions collected in this table.

Parameter	Dimensions [µm]								
Slit length (L):	6.0	-	-	-	-	-	-	-	Fixed
Slit width (W)	0.8	1.0	1.2	1.4	1.6	1.8	2.0	-	Variable
Distance between slits (D)	0.6	0.8	1.0	1.2	1.4	1.6	1.8	2.0	Variable

Subsequently, channels in the silicon are etched through the meshed SiO_2 hardmask in a single DRIE using an optimized Bosch process. In this process, cycles of dry silicon etch (using SF_6), wall passivation (using C_4F_8), and break-through of the passivation layer on the bottom of the trench are alternatively performed in a number of repeating loops. The DRIE process is tuned in such a way that in each loop, at the early stage of

[1] Chapter adopted from the Eurosensors 2017 conference proceedings: Kluba, 2017.

the process, the sidewalls of the small trenches under individual slits are slightly over etched (Figure 4.2c). At some point during the DRIE process, the sidewalls between individual trenches are completely removed, and the large channel is formed underneath the meshed mask (Figure 4.2d). The formation of the channel changes the etching mechanism so that it resembles more etching of an open structure rather than etching through a meshed mask. Finally, the channel is sealed with a 2 µm thick layer of PECVD SiO_2 deposited on top of the remaining SiO_2 mask with slits (Figure 4.2e).

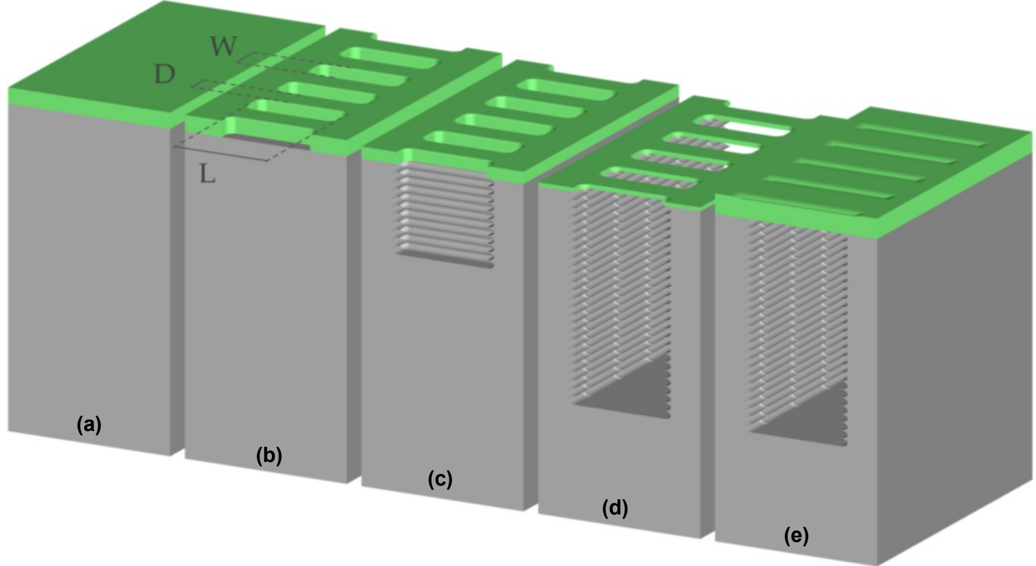

Figure 4.2: The HAR, embedded microchannels fabrication stages. (a) Deposition of the silicon dioxide. (b) Patterning the SiO_2 hardmask. (c-d) Simultaneous etch of trenches in the silicon and the walls between them in the tuned single-step DRIE process. (e) Closing the channels with a PECVD SiO_2.

The duration of the silicon etch cycle varies from 1.5 s through 4 s up to 8 s. The number of etch-passivation loops, and thus the total etch time, is increased from 10 loops up to 150 loops for the long etch cycle (8 s) and up to 500 loops for the short etch cycle (1.5 s). The total etch time is limited so that at least 500 nm of the silicon dioxide hardmask is preserved on top of each channel. The preserved mesh mask is closed with a 2.0 µm thick layer of PECVD SiO_2 to form the embedded network of microchannels.

The cross-section of each fabricated channel is inspected in 45° and 90° tilt with an SEM (Scanning Electron Microscope) to determine its dimensions and examine the silicon dioxide mesh mask before and after the closing of the channel.

4.2.3 Results and Discussion

Several microchannels were etched in silicon through the 2 µm thick hardmask of silicon dioxide. At first, it was observed that very uniform (approximately 590 µm long and 6 µm wide) channels with a depth of almost 60 µm were etched in the silicon when the walls between the single trenches were removed (Figure 4.3a). This results in aspect ratios of up to 10. The maximum achieved depth of the channel was limited only by the thickness of the SiO_2 mask, which had to be preserved to allow for CMOS-compatible and low-topography sealing of the structures with PECVD SiO_2 (Figure 4.3b,c).

The mechanism of an open channel formation underneath a mesh mask during a single DRIE etching process was further studied in respect to the Bosch process parameters: the silicon etch cycle time, the number of etch-passivation loops; as well as the mesh design parameters like the width of the slits and the distance between the slits (the length of the slit is fixed).

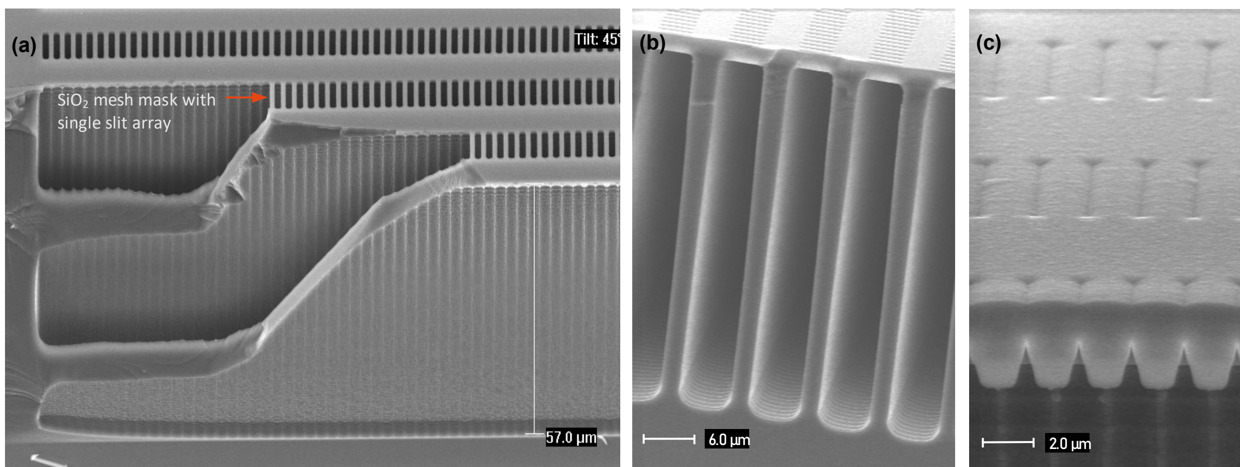

Figure 4.3: SEM image of 6 µm wide and 57 µm deep vertical microchannels etched through an oxide mesh mask in a single-step DRIE process. (a) Cross-section through channels with preserved thin silicon dioxide mesh mask. (b) Cross-section through a row of parallel channels after sealing them with PECVD SiO_2. (c) Cross-section through sealing of an embedded channel.

4.2.4 Process Parameters

To evaluate the influence of process parameters on the formation of the channels and the etch rate, three series of wafers with etch cycle times t_{etch} = {1.5 s; 4.0 s; 8.0 s}, and an increasing number of etch-passivation loops were etched through the oxide mesh with the same, fixed slit dimensions. The total etch time, t_{total} was calculated from the equation: t_{total} = *number of loops* · (t_{etch} + $t_{overetch}$), where $t_{overetch}$ is the time of the silicon etch during the passivation break-through cycle after the passivation layer has been removed ($t_{overetch}$ = 1 s). The dependence of the trench depth as a function of total etch time t_{total} is plotted in Figure 4.4a. For short total etch times (t_{total} ≤ 250 s), the etch rate and depth are comparable for all three series. For longer total etch time (t_{total} > 250 s), the walls between trenches with smaller scallops (t_{etch} = 1.5 s) are still present, and a slight trench depth saturation can be observed. For trenches with larger scallops (t_{etch} = {4 s; 8 s}), the walls are removed at t_{total} ≈ 800 s and t_{total} ≈ 400 s, respectively (the exact wall removal moment is hard to determine as it is a gradual process). The wall removal is directly connected with the jump in the etch rate curve, which allows for the etching to continue without noticeable signs of trench depth saturation.

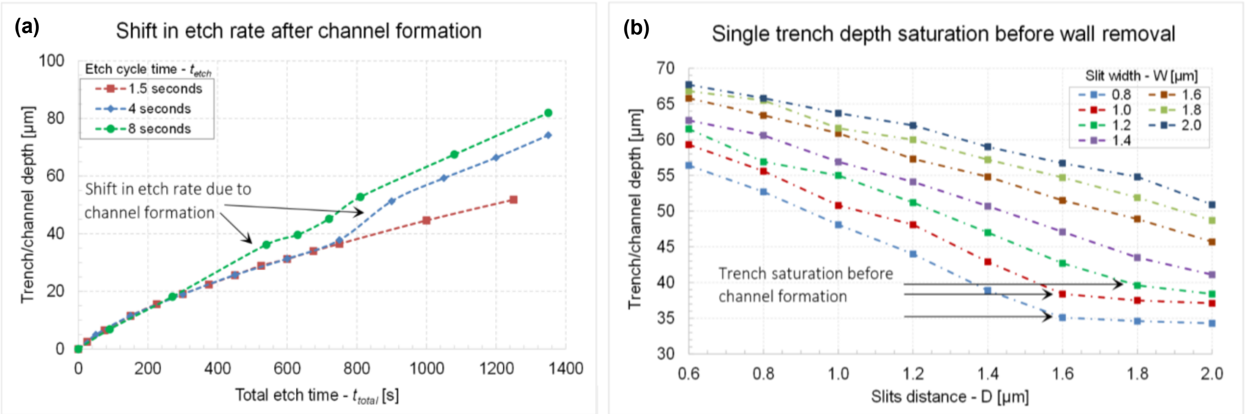

Figure 4.4: (a) The influence of the etch parameters on the channels formation and the etch rate of the structures (fixed design parameters: L=6.0 µm; W=1.0 µm; D=0.8 µm). (b) The influence of the design parameters on the channels formation and the depth of the structure (fixed process parameters).

4.2.5 Design Parameters

In a second experiment the process parameters were fixed (90 loops, t_{etch} = 8 s) while the mesh mask design parameters were varied: W [μm] = {0.8; 1.0; 1.2; 1.4; 1.6; 1.8; 2.0}, D [μm] = {0.6; 0.8; 1.0; 1.2; 1.4; 1.6; 1.8; 2.0}; resulting in channels with various depths. The dependence of the trench depth on the slit width W, and the distance between the slits *D* is plotted in Figure 4.4b. The trench depth is directly proportional to W, corresponding to the open mask area, and inversely proportional to D, corresponding to the trench wall thickness. The increase of the channel depth with decreasing slits distance is only noticeable when the wall between the channels is removed, resulting in the formation of the channel. The thinner the walls between trenches, the faster they merge into channels preventing DRIE etch saturation.

4.2.6 Conclusions

With the new single-step DRIE process presented in this paper, it is possible to etch multidimensional microchannels with a uniform depth and a high aspect ratio of up to 10. By modifying the meshed hardmask design parameters (slit dimensions) and the Bosch process (DRIE) parameters, it is possible to simultaneously etch trenches and remove the walls between them, forming a channel underneath the hard-etch mesh mask. The channel formation underneath the mask changes the etching mechanism preventing DRIE etch saturation, allowing for the fabrication of HAR microchannels. After etching, the remaining mesh mask can be closed with PECVD SiO_2 to form the embedded microchannels. Channels with different dimensions can be etched in the same single-step process by tuning the mask design parameters.

Future work will include application studies, such as integrating sensors on top of the embedded microchannels and optimizing the mask to reach even higher aspect ratios.

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4.3 WAFER-SCALE INTEGRATION FOR NEURAL IMPLANT MINIATURIZATION[2]

Abstract: *In this paper, we present a novel, wafer-based fabrication process that enables the integration and assembly of electronic components, such as ASICs and decoupling capacitors, with flexible interconnects. The electronic components are fabricated in or placed on precisely defined and closely-spaced silicon islands that are connected by interconnects embedded in a parylene-based flexible thin film.*

This fully CMOS compatible approach uses optimized DRIE processes and a SiO_2 *mesh-shaped mask, allowing for the simultaneous definition of micrometer- to millimeter-sized structures without compromising the flexibility of the device. In a single fabrication flow, unique freedom in dimensions of both the flexible film and the silicon islands can be achieved, making this new technique ideal for the realization of semi-flexible/foldable implantable devices, where structures of different sizes have to be combined together for the ultimate miniaturization.*

4.3.1 Introduction

After the success of cochlear implants, the field of neurostimulation has rapidly taken off finding new applications in the treatment of brain-related disorders [1][2] and spinal cord neuromodulation [3]. As an alternative to the standard passive electrode leads, active neurostimulation probes, consisting of rigid silicon chips connected with flexible interconnects, have been proposed. The active probes are manufactured by either chip transfer and consequent fabrication of parylene-based interconnects [4], or in a monolithic process using a two-step DRIE (Deep Reactive Ion Etching) release method [5]. In the first approach, the miniaturization of the implant is limited by issues connected with manual alignment and handling. In the second method, the design, and thus the intrinsic dimensions of the probe, are constrained by the differences in etch rate of large and small structures in the DRIE process.

In this paper, we present a manufacturing method that does use the monolithic, wafer-scale approach and at the same time allows for the fabrication of neural probes with unconstrained dimensions.

4.3.2 Materials and methods

The process for the integration of electronic components into the neural implants (see Figure 4.5) starts with the accurate definition of silicon-based islands. Next, Parylene C is used to fabricate a flexible film connecting the pre-defined structures in silicon. Finally, the semi-flexible device is released using a DRIE process. Each of these steps is described in detail in the following subsections.

Precise definition of the electronic components

At the beginning of the fabrication process, several silicon islands are precisely defined by implementing a specially developed DRIE process (see Section 4.2) to fabricate HAR embedded trenches [6]. First, a 2 µm thick PECVD SiO_2 layer is deposited and patterned with submicron size slits to form a mesh-shaped hardmask on an SOI (Silicon-on-Insulator) wafer with the desired device thickness (Figure 4.5a). Next, the silicon chips are precisely defined in a front-side DRI etch by high aspect ratio trenches using the buried oxide (BOX) as an etch stop layer (Figure 4.5b, Figure 4.6a). The DRIE process was optimized so that in one etch step individual trenches merge underneath the slits in the hardmask to form large trenches defining the silicon islands. The slits in the remaining 500 nm thin SiO_2 mask are then sealed with a 2 µm thick layer of PECVD SiO_2 (Figure 4.5c), which allows for further wafer-scale processing.

[2] Chapter adopted from the Eurosensors 2018 conference proceedings: Kluba, 2018.

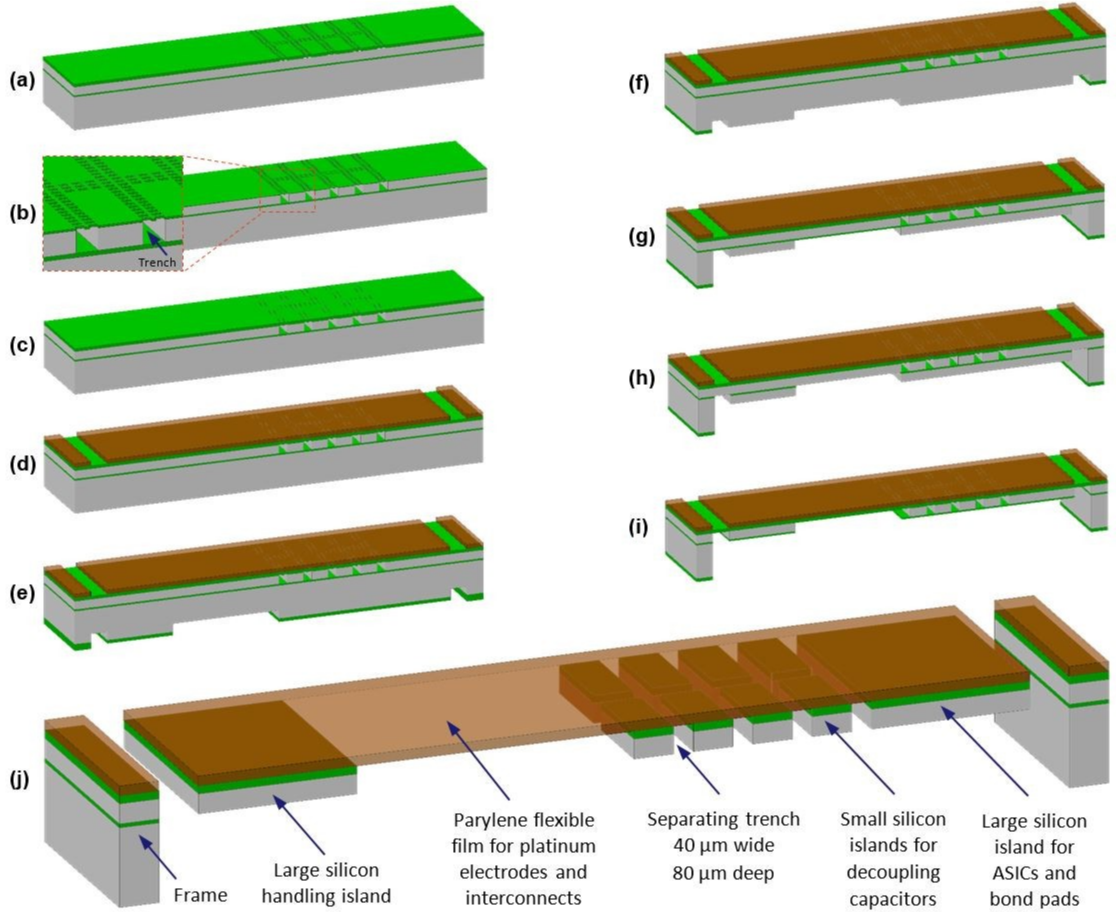

Figure 4.5: Fabrication flowchart of the flexible device with 80 µm thick silicon islands integrated with parylene interconnects. (a) Deposition and patterning of the SiO_2 mesh-shaped mask on an SOI substrate. (b) Definition of the silicon islands with trenches. (c) Sealing of the trenches with PECVD SiO_2. (d) Deposition and patterning of the parylene film. (e) Etching of the advance in the bulk silicon. (f) Partial removal of the backside SiO_2 hardmask. (g) Thinning the bulk silicon until the BOX etch stop layer. (h) Removing the exposed buried oxide layer. (i) Silicon islands thinning and device release. (j) The remaining BOX and SiO_2 etch stop layer removal.

Fabrication of the flexible interconnection

At this stage, the silicon islands, which can contain almost any type of prefabricated active or passive components, are pre-defined in the SOI substrate by the buried trenches. After the closure of the slits in the oxide hardmask, the surface of the wafer becomes fully planar again, allowing for the fabrication of flexible interconnects that will mechanically and electrically connect the islands. In the complete process flow, these biocompatible interconnects would consist of platinum interconnects sandwiched between two 5 µm thick layers of parylene C [4]. In this short process flow demonstration, the full stack has been replaced by a single 10 µm thick Parylene C film (Figure 4.5d).

Device release and thinning

The final step in the fabrication process is the device release and the thinning down of the silicon islands, which can serve as miniature substrates for ASICs, passive components, or to hold bond pads for wire connections. In an optimized back-side DRIE process, an advance is dry-etched in the bulk silicon through a two-step PECVD SiO_2 hardmask (Figure 4.5e). Next, part of the SiO_2 hardmask is etched away (Figure 4.5f), and subsequently, bulk silicon is thinned down in the second DRIE step until the BOX etch stop layer is reached (Figure 4.5g). Then, the partially exposed buried oxide layer

is removed (Figure 4.5h), and the final silicon substrate thinning and device release are simultaneously performed in the last silicon etch step (Figure 4.5i). Lastly, the landing BOX layer and the SiO_2 layer deposited while closing the trenches are etched away. The result is a semi-flexible device with 80 µm thick rigid silicon islands connected by a flexible parylene film (Figure 4.5j, Figure 4.6b).

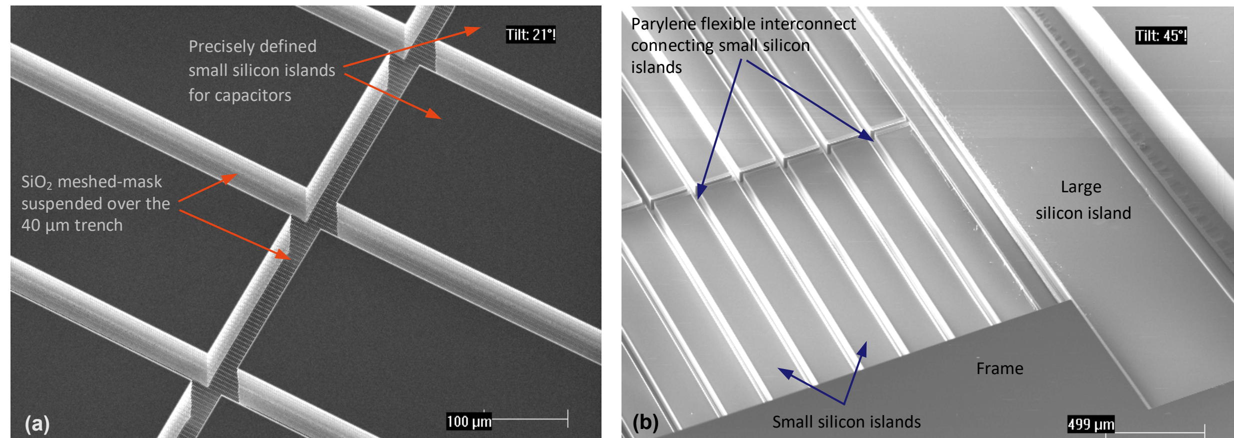

Figure 4.6: SEM images of the precisely defined 80 µm thick silicon islands. (a) Top view of the remaining SiO_2 mesh-shaped mask after the trench front-side DRIE process. (b) Bottom view of the final device with separated small and large silicon islands after the back-side two-step DRIE release.

4.3.3 Results and Discussion

The key fabricate steps have been successfully combined to manufacture an 11 mm wide, 18 mm long and 80 µm thick proof of concept device (Figure 4.7:) composed of:

- One hundred twenty-eight (128) small silicon islands (2070 µm x 210 µm), separated by 40 µm wide trenches, that in the final implant will contain high-density decoupling capacitors for stimulation electrodes.
- Two large silicon islands (17 mm x 1 mm and 18 mm x 1 mm), which can accommodate an ASIC, contain bond pads for wire bonding or allow for device handling during assembly.
- A 10 µm thick parylene film, which at the same time connects the multidimensional silicon islands and can contain flexible stimulation electrodes in the large flexible area (17 mm x 5 mm).

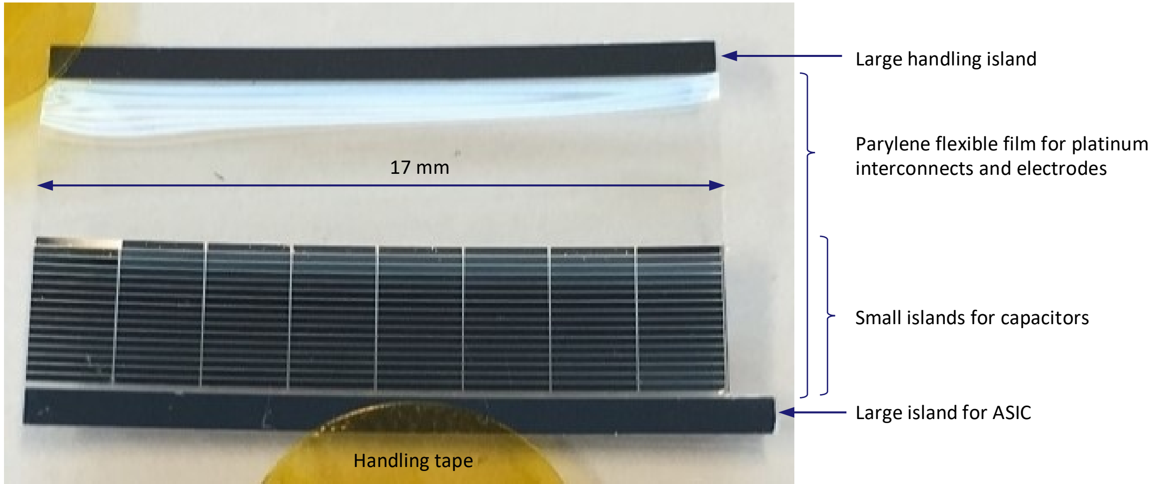

Figure 4.7: Top-view photography of the 80 µm thin released device composed of 128 small (2070 µm x 210 µm) and two large (17 mm x 1 mm and 18 mm x 1 mm) silicon islands separated by 40 µm wide trenches and connected with the 10 µm thick parylene-based flexible interconnect.

The fine level of silicon wafer segmentation, and component connection with the parylene film, ensures the flexibility of the device and enables it to be wrapped into an 18 mm long cylindrical structure with a diameter of only 1.3 mm (Figure 4.8). The cylinder will eventually form the active electrode tip of a Deep Brain Stimulation probe.

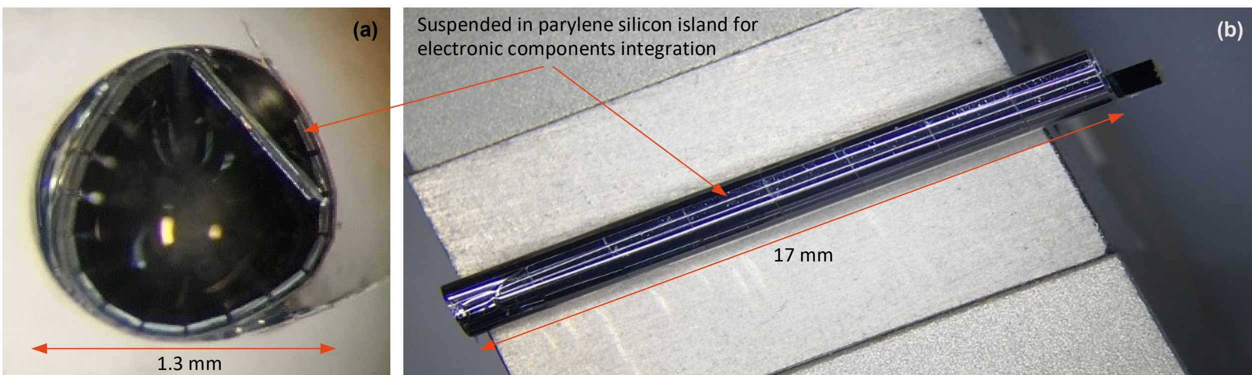

Figure 4.8: Photography of the 10 mm wide and 17 mm long device, with integrated various-size silicon island, wrapped into a 1.3 mm diameter needle-like shape. (a) Cross-section of the device with 200 µm wide small silicon islands suspended in parylene film. (b) Side-view of the 17 mm long needle-shaped device.

4.3.4 Conclusions

In this paper, we have presented a technology concept that can serve as an integration and assembly platform for minimally invasive implantable devices. In the concept, silicon islands of arbitrary shapes and thickness are connected by flexible interconnects sandwiched in between two parylene layers. The technology concept is validated with a non-functional demonstrator presented in this paper. The successful fabrication and rolling of this device into a DBS probe-shape structure proves the feasibility of the concept. Further steps comprise the inclusion of the platinum interconnects and the fabrication of the stimulation electrodes.

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4.4 CAVITY-BOX SOI: ADVANCED SILICON SUBSTRATE FOR MEMS DEVICES[3]

***Abstract**: Several Silicon on Insulator (SOI) wafer manufacturers are now offering products with customer-defined cavities etched in the handle wafer, which significantly simplifies the fabrication of MEMS devices such as pressure sensors. This paper presents a novel cavity buried oxide (BOX) SOI substrate (cavity-BOX) that contains a patterned BOX layer in contrast to cavities buried in silicon. The patterned BOX can form a buried microchannels network or serve as a etch stop layer and a buried hardmask to accurately pattern the device layer while etching it from the backside of the wafer using the cleanroom microfabrication compatible tools and methods.*

The use of the cavity-BOX as a buried hardmask is demonstrated by applying it to the fabrication of deep brain stimulation (DBS) demonstrator. The demonstrator consists of a large flexible area and precisely defined 80 µm thin silicon islands wrapped into a 1.39 mm diameter cylinder. With cavity-BOX, the process of thinning and separating the silicon islands was significantly simplified and became more robust. This test case illustrates how cavity-BOX wafers can advance the fabrication of various MEMS devices, especially those with complex geometry and added functionality, by enabling more design freedom and simplifying the fabrication process optimization.

4.4.1 Introduction

Silicon on Insulator (SOI)

Standard SOI substrates were initially developed to enable perfect dielectric isolation in electronic devices. Nowadays, SOI wafers have also become an important substrate material for the fabrication of MEMS devices. SOI wafers consist of a handle wafer that provides mechanical strength during the fabrication process, a device layer into/onto which the devices are fabricated, and a buried oxide (BOX) layer that separates the device layer from the handle wafer (Figure 4.9a). Apart from electrical isolation, the BOX layer also allows for the fabrication of MEMS devices with a well-defined device layer thickness, and it can serve as a release layer in floating structures. SOI wafers are used in a wide range of applications such as pressure sensors [1], resonators and inertial sensors [2], microchannels [3], and miniaturization of microfabricated medical devices [4][5].

Cavity-SOI

A Cavity-SOI substrate is a substrate that has been derived from the silicon-on-insulator family [6]. It is a customized SOI substrate whereby the manufacturer of the SOI substrates has integrated customer-defined buried cavities in the silicon handle wafer (Figure 4.9b). It has been demonstrated that customized SOI substrates with prefabricated cavities can significantly simplify the fabrication process of complicated MEMS devices such as pressure or inertial sensors [2][7][8][9][10]. Cavity-SOI substrates allow for eliminating the cumbersome step of etching cavities in the handle layer later in the process flow and permit for the pre-patterning of complex cavities systems. However, the range of the cavity dimensions in the cavity-SOI wafers is limited. On the one hand, large cavities that are not supported with pillars would make the wafer fragile and can lead to wafer or device layer deformation. On the other hand, small buried structures are out of cavity-SOI scope due to the low alignment precision of the prefabricated cavities with the structures fabricated later in the device layer.

[3] Chapter adopted from the Micomachines 2021 journal paper: Kluba, 2021.

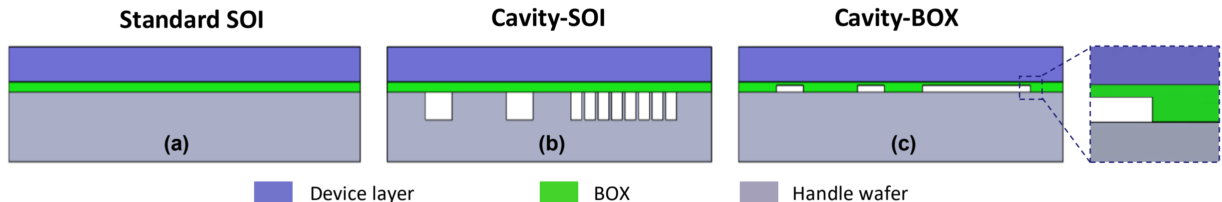

Figure 4.9: A comparison of three substrate architectures. (a) Standard SOI substrate. (b) Cavity-SOI substrate with cavities in handle wafer. (c) Cavity-BOX substrate with the pre-patterned buried oxide layer.

Cavity-BOX

Cavity-BOX is an advanced substrate with custom-defined cavities etched in the buried oxide, see Figure 4.9c. It is the newest member of the SOI substrate family. Its exemplar preparation process and application are presented in this paper. The cavities can be formed by etching through the complete thickness of the BOX or by partially etching the BOX to create a hardmask with a step. In cavity-BOX substrates, only the thin layer of buried silicon oxide is patterned, which enables the almost unlimited design of the cavities without weakening the mechanical properties of the wafer. A newly developed marker transferring strategy ensures the high precision alignment (<500 nm) of the prefabricated cavities with the structures fabricated later in the device layer. The method uses a set of primary alignment markers on the SOI wafer terrace that are transferred onto the device layer using front-to-front alignment [11]. The patterned BOX can serve as an etch stop layer during the handle layer thinning, and it can be used as a hardmask during the device layer patterning from the backside. The high resolution of the DRIE process is maintained by bringing the hardmask, formed by the patterned BOX layer, directly to the device layer. This allows for a precise definition of micron-sized cavities in the device layer and simultaneously enables patterning centimeter-sized structures in the device layer.

The use of the cavity-BOX as a etch stop layer and a buried hardmask is demonstrated by applying it for the fabrication of a deep brain stimulation (DBS) demonstrator probe. First, the DBS device design and standard fabrication process are presented and compared with the process that uses the cavity-BOX to show how the cavity-BOX substrate can enable more design freedom and simplify the fabrication process. Next, the preparation of the customized cavity-BOX substrate, and the fabrication process of the DBS demonstrator, are described. The DBS demonstrator is a mechanical structure composed of only silicon islands connected with a polymer-based flexible film. Finally, the DBS demonstrator fabrication results are presented and discussed.

4.4.2 Deep Brain Stimulation (DBS) device - process and design

The advanced SOI substrate with cavities in the BOX can significantly simplify processes such as the microfabrication of highly integrated foldable devices [4][5] or 3-dimensional circuit integration using TSVs in the device layer [12]. An example of the cavity-BOX application is a monolithic fabrication process of foldable deep brain stimulation (DBS) probe (Figure 4.10).

Fabrication process using SOI and cavity-BOX substrate

In Section 4.3, the standard SOI substrate and the trench-based F2R technology was employed to accomplish monolithic fabrication of a device where small, 80 µm thick silicon islands, separated with 40 µm wide trenches, could coexist with millimeter-sized flexible area etched from the backside of the wafer [5][13]. Due to the resolution limitations of the backside DRIE process, the precise separation of the small silicon

islands (210 µm x 2070 µm) could not be achieved. Therefore, the HAR trenches were etched in the device layer from the front side of the wafer to separate the silicon islands subsequently sealed with a silicon dioxide membrane (Figure 4.10a) to enable further wafer processing (Figure 4.10b). However, the trench etching and sealing processes require precise optimization, and they have very tight process windows. Moreover, failures of the fragile SiO_2 membrane can severely hamper the follow-up processes. Employing the cavity-BOX substrate with a patterned buried oxide (Figure 4.10e) allows for a more robust process by maintaining the device layer intact until the very end of the front side processing (Figure 4.10f). All the structures are released at the end of the process by DRIE etching from the backside using the cavity-BOX as a hardmask.

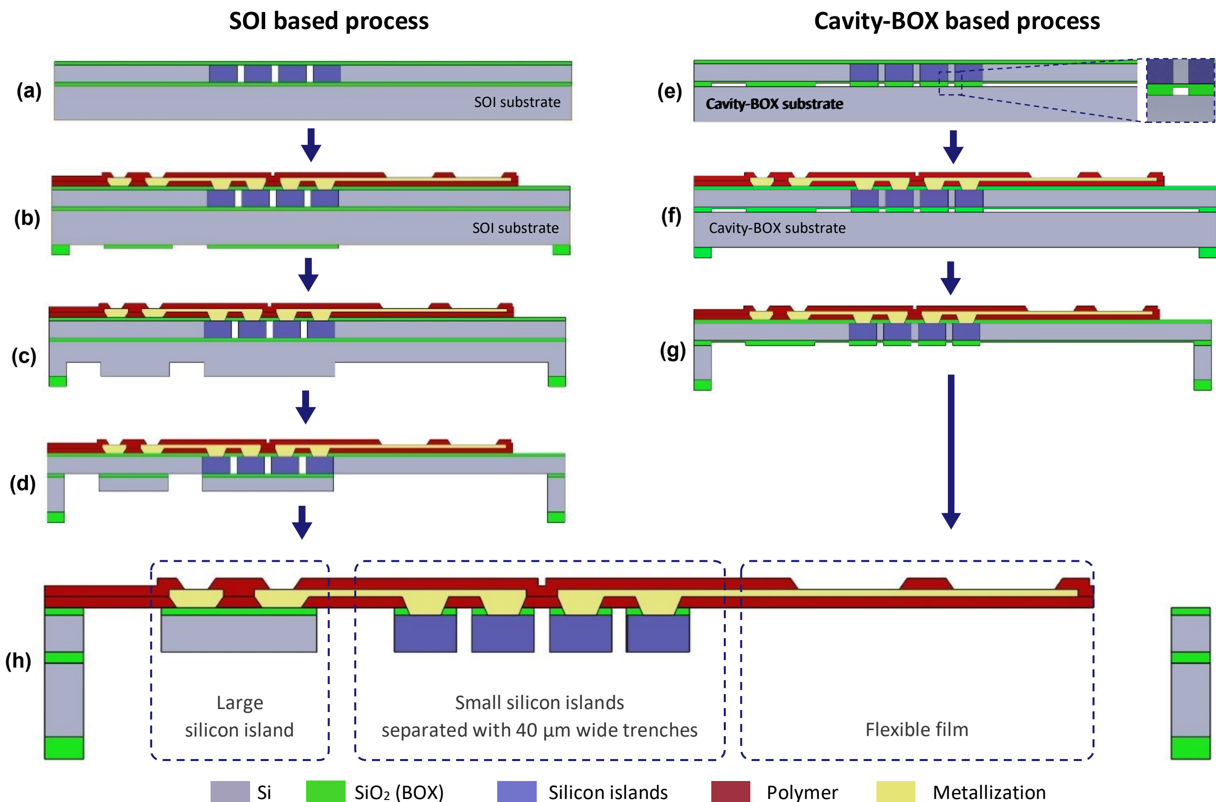

Figure 4.10: Simplified manufacturing process flow diagrams of semi-flexible DBS device using the trench-based F2R technology versus using the cavity-BOX substrate [5]. This allows for a high level of electronic components integration. Left (a-d): The SOI-based process with sealed trenches on the front side of the wafer and a two-step backside etch process. Right (e-g): The cavity-BOX-based process using patterned BOX as an etch stop layer and hardmask. Bottom (h): Finished device.

After the front side processing is finished, the DRIE etching is applied from the backside of the wafer for thinning down and releasing the flexible structures. In the standard SOI process, this is realized by multiple steps of alternating silicon dioxide etch and silicon etch through a two-step hardmask located on the backside of the handle wafer (Figure 4.10c,d,h). The buried oxide layer of the standard SOI wafer serves as an etch stop layer that defines the device thickness. This approach is cumbersome and heavily relies on the uniformity of each dry etching step.

The cavity-BOX can significantly simplify the process by bringing it down to just three steps. First, the substrate is thinned down from the backside of the wafer to 80 µm using a simple hardmask patterned on the backside of the handle wafer. Here the BOX serves as an etch stop layer that balances the DRIE uniformity of the handle wafer etching (Figure 4.10g). Secondly, the exposed cavity-BOX with a step mask is thinned

down to form the hardmask. Finally, the hardmask formed in the BOX is used to separate the 80 µm thick silicon islands with the 40 µm wide trenches and simultaneously release the flexible film in the final DRIE step (Figure 4.10h). The high resolution of the DRIE process and coexistence of the structures with a wide range of dimensions is ensured by bringing the hardmask – the patterned BOX – directly to the device layer rather than optimizing the DRIE process to its extreme.

DBS device design

The application of the cavity-BOX substrate is demonstrated using a simplified fabrication process of an 18 mm long Deep Brain Stimulation (DBS) probe (Figure 4.11). The highly integrated DBS tip was designed to accommodate 40 circular electrodes on a semi-film substrate. The small silicon islands can contain prefabricated decoupling capacitors, and the large silicon island permits for wire bonding and back-end integration of ASICs inside the probe (e.g., flip-chip). All the structures are connected with flexible interconnects. This enables the activation of each individual electrode using only a couple of power and signal wires reaching out of the probe. As a result of the semi-flexible structure consisting of multiple silicon islands connected with a flexible film, the device can be folded into a 1.3 mm diameter cylinder (Figure 4.12).

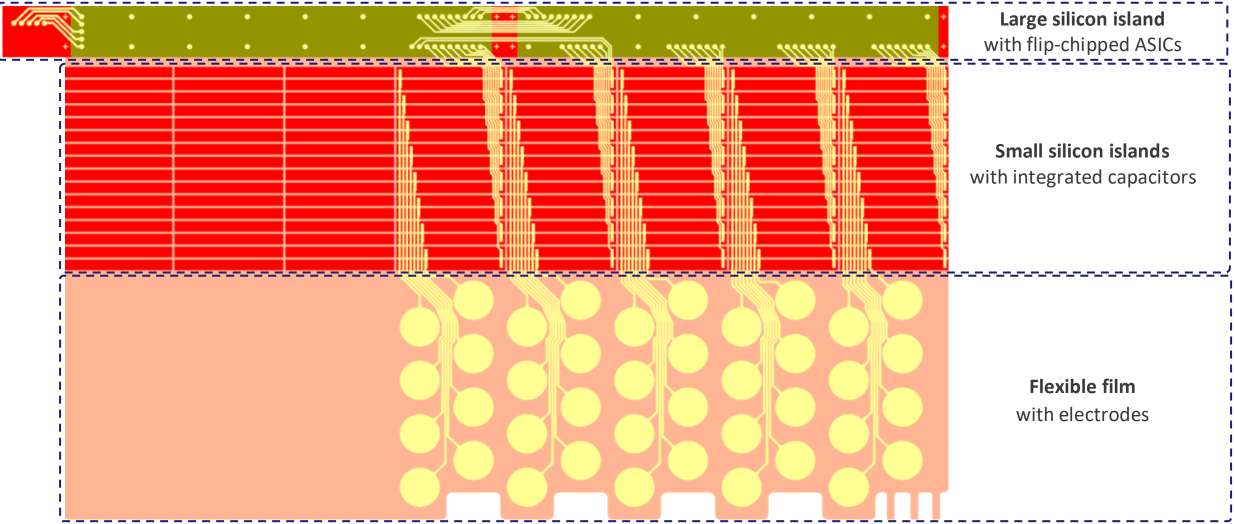

Figure 4.11: 2D representation of the 40-electrode DBS design with integrated electronic components. The large silicon island (18 mm x 1 mm) can contain flip-chipped ASICs. The small silicon islands (210 µm x 2070 µm) are separated with 40 µm wide trenches and can accommodate prefabricated de-coupling capacitors. The flexible film can contain 40 flexible electrodes.

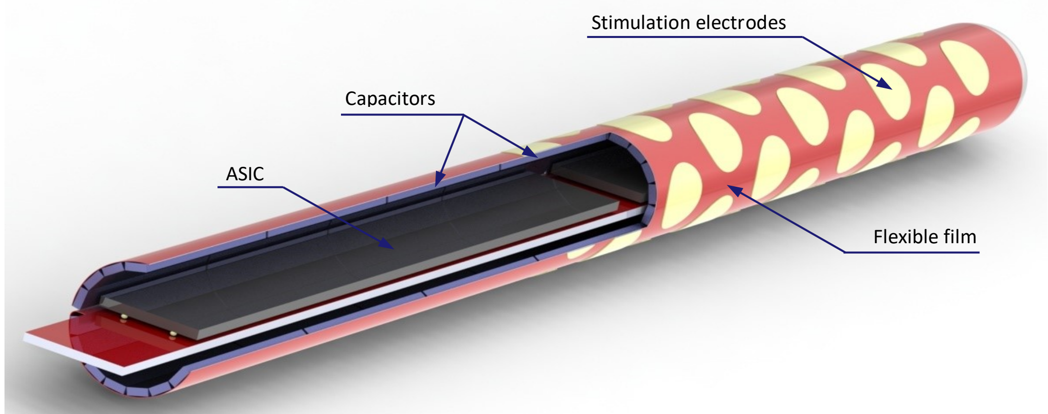

Figure 4.12: 3D model of the Chip-in-Tip concept incorporating two ASICs (chips) and eighty blocking capacitors inside the tip of the 40-electrode DBS probe.

4.4.3 DBS demonstrator fabrication using cavity-BOX

The DBS demonstrator is fabricated to illustrate the advantages resulting from applying the cavity-BOX to the process. The DBS demonstrator presented in this paper is a semi-flexible mechanical structure composed of silicon islands and a polymer-based flexible film. It does not contain interconnects, electrodes, or integrated electronic components.

The fabrication of the DBS demonstrator can be separated into two parts: the cavity-BOX SOI substrate preparation and the DBS demonstrator fabrication. The main technical challenge arises from the fact that the submicron (less than1 μm) alignment accuracy between the buried cavity-BOX mask and the structures on top of the device layer must be guaranteed. To overcome this problem, the alignment marker transferring strategy, proposed and developed by C. Mountain et al. [12], is applied to ensure high precision alignment of the structures.

Cavity-BOX preparation

A schematic process flow of cavity-BOX substrate preparation is presented in Figure 4.13. A 380 μm thick 6-inch double side polished (DSP) handle wafer was used as a starting material. First, two 140 nm deep ASML markers were patterned into the silicon substrate at a 1.2 mm distance from the left and right edge of the wafer. Next, 1 μm of high-quality thermal SiO_2 layer for wafer bonding was grown on both sides of the wafer. The customized cavity-BOX pattern was aligned with the markers, and dry etched into the SiO_2 layer, landing on the silicon (Figure 4.13a). The handle wafer was subsequently fusion bonded with the device layer[4], which also had a 500 nm thick layer of thermal oxide. The two oxide layers were bonded and merged into the cavity-BOX with the pre-patterned step oxide mask (Figure 4.13b). Finally, the device layer was thinned down to 80 μm, and a terrace with a width of 4 mm was created by a combination of edge trimming and wet etching (Figure 4.13c). The alignment markers on the handle wafer were revealed during this process.

The 4 mm terrace width was chosen to keep the edge of the device layer as far as possible from the alignment markers on the handle wafer in case of any possible optical interference during the marker transferring processes. The cavity-BOX substrate is ready after the terracing process. It contains a patterned step buried oxide layer (1.5 μm at its full thickness, 500 nm at its step thickness), an 80 μm thick device layer, and a 1 μm thick layer of thermal oxide on the backside of the wafer.

DBS demonstrator fabrication

To continue with the demonstrator fabrication, the handle wafer markers were first transferred to the standard ASML position on the device layer, placed 10 mm from the wafer edge, and etched 140 nm deep into the silicon (Figure 4.13d). A 2 μm thick PECVD SiO_2 layer was then deposited on top of the original 1 μm thick thermal oxide layer on the backside of the wafer and patterned into the silicon DRIE etching mask. Next, a 500 nm thick PECVD SiO_2 layer was deposited on the front side of the wafer as a structural layer and to improve the adhesion of the polyimide. Subsequently, a 3 μm thick polyimide layer (PI2610 Microsystems) was coated on top of the SiO_2 adhesion layer (Figure 4.13e) and cured. After that, the silicon DRIE etching step was applied from the backside of the wafer to remove the silicon substrate underneath the cavity-BOX landing on the step oxide mask (Figure 4.13f). The step oxide mask enables the silicon over etch to balance the etching non-uniformity across the wafer. An overall SiO_2 dry etching was subsequently applied to thin down the step oxide mask in the cavity-

[4] The exact bonding process details are proprietary to the project partner Okmetic.

BOX layer until the pre-patterned oxide mask was opened through to the device layer (Figure 4.13g). Finally, the 80 µm device layer and the 500 nm SiO_2 layer were dry-etched, landing on the polyimide layer (Figure 4.13h). After the etching of the device layer, all the silicon islands were separated and only linked with each other by means of the flexible polyimide film. The finished demonstrator is suspended in a silicon wafer frame through polyimide tabs.

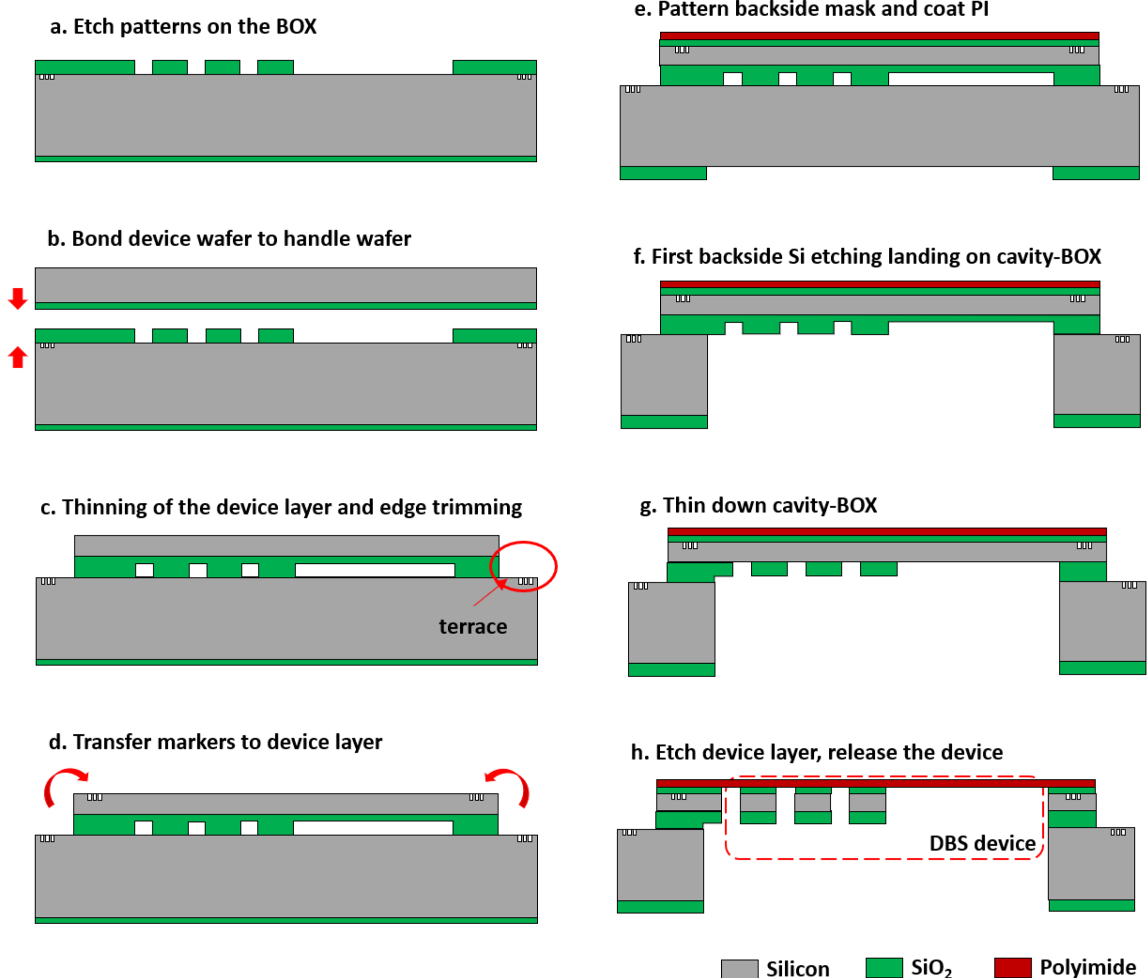

Figure 4.13: Cross-section drawings of the cavity-BOX substrate preparation and DBS demonstrator fabrication. (a) Positioning markers at 1.2 mm to wafer edge and etching patterns in the BOX on top of the 380 µm handle wafer. (b) Fusion bonding of the device wafer to the handle wafer with patterned BOX (in vacuum and room temperature. (c) Thinning of device layer to 80 µm and edge trimming to create a 4 mm width terrace. (d) Transfer markers from the terrace to the device layer. (e) Patterning backside etching mask and coating wafer with polyimide using silicon oxide as an adhesive layer. (f) Etching handle wafer from wafer backside and landing on the cavity-BOX. (g) Thinning down the cavity-BOX and exposing the buried oxide mask for device layer etching. (h) Etching device layer and silicon oxide adhesion layer, landing on polyimide.

4.4.4 Results and discussion

Both the substrate preparation and the demonstrator fabrication are straightforward, but there are several critical steps in the process. The bonding quality of the cavity-BOX can directly affect the substrate and the final device functionality. The marker transfer process determines the alignment accuracy between the BOX pattern and the structures on the device layer. The modified width of the SOI wafer terrace changes the substrate geometry, and thus it can influence its compatibility with standard microfabrication equipment. These issues will be further evaluated and discussed in this section. Finally, the DBS demonstrator fabrication and assembly results will be presented.

Preparation of the cavity-BOX

The cavity-BOX is formed by the bonding process of two oxide layers: 1 µm of pre-patterned SiO_2 layer from the handle wafer and a 500 nm thick SiO_2 layer from the device layer (Figure 4.13b). The potential concerns of the bonding process include bonding failures of the small oxide features to the handle wafer, undesired bonding in the large dimension cavities between the silicon substrate of the handle wafer and the SiO_2 layer from the device layer, and depressions in the device layer due to the cavities in the BOX.

After the cavity-BOX substrate preparation, no visible depressions were observed on the surface of the device layer. A scanning acoustics microscopy (SAM) was applied to inspect the bonding quality (Figure 4.14). The bonded area has a high transmission to the acoustic waves, hence it is displayed as a dark field in the picture, while air gaps reflect the acoustic waves and therefore are displayed as bright fields. The images indicate that the areas without cavities were bonded successfully, and there was no undesired bonding in the large cavity areas. No bonding defects have been observed among the small features in the SAM images. After the etching of the handle wafer landing on cavity-BOX (Figure 4.13f), no loss of smaller features with a dimension of 210 µm by 2070 µm was observed, which proves the excellent bonding result.

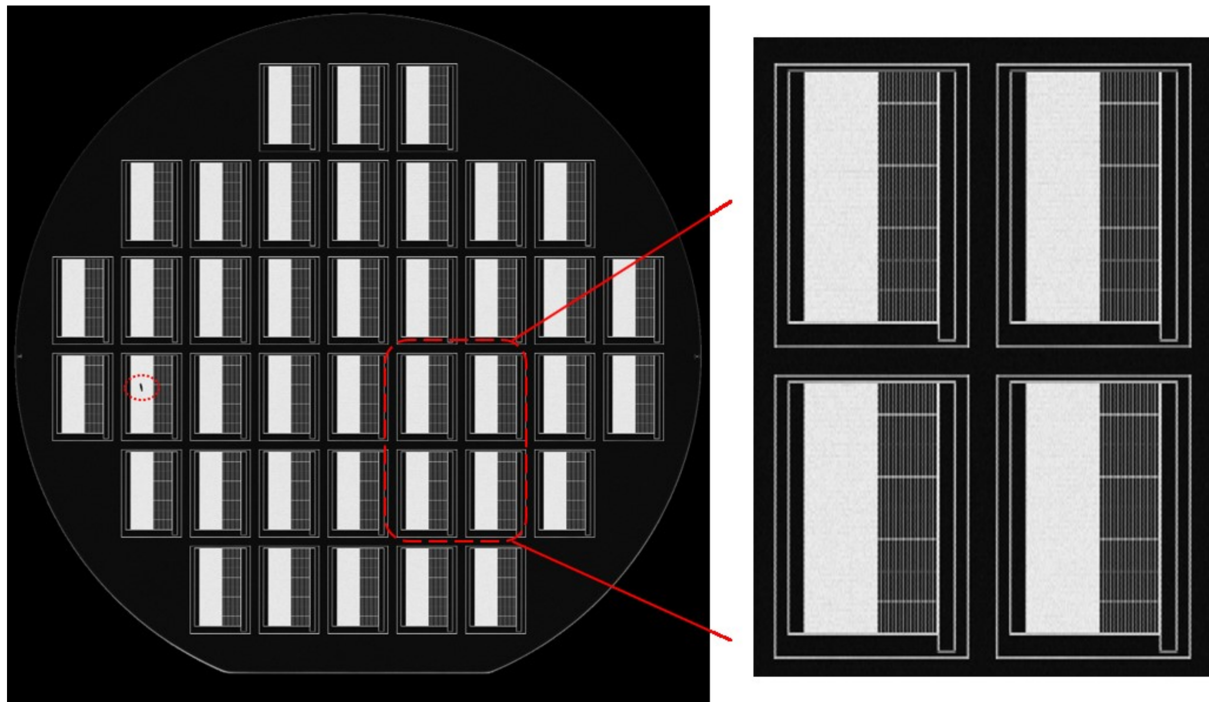

Figure 4.14: Scanning acoustic microscopy (SAM) to inspect bonding quality. A particle appeared as a black dot on the left side, and a zoomed-in SAM image of four dies.

Cavity-BOX terrace width

During the backside processing, it appeared that the 4 mm terrace width on the front side of the SOI wafer caused compatibility issues with the PAS5500 ASML wafer stepper and the SPTS Pegasus DRIE etching tool. During the backside lithography process, the wafer stepper needed to handle the wafer from the front side. The positioning of a few vacuum pads on the wafer stepper robot arm was in the 4 mm terrace region, leading to a vacuum loss. The wide terrace also caused helium leakage problems on the chuck of the dry etching tools. To continue processing the 4 mm terrace cavity-BOX SOI wafers, the robot arm of the wafer stepper was explicitly tuned to accept the wafers, and special

dry etching recipes with a low helium flow were developed for the silicon and SiO_2 etch. As a result of reducing the helium flow in the etching recipes, the wafer temperature cannot be well maintained during the process, leading to an increased non-uniform etch rate across the wafer. The etching slop was also enlarged due to the loss of temperature control.

To prevent the substrate compatibility issues, the terrace width is preferred to be as small as possible. At the same time, the terrace edge should be as far as possible from the markers to avoid its interference in the alignment process, requesting large terrace width. Therefore, a trade-off test was performed to define the optimal terrace width. Wafers with different terrace widths were tested in the standard 6-inch cleanroom processing line on a PAS5500 ASML wafer stepper, and SPTS Pegasus, ICP, APS etching tools. The test results indicate that a terrace width of 1.8 to 2.5 mm makes the wafers compatible with the above-mentioned cleanroom equipment while at the same time it does not affect the alignment accuracy.

Backside etching of the DBS demonstrator

To fabricate the demonstrator and form the semi-flexible device structure, several etching steps are performed from the backside of the wafer. The etching steps include the DRIE etching of the handle wafer substrate landing on the cavity-BOX, thinning down the cavity-BOX to form the pre-patterned oxide mask, etching of the device layer and the polyimide adhesion oxide layer using the oxide mask (Figure 4.13f-h).

Figure 4.15a depicts the wafer after the first step of the backside bulk silicon etching process landing on the cavity-BOX. The thickness of the remaining step cavity-BOX after silicon etching was measured with a reflectometer (Nanospec). The thinner part of the step cavity-BOX ranged from 120 nm to 350 nm (originally 500 nm), and the thicker part ranged from 1150 nm to 1380 nm (originally 1500 nm). It can be concluded that the cavity-BOX has fulfilled its function as an etch stop layer, even though the remaining slayer was very thin, suggesting a rather small process margin.

Figure 4.15b presents the wafer with the etched device layer after the third backside etching step. The large rectangular opening is transparent, as the etching landed on the SiO_2-polyimide-based layer deposited on the front side of the wafer. All the silicon structures, including the 40 µm wide trenches between the silicon islands and the gaps that defined the silicon frame, were successfully fabricated.

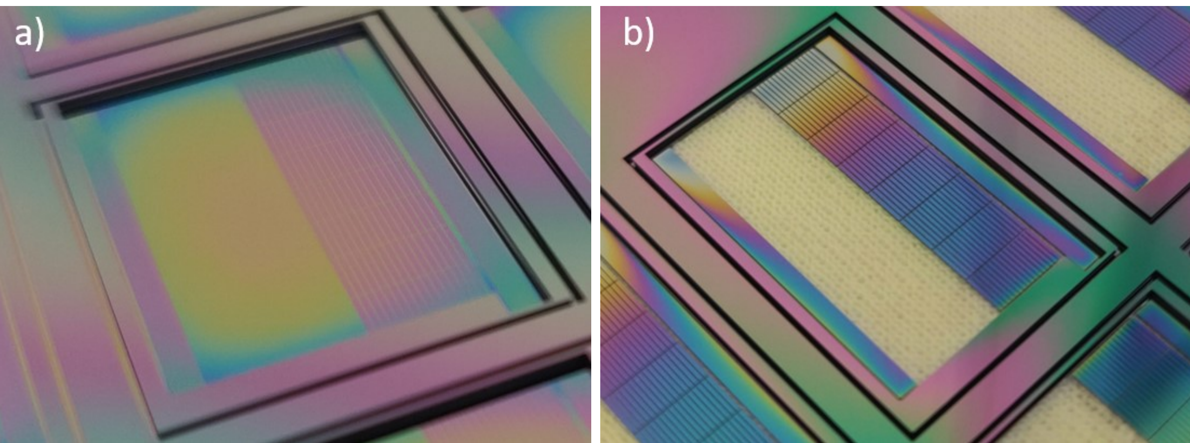

Figure 4.15: (a) Backside etching result of a silicon substrate, landing on cavity-BOX. (b) Etching device layer while using the patterned cavity-BOX as a mask, landing on polyimide.

Figure 4.16 shows SEM images of the silicon islands separated with the 40 µm trenches. The top part of the trench between the small silicon islands is 41.4 µm wide, while the bottom part is 54 µm wide. The measurement indicates an under etch of 6.3 µm from each side during the device layer etching, which is not ideal considering an etching depth of only 80 µm. The large under etch was mainly caused by the increased wafer temperature during etching which was a result of reducing the cooling gas (helium) flow that was necessary to process the wafer on the chuck of the silicon etcher. A better etching profile can be achieved for wafers with a smaller terrace width, which can be etched using the standard DRIE process without modifying the cooling gas flow.

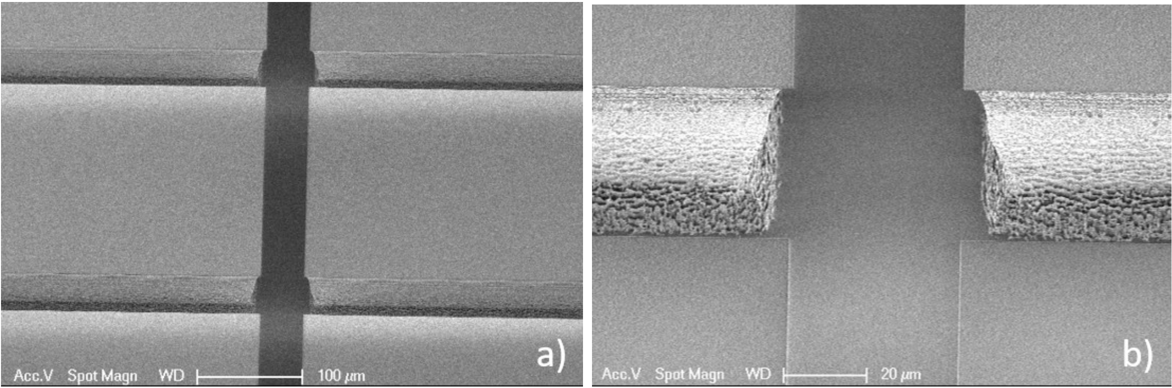

Figure 4.16: (a) SEM image of the 40 µm gaps between the silicon islands. (b) Zoom-in image of the 80 µm thick device layer etching profile, with 6.5 µm under-etch from each side.

DBS demonstrator assembly

After the fabrication, the demonstrator was taken out of the silicon frame (Figure 4.17). It consists of one large silicon island that can accommodate ASICs, 128 small silicon islands separated with 40 µm trenches, a large flexible film area, and a silicon island for handling. In the final DBS device, the DC blocking capacitors are located on each small silicon island, and the electrodes are located on the flexible film. During the assembly process, the silicon island for ASICs was attached to a thin metal string with a double-side adhesive tape. The metal string was slowly rotated, together with the silicon island, wrapping the semi-flexible device into a cylindrical probe. The assembled demonstrator has a length of 18 mm and a diameter of 1.39 mm (Figure 4.18).

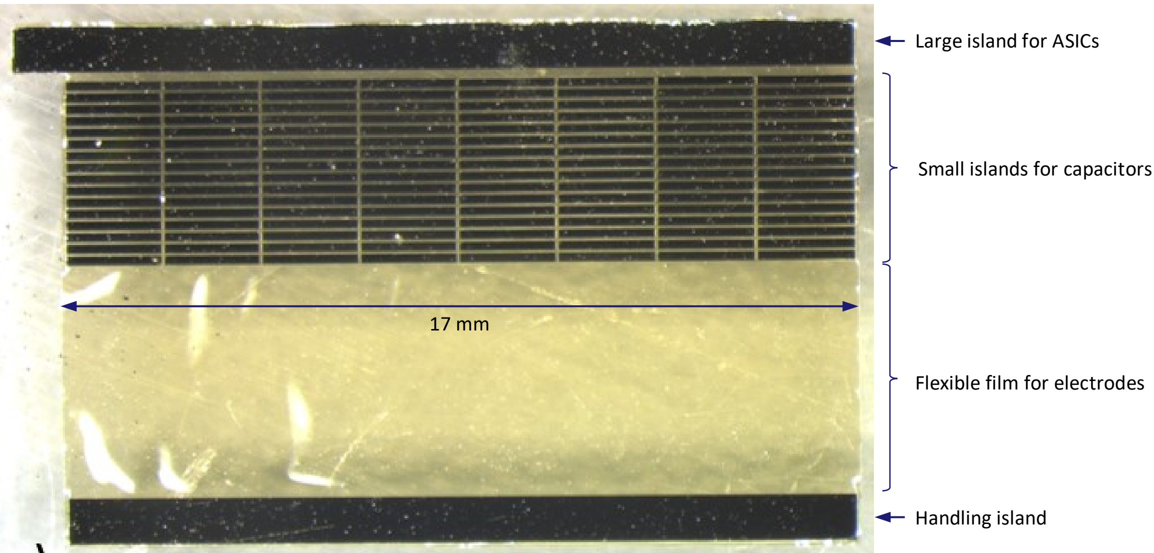

Figure 4.17: DBS demonstrator released after the fabrication. All the 80 µm thick silicon islands are connected by the flexible film. The small silicon islands are isolated by 40 µm wide gaps.

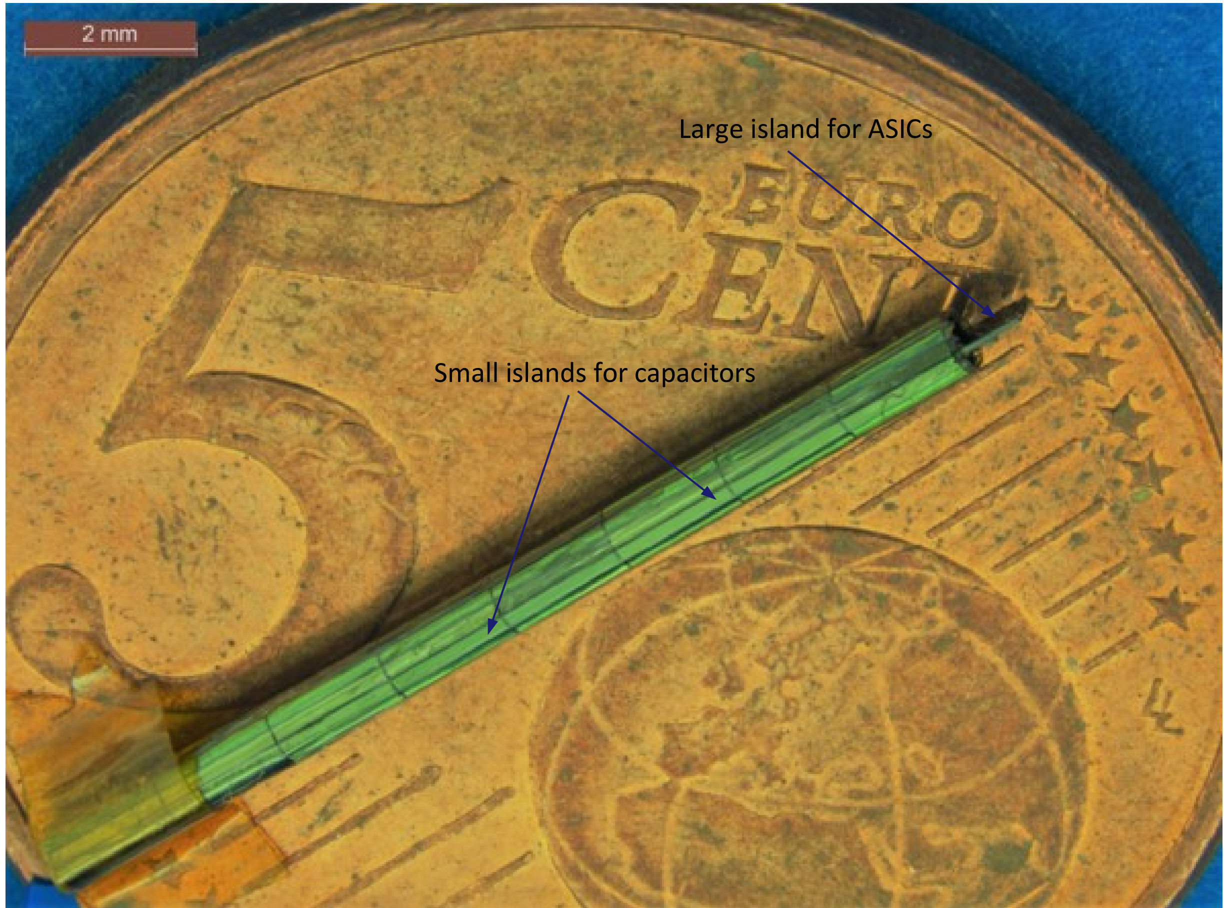

Figure 4.18: The DBS demonstrator wrapped into a cylindrical probe with a length of 18 mm and a diameter of 1.39 µm. The large silicon island for ASICs is wrapped inside the probe.

4.4.5 Conclusions

In this paper, an advanced cavity-BOX SOI substrate with a buried oxide mask was developed, prepared, and applied in the process of a semi-flexible microfabricated device. The oxide mask was first fabricated on the handle wafer and then bonded with the oxide on the device layer to form the cavity-BOX. The alignment between the structures on the device layer and the buried oxide mask was successfully realized by employing the front-to-front marker transfer strategy. The advanced SOI substrate was used in the fabrication of a DBS probe demonstrator. The cavity-BOX layer was used as an etch stop layer and a pre-patterned two-step DRIE mask to etch through the device layer from the backside of the wafer. The application of the cavity-BOX substrate to the DBS demonstrator fabrication resulted in a more robust and significantly simplified process and large design freedom, including the coexistence of high-precision micron-sized features and a large millimeter-sized opening. The semi-flexible DBS demonstrator with a length of 18 mm and a diameter of 1.39 mm was successfully fabricated and assembled.

Cavity-BOX SOI has a great potential to simplify the fabrication of various MEMS devices where device thinning and precise silicon structure separation/definition is needed. The cavity-BOX SOI substrate with a terrace width from 1.8 mm to 2.5 mm is compatible with standard cleanroom equipment for both the front and the backside processes. This terrace width also permits applying the high precision front-to-front alignment strategy. Depending on the design, the customized cavity-BOX SOI can be provided by the commercial SOI suppliers in large volume, hence extensively enabling the scaling up of the production.

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4.5 TRENCH CAPACITOR INTEGRATION PROCESS

The 40-electrode DBS lead design requires the integration of electronic components directly into the tip of the probe. The highly integrated tip must accommodate not only the steering electronics (two ASICs) but also a set of 40 safety capacitors that block direct current (DC) from reaching the brain tissue. The high-density trench capacitor technology developed by Murata is the only available technology that can provide the required capacitance of approximately 75 nF per electrode [1][2] without compromising the device diameter of 1.3 mm.

This silicon-based capacitors fabrication process is in theory compatible with the Flex-to-Rigid (F2R) technology employed for the DBS device fabrication process. Therefore, it is possible to integrate the capacitors onto the lead by prefabricating them directly onto the wafer substrates in the capacitors foundry already before the DBS fabrication process starts. Prefabricating the capacitors directly onto the substrate, instead of using the pick and place method, allows to minimize the space occupied by the capacitor and, at the same time, maximizes the capacitance density per electrode.

In this section, the feasibility of the inter-facility trench capacitor integration process is addressed. First, the employed capacitor manufacturing technology is introduced. Then the DBS design and the capacitors' design are carefully aligned, including establishing a common wafer alignment method. Finally, topics such as wafer resizing from 6 inches to 4 inches and inter-facility contamination prevention are addressed.

4.5.1 Trench capacitor technology

The PICS3 trench capacitors technology is used in this thesis. These 80 µm deep components have a capacitance of 100 nF/mm^2. The capacitors are fabricated on silicon substrate using standard semiconductor MOS processes, materials, and tools, making them compatible with the DBS process (Figure 4.19).

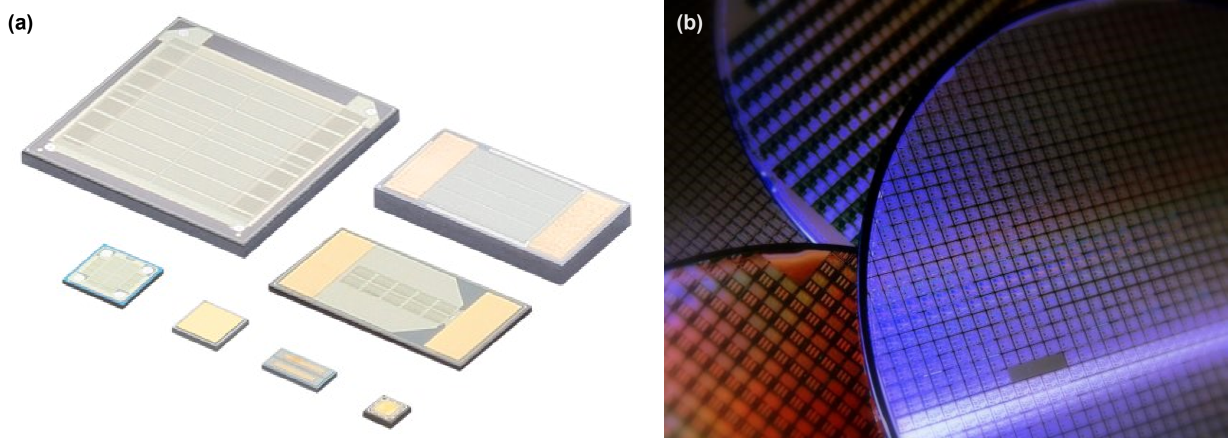

Figure 4.19: Trench capacitors fabricated in PICS technology [2]. (a) Various types of trench capacitors. (b) Full wafers with trench capacitors.

The trench capacitors (Figure 4.20) use the 3rd dimension of the wafer to increase the capacitor surface, and thus its capacitance, without occupying a larger area of the wafer [3]. The tripod-trench structure, developed by Murata, results in an even higher capacitance density than the traditional hole-trench structure. The footprint of the tripod-based capacitor versus planar capacitor with the same capacitance can be decreased by even two orders of magnitude (Figure 4.21).

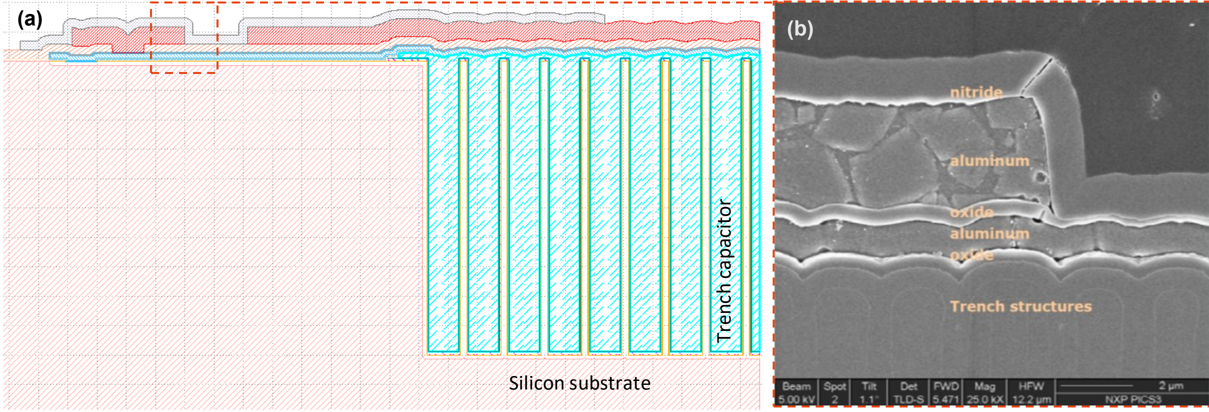

Figure 4.20. Trench capacitor cross-section. (a) Design model. (b) Zoom-in SEM image with marker stack layers. Source: InForMed.

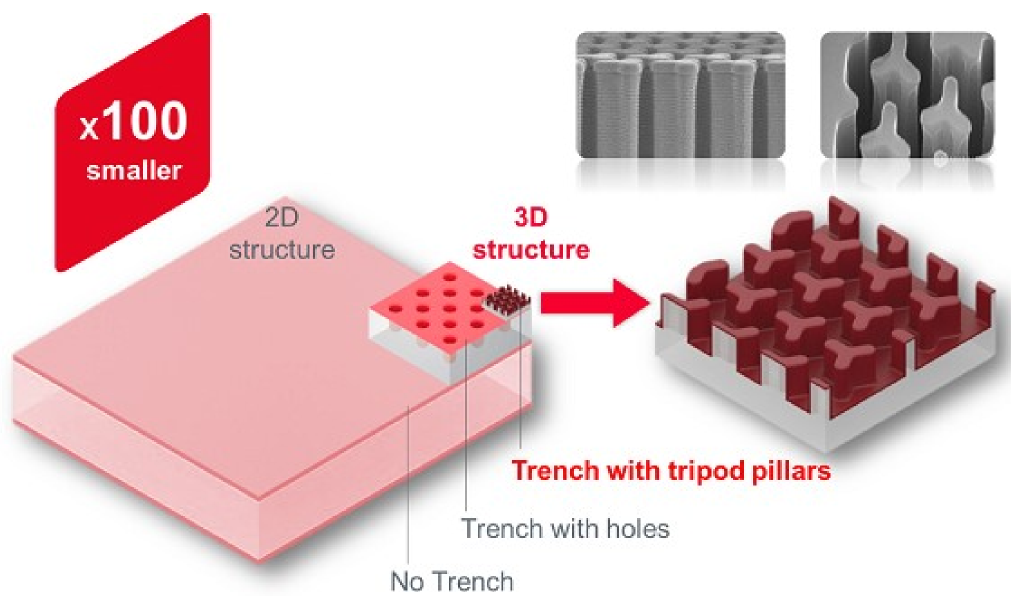

Figure 4.21. The footprint of the capacitors fabricated as a planar 2D structure, a trench with holes 3D structure, and a tripod pillars 3D structure [2].

Such densely packed capacitors enable significant electronic device miniaturization without compromising on unit capacitance that, in the case of the DBS device, can have a direct impact on patient safety. The layout of the capacitors is highly customizable. This makes the trench capacitors suitable for high-level pre-integration onto the F2R-based substrate (e.g., in the DBS process), already before the actual device is fabricated.

4.5.2 Structures alignment

The alignment of the capacitors process with the DBS process was performed in close cooperation with Murata. It was done to ensure that the capacitors with required parameters that are prefabricated at one facility (Murata) can be easily integrated into the DBS device fabricated at another facility (EKL). During the alignment phase, the design, the fabrication process, and the materials of the DBS device have been adopted to accommodate the capacitors in the proper configuration and ensure sufficient capacitance (for more details about the DBS design, see Chapter 2).

SOI substrate

The trench capacitors (PICS3 technology) selected for this trial require a minimum substrate thickness of 80 µm [2]. This thickness has been applied to the entire DBS design, namely to the silicon islands intended for the pre-fabrication of the capacitors, and to the island designated for integrating the ASIC via flip-chip. The 80 µm thick device layer ensures sufficient mechanical strength of the structures, and at the same time, allows for the folding of the miniaturized structures. An SOI wafer with an 80 µm thick device layer is used to ensure the correct substrate thickness. The desired device thickness is reached by DRIE etching the handle wafer from the backside and stopping on the 1 µm thick BOX layer.

Design alignment

To match the design parameters such as capacitance required per electrode or the capacitor islands layout, the quantity, size, and distribution of the components over the DBS device area are determined. Each of the 40 electrodes is linked to two capacitors, connected in parallel, ensuring sufficient space for integrating the total capacitance of approximately 75 nF per electrode. The capacitors are separated with trenches to make the structure foldable and to electrically isolate the capacitors (Figure 4.22). The capacitors and DBS metallization combined form metal tracks with the total length from bond pad to electrode between 7000 µm to 12100 µm.

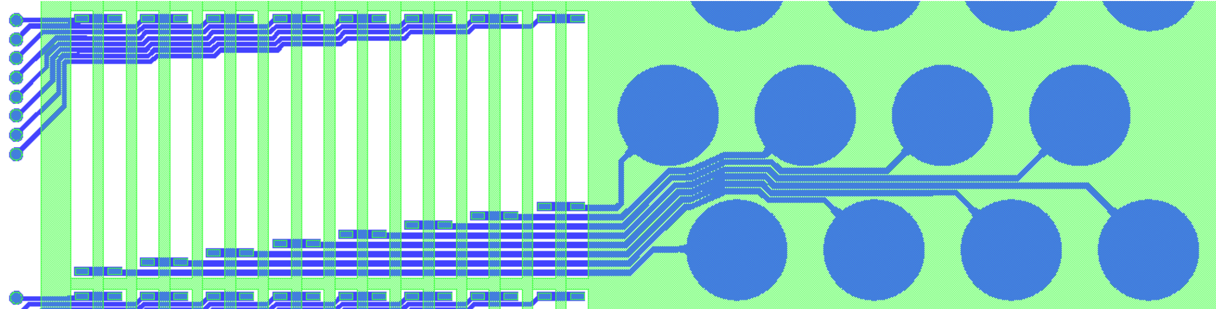

Figure 4.22: Fragment of the Chip-in-Tip DBS design showing the schematic of connecting the trench capacitors (white) with the circular electrodes (large blue circles). The green area indicates the flexible film.

The capacitors and DBS lead designs have been performed simultaneously. On the one hand, it was done to ensure connectivity between the flexible interconnects and the capacitors. On the other hand, joint process design allowed for sufficient overlap between the successive layers of the two structures. The detailed designs of the capacitors and the DBS lead performed at Murata and at TU Delft, respectively, comply with the local processing guidelines. More details about the DBS design can be found in Chapter 2.

Wafer layout

The capacitor integration method explored in this chapter assumes the fabrication of the capacitors on a 6-inch silicon substrate (at Murata) and subsequent DBS device fabrication on the same substrate but resized to 4 inches (at EKL). Additionally, each part of the process occurs in a different facility. The design of the structures and the die distribution over the wafer are carefully aligned to enable the inter-facility integration process. Accordingly, 16 DBS dies (Figure 4.23a) are distributed in the center of a 6-inch wafer, but only within the frame of a 4-inch wafer (Figure 4.23b).

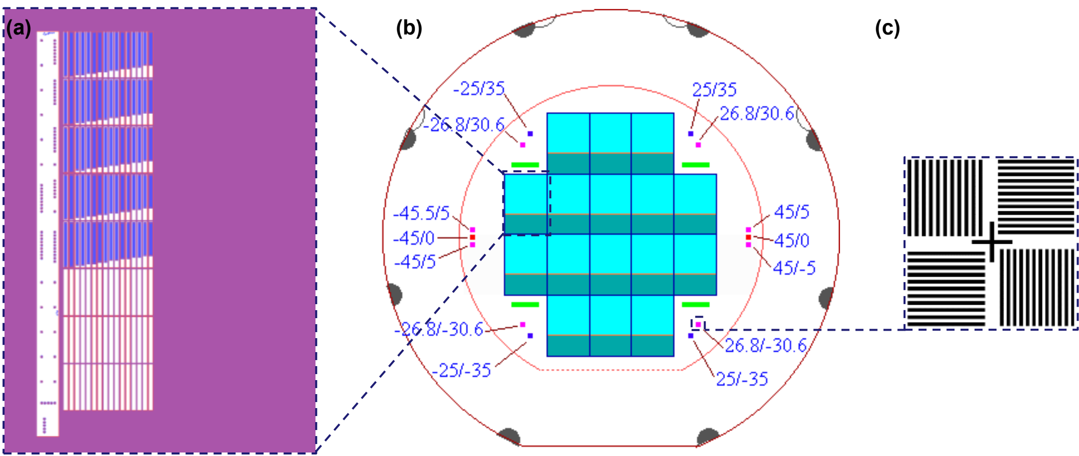

Figure 4.23: (a) DBS structure design. (b) Wafer layout of the trench capacitor custom-designed for the Chip-in-Tip DBS. Capacitors and alignment structures are placed on a 6-inch substrate within a 4-inch wafer frame. Source: Murata. (c) Standard ASML alignment marker.

Wafer alignment strategy

Besides alignment markers applicable for the 6-inch based capacitors process, the wafer has an additional set of ASML alignment markers (Figure 4.23c). The 14 secondary alignment markers are placed within the 4-inch wafer frame (Figure 4.23b). These secondary markers are compatible with the 4-inch based TU Delft facility, where the final integration takes place. These alignment markers are also used for wafer positioning during the wafer resizing process from a 6-inch to a 4-inch diameter.

4.5.3 Process alignment

The wafer-level component integration process is performed on the same substrate but at two different manufacturing sites. The capacitors are fabricated at Murata, and the DBS structure is fabricated at EKL. It requires extreme precision in the fabrication process alignment, including the lineup of tools and techniques used for material deposition and patterning (etching) of layers. Both facilities should be able to work with the selected materials. At the same time, the risk of cross-fab contamination has to be minimized. Moreover, all the layers used during the manufacturing of the capacitors must be taken into account to enable a smooth transition to the fabrication of the DBS device. For that, some layers have been modified (e.g., thickness, material, pattern) to fulfill their function both in the capacitors process and in the DBS process.

In an integration trial, dummy capacitors are used to align the inter-lab processes in a cost- and time-efficient manner. The dummy structures do not include the complete trench capacitor but only the silicon oxide passivation layers, the patterned aluminum top metallization layer, and the silicon nitride encapsulation layer. After the dummy capacitor fabrication, the wafers are resized from 6-inch to 4-inch diameter and the integration process is continued.

4.5.4 Integration

In this integration trail, the focus is shifted to the cross-lab alignment of the structures and establishing an electrical connection between the dummy capacitors' bond pads and the DBS metallization, including electrodes. For this, a simplified integration process is performed (Figure 4.24). It includes fabrication of dummy capacitors, wafer resizing, and integration of the DBS metallization. The simplified integration process does not include silicon islands separation with the trenches and the device release in the backside DRIE process.

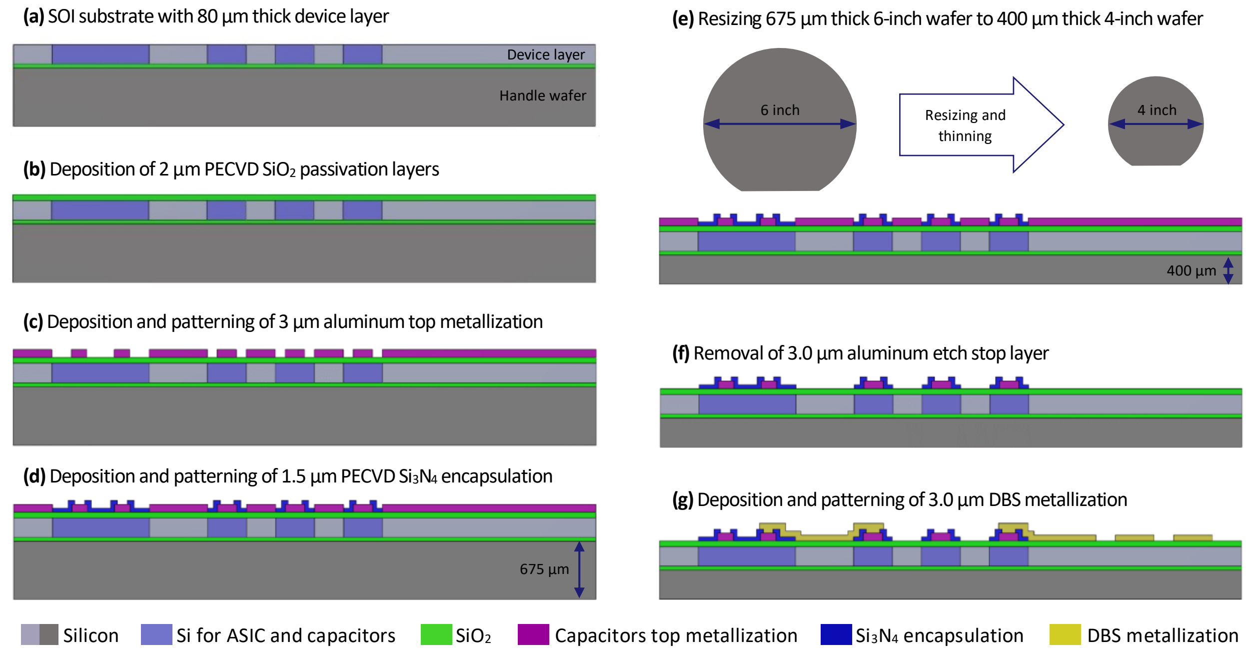

Figure 4.24: Simplified process for capacitors integration onto the DBS structure. (a-d) Dummy capacitors fabrication. (e) Resizing of the 6-inch substrate to the 4-inch substrate. (f-g) Integration of the DBS metallization.

SOI substrate

In this study of integration process feasibility, customized 6-inch SOI wafers are used. The wafers have a device layer of 80 µm, a BOX layer of 1 µm, and a total thickness of 675 µm (Figure 4.24a). The wafers are compatible with the final process, where capacitors structures are separated by trenches etched in the silicon.

Dummy capacitors fabrication

The dummy capacitors fabrication starts at Murata with the deposition of the two passivation layers: 0.3 µm PECVD TEOS and 1.7 µm PECVD SiO_2 (Figure 4.24b). The patterning of the total 2 µm thick silicon oxide layer is not performed due to the absence of any underlying structures. The composition and thickness of the test stack are preserved to mimic the layers present in the final stack (see Section 2.4.5). Next, a 3.0 µm thick pure aluminum layer is deposited by sputtering and is subsequently patterned (Figure 4.24c). In the capacitor fabrication flow, this layer serves as top metallization. In contrast, in the DBS flow, this layer serves as additional under-bump metallization for the final flip-chipped ASICs and as a etch stop layer during patterning of the encapsulation of the capacitors. Its purpose is to protect the earlier deposited SiO_2 passivation layers used in the complete DBS flow (see Section 2.4.5) as a hardmask for defining the silicon islands with trenches. Finally, the 1.5 µm thick PECVD Si_3N_4 encapsulation layer is deposited and patterned (Figure 4.24d). This layer encapsulates the top metallization in the areas with capacitors and bond pads for ASICs mounting. The maximum temperature during the fabrication of the capacitors is 400°C, which is maintained further down the integration process.

Wafer resizing

After the dummy capacitors are fabricated, the 6-inch wafers with a thickness of 675 µm are resized to 4-inch substrates with a 400 µm thickness (Figure 4.24e). This step is performed to ensure compatibility of the substrate with the EKL facility, where the capacitors integration is taking place. For proper alignment, four alignment markers

are used. The markers lie within the 4-inch wafers border, at the coordinates: X = {+26.8 mm; -26.8 mm} and Y = {+30.6 mm; 30.6 mm} with respect to the center of the wafer (Figure 4.23b).

The resizing starts with wafer thinning to 400 ± 5 µm thickness. The process consists of coarse grinding of the handle wafer from the backside, followed by a dry polishing step. Next, the wafer is installed front side up, and a 2-step circular bevel cut is made to resize a 6-inch substrate to 4-inch size. In the 2-step process, a cut into the wafer is made first using a straight blade. Then a V-shaped blade with a 45-degree angle[5] is used to create the chamfer on the top side of the wafer. The 2-step cut is repeated to define a primary flat[6] with a chamfer. Now, the wafer is placed on the dicing table with its backside up. A 45-degree chamfer cut is performed around the circumference and at the primary flat of the wafer.

The resizing process has been outsourced to a facility specializing in wafer dicing, resizing, grinning, and polishing (DISCO Hi-Tec Europe, Munich). The facility usually performs wafer post-processing, meaning that the diced wafers do not return to the fabrication stage. Moreover, all kinds of substrates and materials, including various polymers and metals, are permitted for processing.

To be able to perform the wafer-based integration of the capacitors with the DBS metallization, the wafer must be free of contamination with materials that are considered non-standard at the EKL facility. That includes, for example, the “red metals” such as platinum, copper, and gold. Moreover, the already exposed contact pads of the capacitors should be protected. Several means have been applied to prevent damage to the device or wafer contamination during the resizing process:

- Throughout all the processes, the front side of the wafer is always covered with a protective foil. The backside of the wafer is also always protected except during the backside grinding and polishing process.
- The wafer is never placed directly on the chuck of any machine. The surface that is facing down is always protected with a dicing foil.
- Only contamination-free wheels are used for wafer grinding and polishing.
- Only contamination-free dicing blades are used for wafer cutting.
- The wafer is always handled with dedicated, tweezers touching only its edge.

DBS structures fabrication

The resized to 4-inch diameter and 400 µm thickness wafers containing the dummy capacitors structures are further processed in the EKL facility, where the DBS structures are integrated with the existing capacitors. The integration starts with removing the 3.0 µm thick aluminum etch stop layer using a chlorine-bromine-based RIE process (Figure 4.24f). The exposed dummy capacitor contact pads and the bond pads on the silicon island intended for ASICs integration are protected with a 2.1 µm thick positive photoresist. Next, a 3.0 µm thick pure aluminum layer is sputter deposited and dry patterned using a chlorine-bromine-based plasma and a 2.1 µm thick positive photoresist as a mask (Figure 4.24g). At this point, the DBS metallization, comprised of electrodes and metal tracks with a minimum width of 30 µm and a pitch of a minimum of 40 µm, is integrated with the top metallization of the capacitors.

[5] Straight blade: 200 µm wide, V-shaped blade: 350 µm wide.
[6] Primarily flat at standard positon on the bottom of the wafer. Length: 32.5 ± 2.5 mm

4.5.5 Results and discussion

After completing the integration process, the inter-laboratory process feasibility has been evaluated. First, the substrate resizing process and wafer alignment were assessed. Second, the integration process was evaluated. Third, the actual structures integration and electrical connectivity were checked.

Substrate resizing

The 6-inch wafers, containing fabricated dummy capacitors structures, have been resized to 4-inch size and thinned down from 675 µm to 400 µm (Figure 4.25). During the process, no issues were observed. After grinding and polishing, the average thickness of the thinned down 6-inch substrates was 400.5 ± 2.0 µm, which is within the specifications (Figure 4.26). The total warp of 3.46 µm suggests that the thinning process was uniform and did not cause wafer deformation due to possible residual backside wafer damage remaining after the polishing process. Furthermore, no structures were damaged during the resizing process.

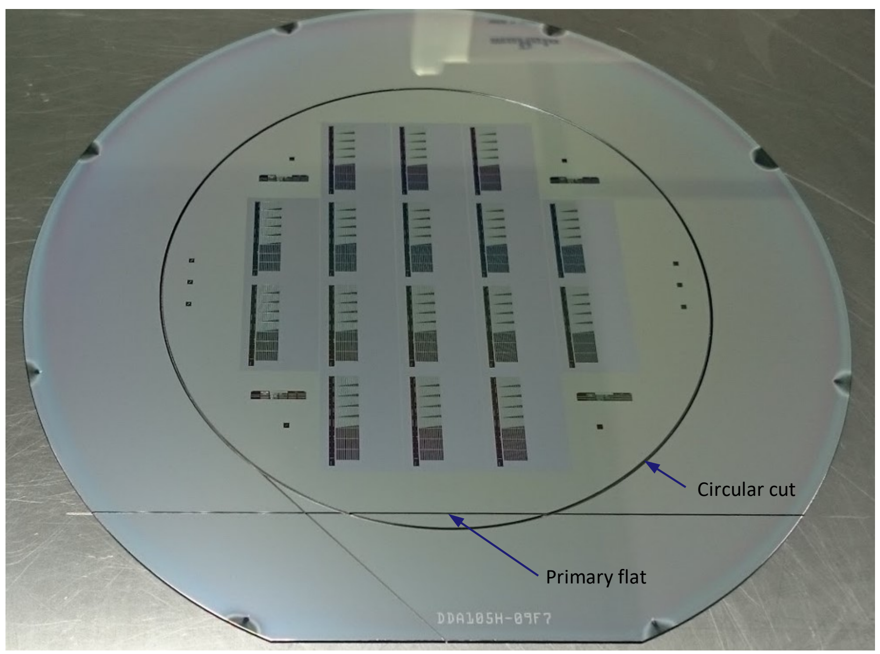

Figure 4.25: The resized 4-inch wafer in a 6-inch wafer frame including the chamfer cut and the flat cut at 32.5 ± 2.5 mm from the middle of the wafer. The 4-inch substrate contains 16 DBS structures with dummy capacitors in the middle of the wafer and a series of square alignment markers at the edges of the wafer.

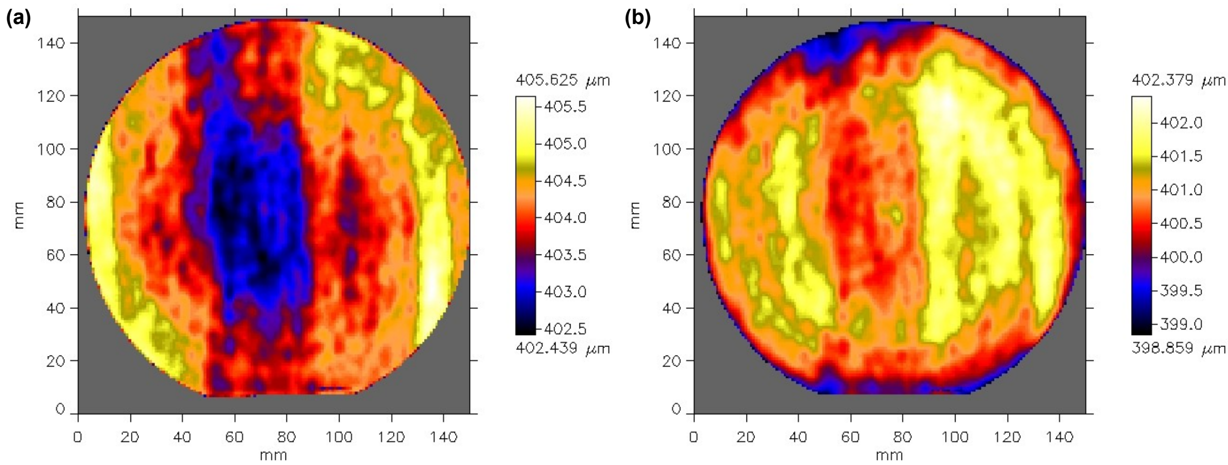

Figure 4.26: The thickness of the thinned down 6-inch wafer. (a) After coarse grinding. (b) After polishing.

Wafer alignment

The resized wafers were passed over the PAS5500 ASML wafer stepper. All the wafers were recognized and correctly handled throughout all the stages of alignment. This confirms that the wafer's diameter, the location and size of the primary flat, and the bevel cut were correctly defined. Furthermore, all 16 alignment markers have been detected, confirming their correct dimensions and placement.

During the first lithography steps of the integration process, several alignment adjustments were needed to ensure proper alignment of the prefabricated dummy capacitors to the DBS pattern. First, a global shift of +500.0 µm in the Y direction and +147.5 µm in the X direction was needed. The shift was related to the modified position of the dies in the coordinate system defined by the 4-inch substrate alignment markers. The die coordinates were modified to comply with Murata's standards for the layout of the structures on the wafer.

Integration process

During the integration process, the prefabricated dummy capacitors were combined with the DBS metallization (Figure 4.27). The DBS metallization was successfully deposited and patterned on top of the existing dummy structures. During the process, every two individual capacitors are connected with a single bond pad and a single electrode (Figure 4.28). After the integration, it was possible to establish an electrical connection from the bond pads, through capacitors' metallization, to the electrodes.

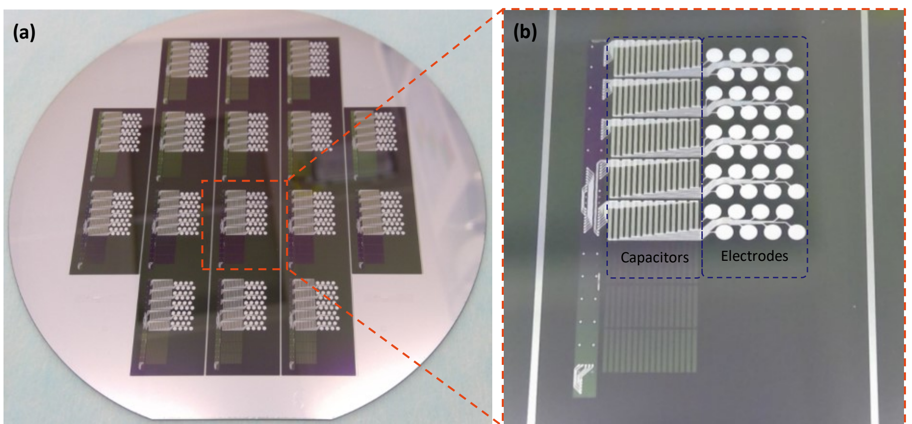

Figure 4.27: Wafer containing dummy capacitors integrated with the DBS metallization. (a) Finished 4-inch wafer with the integrated devices. (b) Zoom-in photography of one integrated device.

Electrical connectivity

The connectivity of the integrated dummy capacitors structures with the DBS metallization was evaluated using a manual probe station SÜSS MicroTec PM5 (Figure 4.29). The resistance of the integrated metal tracks was measured. During the measurements, one probe was contacted with the bond pad while the other probe was contacted with the corresponding electrode.

It was possible to make an electrical connection between the bond pads and the electrodes in over 70% of the integrated metallization tracks. The majority of the conductive tracks show resistance ranging from 6.4 Ω to 38.3 Ω, with an average value of approximately 18 Ω. The measured values are within the expected range of resistances from 4.7 Ω to 8.2 Ω or one order of magnitude higher[7].

[7] Resistivity ρ = 0.061 Ω·µm. Source: Karoui, 2011 [4]

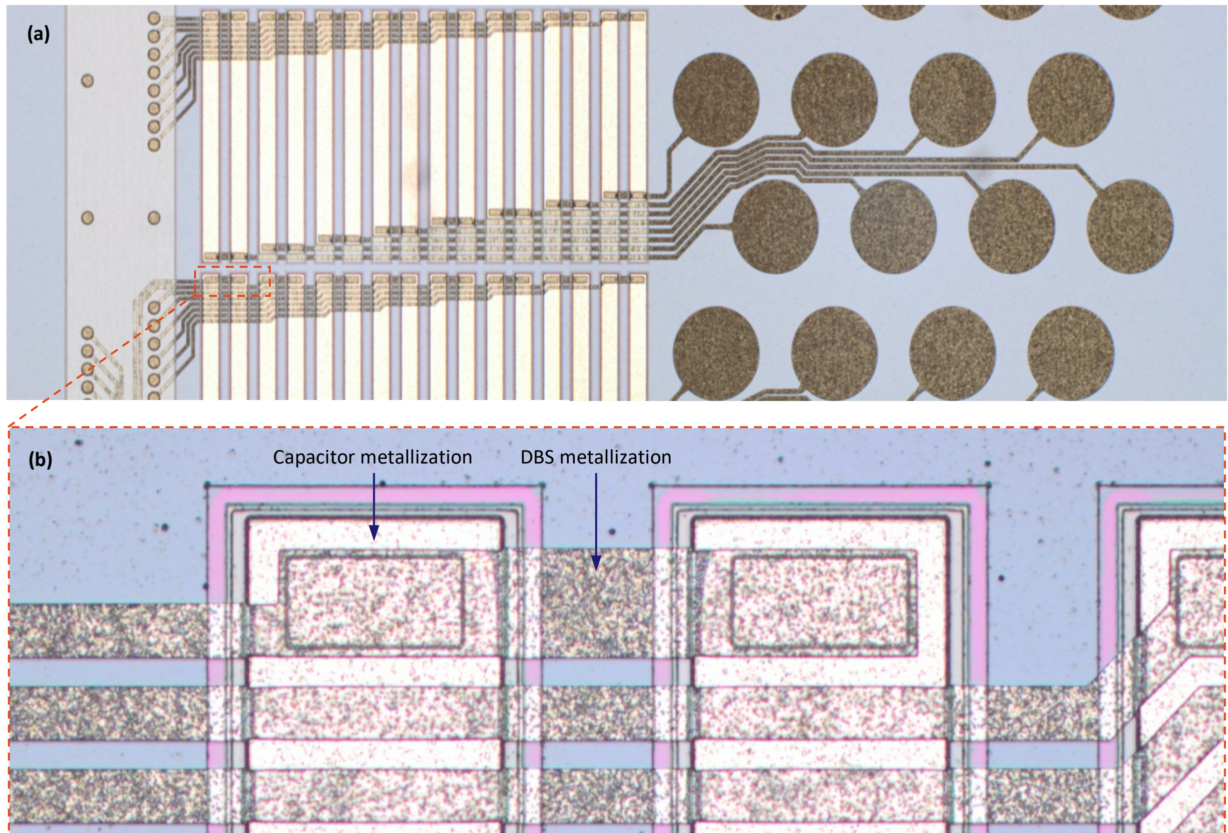

Figure 4.28: (a) Microscope image showing a fragment of the DBS metallization (brown) integrated with the dummy capacitors structures (white). (b) Zoom-in image showing the connection between the DBS metallization and the dummy capacitors.

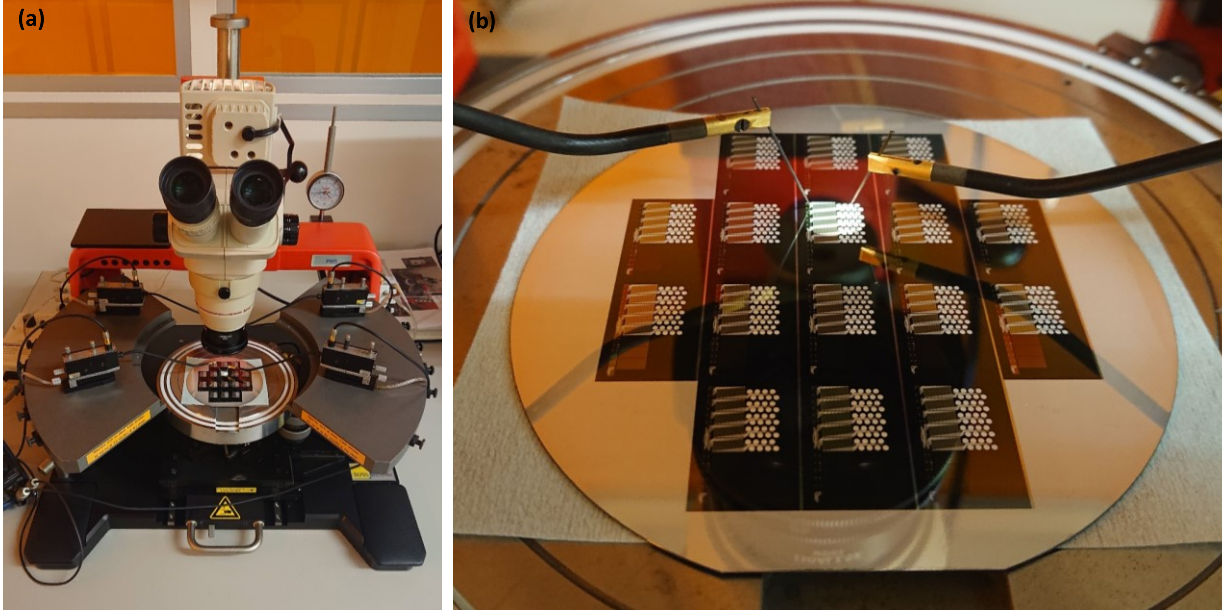

Figure 4.29: (a) Probe station SÜSS MicroTec PM5. (b) Wafer mounted on the probe station with two probes.

Some variation in the inter-track resistance is expected due to the specific design parameters such as the total track length, the varying track width, or the 3D geometry of the tracks. Another reason for the widely spread resistance values can be the varied location of the probe contact, especially on the large electrode area, and the contact accuracy on the small bond pad area.

The spread of the resistance values among the working metal tracks, and the lack of connectivity in the non-performing tracks, can be related to the fabrication process itself. For example, insufficient step coverage of the 3 µm thick DBS metallization over the topography of the dummy capacitors can result in metal tracks that are locally thinner than expected or even disconnected, leading to higher track resistance or even an open circuit.

4.5.6 Conclusions

The processing of silicon wafers in two completely different cleanroom facilities, such as post-processing the F2R-based DBS structures on a wafer containing prefabricated trench capacitors, requires close collaboration between the two manufacturing units. Such an inter-facility integration process has been described in this section, and a proof of concept wafers have been fabricated to demonstrate its feasibility. The close cooperation established between the manufacturing enabled excellent alignment of the device structures, even after substrate resizing from 6-inch to 4-inch. The carefully selected and matched materials, tools, and methods allowed for the successful inter-facility fabrication of dummy capacitor structures integrated with the DBS metallization. Over 70% of the integrated metallization tracks were correctly integrated.

Recommendations

The goal of this section was to demonstrate the feasibility of a mutual design and inter-facility integration process. Therefore, the fabrication process has been significantly simplified. For example, the SiO_2 passivation layers, which in the final DBS flow will serve as a hardmask for patterning the trenches that separate the capacitors, were slightly etched during the aluminum etch stop layer removal in one dry etch step. In the final fabrication process, these layers must be protected. Therefore, a combination of dry- and wet-etch is suggested. During the dry-etch step, the bulk metal is etched. The layer patterning is finished with a soft landing wet-etch step that is selective to silicon.

Another point of attention is the metallization material. To simplify the fabrication process and avoid the contamination-related processing restrictions, the aluminum layer was used in this experiment instead of the platinum metallization intended for the final DBS device. Consequently, several tool usage restrictions related to the presence of platinum will have to be managed. Furthermore, the platinum deposition and etching methods have to be matched with the properties of the prefabricated capacitors, such as maintaining the temperature budget below 400°C or establishing proper adhesion between the aluminum and the platinum metallization. Finally, to overcome the significant difference in the metallization thickness and achieve sufficient platinum step coverage, a special deposition method can be applied, such as a substrate tilt-rotation combination during the platinum deposition.

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4.6 CONCLUSIONS

In this chapter, a set of enabling technologies was developed to allow for the monolithic integration of prefabricated, custom-designed trench capacitors to the deep brain stimulation (DBS) device designed in the Flex-to-Rigid (F2R) platform. Two methods were developed to improve the F2R resolution and be able to separate silicon islands with only 40 µm wide trenches. One method exploits the sealable trenches, and the second method uses a customized cavity-BOX SOI substrate. Such closely-spaced silicon islands allow achieving the round shape of the DBS device after folding and ensure sufficient silicon area for integrating the high-density capacitors.

The compatibility of the F2R-based DBS fabrication process with the PICS3 capacitor technology was assessed. Both technologies use the IC-compatible tools and methods, which allowed for inter-facility processes alignment and monolithic fabrication of a DBS demonstrator with integrated dummy capacitor structures.

The developed in this chapter enabling technologies and the demonstrated feasibility of the monolithic inter-facility high-density capacitors integration process can greatly contribute to the miniaturization of all kinds of microfabricated devices. Flexible and foldable microelectronic devices such as neural implants can especially benefit from the upgraded F2R platform and the developed cavity-BOX substrate. Besides further miniaturization, they can provide more structural biocompatibility with the body and help in reducing the physiological impact of the miniaturized implantable device.

F2R with sealable trenches

The first enabling technology, developed for the precise definition and release of silicon islands with a 40 µm wide and 80 µm deep trench, uses standard SOI substrates and combines the sealable HAR microchannels with the Flex-to-Rigid (F2R) platform. In this method, the newly developed front-side etching method to form sealable HAR microchannels through a meshed mask was combined with the backside DRIE release process established within the Flex-to-Rigid platform. The joined approach allowed for the fabrication of the foldable DBS demonstrator with well-defined silicon islands suspended in the flexible film.

The advantage of this combination method, over standard back-side DRIE processes used in the current Flex-to-Rigid platform, is the almost unlimited design freedom where small and large open areas and silicon islands can coexist on one wafer fabricated using a monolithic process. A disadvantage might arise from the fact that at the early stage of the fabrication, the microchannels are etched in the device layer and sealed with a somewhat fragile silicon dioxide layer, making the wafer less mechanically robust during further processing steps. Nevertheless, the seal is reinforced with the flexible interconnects stack that provides sufficient mechanical strength to the DBS structure investigated in this thesis.

In addition, the developed meshed-based method for patterning of sealable HAR trenches in silicon can be applied alone, for example, to form fine microchannels of the advanced silicon-based microfluidic devices.

F2R with cavity-BOX SOI

The second enabling technology, developed for precise silicon islands separation with the 40 µm wide gaps, also employs the F2R back-side DRIE release process. However, this time it is performed on a customized cavity-BOX SOI wafer with a pre-patterned BOX layer. It has been shown how such a custom cavity-BOX can be designed and used

during the backside DRIE release to fabrication the foldable DBS demonstrator. The alignment of the structures has been ensured by applying a novel front-to-front alignment marker transferring strategy.

The use of the cavity-BOX SOI greatly simplifies the F2R-based fabrication process and improves its robustness, making it more scalable than the trench-based F2R process. Even though the cavity-BOX-based process involves a custom SOI substrate, which might generate a major cost increase, especially in small-scale production, the process has great potential to simplify the fabrication of many other microelectronic devices that require precise silicon structure separation.

Capacitor integration process

A monolithic wafer-based process for the integration of the F2R-based DBS device structures with prefabricated trench capacitors has been developed, and its feasibility has been demonstrated. The key points of the inter-facility integration process, such as the joint design, alignment strategy, wafer resizing method, tools and processes alignment, and contamination prevention, have been recognized and addressed early in the process design phase. Thanks to the close collaboration with the capacitor manufacturer, it was possible to complete the DBS design with the required blocking capacitor structures. Finally, a functioning demonstrator consisting of dummy capacitors and the DBS metallization has been fabricated at the two cooperating manufacturing sides.

The advantage of the presented inter-facility integration process is the elimination of the commonly used die-level pick-and-place technology. It reduces the risk connected with die-level handling and allows for significant device miniaturization by integrating components such as ASICs or capacitors directly into and not onto the silicon. Furthermore, such a wafer-scale hybrid integration approach will improve the scalability of many other than Flex-to-Rigid microfabrication processes, especially when device miniaturization plays an important role, and the quality of the outsourced components may not be compromised. Additional costs and time must still be invested in custom component design and establishing the inter-facility integration process.

5

PACKAGING TECHNOLOGIES

5.1 INTRODUCTION

The Chip-in-Tip DBS device is fabricated as a flat semi-flexible structure that, after assembling the ASICs, is folded into its final, cylindrical shape to form the DBS probe. Due to the device-specific construction and somewhat unique assembly approach, some custom technologies had to be developed to enable the packaging of this highly integrated microelectronic device. The wrapping method was developed in collaboration with Philips Innovation Systems (PInS), and the filling method was investigated in collaboration with the Fraunhofer IZM (FIZM).

This chapter explores enabling technologies to wrap and fill the device into a needle-like probe. The focus is on the development of the technologies rather than executing the complete device packaging and assembly process. The assembly of the lead extension and the final device encapsulation are not within the scope of this thesis.

5.2 DEVICE WRAPPING

During the wrapping process, the DBS structure with integrated capacitors and flip-chipped ASICs is folded into a probe with a diameter of approximately 1.3 mm. The inside of the DBS device contains the ASICs, which means that the traditional technique of wrapping around a rod cannot be applied. Therefore, a custom tool has been designed to wrap the device into its cylinder shape without the need for a mechanical support.

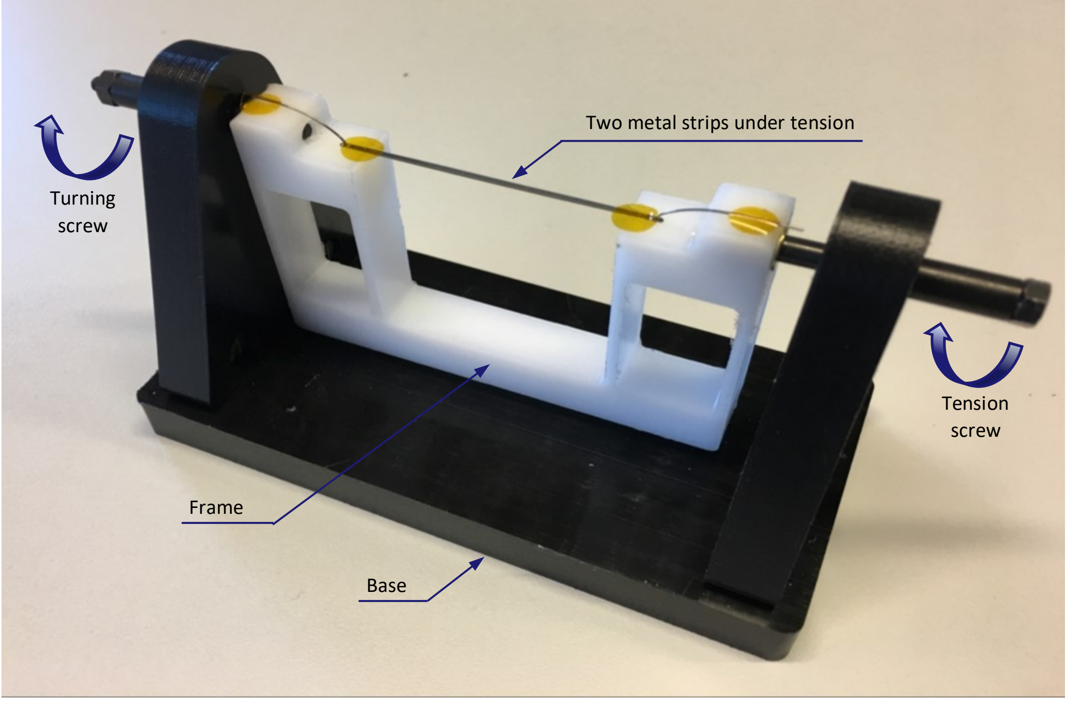


Figure 5.1: Custom-designed tool for wrapping the fabricated DBS device into a cylinder-shaped probe. Source: PInS.

Mock-up DBS devices are used for testing the wrapping process. These parylene-silicon-based structures are composed of 80 µm thick silicon islands suspended in a 10 µm thick parylene flexible film. The structures do not include integrated components or metallization.

5.2.1 Wrapping tool

The tool prototype is composed of a base in which a rotating frame with two thin metal strips is mounted (Figure 5.1). The frame is mounted in the base using two screws. One of the screws (turning screw) is fixed to the frame and allows the complete frame to be rotated around its axis to wrap the device. The other screw (tension screw) is movable, and it is used to adjust the tension of the metal strips so that the device can be clamped between them.

5.2.2 Wrapping process

The released from the wafer mock-up device (Figure 5.3a) is mounted in the wrapping tool in such a way that the silicon island designated for ASICs is clamped between the two tensioned metal strips (Figure 5.2a). The parylene film is facing upwards while the silicon islands are hanging down. At that point, an adhesive glue is applied to the flexible film from the bottom. Next, a transparent foil with equal weights on both sides is placed on top of the device (Figure 5.2b). The weighted foil rolls together with the device during the wrapping process, ensuring the transverse force necessary to wrap the device. The proper alignment of the structures, tight closure of the capacitor ring, and the final device diameter are tuned by adjusting the applied weight. The double-wrap design, shown here, is wrapped in two full turns of the frame (Figure 5.2c). During the second turn, the applied glue is distributed across the device. The amount of glue and its application pattern is optimized to prevent adhesive overflow, which might cover the electrodes. The wrapped device is set aside for the glue to cure. When the glue is cured, the tension is released from the metal strips, and they are removed from the inside of the wrapped device.

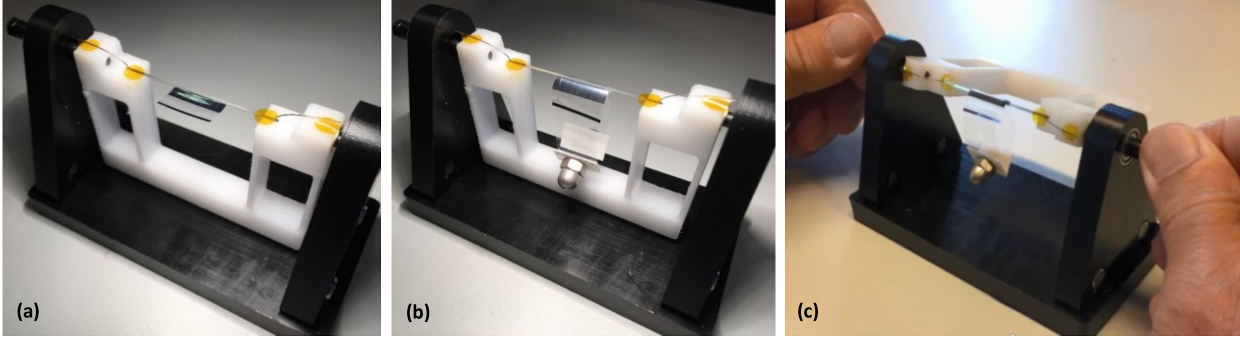
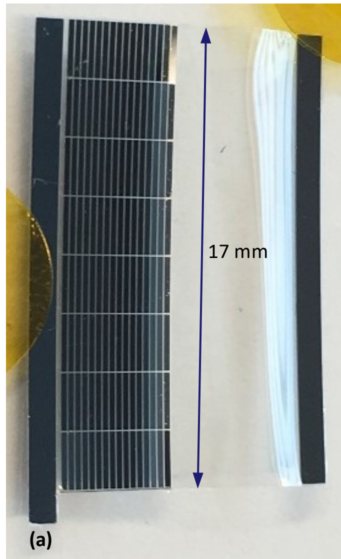
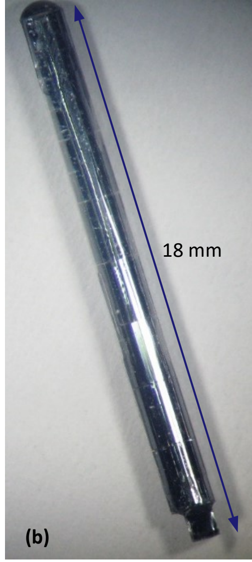


Figure 5.2: The custom-designed wrapping tool. (a) With mounted DBS device. (b) With weighted DBS device. (c) During the wrapping process. Source: PInS.

5.2.3 Results and discussion

It was possible to successfully wrap the mock-up DBS device (Figure 5.3a) into a 1.3 mm diameter cylinder with a straight corpus and cylindrical shape (Figure 5.3b,c). After wrapping, the structure is somewhat resistant to bending along the cylinder, but it is relatively fragile when force is applied across the cylinder. The final stiffness of the device, required for its proper implantation, is to be ensured later on during the device filling process.





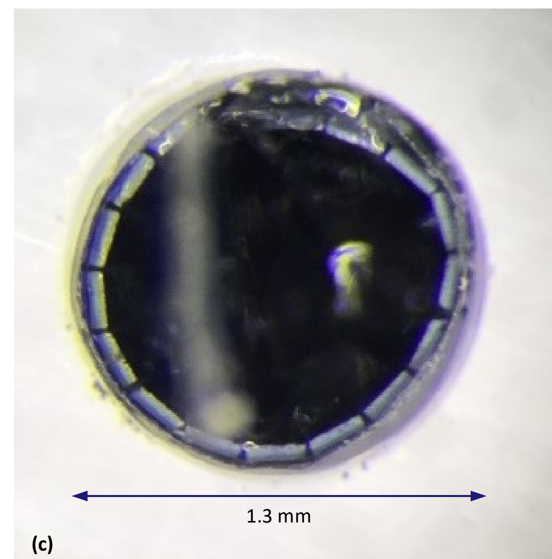


Figure 5.3: The mock-up DBS device. (a) Before wrapping. (b) Side-view after wrapping. (c) Top-view after wrapping with visible capacitor islands around the device circumference. Source: PInS.

The diameter of the wrapped device meets the design requirements. Also, most of the capacitor islands are evenly distributed around the circumference of the device. However, the transition point from the first wrap layer (with the capacitor islands) to the second wrap layer (flexible film) is not as smooth as expected. It also seems that there is a 200 µm wide gap between the first and the last capacitor island in the row, while the gap planned in the design is 80 µm wide. For a tighter fit, the weight applied during the wrapping process should be slightly increased.

5.3 DEVICE FILLING

After wrapping, the DBS device forms a hollow cylinder (diameter of 1.3 mm) with a loosely floating silicon island inside it. The cylinder must be filled with a biocompatible material suitable for application in long-term implantable devices. This is to provide the stiffness to the device, fix the floating silicon island in place, and internally encapsulate all the components to protect the device from corrosion due to moisture. No voids should be present inside the cylinder and between the capacitors as they might become an origin for moist condensation and consequent device failure. In this section, a thin medical-grade epoxy (EPO-TEK MED-301-2FL) with a viscosity of 0.1-0.2 Pa·s is tested as a potential candidate for the DBS probe filler.

5.3.1 Methods

To properly evaluate the suitability of the tested filling process and material, two 100 µm thick dummy chips with platinum stud bumps were additionally mounted onto the designated silicon island (Figure 5.4). Subsequently, the mock-up DBS devices were wrapped into the cylinder shape (Figure 5.5).

The wrapped mock-up devices with attached ASICs were placed vertically in a mold with a diameter of 1.4 mm. Subsequently, the medical-grad epoxy was dispensed inside the mold. The low viscosity of the material allows for capillary filling of the narrow device, including the trenches between the capacitor islands. After the filling, the epoxy was cured at 60°C for four hours, and the filled devices were removed from the mold.

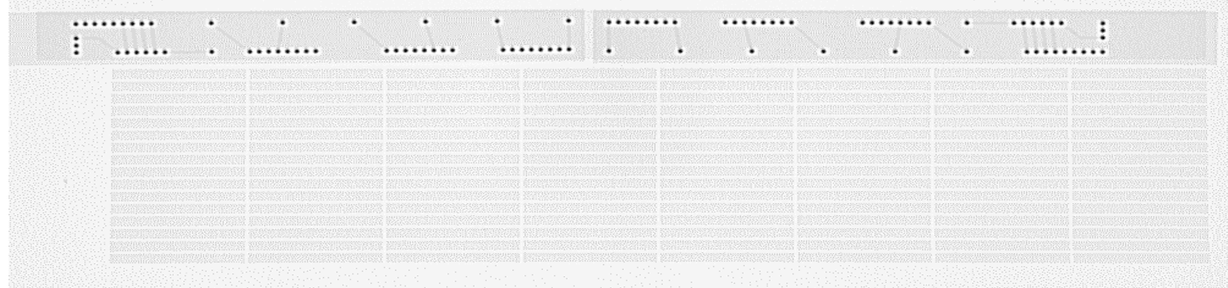


Figure 5.4: An X-ray image of part of the unwrapped mock-up DBS device with two 100 µm thick ASICs mounted on the designated silicon island. Source: FIMZ.

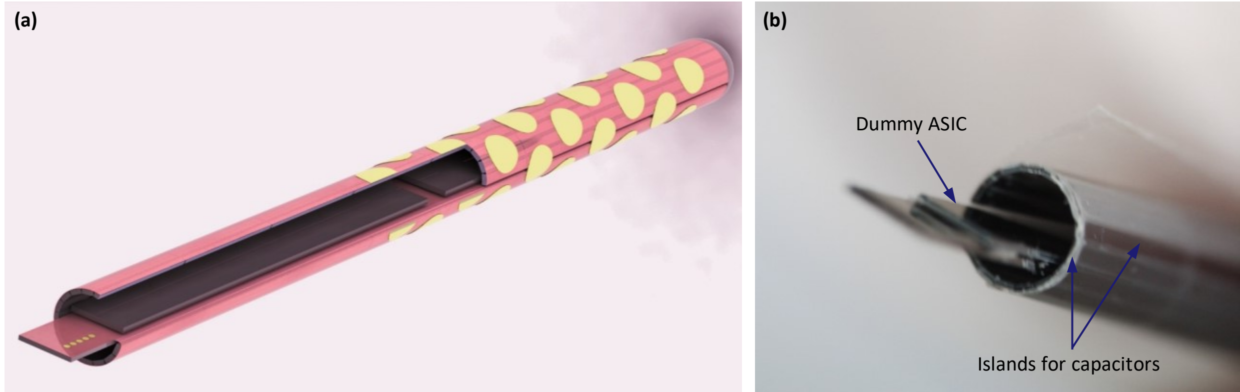


Figure 5.5: (a) A 3D model of the Chip-in-Tip DBS device. (b) An image of the end of the wrapped mock-up DBS device with islands for capacitors integration and mounted 100 µm thin dummy ASICs. Source: FIZM.

5.3.2 Results and discussion

Figure 5.6 shows the mock-up devices filled with epoxy. The device has a diameter of 1.4 mm, corresponding to the size of the mold. If needed, the diameter can be further decreased by using a mold with a smaller diameter. The cured epoxy provides mechanical support for the structures located inside and around the cylinder and ensures sufficient stiffness of the filled device.

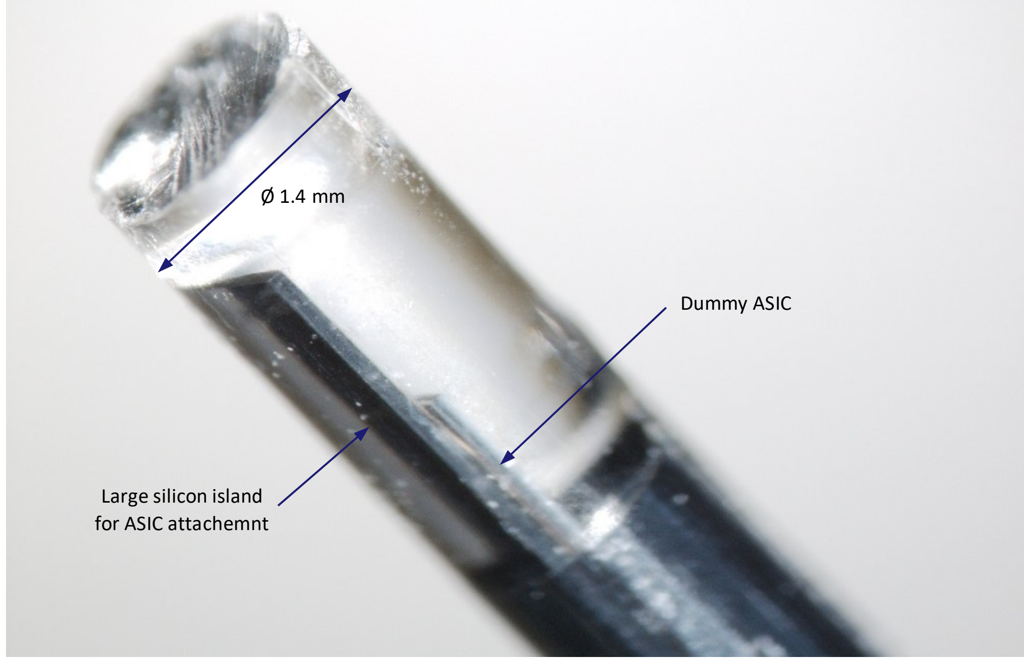


Figure 5.6: The mock-up DBS device filled with medical-grade epoxy EPO-TEK MED-301-2FL. Source: FIZM.

Besides optical inspection, X-ray imaging was used to determine whether the capillary-based process resulted in voidless filling of the device. The X-ray imaging (Figure 5.7a) and the inverted X-ray imaging (Figure 5.7b,c) do not indicate any issues with adhesion nor show signs of voids around the island with ASICs or in between the capacitor islands. The device was filled completely and without voids.

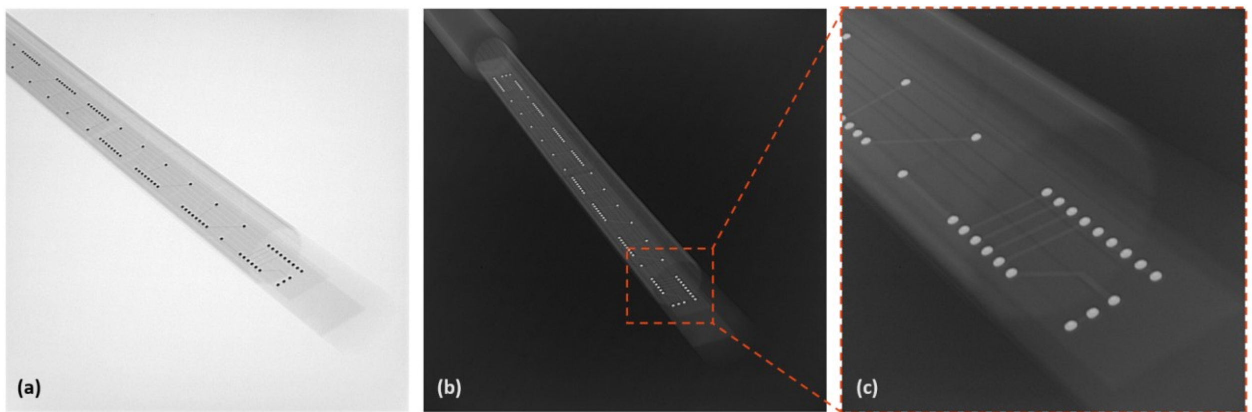


Figure 5.7: The mock-up DBS device filled with medical-grade epoxy EPO-TEK MED-301-2FL with visible DBS structures and the platinum stud bumps. (a) X-ray image. (b) Inverted X-ray image. (c) Close-up inverted X-ray image. Source: FIZM.

5.4 CONCLUSIONS

Wrapping

In this chapter, it has been shown that a mock-up DBS device with attached dummy ASICs can be successfully wrapped into a cylinder with a diameter of 1.3 mm using a custom-designed wrapping tool. Thanks to an innovative mounting method, where the device is clamped between two metal strips, the device can be rolled into a cylindrical shape without the need of introducing additional elements, such as metal rods, that would remain inside the probe after the assembly process is finished. Furthermore, the developed wrapping technique minimizes the manual handling of the device.

The prototype wrapping tool proved to be suitable for the Chip-in Tip device, and with some optimization, can be applied to other devices where 2D structures must be wrapped into a 3D cylinder. For this, it is recommended to develop a system for exact device alignment during mounting, for example, by optimizing the metal strips profile and adding an edge to which the device can be aligned. Additionally, the way of applying and optimizing the transverse force can be improved. Applying a multi-point tension only at the end of the device (e.g., to the handling structure) can prevent the direct contact of the weighted foil with the structures of the device. This approach requires automation and synchronization of the wrapping rotations with the forward approaching tension source, which is recommended especially if large-scale production is considered.

Filling

The wrapped mock-up devices were filled with a low viscosity medical-grade epoxy (EPO-TEK MED-301-2FL) that provided the mechanical strength and secured all the structures in place. The low viscosity of the epoxy allowed for the capillary filling of the narrow trenches between the capacitor islands without voids. However, the suitability of the epoxy for active implantable devices exposed to bodily fluids for an extended period still needs to be evaluated.

During the filling process, the device with a diameter of 1.3 mm was placed in a mold with a diameter of 1.4 mm, which was then completely filled with epoxy. In effect, the filling material has also leaked to the outside of the cylinder and coated the flexible film on which the exposed electrodes will be located. In future iterations, it is recommended to precisely apply the right amount of epoxy only to the inside of the cylinder. This prevents any leakages to the outside of the device and maintains its original dimensions.

6

PARYLENE PROCESSING IN MICROFABRICATION CLEANROOM[1]

6.1 INTRODUCTION

In the field of implantable devices for neurostimulation, there is a strong tendency to move towards more flexible structures that are more mechanically compatible with the body. In the case of deep brain stimulators, such as DBS, the choice of materials that can be used in the device is additionally restricted as they have to comply with a higher biocompatibility class (USP class VI). Parylene C (further called parylene) is a flexible polymer that complies with the biocompatibility and biostability restrictions set for brain neurostimulation devices. In combination with platinum metallization, it can be used to fabricate flexible neurostimulation devices.

However, a scalable and, more importantly, robust process for the fabrication of such devices in a microfabrication cleanroom (CL100) environment is still challenging. First of all, parylene is still considered an exotic material in the CL100 environment [1]. At the start of the project, there was very little knowledge on how to process wafers containing this material in microfabrication laboratories. The processing hygiene and good practice had to be established to avoid tool contamination and parylene layer damage. Secondly, parylene is resistant to many solvents, such as acetone or isopropanol, and mild etchants, such as PES (phosphate-buffered saline). However, it is vulnerable to oxidizing agents, such as concentrated or boiling HNO_3, or oxygen plasma that are used in microfabrication cleanrooms for wafer cleaning or photoresist stripping (e.g., at the EKL Laboratory). Therefore, an alternative processing method or agents had to be tested. Finally, parylene has a very low temperature budget. At temperatures higher than its glass transition temperature, which is in a range from 80°C to 100°C, parylene can undergo irreversible changes (crystallization), and it can start reacting with oxygen to which it is directly exposed. This means that, for example, photoresist baking steps performed during the soft lithography process have to be customized and kept below 100°C. Furthermore, the melting point of parylene is at 280°C, which prohibits steps like PECVD or LPCVD depositions of layers such as SiO_2 or Si_3N_4 that usually are performed at around 400°C and higher. These layers often serve as insulators and are essential when working with silicon substrates. So far, practices like wafer transfer, using a sacrificial layer, and manual release of the final device have been applied to move the parylene deposition to the very end of the fabrication process and overcome this restriction [2]. However, such a practice does not make a robust and scalable process.

In Chapter 2 a design of a novel parylene-platinum based DBS device has been presented, and a monolithic fabrication flowchart, which does not involve wafer transfer, has been proposed. In this chapter, the fabrication process steps are investigated individually or through short-loop experiments that combine a couple of steps to

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[1] The chapter is partially based on the work of supervised master students A. Kanhai [30] and D. Wu [10].

determine the suitability of the customized processes for parylene processing. All the processes proposed in the flowchart can be performed both at the EKL and PInS CL100 facility. They are also compatible with most MEMS cleanrooms, which potentially allows for the process transfer and scaling up. First, the adhesion at the interface between platinum and parylene is investigated to determine whether the selected fabrication methods allow for the fabrication of a film with flexible interconnects. Then, the surface cleaning methods were adopted, and the contamination prevention in two-sided wafer processing was endured. Next, the parylene etching methods were developed. Finally, a process for platinum deposition and patterning directly on parylene was developed.

6.2 ADHESION IN THE PARYLENE-PLATINUM-BASED INTERCONNECTS

Poor adhesion between the layers of an implantable device unavoidably leads to its failure. Especially for long-term implants, all the device layers must be adhering well to each other. This must be true in every configuration, regardless of the harshness of the working conditions. In the case of the devices with parylene-platinum based interconnects, the challenge is even greater since neither the fabrication process of such devices has been well established, nor has their long-term reliability been thoroughly tested.

In this study, the adhesion between the layers of the parylene-platinum based flexible interconnects, fabricated using selected cleanroom compatible processes and methods, are investigated. Several adhesion promoting treatments like surface priming, surface roughening, plasma treatment, or bulk annealing are tested. The adhesion in the stack is also evaluated after performing typical microfabrication process steps, such as wafer cleaning with acetone or baking on a hot plate performed during lithography.

6.2.1 Methods

Three test stacks are prepared to unambiguously evaluate the adhesion between the layers forming a parylene-platinum-parylene flexible film (Figure 6.1). Each stack represents one interface from those occurring in the complete flexible film. The three isolated stacks are platinum on parylene (stack A), parylene on platinum (stack B), and parylene on parylene (stack C).

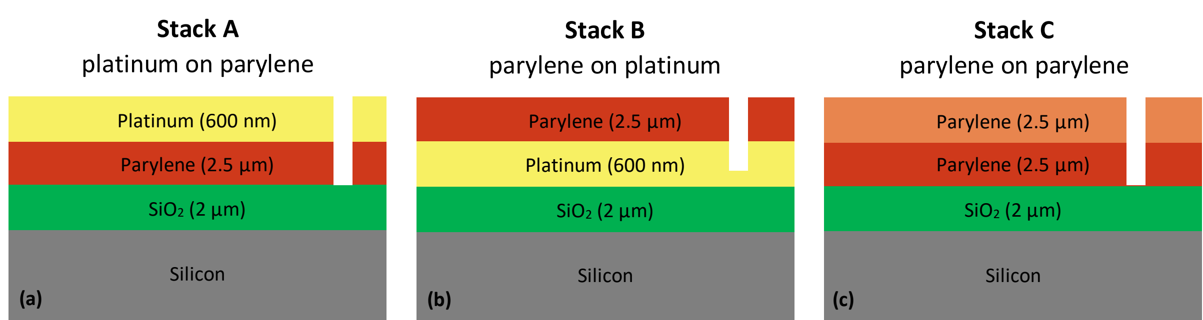

Figure 6.1: The three stacks prepared to evaluate the adhesion between the layers of the parylene-platinum-bases flexible interconnects.

Each test stack was deposited on substrates composed of 525 µm thick single-side-polished (SSP) silicon wafers provided with a 2 µm thick PECVD SiO_2 layer. The silicon dioxide ensures good adhesion of the first layer in the stack, whether it is parylene or platinum [3], so that the adhesion of the second deposited layer in the stack can be distinctively evaluated. The parylene is deposited in an SCS Labcoater® CVD deposition tool, and the platinum is sputter deposited in the cleanroom of Philips Innovation Services (PInS).

After depositing the three stacks, the adhesion between the metal-polymer or polymer-polymer interfaces was evaluated with an adopted thin-film cross-cut test. A cutting tool with a six-blade element (CC3000 tool by TQC) was used to cut a grid composed of twenty-five squares, with a surface of 1 mm^2, on every sample. The cuts were made according to the ASTM D3359 guidelines [4]. Next, certified adhesive tapes, with an adhesive force of 4.3 N/cm and 7.6 N/cm, are applied on the grid and peeled from the sample at 180 degrees. The adhesion is graded according to the ASTM Classification based on the number of entirely or partially peeled-off squares of the layer (Figure 6.2).

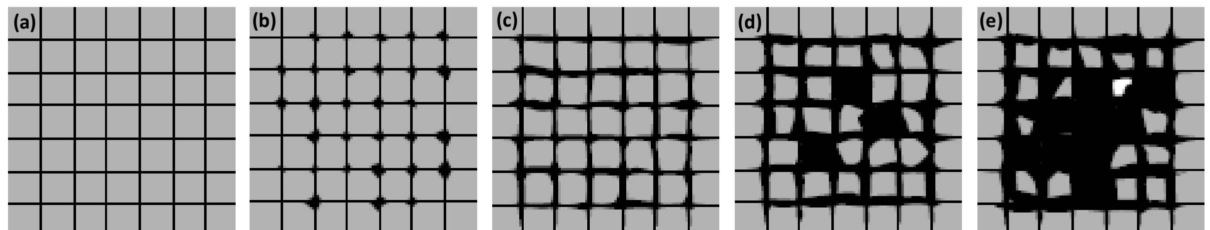

Figure 6.2: ASTM D3359 guidelines for evaluation of thin film layer adhesion. (a) Class 5B – 0% structures are affected. (b) Class 4B – <5% structures are affected. (c) Class 3B – 5-15% structures are affected. (d) Class 2B – 15-35% structures are affected. (e) Class 1B – 35-65% structures are affected. Source: ASTM D3359.

The process for the fabrication of parylene-platinum-based interconnects was developed for implantable devices. Therefore, the adhesion of the stacks was also tested after soaking the samples in PBS at 37°C for two days (body-like conditions) and at 55°C for ten days (accelerated aging test) according to the ASTMF1980-16 [5].

In each test, new cuts were made after the soaking. The adhesion between the tested layers was also evaluated before applying and peeling off the adhesive tapes. This is because, in some cases, the cutting itself already caused layer delamination.

6.2.2 Platinum on parylene (stack A)

Sample preparation

In platinum on parylene stack A, 2.5 µm of parylene is first deposited on substrates with 2.0 µm of PECVD SiO_2. An A-174 primer was applied in-situ to increase the adhesion between the parylene and substrate. Next, all samples are sputter etched in an argon plasma for 15 seconds at 25°C to clean and roughen the surface of the wafer and therefore improve the adhesion of the metallization [3]. Then, without breaking a vacuum, the metallization layer is deposited in two manners. First, 20 nm of a titanium adhesion layer, commonly used to improve platinum adhesion to ceramic layers such as SiO_2 [3][6], and 600 nm of platinum is deposited on samples A-1 and A-3. On sample A-2, only the 600 nm of platinum is deposited to investigate the influence of the titanium on the adhesion of platinum directly on parylene. After the metallization deposition, sample A-3 is additionally annealed at 200°C for 1 hour in an ambient, nitrogen atmosphere. This step can improve the adhesion between parylene and metallization [7]. The sample overview can be seen in Table 6.1.

Results and discussion

The platinum on parylene stack A test results are collected in Table 6.2 and Figure 6.3. In this stack, the cut went through all the layers: platinum, titanium, and parylene, down to the silicon dioxide. Minimal delamination of parylene from silicon dioxide was observed at the corners of the squares already after cutting through the layer. In theory, the adhesion of parylene to SiO_2 is very good [3][8]. However, it seems that the adhesion

Table 6.1: Process step and adhesion treatments performed on stack A samples (platinum on parylene).

Process step/Treatment	**Platinum on parylene**		
	A-1	**A-2**	**A-3**
PECVD SiO_2 (2.0 µm)	✓	✓	✓
Silane A-174	✓	✓	✓
Parylene deposition (2.5 µm)	✓	✓	✓
Sputter etch Argon for 15 seconds (vacuum)	✓	✓	✓
Titanium adhesive layer (20 nm)	✓		✓
Platinum sputtering (600 nm)	✓	✓	✓
Anneal (N_2/vacuum) 200°C for 1 hour			✓

Table 6.2: Layer adhesion quality in stack A evaluated according to the ASTM D3359 guidelines before and after tape test. Color indications: excellent; good; moderate; poor; bad; none.

Adhesion evaluation scheme tape peeling force	**Platinum on parylene**		
	A-1	**A-2**	**A-3**
Before soaking (after cutting)	4B	4B	4B
4.3 N/cm	4B	4B	4B
7.6 N/cm	4B	4B	4B
2 days in PBS at 37°C (after cutting)	4B	4B	4B
4.3 N/cm	4B	4B	4B
7.6 N/cm	4B	4B	4B
10 days in PBS at 55°C (after cutting)	4B	4B	4B
4.3 N/cm	4B	4B	4B
7.6 N/cm	4B	4B	3B

has been slightly worsened in this case. This might be due to the short argon sputter etching performed before the platinum deposition, which is known to impair the parylene to silicon dioxide adhesion (it was tested in a separate short loop). Since platinum did not show any detachment from parylene after the cutting, and the adhesion of parylene on silicon dioxide is good, it can be assumed that the initial platinum to parylene adhesion is at least on the same level, thus good.

In most samples, no platinum delamination was observed when applying the adhesive tapes with a peeling force of 4.3 N/cm or 7.6 N/cm neither before nor after PBS soaking for two days at 37°C or accelerated soaking in PBS solution for ten days at 55°C. The exception was sample A-3, annealed after platinum deposition at 200°C for one hour, which showed only moderate adhesion of platinum to parylene after accelerated aging and using the tape with a peeling force of 7.6 N/cm. Adhesion of platinum on parylene for all the other samples was qualified as good. No significant differences in adhesion were observed among the samples with or without the titanium adhesion layer.

The adhesion of platinum on parylene in stack A is good. It seems to be independent of the insertion of the titanium adhesion layer, which is necessary for good adhesion between platinum and silicon dioxide at the bond pads areas. The post-deposition annealing, which can improve the parylene-parylene adhesion in the final flowchart [7], slightly reduces the adhesion of platinum to parylene (sample A-3). The soaking tests have no (sample A-1 and A-2) or only a slight (sample A-3) effect on the initial adhesion in the stack, regardless of the applied treatments.

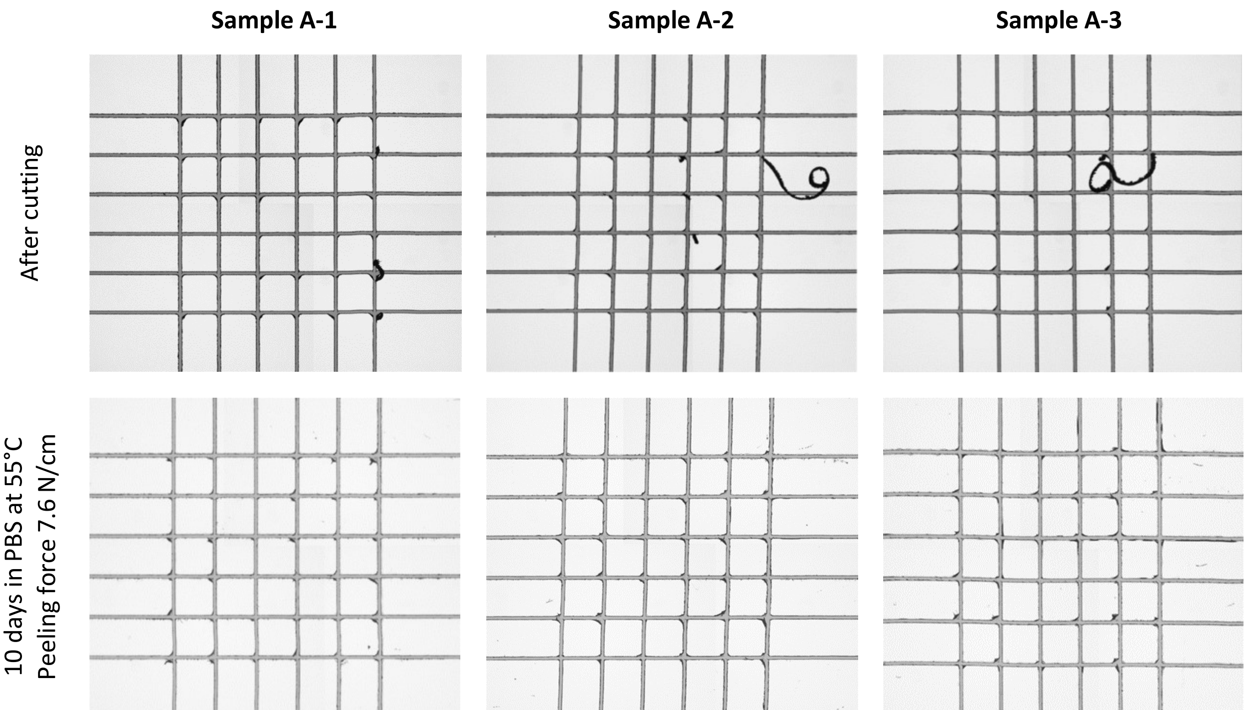

Figure 6.3: Cross-cut test results for samples from stack A before and after accelerated aging and peeling with a force of 7.6 N/cm.

6.2.3 Parylene on platinum (stack B)

Sample preparation

In parylene on platinum stack B, 20 nm of titanium (adhesion layer) and 600 nm of platinum are first deposited on the substrate with 2 µm SiO_2. As standard, the wafer was first cleaned with a 15 seconds argon plasma. Three out of five samples, samples B-2, B-3, and B-5, are then annealed at 200°C for 1 hour in a nitrogen atmosphere. On samples B-1 and B-2, 2.5 µm of parylene is deposited using the A-174 primer in situ. On sample B-3, parylene is deposited without applying any primer.

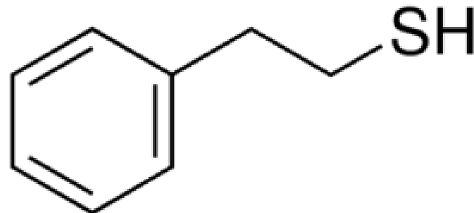

Figure 6.4: The chemical structure of the 2-phenylethanethiol.

In samples B-4 and B-5, the 2-phenylethanethiol (Figure 6.4) primer is used before parylene deposition on platinum. This primer is composed of the hydrophobic phenyl group (~C6H5) and a thiol group (~SH). The phenyl group has a high affinity to parylene, while the thiol tail provides bonding locations for platinum. A monolayer of 2-phenylethanethiol is applied on the waters from a 1-2% solution in isopropanol directly after surface activation with O_2 plasma for 10 seconds at 50 W. The excessive material is rinsed off using isopropanol, and the substrate is subsequently rinsed in water and dried. Finally, the top 2.5 µm of the parylene layer is deposited within one hour after the priming procedure. The sample overview can be seen in Table 6.3.

Table 6.3: Process step and adhesion treatments performed on stack B samples (parylene on platinum).

Process step/Treatment	Parylene on platinum				
	B-1	**B-2**	**B-3**	**B-4**	**B-5**
PECVD SiO_2 (2.0 µm)	✓	✓	✓	✓	✓
Sputter etch Argon for 15 seconds (vacuum)	✓	✓	✓	✓	✓
Titanium adhesive layer (20 nm)	✓	✓	✓	✓	✓
Platinum sputtering (600 nm)	✓	✓	✓	✓	✓
Anneal (N_2/vacuum) 200°C for 1 hour		✓	✓		✓
O_2 plasma treatment for 10 seconds at 50 W				✓	✓
SH:IPA solution (1:100) for 5 minutes				✓	✓
IPA for 5 minutes				✓	✓
DI for 5 minutes				✓	✓
Rinse and dry				✓	✓
Silane A-174	✓	✓			
Parylene deposition (2.5 µm)	✓	✓	✓	✓	✓

Table 6.4: Layer adhesion quality in stack B evaluated according to the ASTM D3359 guidelines before and after tape test. Color indications: excellent; good; moderate; poor; bad; none.

Adhesion evaluation scheme tape peeling force	Parylene on platinum				
	B-1	**B-2**	**B-3**	**B-4**	**B-5**
Before soaking (after cutting)	5B	5B	5B	5B	5B
4.3 N/cm	5B	5B	5B	5B	5B
7.6 N/cm	5B	5B	5B	5B	5B
2 days in PBS at 37°C (after cutting)	5B	5B	5B	5B	5B
4.3 N/cm	5B	5B	5B	5B	5B
7.6 N/cm	5B	5B	5B	3B	5B
10 days in PBS at 55°C (after cutting)	5B	5B	5B	5B	5B
4.3 N/cm	4B	2B	4B	0B	2B
7.6 N/cm	0B	0B	1B	0B	0B

Results and discussion

The parylene on platinum stack B test results are collected in Table 6.4 and Figure 6.5. In this stack, the cut went through the top layer of parylene and landed within the platinum film. The SiO_2 layer was not exposed. In this stack, significant differences between the samples were observed, especially after accelerated aging in PBS. Initially, the cutting lines on all the samples were very smooth, and the layer adhesion was excellent. The adhesion remained excellent also after cutting and applying the adhesive tapes after two days of soaking in PBS at 37°C. The exception was the not annealed sample treated with the SH primer (B-4). For this sample, parylene started delaminating from the platinum film when the tape with a peeling force of 7.6 N/cm was used on a sample soaked in PBS at 37°C, indicating only a moderate adhesion. After the accelerated aging at 55°C, the annealed sample with A-174 primer (B-2) and the samples where the primer with the ~SH group was used (B-4 and B-5) showed poor and no adhesion already when applying the tape with force 4.3 N/cm. The other samples (B-1 and B-3) failed only when stronger tape (7.6 N/cm) was applied. Except for sample B-3,

in which at the end of the test, parylene showed bad adhesion to the platinum, in all the other samples, parylene completely peeled from the parylene surface showing no adhesion at all.

The weakest adhesion in the parylene-platinum based interconnect is at the parylene on the platinum interface (stack B). The initial results right after deposition are excellent. However, the parylene encapsulation completely peels off from the platinum only after ten days of accelerated aging in PBS at 55°C. Samples that had slightly better results were those on which either an annealing or A-174 primer was applied. The 2-Phenylethanethiol primer scored lowest. This might be because the oxygen plasma cleaning (temporary) modified the platinum surface to hydrophilic [9], so the applied monolayer of SH primer did not attach properly to the surface.

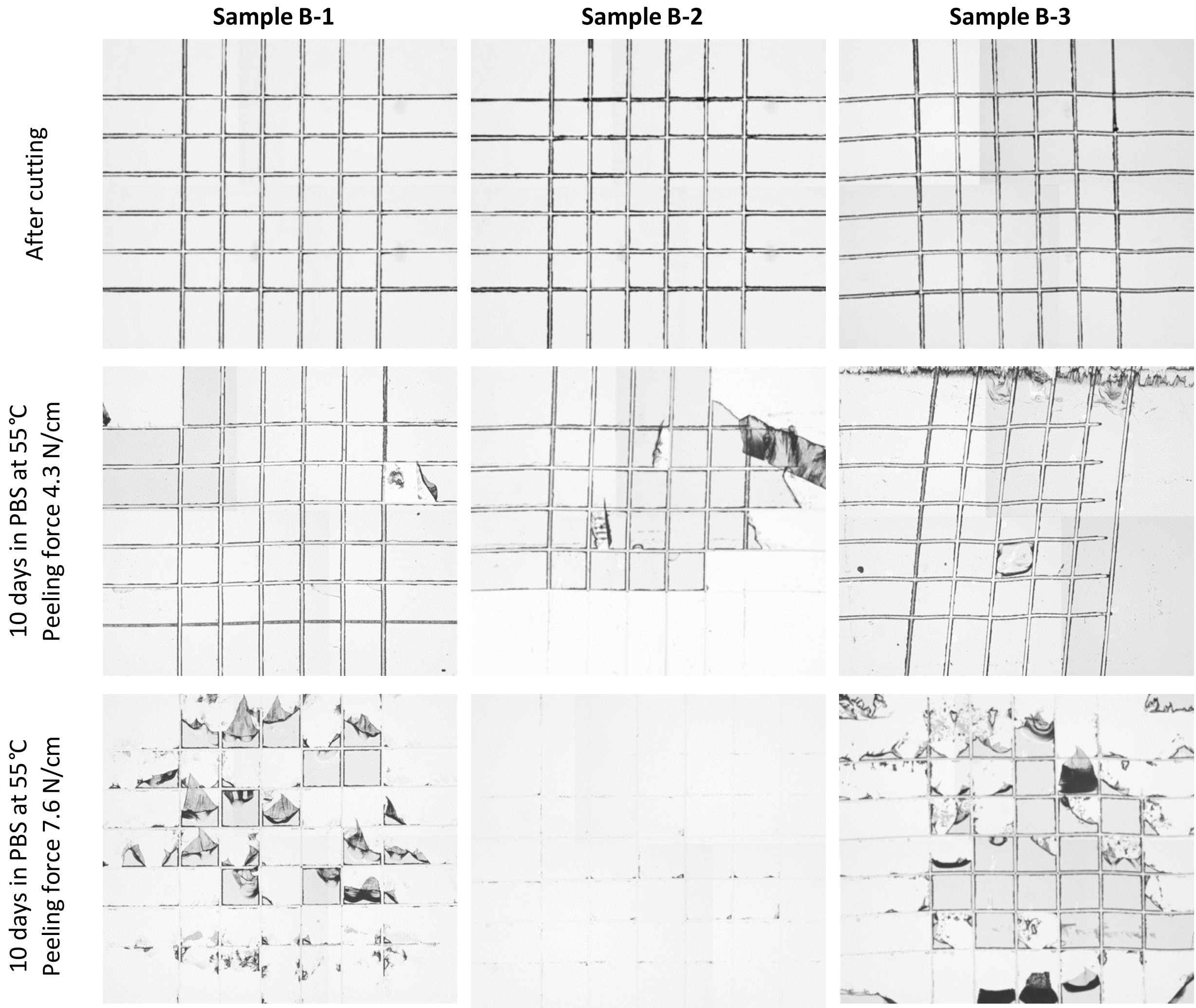

Figure 6.5: Cross-cut test results for samples from stack B before and after accelerated aging and peeling with a force of 4.3 N/cm and 7.6 N/cm.

6.2.4 Parylene on parylene (stack C)

Sample preparation

In parylene on parylene stack C, a layer of 2.5 µm thick parylene is first deposited on the substrate with 2.0 µm of PECVD SiO_2 using the A-174 primer. On samples C-3 and C-4, the second 2.5 µm layer of parylene is deposited directly after the first parylene deposition with the use of the A-174 primer for sample C4 and without the primer for

Table 6.5: Process step and adhesion treatments performed on stack C samples (parylene on parylene).

Process step/Treatment	Parylene on parylene			
	C-1	**C-2**	**C-3**	**C-4**
PECVD SiO_2 (2.0 µm)	✓	✓	✓	✓
Silane A-174	✓	✓	✓	✓
Parylene deposition (2.5 µm)	✓	✓	✓	✓
Parylene backside cleaning with acetone	✓	✓		
Sputter etch Argon for 15 seconds (vacuum)	✓	✓		
Acetone treatment + IPA	✓	✓		
Hotplate at 100°C for 2 minutes	✓	✓		
Silane A-174	✓			✓
Parylene deposition (2.5 µm)	✓	✓	✓	✓

Table 6.6: Layer adhesion quality in stack C evaluated according to the ASTM D3359 guidelines before and after tape test. Color indications: excellent; good; moderate; poor; bad; none.

Adhesion evaluation scheme tape peeling force	Parylene on parylene			
	C-1	**C-2**	**C-3**	**C-4**
Before soaking (after cutting)	≥3B	≥3B	≥4B	5B
4.3 N/cm	≥3B	≥3B	≥4B	5B
7.6 N/cm	≥3B	≥3B	≥4B	5B
2 days in PBS at 37°C (after cutting)	-	-	-	-
4.3 N/cm	-	-	-	-
7.6 N/cm	-	-	-	-
10 days in PBS at 55°C (after cutting)	≥3B	≥3B	≥4B	5B
4.3 N/cm	≥3B	≥3B	≥4B	5B
7.6 N/cm	≥3B	≥3B	≥4B	5B

sample C-3. Samples C-1 and C-2 are first pre-treated with an acetone spin clean of the backside, argon plasma for 15 seconds at 25°C, acetone and IPA batch, and a 2-minute baked on a hot plate at 100°C. These steps are introduced to mimic the platinum deposition and patterning steps that are omitted in this stack but will occur in the complete fabrication flowchart. After the pre-treatment, the second layer of 2.5 µm parylene is deposited with (sample C-1) and without (sample C-2) using the A-174 primer. The sample overview can be seen in Table 6.5.

In principle, for samples C-1 and C-4, applying the A-174 primer is not needed as the adhesion between the two layers of parylene should already be good [7]. However, it is crucial to investigate its influence on the parylene to parylene adhesion, as it might be necessary to use this primer in the fabrication flow to improve the adhesion of metallization to the silicon at the bond pad area.

Results and discussion

The parylene on parylene stack C test results are collected in Table 6.6 and Figure 6.6. In this stack, the cut was made through both layers of parylene, landing on the SiO_2. The samples were carefully investigated during the test to determine which layer of parylene is peeling and whether the treatments influenced either the oxide-parylene or the parylene-parylene interface. No significant delamination of the top parylene from the bottom parylene was observed. Therefore, the parylene to parylene adhesion is classified as at least as good as the adhesion of the bottom parylene to the silicon dioxide.

In the case of the adhesion between the bottom parylene and the silicon oxide film, a significant variation in the adhesion was observed between the samples that were subjected to the pre-treatment. Surprisingly, the initially determined adhesion was not affected by any of the aging tests, regardless of the force of the applied tape. The samples C-1 and C-2, subjected to steps mimicking platinum deposition and patterning, showed moderate adhesion due to layers peeling at the cutting line. The samples C-3 and C-4, without the pre-treatment, showed good and excellent adhesion, respectively.

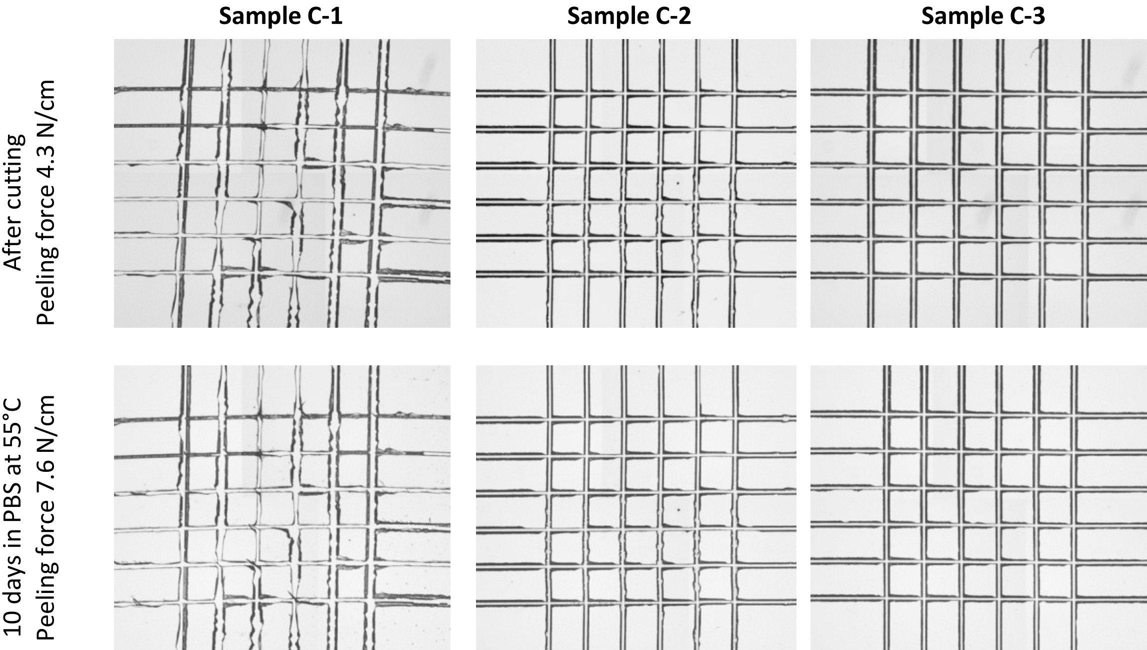

Figure 6.6: Cross-cut test results for samples from stack C after accelerated aging and peeling with a force of 4.3 N/cm and 7.6 N/cm.

It was impossible to directly assess the adhesion between the bottom parylene and the top parylene in stack C due to the delamination of the stack from the SiO_2 substrate. It can be assumed that it is at least as good as the adhesion of the stack to the substrate or better. Regarding the parylene stack to SiO_2 substrate adhesion, excellent and good adhesion can be achieved with and without silane A-174 primer (samples C-3 and C-4). Sample C-4, where the second parylene layer was deposited using the A-174 primer and without pre-treatment, showed the best adhesion. The adhesion of parylene to the SiO_2 remained unchanged after the soaking and peel tests.

The adhesion of the parylene stack to the substrate in samples C-1 and C-2 was moderate as it has been compromised by the steps introduced to mimic the platinum deposition and patterning process. In a follow-up experiment, it has been shown that the treatment affecting the interface is the 15 seconds of argon plasma sputtering [10]. This treatment is performed before the platinum deposition to pre-clean and micro-

roughen the surface of the substrate, which usually is a ceramic layer such as SiO_2 or Si_3N_4 [3][11]. Further research should be conducted to determine whether such treatment is necessary and could be either avoided or replaced by other cleaning techniques compatible with wafers containing parylene.

6.2.5 Conclusions

In this section, the adhesion between three interfaces, occurring in the parylene-platinum-based flexible film, has been tested using a cross-cut method adopted for thin-film testing. With this method, it was possible to evaluate the adhesion of the three interfaces and get qualitative results. Based on the results, it was determined which processing methods are suitable for the fabrication of parylene-platinum based implantable devices and which adhesion-enhancing treatments influence the bond between the occurring in the stack interfaces.

The results presented in this section show that it is possible to fabricate the individual interfaces with excellent and good adhesion directly after fabrication and after two days of soaking in PBS at 37°C. The adhesion of platinum to parylene (stack A) and parylene to parylene (stack C) remains unchanged even after ten days of soaking at an elevated temperature of 55°C. However, the soaking test at elevated temperature performed on stack B (parylene on platinum) caused complete delamination of the parylene from the platinum surface, regardless of the applied adhesion treatment. Furthermore, the adhesion of parylene to the substrate (SiO_2 layer) seems to be impaired by the steps introduced to mimic the platinum deposition.

In order to be able to fabricate a complete parylene-platinum based interconnect, the adhesion in stack B and stack C needs to be improved. First, the adhesion between the first parylene and the substrate (SiO_2) in stack C must be maintained throughout the platinum deposition and patterning process. This can theoretically be done by 48h long post-annealing of the complete device at 200°C [1]. It is also recommended to further research whether the argon plasma treatment is necessary to enhance adhesion of platinum to ceramic layers or if another cleaning method, such as O_2 plasma flash or RCA-2 solution, can be used instead.

Secondly, the long-term stability of the parylene encapsulation of platinum (stack B), the most challenging interface worldwide [1], has to be significantly improved. Treatments worth further testing are: an alternative method for more efficient surface cleaning; applying the still promising 2-Phenylethanethiol primer onto untreated with O_2 plasma and thus still hydrophobic platinum surface; introducing an additional adhesion layer to the interface such as SiO_2 or Si_3N_4 ceramic layers that are known to form a good bond with platinum and are often used to encapsulate platinum interconnects [11]. The latter method, involving introducing a ceramic layer to the parylene-platinum-based interconnect, is investigated in Chapter 8.

6.3 CLEANING WAFERS CONTAINING PARYLENE

Another important aspect of MEMS fabrication process is wafer cleaning. The most common contaminants are micro- and nano-sized particles, metals, and organic residues like photoresists remaining after the lithography process. When left on the surface of the wafer, these compounds are embedded in the next deposited layer, which might lead to a device failure in the short term (e.g., electrical short) or long term (e.g., delamination due to impaired adhesion). On top of that, in the case of implantable electronics, the impurities might affect the reliability of the device or even cause a foreign body reaction.

In standard MESM production, the majority of these contaminants are not a thread for regular processes. They can be cleaned using a high-power O_2 plasma, two-step nitric acid cleaning, or the RCA-1 and RCA-2 cleaning solutions [12][13]. However, in many cases, these treatments cannot be performed on wafers with parylene as they will affect the layer itself or the underlying layer. Therefore, in the following sections, several methods have been tested to clean the parylene surface safely.

6.3.1 Spin cleaning with organic solvents

Many particles acquired during wafer handling or placing on chucks can be mechanically removed from the surface of the wafer in a spin cleaning process that uses organic solvents such as acetone, isopropanol, or pure ethanol. All of the mentioned chemicals are "safe" to be used on the parylene surface when applied for a short time [14]. Furthermore, acetone is a common photoresist solvent that allows for cleaning the wafer from acquired photoresist residues or stripping the photoresist after photolithography [1].

6.3.2 Low-power O_2 plasma

Sometimes the photoresist residues are so persistent that the spin-cleaning is insufficient (Figure 6.7a). This is especially true when a metal hardmask, used for consequent etching of exposed parylene, is patterned using a dry, plasma-based etching method. In this case, it is hard, or even impossible, to completely remove the modified photoresist in acetone. To strip the remaining photoresist from the patterned layer of metal, a low-power (≤100 Watt) O_2 plasma flash can be used. After treatment, the organic residues from the wafer have been successfully removed (Figure 6.7b). The oxygen-based plasma can also etch parylene. However, during this specific process, the parylene layer is protected with the patterned hardmask. During the process, the temperature of the wafer was maintained below 100°C to prevent parylene decomposition and bubbling [15].

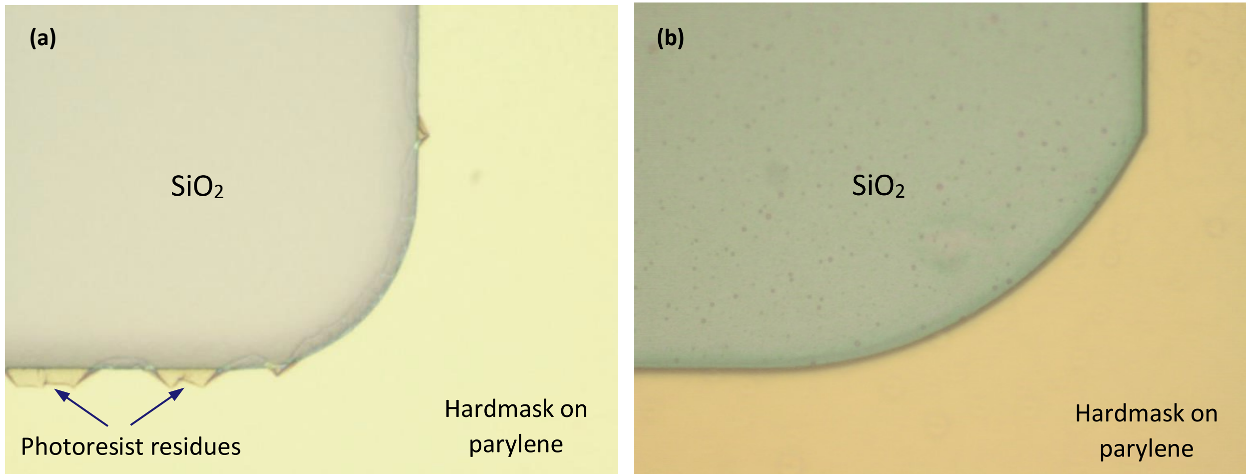

Figure 6.7: Parylene layer patterned using a hardmask. (a) Wafer after photoresist removal using acetone spin cleaning. Photoresist residues are clinging from the edge of the structure. (b) Wafer after additional O_2 plasma flash.

6.3.3 Metal cleaning

Clanging silicon wafers from metal residues is crucial, especially during the fabrication of active devices such as transistors and diodes. In those devices, metal impurities such as gold or copper that can diffuse through the silicone and be dissolved in the silicon matrix can lead to current leakage [16]. In the case of passive MEMS devices, metal

contamination on a molecular level is less severe because the silicon wafer is used only as a carrier. This is also the case for the DBS device fabrication process that is developed in this thesis. The specific metal cleaning steps will not be included in the DBS flowchart after the deposition of parylene because the available metal cleaning method at EKL is wafer submersion in a boiling 69% nitric acid at 110°C, which will melt the parylene. If a metal cleaning method proves to be necessary, hydrofluoric or hydrochloric acid in combination with hydrogen peroxide (also present in RCA-2 - a clean solution for metal contamination) could be used instead. All these substances are compatible with parylene. However, the effect of the RCA-2 cleaning solution on the parylene still has to be studied.

6.4 CONTAMINATION PREVENTION IN TWO-SIDE WAFER PROCESSING

In the previous section, several methods for cleaning the wafers containing parylene have been presented. However, parylene is a rather sensitive material regarding temperature resistance or resistance to acids and bases, and during long exposure it can be permeable to some chemicals such as hydrofluoric acid leading to damage of underlying layers [3]. Therefore, the available cleaning methods must be quite gentle, and most probably, they have limited effectiveness. This is quite problematic because even the finest contamination of any type can negatively influence the adhesion of the parylene-platinum-parylene interface and thus the stability of the medical device.

The contamination problem is even more severe when the wafer has to be processed from both sides, for example, during the silicon DRIE etch. A flipped wafer touches various surfaces like chucks and forks of the machines that might introduce mechanical damage and hard to remove surficial or embedded contamination of all types. In this case, even the standard MEMS cleaning methods do not guarantee contamination and defect-free surface.

The most successful method for maintaining the front side of the wafer clean during backside processing is contamination prevention. This can be done by preventing contact with the machine elements by, for example, using a protective layer that is removed after the backside processing is finished, or designing the fabrication process so that the potential contaminants are not affecting the device.

In this section, the riskiest backside processing steps in the Chip-in-Tip DBS flowchart presented in Chapter 2 have been identified and investigated. Further, possible contamination prevention methods have been selected.

6.4.1 Two-side wafer processing in tools

According to the flowchart presented in Chapter 2, the wafer is processed on its backside twice during the fabrication process. First, when the PECVD SiO_2 mask for backside release in DRIE is deposited and patterned, and secondly, when the silicon is etched in the DRIE process. During the silicon etch step, the front side of the wafer is protected with a hardmask that is already deposited on the front side of the wafer. The possible contamination is removed together with the hardmask after the parylene etching. However, during the two-side PECVD SiO_2 deposition, the bare wafer is not protected neither on front nor on the back side.

In a series of short-loop experiments, it has been found that after the 2 µm SiO_2 PECVD deposition on the front side of the wafer, its back side had many scratches and particles at the location of contact with the handling arm of the tool (Figure 6.8).

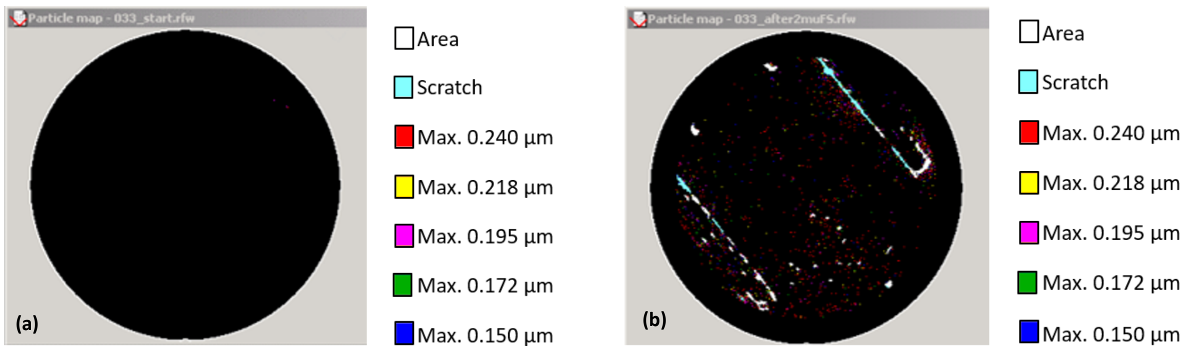

Figure 6.8: Results of particle count on the backside of the wafer (a) before and (b) after the PECVD SiO_2 deposition on the front side of the wafer.

It was not possible to remove the participles or prevent the scratches regardless of using extensive cleaning methods such as oxygen plasma followed by two-step HNO_3 cleaning, or etching native silicon dioxide in a mild HF solution of 0.55% followed by Marangoni drying process [17]. Also, depositing a 200 nm thin film of LPCVD thermal dioxide as a sacrificial layer, removed after the PECVD deposition, was not effective. The particles were persisting on the back side of the wafer leading to micromasking during the backside silicon etch in the DRIE process (Figure 6.9).

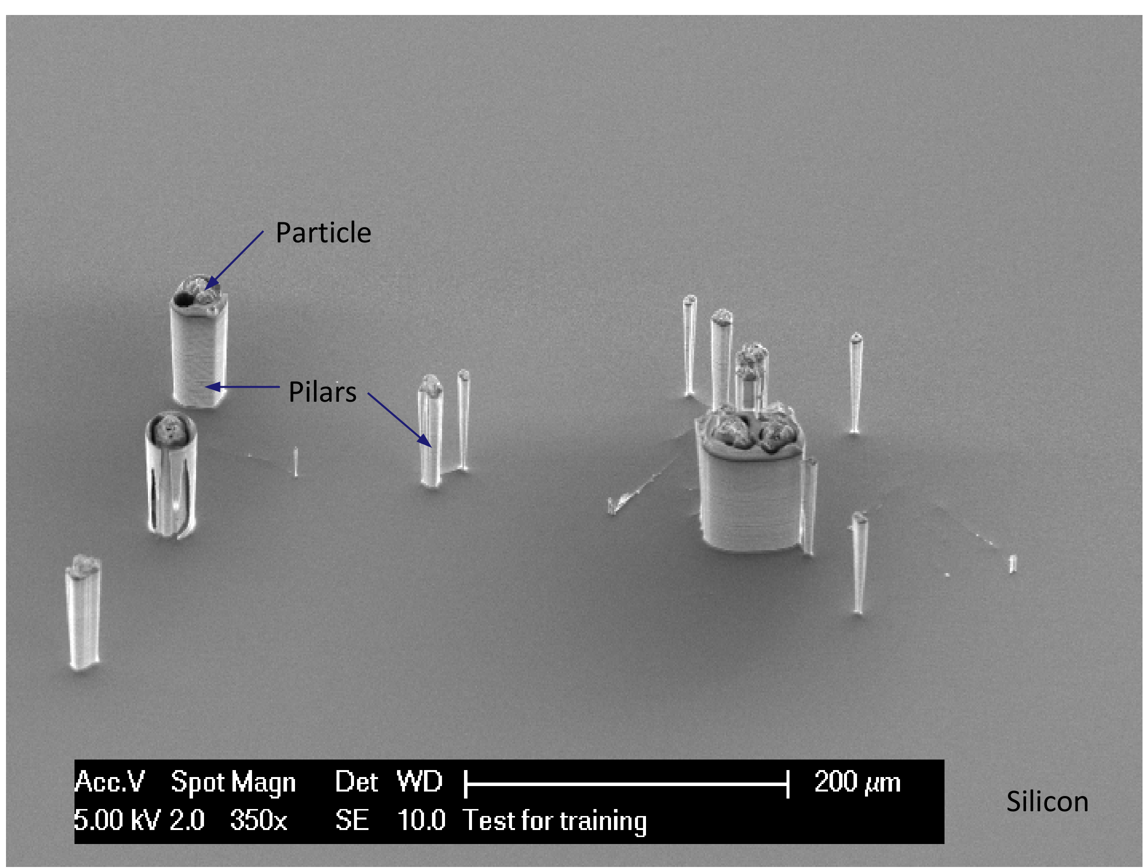

Figure 6.9: Pillars forming on the surface of a silicon substrate due to micromasking during the DRIE etching of the first 80 µm of silicon from the backside of the wafer.

This problem has to be tackled as the released device with remaining pillars loses its flexibility, it can be damaged during folding by the needle-like residues, and most importantly, the pillars can easily break or detach from the device. Since neither wafer cleaning nor application of sacrificial layer allowed to prevent contamination of the backside of the wafer, another approach allowing for “moving” the problem to the front

side of the wafer rather than solving it has been investigated. By reversing the order of processing steps, the backside of the wafer is maintained clean, preventing micromasking during the final backside silicon etch in the DRIE process. This has been done by depositing the 6 µm PECVD SiO_2 on the backside of the wafer first and only then performing the front side processing, including the alignment marker patterning and 2 µm PECVD SiO_2 layer deposition.

Unfortunately, in this method, the front side of the wafer most probably contains some permanent contamination. In the flexible interconnect area, this contamination is removed together with the silicon during the backside DRIE etch, followed by the wet etch removal of the 2 µm SiO_2 etch stop layer. However, the particles and possible defects present in the rigid regions of the device remain encapsulated with the 2.0 µm thick silicon dioxide layer. The possibilities of maintaining both sides of the wafer clean should be further investigated. This should be done in combination with identifying the contaminants and implementing an efficient wafer cleaning method.

6.4.2 Two-side wafer inspection and measurements

Another source of contamination and, most importantly, mechanical damages are chucks, especially those of measurement and inspection tools where the wafer is manually placed, or onto which the wafer is mechanically (vacuum) clamped. On top of that, the wafers have a parylene layer on the front side. This polymer is prone to mechanical damage and scratching, but it is also difficult to clean using standard wafer cleaning methods available at EKL. Therefore, to protect the wafer's front side from damages, it is essential to prevent or limit its direct contact with chucks during processing and inspections. Where applicable, a dedicated edge chuck can be used, for instance, during lithography steps or spin cleaning. In situations when the wafer has to be manually placed face down on a chuck, a specially prepared spacer (e.g., thin aluminum ring) can be used to prevent the direct contact of the wafer with the chuck.

6.5 PARYLENE ETCHING AND PATTERNING

Parylene is deposited in a CVD process where a conformal layer of material is coating all the exposed surfaces – both sides of the wafer. Parylene is a chemically inert material resistant to common organic solvents such as acetone or isopropanol, and it can only be "wet etched" or rather attacked by strong oxidizing agents such as aqua regia. This solution, however, also etches other thin-film materials, especially metals, including platinum. To etch parylene selectively, dry etching methods have to be used, such as oxygen plasma that etches parylene isotropically or O_2-based reactive ion etching that allows for anisotropic etching of parylene [1]. During the etching, the temperature has to be maintained below 100°C to prevent parylene oxidation. Furthermore, the layer must be well adhering to the clean substrate to prevent the formation of bubbles in or under the parylene layer due to the rapidly escaping gases in an elevated temperature or low-pressure conditions.

In this section, an oxygen-based RIE process for parylene etching is developed in the EKL facility using the ICP Trikon Omega 201 and the Alcatel GIR 300 tools. In parallel, a photoresist and two metals: aluminum and titanium, all of which are compatible with the lab policy, have been investigated as a masking material for the parylene etching. All the selected masking materials can be selectively removed from parylene in a wet etch. Next, the effect of the addition of CF_4 to the oxygen plasma on the slope of the parylene structure was investigated. Finally, methods for parylene one-side deposition and wafers backside cleaning are explored.

6.5.1 Parylene patterning using a photoresist mask

In order to fabricate functional devices with parylene-encapsulated metal tracks, it is crucial to be able to etch the parylene layer in a controlled way using microfabrication cleanroom processes. This means that using the selected patterning method and masking material, the structure with clearly defined dimensions, like line width and etching slope angle, can be achieved in a reproducible and preferably scalable way.

An O_2 based RIE plasma recipe was used to etch parylene anisotropically at the bond pad openings. Then the influence of CF_4 on the parylene etch rate and the slope profile was investigated. Through these experiments, a thick AZ9260 photoresist mask was used. This photoresist does not react with parylene, and it can be removed from it using photoresist solvents.

Straight feature slope etched in O_2 plasma

A non-directional O_2 plasma etches parylene isotopically. A directional plasma with additional RF bias can be used to achieve a pseudo anisotropic effect. The recipe for parylene etching was optimized on two tools: ICP-Trikon Omega 201 etcher and Alcatel GIR 300 etcher. The optimized recipe parameters are collected in Table 6.7.

Table 6.7: Parameters and properties of optimized recipes for anisotropic parylene etching using O_2 plasma in Trikon Omega 201 and Alcatel GIR 300 RIE tools.

Recipe parameters	Trikon Omega 201	Alcatel GIR 300
O_2 gas flow	80 sccm	70 sccm
RF etch power	50 W	60 W
RF bias power	500 W	-
Bias voltage	-	2·200 V
Chuck temperature	20°C (active)	25°C (passive)
Pressure	50 mTorr	50 mTorr
Recipe properties	**Trikon Omega 201**	**Alcatel GIR 300**
Etch rate (wafer edge)	240 nm/min	220 nm/min
Etch rate (wafer middle)	350 nm/min	260 nm/min
Etch rate (10% open area)	650 nm/min	220 nm/min

A set of test wafers with a photoresist was prepared to develop a safe recipe to pattern and etch parylene in O_2 plasma. The 400 µm thick double side polished wafers, with 2 µm thick silicon dioxide and 2.5 µm thick parylene on the front side, were prepared (Figure 6.10a). Lithography was performed using a 6 µm thick high-resolution AZ9260 photoresist. To avoid parylene crystallization, all lithography steps were performed at a maximum of 100°C. The standard application of hexamethyldisilazane (HMDS) adhesion layer, usually performed at 115°C to enhance adhesion of photoresist to silicon [18], was omitted and replaced with a 2-minute long bake at 95°C to degas the wafer. To prevent the thick photoresist bubbling after spin-coating, a 5 minutes and 30 seconds long bake at 95°C was performed, which should allow for all the solvent to gently evaporate from the photoresist. The wafers were etched using the optimized recipes to pattern the 2.5 µm thick parylene layer. After the etching, the photoresist mask was stripped with acetone spin clean, and the wafers were inspected under an optical microscope (Figure 6.10b) and in SEM with 45-degree tilt (Figure 6.11).

The parylene was etched in O_2-based plasma without residues (Figure 6.10b). No photoresist residues were observed after the acetone spin cleaning process. In Figure 6.11, the results of the SEM inspection can be seen. The etching of the parylene layer was in fact anisotropic and resulted in a straight wall profile.

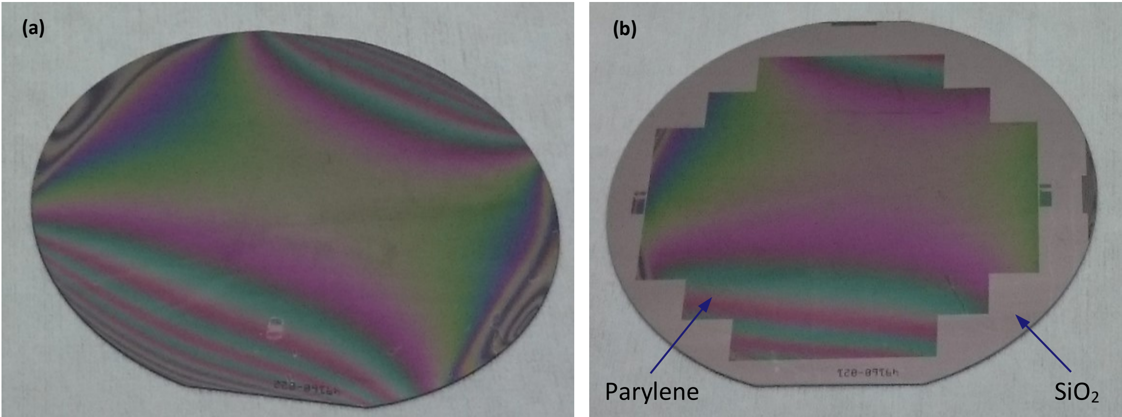

Figure 6.10: Silicon wafer with parylene layer. (a) Parylene layer before etching. (b) Parylene layer patterned in Trikon Omega 201. The photoresist mask was removed.

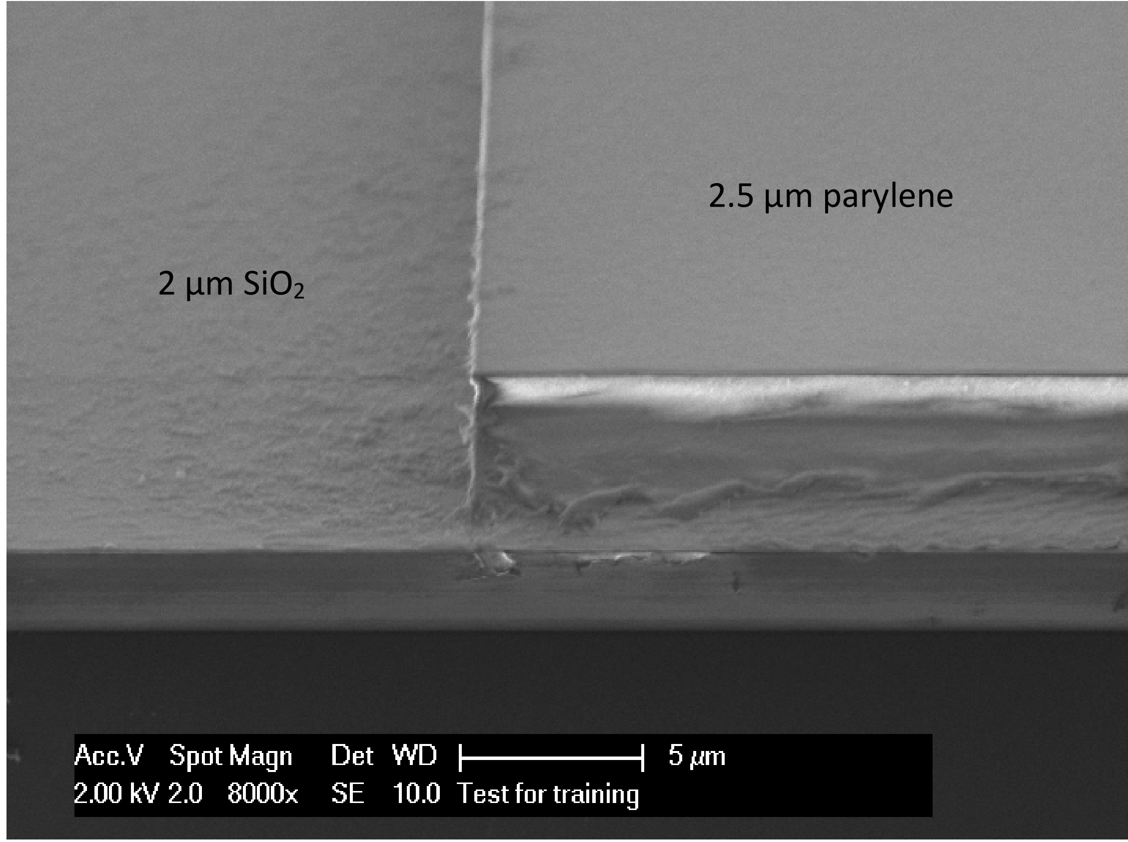

Figure 6.11: SEM image of parylene layer patterned in O_2 plasma. The photoresist mask was removed.

Positive feature slope etched in O_2/CF_4 plasma

A sufficient positive feature slope is desired to ensure a good step coverage of the platinum metallization on top of the patterned parylene layer. This, in theory, can be done by adding a fraction of CF_4 into the pure O_2 plasma. Introducing the CF_4 causes a semi-isotropic etch effect when etching parylene in directional plasma tools [19]. The influence of CF_4 addition to the directional O_2 plasma on the parylene etch rate and etch profile will be investigated in this section.

The 500 µm thick wafers were prepared with 100 nm SiO_2 layer, serving as an etch stop layer and structural layer, and 2.5 µm parylene layer. Lithography was performed using the process developed earlier for the 6 µm thick AZ9260 photoresist. The wafers were etched in Trikon Omega 201 RIE tool using three recipes with varied O_2 and CF_4 gas flow ratios (see Table 6.8). After etching, the photoresist mask was stripped with acetone spin clean, and the cross-section of the wafers was checked in SEM. The etch rate and the profile of the structures were inspected.

Table 6.8: Parameters and properties of optimized recipes for parylene etching using O_2/CF_4 plasma in Trikon Omega 201 tool.

Recipe parameters	**#Par1**	**#Par2**	**#Par3**
O_2 gas flow	80 sccm	75 sccm	70 sccm
CF_4 gas flow	0 sccm	5 sccm	10 sccm
RF etch power	50 W	50 W	50 W
RF bias power	500 W	500 W	500 W
Chuck temperature	20°C (active)	20°C (active)	20°C (active)
Pressure	50 mTorr	50 mTorr	50 mTorr
Recipe properties	**#Par1**	**#Par2**	**#Par3**
Parylene etch rate (average)	187 nm/min	965 nm/min	746 nm/min
Parylene sidewall angle	90 degree	45 degree	55 degree
Silicon dioxide etch rate (est.)	0 nm/min	25 nm/min	66 nm/min

For all three recipes, parylene was etched completely, and no photoresist residues were observed neither on the edge of the parylene structures nor on the surface of the etch stop layer (SiO_2). The etch rates of parylene when using recipes #Par1, #Par2, and #Par3 were 187 nm/min, 965 nm/min, and 746 nm/min, and the slope angles were 90 degrees, 45 degrees, and 55, respectively. The measurement results are collected in Table 6.8. The slopes in the parylene structures etched using recipes #Par2, and #Par3 can be seen in Figure 6.12.

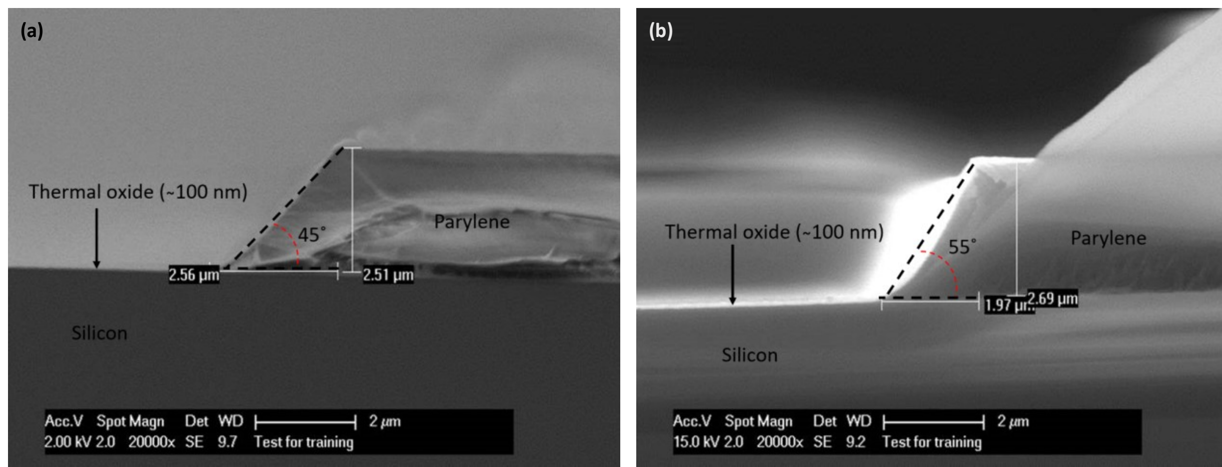

Figure 6.12: SEM images of the parylene structures with positive slope etched RIE process using O_2/CF_4 plasma. (a) Sample etched using recipe #Par2 with 75 sccm O_2 and 5 sccm CF_4. Slope angle 45 degrees. (b) Sample etched using recipe #Par3 with 70 sccm O_2 and 10 sccm CF_4. Slope angle 55 degrees. The isotropic etching arc is visible.

Next, the recipes selectivity to the photoresist mask and the silicon dioxide etch stop layer was checked. As expected, the photoresist etch rate compared to the parylene etch rate was approximately 1:1 for all the recipes, whether they had the addition of CF_4 in

the plasma or not. The selectivity towards silicon dioxide has decreased with increasing the CF_4 content. The O_2-based plasma did not affect the SiO_2 layer at all, while the etch stop layer consumption was observed after adding CF_4 (Table 6.8). The estimated SiO_2 etch rate was approximately 25 nm/min for the #Par2 recipe and 66 nm/min for the #Par3 recipe.

During the optical inspection of the structures, etched using recipes containing the addition of CF_4, it was observed that parylene was consumed from the sidewall of the structures both at its top and at its bottom. For example, in wafer etched using #Par3 recipe with 70 sccm O_2 and 10 sccm CF_4, the width of the top surface of parylene is 82.7 µm, and the width at the bottom of the parylene structure is 85.8 µm (Figure 6.13). Since the original width of the photoresist mask is 90 µm, a parylene loss of 4.2 µm to 7.3 µm has occurred while etching a 2.5 µm thick parylene layer. The horizontal etch has to be taken into account when designing a photolithographic mask for the fabrication process. Moreover, the lateral consumption of the material will increase with the etch duration, which has to be taken into account, for example, when increasing the thickness of the parylene layer.

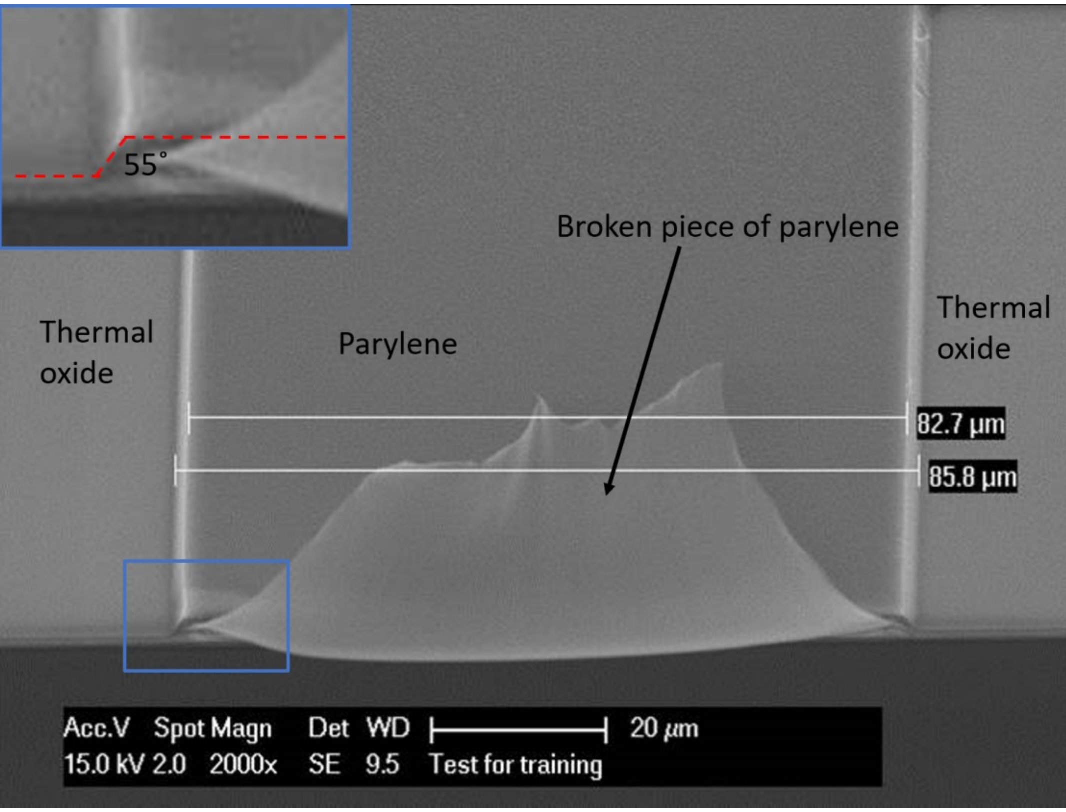

Figure 6.13: SEM image of the parylene layer etched using #Par3 recipe with 70 sccm O_2 and 10 sccm CF_4. Parylene was consumed from the sidewalls of the structures during the slightly isotropic etch.

Discussion

The addition of CF_4 to O_2 plasma allows for achieving a higher etch rate of parylene in the RIE process (Figure 6.14a). The samples etched with plasma, where the gas flow ratio of O_2 to CF_4 was 5:75 sccm/min, were etched faster than the samples etched with plasma where the gas flow ratio was 0:80 sccm/min or 10:70 sccm/min. Such unusual etch rate change has been reported in the literature for benzene-based polymers (e.g., parylene, BCB) etched in O_2 plasma with CF_4 addition (see Figure 6.14b) [19][20]. In the studies, the initial increase of etch rate is linked to the presence of fluorine in plasma that is more reactive than oxygen and reacts faster with the hydrogen in the benzene

groups building parylene structures[2]. The carbon in the open benzene rings is then oxidized with the oxygen to carbon-oxides [20]. The drop of the etch rate, occurring after the threshold of the CF_4 concentration has been reached, is linked to the dropping concentration of the O_2, which is directly involved in the parylene etching process [19].

Change of parylene etch rate with increasing CF_4 fraction in O_2 plasma

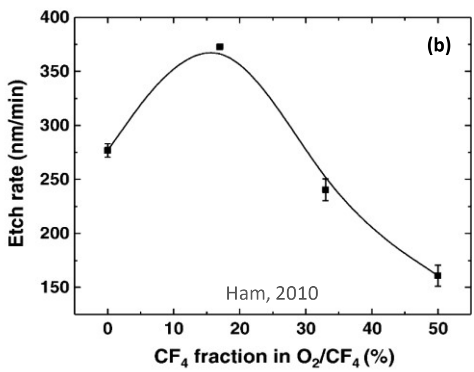

Figure 6.14: The change in parylene etch rate related to the addition of CF_4 to the O_2 plasma in the RIE process. (a) Experimental data. (b) Data collected by Ham, 2010 [19].

The anisotropic etching pattern of parylene observed for the directional O_2 plasma has been modified by adding the CF_4 resulting in a semi-isotropic etching pattern. In addition to vertical etching, a slight etching in the latera direction was noted. In literature, this has been linked to the accelerated opening of the benzene rings in parylene due to the presence of fluorine in the plasma. The exposed benzene rings, open by fluorine bonding with hydrogen, can be easier accessed by oxygen and etched faster also in the horizontal direction [19].

With an increase of the CF_4 addition, an increase of the positive slope angle has been observed. In Liao 2006, the slope change was linked to the changes of plasma parameters [20]. However, besides the gas composition and concentration, all the plasma settings remained unchanged in this experiment. In the case of a silicon substrate, it is possible to etch tapered structures using a modified Bosch process by consecutively switching between anisotropic and isotropic etching during one etching session [21]. The isotropic etching in the Bosch process is achieved by depositing the passivation layer on the structure and removing it only on the bottom of the structure during a breakthrough step that is performed right before the etching step. When investigating the CF_4 influence on benzene-based polymer etching in directional plasma, Liao et al. suggested that the fluorocarbon polymer layer can be formed on the sidewalls of the etched structure, forming a diffusion barrier [20]. The formed fluorocarbon polymers might act as a passivation layer, imitating the modified Bosch process.

The proposed mechanism of tapered parylene structures formation in the RIE process using CF_4 and O_2 gases assumes occurrence of the following steps in a loop:

- Anisotropic etch of parylene achieved by the addition of CF_4 to the O_2 plasma,
- Deposition of fluorocarbon polymer film on the bottom and walls of structures,
- Fast removal of the fluorocarbon polymer from the bottom of the structure and subsequent vertical parylene etch,
- Simultaneous but slower removal of the fluorocarbon polymer from the sidewalls of the structure and subsequent horizontal parylene etch.

[2] Pauling electronegativity of fluorine: 3.98, and of oxygen: 3.44 [31][32].

Conclusions

It was possible to perform lithography and etch parylene in the oxygen plasma RIE process using a photoresist mask without causing parylene deformation of photoresist bubbling. Afterward, the AZ9260 photoresist was cleanly removed from the parylene surface without residues by using only acetone spin clean.

A straight parylene structure slope has been achieved when using an O_2-based RIE anisotropic process. By adding CF_4, it was possible to achieve a semi-isotropic etching effect resulting in a slope of 45 degrees. Such a slope is desirable as it will ensure better step coverage of the bond pads with subsequently deposited platinum metallization.

The addition of CF_4 to the O_2 plasma contributed to an almost five times higher parylene etch rate. This is due to the presence of fluorine in the plasma that allows for accelerating the process of opening and etching of the benzene rings that form the parylene layer. On the other hand, introduced CF_4 can react with and etch underneath material such as silicon dioxide that in this flow is part of the design and should be intact after the process of parylene etching. To protect the SiO_2 layer, a soft landing on the SiO_2 using only O_2-containing plasma can be performed at the end of bulk parylene etching with CF_4/O_2 based plasma.

Finally, parylene etching using the RIE process is semi-isotropic, which means that parylene is also etched vertically, causing an under etch beneath the photoresist mask. As a result, the feature patterned in the parylene is larger (wider) than the mask. This should be taken into account during the design phase and reticle preparation.

6.5.2 Parylene patterning using metal hardmask

In the previous section, it was shown that parylene could be patterned using a photoresist mask. However, due to almost zero selectivity, this can be problematic when etching a thick layer of parylene, which is the case for the process proposed in this chapter, where more than 10 µm of parylene is etched in one step. Moreover, according to the proposed fabrication sequence, the photoresist mask for etching of the dual-parylene layer is deposited and pre-patterned before the device is released in the DRIE etcher. During the release, the device is in direct contact with the chuck of the etcher, which can cause mechanical damage to the soft photoresist mask. Also, there is a risk of the photoresist sticking to the chuck and contaminating it. Hardening of the photoresist by extensive baking is limited to 100°C because of the underlying parylene layer. Moreover, the extensively baked photoresist might be hard to remove later using an acetone spin clean. Finally, the thick photoresist layer might obstruct the heat transfer between the chuck of the etcher and the wafer and damage the temperature-sensitive parylene film during etching.

In this section, the use of a metallic hardmask for the final patterning of the parylene layer will be investigated. The metal mask must be selectively removed from a wafer with already released flexible devices by wet etching. The etching method and the etchant itself should not react or damage any of the materials present in the device (silicon, silicon dioxide, platinum, parylene). Two metals were selected: aluminum and titanium. These metals have already been used as hardmask for the etching polymers in a cleanroom environment [1][3][22], and both are available at the EKL research facility where the experiments are conducted.

Aluminum hardmask

First, aluminum has been investigated as an alternative masking material for parylene etching. Similarly, to all other processes performed on wafers containing parylene, their temperature budget has to be maintained below 100°C. This applies to both the aluminum layer deposition on parylene and subsequent lithography of the aluminum hardmask. For example, the parylene layer needs to be clean and dry to prevent micro bubble formation during the low-pressure aluminum sputter deposition process. Before the aluminum layer deposition, it is essential to properly clean degas the parylene surface and bulk to prevent the micro-bubble formation in the parylene layer (Figure 6.15a). This means that the parylene surface needs to be free from possible particles and that the layer volume should not contain trapped gas or liquid compound such as moisture. Exceeding this temperature limit during lithography leads to the parylene layer damage occurring underneath the aluminum layer (Figure 6.15b).

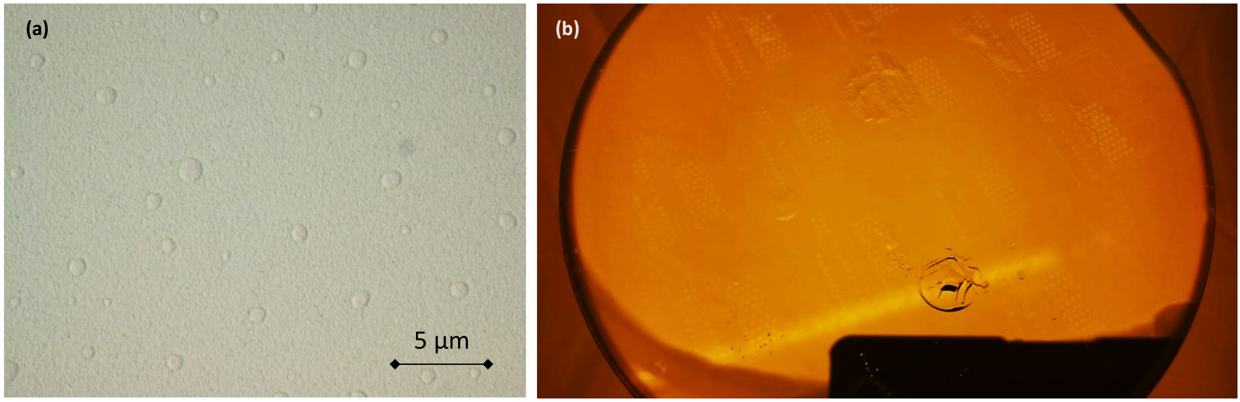

Figure 6.15: Defects in the parylene layer occurred during the hardmask deposition and lithography process. (a) Micron-sized bubbles trapped underneath the parylene and aluminum layer after the metal sputter deposition was performed without prior parylene degassing process. (b) Parylene layer damage underneath the aluminum and photoresist layer occurred after the lithography step performed at 115°C.

For this experiment, wafers with 2 µm of SiO_2 structural layer and 4.5 µm of parylene were prepared. Next, the wafer was spin-cleaned with acetone and dried on a hot plate at 100°C for 2 minutes. This step is to prevent bubble formation, during the low-pressure process of aluminum sputter deposition, due to moisture and acetone that can be trapped in the parylene layer. Now, 250 nm of aluminum was gently deposited at low power of 1 kW and at low temperature of 25°C to ensure that the metal will not imbed into the polymer [1]. The selected thickness is sufficient to prevent pinholes, and at the same time, does not induce much stress into the layer. To pattern the aluminum hardmask, a 1.4 µm thick SPR3012 positive photoresist was used. The lithography process was optimized in such a way that the temperature was kept below 100°C to prevent bubbles formation in parylene. Next, the aluminum hardmask has been patterned using chlorine and bromine chemistry in a Trikon Omega RIE plasma etcher. After patterning the aluminum hardmask, the photoresist mask was stripped with an acetone spin clean followed by a short O_2 plasma flash. Next, the parylene was dry-etched for 8 minutes 30 seconds in O_2 plasma in Trikon Omega RIE etcher with a power set to 50 W (recipe details can be found in Table 6.7). Then the aluminum hardmask was removed in PES at room temperature.

The developed processes for aluminum hardmask sputter deposition on parylene, and the subsequent lithography, mask patterning in chlorine-bromine-based plasma, and final removal of the photoresist mask were successful. No parylene damage or bubbling has been observed. Furthermore, parylene has been successfully etched in the O_2

plasma RIE process using an aluminum hardmask resulting in well-defined structures with almost straight slope. The aluminum mask was completely removed from the surface of parylene without residues. The etched structure after removing of aluminum hardmask in PES can be seen in Figure 6.16.

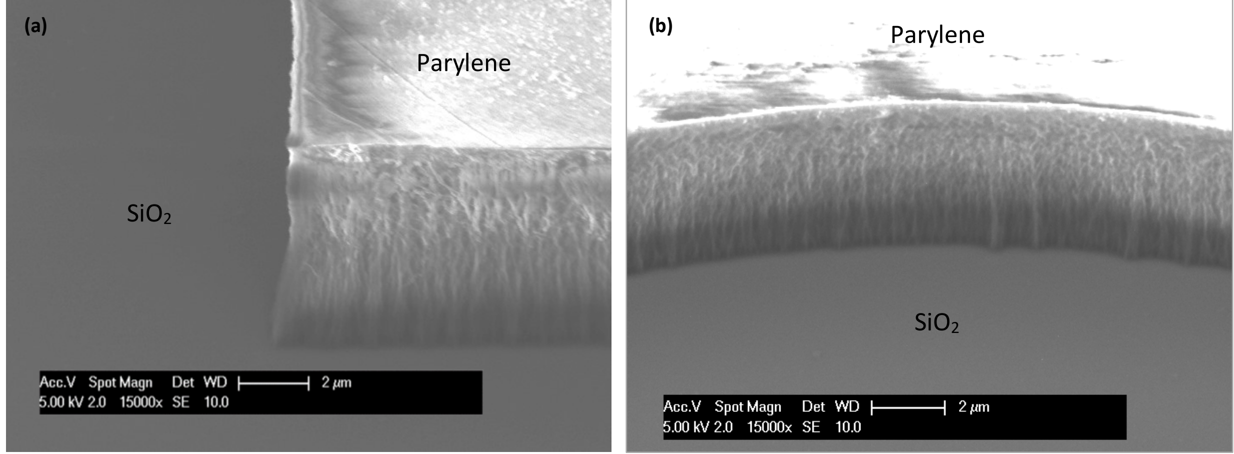

Figure 6.16: Results of parylene etching with O_2 plasma in Trikon Omega RIE using aluminum hardmask. Visible charging of the parylene top surface and characteristic fiber-like wall of the structures. (a) Metal line. (b) Electrode.

Titanium hardmask and titanium buried mask

Next, the use of titanium as a hardmask (fabrication flow in Chapter 7) and as a buried hardmask (fabrication flow in Chapter 8) for parylene etching was investigated. In the case of a buried hardmask, the patterned titanium is sandwiched in between two parylene layers. In a single etch process, it serves as an etch stop layer during removing of the top parylene layer and as a hardmask for patterning the bottom parylene layer. In this process, the use of titanium as a mask is essential because of its selectivity towards the PES aluminum etch, to which the patterned hardmask will be exposed at a certain point in the fabrication sequence (see flowchart in Figure 8.3). For this experiment, a short loop fabrication process was defined (Figure 6.17).

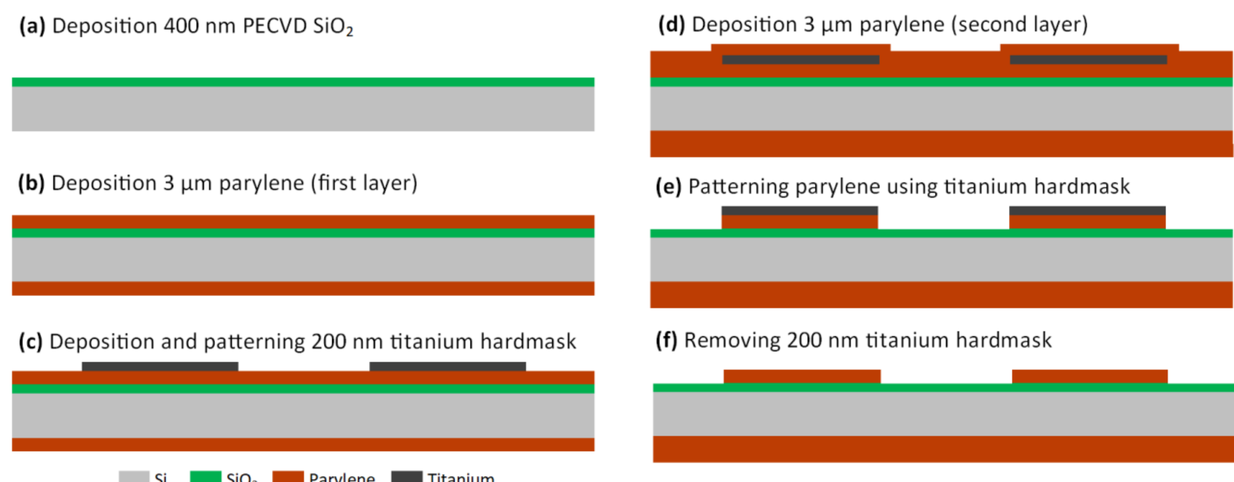

Figure 6.17: Short loop process for investigating the use of titanium (buried) hardmask for parylene etching.

A set of 500 µm thick singe side polished wafers were prepared with 400 nm of PECVD SiO_2 (Figure 6.17a) and 3 µm of parylene (Figure 6.17b). Then 200 nm of titanium is sputter deposited at a low temperature of 25°C and 6kW. Subsequently, lithography and titanium hardmask pattering is performed using a 3.1 µm thick AZ3027 photoresist

mask (Figure 6.17c). Next, the second 3 µm thick parylene layer is deposited on top of the patterned titanium hardmask (Figure 6.17d). Subsequently, the wafers are etched in Trikon Omega RIE etcher using O_2/CF_4-based recipe #Par2 (see Table 6.8). In that step, the second layer of parylene is removed from the wafer. Simultaneously, the first layer of parylene is patterned using the re-exposed buried titanium hardmask (Figure 6.17e). Finally, the hardmask is removed by wet etching (Figure 6.17f).

In this section, three investigated methods of titanium mask patterning (Figure 6.17c) are summarized: wet etching in 0.5% HF solution, wet etching in an ammonia-peroxide-based etchant, and dry etching in a chlorine-bromine-based plasma. The 0.5% HF solution does not seem suitable for patterning the titanium buried mask as the metal etching process was very rapid (30-45 seconds) and thus not very controllable. Besides, there was a thin film of residues remaining on the wafers even after prolonged etching time up to 3 minutes. The extended etching time resulted in fewer residues, but it also caused a large under etch of more than 8 µm.

The ammonia-peroxide-based etchant seems like a viable method for titanium patterning. The etching process was gentle and controllable. The etch rate strongly depended on the age of the etchant, and the number of wafers etched at a time. After hardmask patterning (Figure 6.17c), the exposed parylene surface looked clean and free of residues. The patterns were transferred with minimal lateral under etch, and the edges of the metal hardmask looked smooth. However, after continuing the process with second parylene layer deposition and consequent parylene etching (Figure 6.17d,e), it has been found out that the edges of the titanium hardmask were slightly rough (Figure 6.18a). Nevertheless, the method proved to be safe for all the materials on the wafer, and it can be applied, for example, to remove the titanium buried mask after parylene patterning (Figure 6.17f).

The third promising method for patterning the titanium mask on parylene uses a RIE process chlorine-bromine-based plasma. After titanium dry etching for 2 minutes, the patterned wafers were dipped in the ammonia-peroxide-based etchant for 30 seconds to remove potential titanium fences. After hardmask patterning (Figure 6.17c), the exposed parylene surface looked clean and free of residues. The patterns were transferred without lateral under etch, and the edges of the metal hardmask looked smooth and had no fences. Similarly, the wafers were inspected after second parylene deposition and parylene patterning (Figure 6.17d,e). The edges of the titanium mask are much smoother than when the hardmask was etched using the wet ammonia-peroxide etchant (Figure 6.18b).

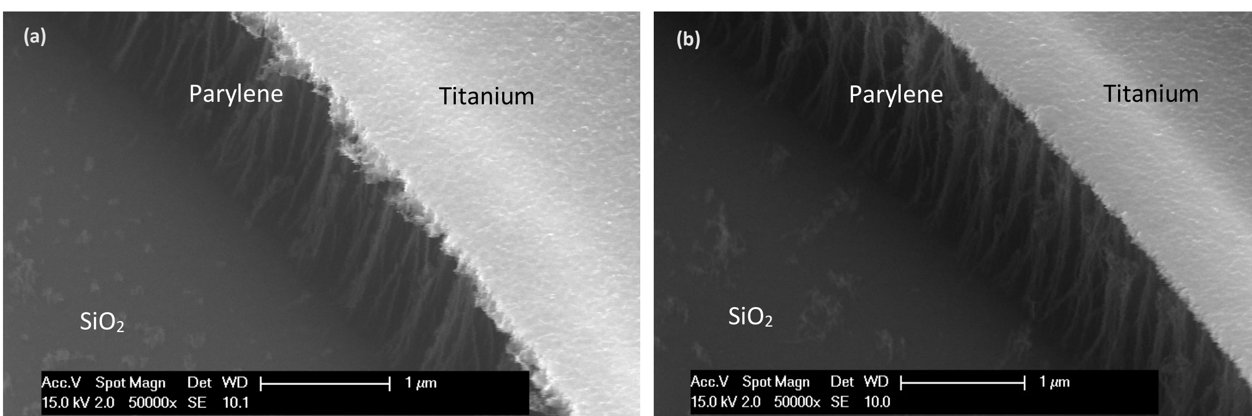

Figure 6.18: Parylene layer etched using a buried titanium hardmask. (a) Titanium mask patterned in the ammonia-peroxide-based etchant. (b) Titanium mask patterned in chlorine-bromine-based plasma.

In summary, parylene was successfully patterned using a 200 nm thick titanium (buried) hardmask. Out of the three tested methods for titanium hardmask patterning on top of parylene, the dry etching method in chlorine-bromine-based plasma combined with the short dip in the ammonia–peroxide-based etchant is the most promising. Compared with the other two etching methods (0.5 % HF solution and ammonia–peroxide-based etchant), it allows for the patterning of the mask in a controlled way resulting in very smooth mask edges and no fences. After parylene patterning, the hardmask can be cleanly stripped in ammonia–peroxide-based etchant.

6.5.3 Parylene removal from the back side of the wafer

In some processes involving parylene coating, it is necessary to maintain one side of the wafer free from parylene. This is the case also in the fabrication processes designed in this thesis and executed in Chapter 7 and Chapter 8. The most common method of local parylene deposition is covering the wafer area, where parylene is not desired, with adhesive tape, a sacrificial layer such as photoresist, or placing the wafer on a carrier. After the parylene deposition, the protective element is removed.

Because parylene deposition is conformal, separating the wafer from the protective material usually requires mechanical cutting or tearing of the parylene at the interface. This process generates particles, among others micro-sized organic-based parylene flakes, that are undesirable in the microfabrication cleanroom environment and are difficult to remove selectively from the wafer containing the parylene layer.

In this thesis, the designed processes for the fabrication of parylene-based devices involved processing the wafer in a cleanroom environment after parylene deposition. For that, the wafer has to be free of particles, which disqualifies the methods using covering layers as an option for selective parylene deposition. Besides, there should be no parylene remaining on the edges of the wafer as it can generate particles during wafer handling, for example, when taking the wafers out of or placing them in the wafer cassette. Therefore, dry etching of the parylene layer in oxygen plasma has been investigated as a particle-free and selective method for one-side parylene removal after its deposition on both sides of the wafer.

The O_2-based directional plasma recipe developed in Section 6.5.1 was used to remove 4 µm of parylene from the backside of test wafers. The front side contained 2 µm PECVD SiO_2 and 4 µm parylene. The process was performed in a Trikon Omega RIE etcher with a front side of the wafer resting on a slightly smaller chuck (5 mm exclusion). The parylene on the backside of the wafers was etched for 25 minutes using low-power, oxygen-based recipe #Par1 (for recipe details, see Table 6.8).

The parylene was completely removed from the backside of the wafers (Figure 6.19, Figure 6.20a). Parylene was also partially etched on the front side of the wafer at the exclusion ring of approximately 5 mm from the edge due to the smaller chuck (Figure 6.20b). This local parylene etch on the front side of the wafer is needed to ensure that the edge of the wafer is clean from parylene. There were no visible damages on the front side of the wafers due to the direct contact with the chuck of the machine.

The etch rate achieved for the purely oxygen-based #Par1 recipe was below 200 nm/min, which is too slow when considering the layer thicknesses in the range of a couple of microns that has to be removed. Therefore, the #Par2 recipe containing small addition of CF_4 (for recipe details, see Table 6.8) has also been investigated. The recipe resulted in almost five times higher etch rate of approximately 950 nm/min, and it was completely and safely etching parylene.

Both receipts are suitable for local removal of parylene. However, a combination recipe can be created if parylene needs to be selectively removed from layers that can be affected by the fluorine addition in the plasma (e.g., SiO_2, aluminum). Such a recipe can use O_2/CF_4 plasma to etch the bulk of parylene and pure O_2 plasma to etch the remaining parylene film and soft-land on the underlying layer.

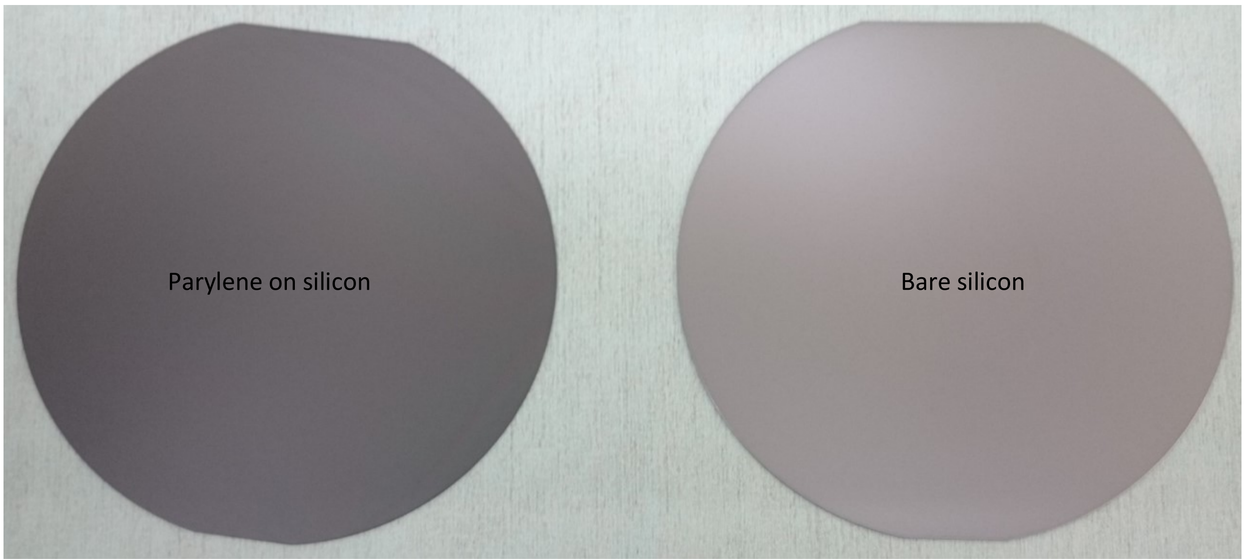

Figure 6.19: Silicon wafer conformably coated with 4 µm of parylene before and after parylene removal from the back side of the wafer using oxygen-based RIE process.

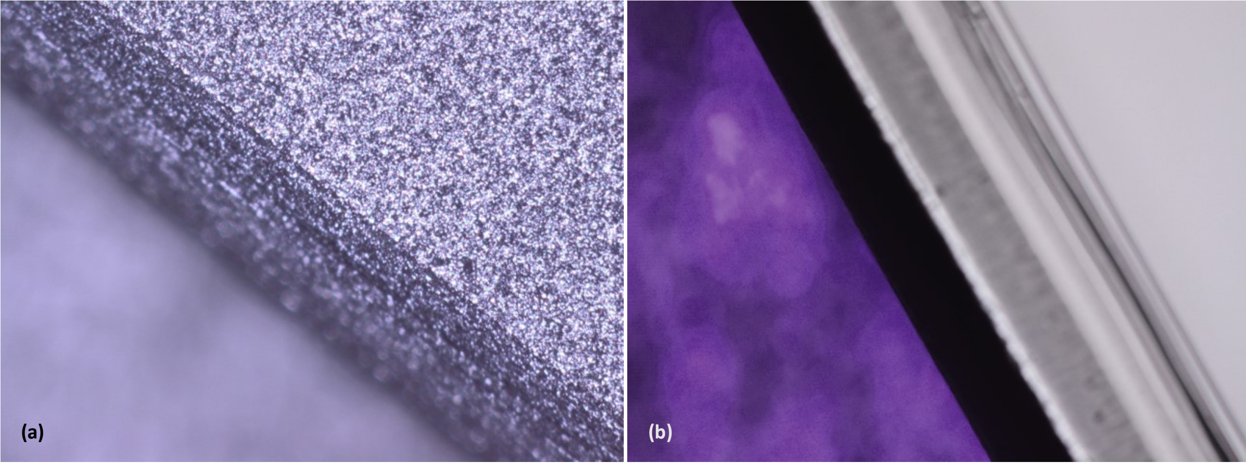

Figure 6.20: The edge of the silicon wafer conformably coated with 4 µm of parylene after parylene removal from the backside of the wafer using an oxygen-based RIE process. (a) Back side. (b) Front side.

6.6 PLATINUM PROCESSING ON TOP OF PARYLENE

The fabrication process designed for the flexible interconnects employs platinum as the only metal that will have direct contact with human brain tissue. Platinum has a number of qualities that make it an excellent material for stimulation electrodes, such as high biological inertness and low corrosively [23]. However, platinum is also one of the most challenging materials to process in a cleanroom environment, especially in combination with polymers. Because platinum is difficult to etch, it is also very hard to remove it from contaminated wafer surfaced or equipment. This increases a high risk of cross-contamination in cleanroom facilities where active devices are processed.

Furthermore, the common platinum patterning methods such as lift-off, etching in aqua regia, or argon sputter etching are often not selective to other materials present on the wafer, including polymers such as parylene. In this section, some methods are developed to process platinum on wafers that contain parylene. It is essential to recognize and address the critical points of the process. The first is the low-temperature budget, not exceeding 100°C, to protect parylene from degradation. The second is maintaining the backside and edges of the wafer clean from platinum to be able to further process the wafers in the EKL facility with specific contamination restrictions concerning platinum.

6.6.1 Platinum deposition on parylene

In the design of flexible interconnects presented in this thesis (Chapter 2), a single metallization is used to form metal tracks (interconnects), electrodes, and bond pad pads. First of all, the platinum layer should be relatively thick, minimum 500 nm, to enable wire bonding directly onto the platinum pad [24]. Furthermore, the platinum layer should be of sufficient density to provide stability of the platinum electrodes and high conductivity of the long interconnects. Sputtering is selected for the deposition of the platinum as this method, compared to evaporation, allows for faster deposition of thick layers, provides better step coverage, and results in a layer with densely packed platinum atoms [25]. Moreover, sputtered platinum adheres better to parylene [3].

Since the platinum target is not available for sputtering at the research location, the platinum deposition is performed at Philips cleanroom facility. To prepare samples for platinum etching experiments, a 20 nm titanium adhesion layer and 600 nm of platinum are sputter-deposited on 400 µm thick double side polished 4-inch wafers with pre-deposited 2 µm of PECVD of SiO_2 and 2.5 µm of parylene. The deposition process was optimized to keep the temperature of the wafer below 100°C. The deposited layer sheet resistance is 0.264 Ω/square.

During the deposition, a specially designed holder with a shielding ring was used (Figure 6.21a). The holder enables processing 4-inch wafers in a tool adapted to 6-inch substrates, and it maintains the back side of the wafer free from platinum. The shielding ring prevents platinum deposition on the 5 mm exclusion ring on the front side of the wafer (Figure 6.21b).

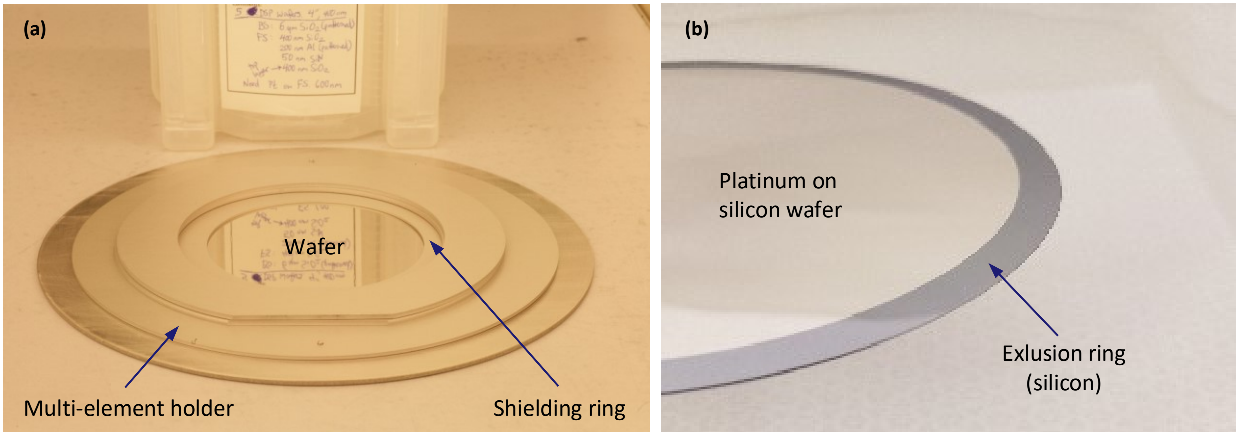

Figure 6.21: (a) An adapter with a shielding ring for processing 4-inch wafers in a sputter deposition tool fit for 6-inch wafers processing. (b) Wafer with deposited platinum layer. The back side of the wafer and the edge of the front side of the wafer (5 mm exclusion) are free of platinum.

6.6.2 One-step platinum etching

A dry sputter etching technique using argon ion beam (also called ion milling) is chosen to pattern the deposited platinum. In this method, accelerated argon atoms bombard the surface of the wafer and knock out the exposed material atoms. In principle, the lighter the material, the easier it is to etch it. Since polymers such as parylene have a relatively higher molecular weight (277g/mol [26]) than platinum (195 g/mol [27]), they are etched much slower during ion bombardment than platinum. This ensures some selectivity of the platinum-etch process towards the parylene.

Several photoresist types, thicknesses, and lithography processes were evaluated during the optimization of the one-step platinum patterning in the ion milling process and the subsequent photoresist mask removal. The key process parameters and experiments results are collected in Table 6.9.

Table 6.9: The one-step platinum etching process parameters and results.

Photoresist type	Photoresist thickness	Photoresist treatment	Ion milling process time	Platinum etching results	Photoresist removal results
SPR3027	4 µm	N/A	26 min 30 sec	+ Complete Pt etch + No shadowing - High fences	Photoresist residues on smaller structures
SPR3027	4 µm	N/A	6 min 40 sec 15 min cool-down 6 min 40 sec 15 min cool-down 6 min 40 sec 15 min cool-down 6 min 40 sec	+ Complete Pt etch + No shadowing - High fences	Photoresist residues on smaller structures
AZ9260	6 µm	Reflow (hot plate) 110°C for 30 sec Peak height 7.3 µm	28 min	+ Complete Pt etch + No shadowing - Short fences	Photoresist residues on metal tracks
AZ9260	6 µm	Reflow (hot plate) 110°C for 60 sec Peak height 8.2 µm	28 min	- Incomplete Pt etch - Shadowing - Short fences	Photoresist residues on metal tracks
HPR504	1 µm	Reflow (oven) 125°C for 30 min	28 min	+ Complete Pt etch + No shadowing + No fences visible	Photoresist could not be removed at all

Plus sign (+) indicates advantages while minus sign (-) indicates disadvantages of the process.

It was possible to cleanly etch platinum on top of parylene using the 4 µm thick SPR3027 photoresists, and no shadowing has been observed. Only 80 nm of parylene was etched at the end of the process, suggesting relatively good selectivity to parylene of the optimized process. However, after removing the photoresists, large fences around all the structures have been noted. Also, it was not possible to completely remove the photoresist, especially from smaller structures (Figure 6.22).

By applying thicker 6 µm layer of AZ9260 photoresist reflowed at 110°C it was possible to reduce the height of fences but not to eliminate them completely. The resist reflowed for 30 seconds resulted in clean platinum etching. However, the resist reflowed for 60 seconds with a peak height of 8.2 µm caused incomplete platinum etching, called "shadowing[3]" (Figure 6.23). Finally, it was not possible to prevent complete photoresist crosslinking and cleanly remove the photoresist after platinum etching by applying a thicker 6 µm layer of AZ9260 photoresist.

[3] Shadowing can occur due to the high of photoresist on closely-spaced structures that are obstructing the ion beam with a 15-degree incident angle used in this process.

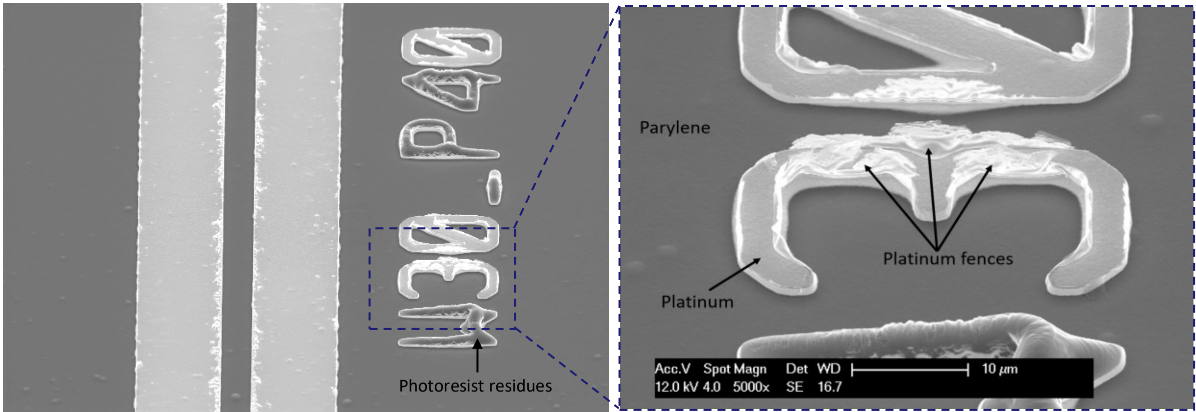

Figure 6.22: Wafers after one-step platinum etching and subsequent 4 µm SPR3027 photoresist removal. Platinum is completely removed from exposed areas. Visible platinum fences around the structures and photoresist residues on smaller structures.

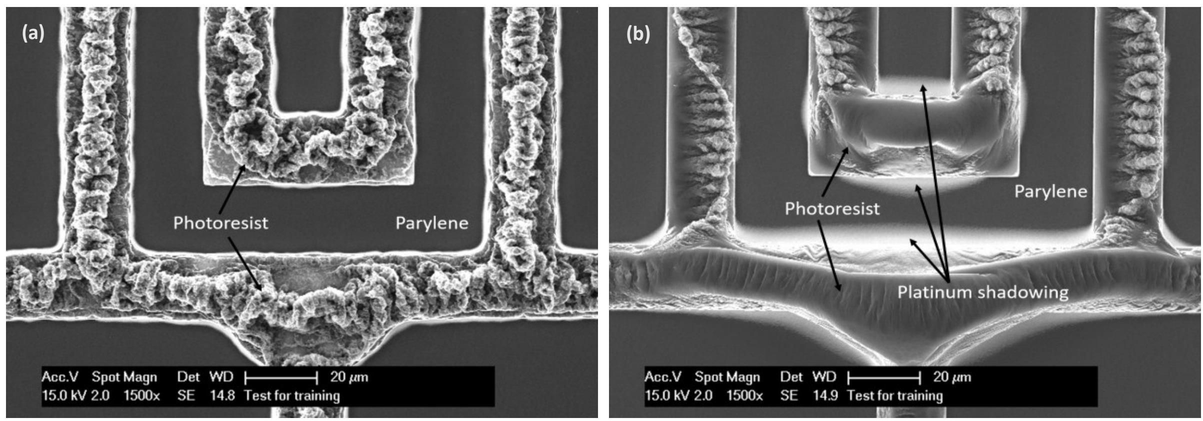

Figure 6.23: SEM images of wafers after one-step platinum etching using 6 µm AZ9260 photoresist reflowed on a hot plate at 110°C. The photoresist was not yet removed. (a) Reflow for 30 seconds resulted in a dome peak height of 7.3 µm. Platinum is completely removed from exposed areas. (b) Reflow for 60 seconds resulted in a dome peak height of 8.2 µm. There are visible residues of platinum due to shadowing.

Both the 4 µm thick SPR3027 and the 6 µm thick AZ9260 photoresists turned out to be too thin to prevent photoresist crosslinking and enable its complete removal from the wafer using solvents. The tested photoresist removal methods were acetone spin cleaning, acetone ultrasonic bath at 40°C, NMP (N-Methyl-2-pyrrolidone) ultrasonic bath at 70°C, and TechniStrip® P1316 ultrasonic bath at 75°C [28]. Moreover, the NMP solvent seemed to penetrate through the parylene layer and impaired the adhesion of the parylene to the underlying SiO_2 layer (Figure 6.24).

Also, the 1 µm thick HPR504 photoresist, specially designed to withstand prolonged exposure to plasma, has burned and could not be removed from the wafer at all with solvents (Figure 6.25). Only O_2 plasma was successfully stripping the photoresist, but this method cannot be applied to the wafers with exposed parylene layer that also etches in oxygen plasma.

The patterning of platinum deposited on top of parylene using the standard one-step platinum patterning approach consisting of lithography, platinum etching, and photoresist stripping failed in multiple ways. Even though in most cases it was possible to etch the platinum completely and selectively to parylene, defects such as fence formation, shadowing, and impossible to remove photoresist were observed. Therefore, in the next section, a novel two-step platinum etching process is developed and described.

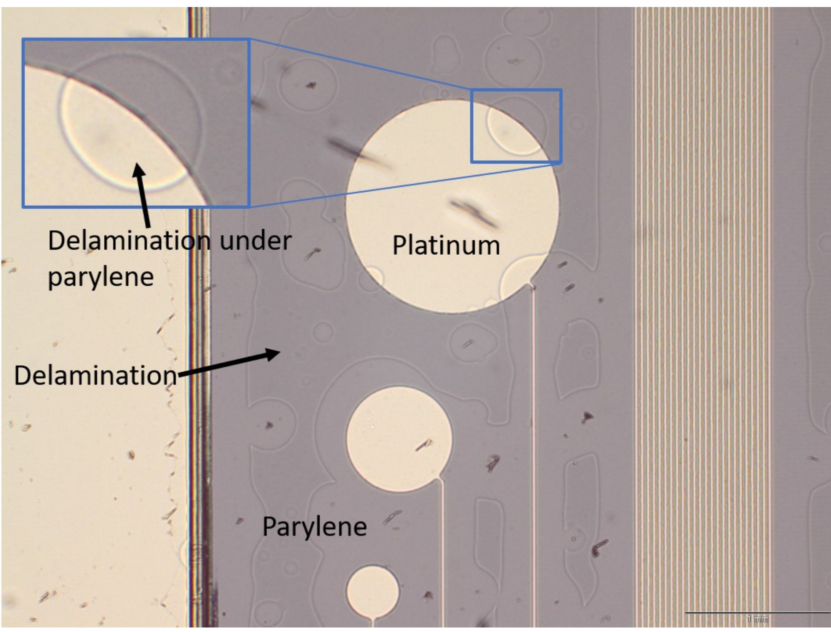

Figure 6.24: Delamination of parylene from underlying SiO_2 layer after 6 µm thick photoresist stripping in NMP ultrasonic bath at 70°C for 3 hours.

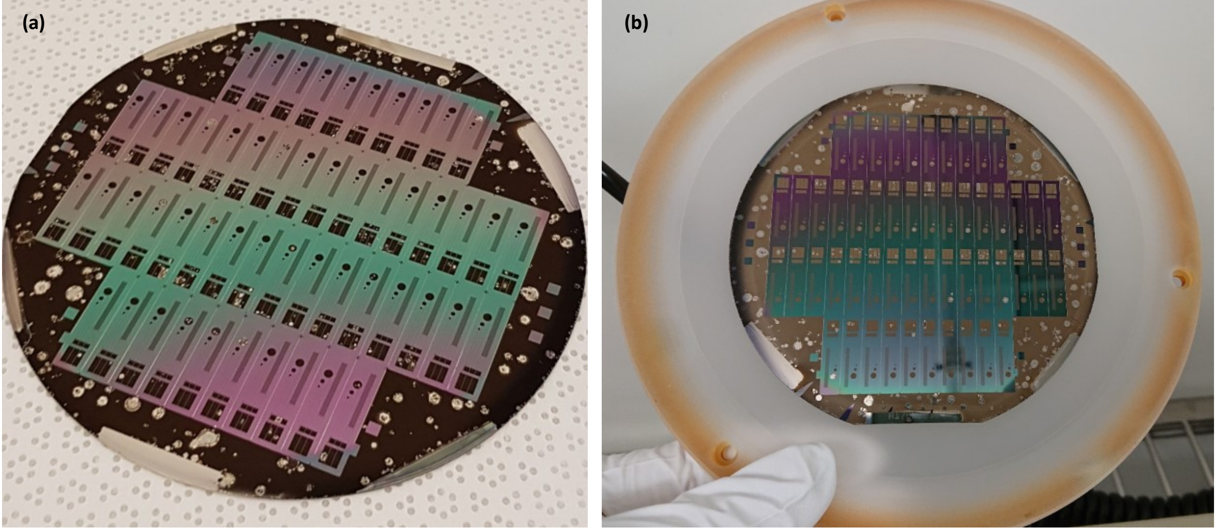

Figure 6.25: (a) Burned 1 µm thick HPR504 photoresist (black) after platinum ion milling and photoresist stripping in acetone ultrasonic bath at 40°C for 4 hours. (b) Photoresist color change (brown) indicating its partial removal after additional 2 minutes long O_2 plasma flash.

6.6.3 Two-step platinum etching

A two-step platinum patterning approach was developed to etch platinum on top of parylene without hard-to-remove residues of either platinum (e.g., in the form of fences) or cross-linked photoresist. In the first platinum etch step, approximately 550 nm, out of the 600 nm thick platinum layer, is etched by ion milling using 1 µm thick HPR504 reflowed in a convection oven at 125°C for 30 minutes. Next, the photoresist is removed using a high-power O_2 plasma stripper, where the wafer temperature was kept below 100°C. At this stage, the parylene is still covered with the remaining platinum, and therefore the oxygen plasma does not affect the polymer. In the second platinum etch step, the remaining 50 nm of platinum and the underlying 20 nm of titanium adhesion layer are etched. During this step, also approximately 70 nm of the platinum metallization is etched. The fabrication flow of the two-step platinum ion milling process is shown in Figure 6.26.

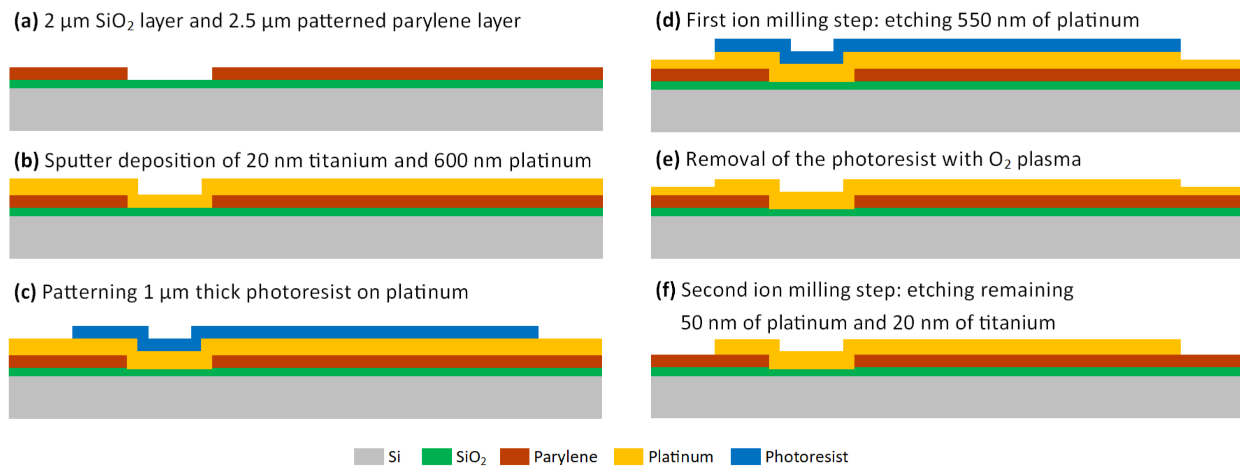

Figure 6.26: The two-step platinum ion milling process for platinum patterning on top of parylene.

Figure 6.27a shows the wafer after the first step of the platinum ion milling and the subsequent photoresists strip in O_2 plasma. In this trial, a bit over 350 nm of platinum was etched. The platinum etching was clean and uniform. The pattern was properly transferred from the photoresist mask to the metal. The photoresist was removed in O_2 plasma without residues. Figure 6.27b shows the wafer after the second step of platinum ion milling. The platinum was completely etched exposing the parylene layer. There are no signs of shadowing or fences formation.

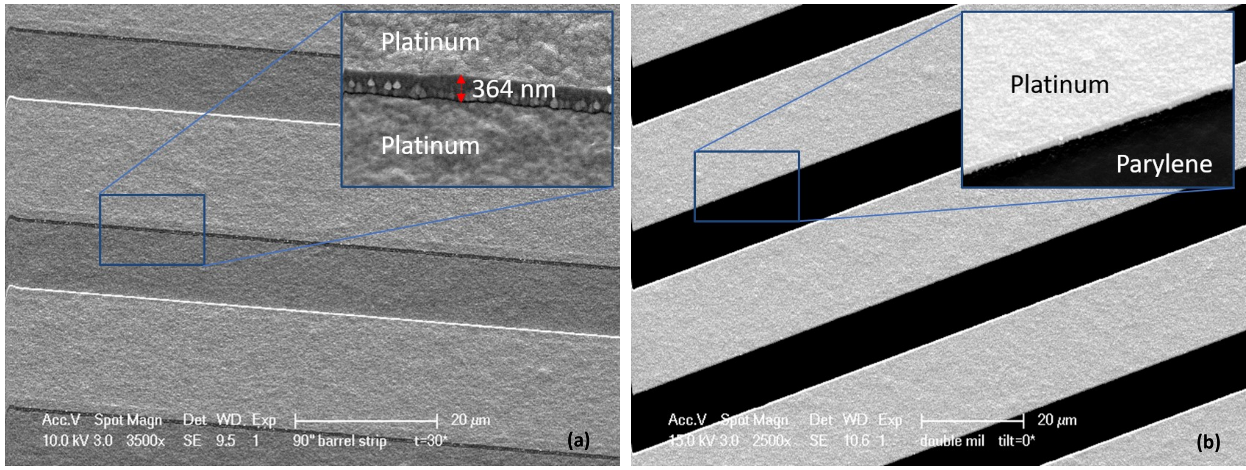

Figure 6.27: SEM images of two-step platinum etching results. (a) Wafer after first etching step and photoresist removal. No signs of fences formation. (b) Wafer after the second etching step. No shadowing.

It has been observed that the edges of the patterned platinum metallization have a slightly positive slope (Figure 6.28), which is favorable as it ensures better platinum coverage with the layers that are deposited next. The slope is probably cleated by the dome-shaped photoresist that is slowly being etched away during the ion milling, exposing more platinum to the plasma. Furthermore, at the edge of the metallization, there are some drop-like structures (Figure 6.28). The pattern most probably reflects the crystal grains of the platinum formed during the sputter deposition process and that etch at slightly different rates [29]. Finally, even though the photoresist reflow was performed at 125°C, exceeding the glass transition temperature of parylene (100°C), the polymer layer after platinum etching was intact and free of defects such as delamination or bubbles formation within or underneath the layer.

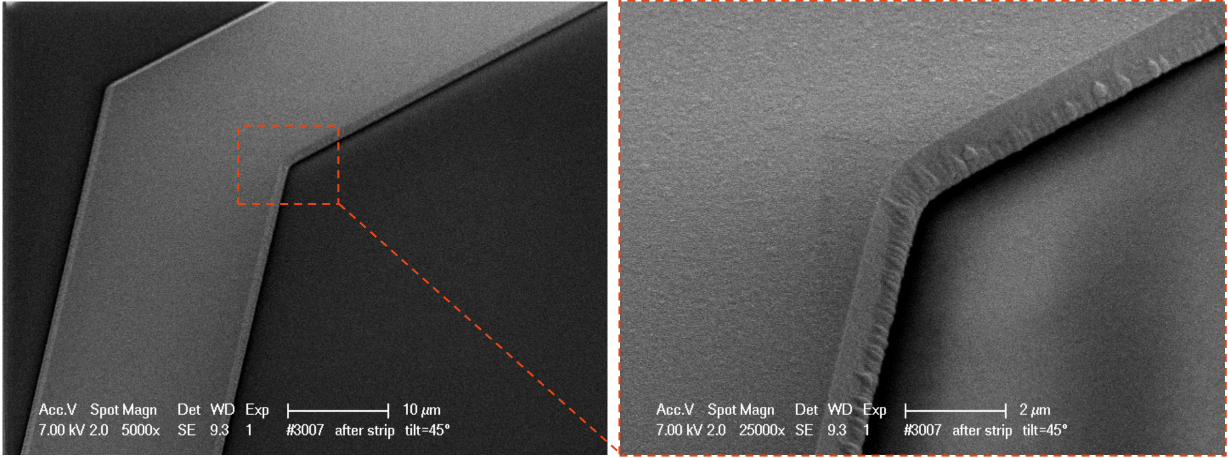

Figure 6.28. SEM images of two-step platinum etching resulted in a clean and bubble-free parylene surface, no shadowing, and no fence formation at the edges of the 550 nm high platinum structures. The metallization has a slightly positive slope with drop-like structures.

The two-step method for etching platinum on top of parylene was successful, and it resulted in clean and residue-free metallization. However, there are two reasons for concern for the two-step vs. one-step platinum etching process. One is that the two-step process requires a 70 nm thicker initial platinum layer. This has to be included in the fabrication process design. The second is related to the surface of the platinum tracks formed in the two-step method that is rougher due to its direct exposure to ion milling. However, in the case of the presented here process flow, this can be advantageous as increased by roughness platinum surface it is likely to improve the adhesion of the consecutively deposited second parylene layer.

6.7 CONCLUSIONS

Adhesion in the parylene-platinum based interconnects

It is possible to fabricate the three interfaces occurring in parylene-platinum flexible interconnect stack: platinum on parylene, parylene on platinum and parylene on parylene; using microfabrication CL100 methods. The adhesion between the layers in the three interfaces can be evaluated and classified using a cross-cut method. The cross-cut method allows for distinguishing which treatments, selected for the specific interface, influence the adhesion within the interface and to what extent.

Regardless of the applied treatment, most interfaces had at least good adhesion directly after fabrication and after two days of soaking in PBS at 37°C. The exceptions here were the parylene-parylene interfaces, where adhesion of parylene to underlying SiO_2 was worsened by introducing the treatments mimicking platinum deposition and patterning. After accelerated aging for ten days at 55°C, the adhesion of platinum to parylene in stack A was almost unchanged, and it reminded good. In stack B, after ten days of samples soaking at 55°C, parylene has completely or almost completely delaminated from the platinum layer. In stack C, the adhesion of parylene to parylene and parylene to underlying SiO_2 remained unchanged regardless of the duration or temperature of soaking. However, a variation of the initial adhesion of the first parylene layer to the silicon dioxide level has already been observed before the soaking.

Before fabrication of the parylene-platinum-based interconnects for long-term applications, such as DBS, the interface between the platinum metallization and the top parylene encapsulation must be significantly improved to be able to pass the extensive

reliability tests developed for implantable devices. Furthermore, the way of maintaining good adhesion of parylene to the substrate (SiO_2) throughout the platinum deposition and patterning process has to be investigated.

Cleaning wafers containing parylene

With acetone spin cleaning, wafers containing parylene can be successfully cleaned from most organic residues and loose particles sticking to their surface. The persistent organic residues might be removed with a short O_2 plasma flash. However, O_2 plasma is slightly etching the exposed polymer layer and results in a pattern transfer onto the exposed parylene layer. Persistent contamination, especially with metals, should be prevented by keeping a high level of working hygiene rather than applying one of the somewhat limited cleaning methods.

Contamination prevention in two-side wafer processing

A set of procedures was developed to keep the wafer clean from contamination when processing it from two sides. First, the order of deposition of the first layers was adopted so that the silicon surface, later etched in the DRIE process, is free from any persistent contamination that might cause micromasking. Secondly, since the cleaning methods for parylene containing wafers are limited, the direct contact of the front side of the wafer containing polymer with chucks has to be prevented. Whenever possible, an edge chuck for wafer clamping can be used. During the manual placing of the wafer front side down on a measurement or inspection tool chucks, an aluminum spacer ring can be used to prevent direct contact of the surface with the chuck. A direct wafer contact with the chuck can be a source of mechanical damage and lead to wafer cross-contamination.

Parylene etching and patterning

Parylene can be etched anisotropically in an oxygen plasma-based RIE process without layer deformation or the 6 µm thick AZ9260 photoresist burning. In the RIE process, a straight slope angle can be achieved by using a pure O_2-based plasma, and a 45°C to 55°C slope angle can be achieved by using O_2/CF_4-based plasma. Acetone spin cleaning has been successfully used to remove the photoresists mask after the polymer etching.

Parylene can also be patterned with excellent selectivity in a directional O_2 plasma using a metallic hardmask, such as aluminum and titanium. During the mask deposition at low temperature of 25°C, and subsequent patterning using a photoresist mask, no damage to the parylene layer was observed. The parylene patterned with the use of aluminum and titanium hardmask in the O_2-based RIE process had a well-defined structure with a straight slope.

Furthermore, the titanium can be used as a top hardmask or a buried hardmask for parylene etching. In the latter case, it can be used in combination with the aluminum etch stop layer that can be selectively removed from the wafer in PES without damaging the exposed titanium mask (see fabrication flowchart from Chapter 8). After the polymer etching in O_2-based plasma, the mask can be cleanly and selectively removed in an ammonia–peroxide-based etchant.

In the fabrication processes presented in this thesis, one-sided parylene deposition is required. Standard masking methods for parylene deposition on one side of the wafer are not microfabrication cleanroom compatible. In this thesis, a method was investigated for selective parylene removal after its conformal deposition on both sides of the wafer. The parylene can be efficiently and completely removed from the backside

and the edges of the wafer using O_2/CF_4 based plasma in the RIE etcher. When landing on device layers that can be etched in fluorine-based plasma, such as SiO_2 or aluminum, the slower and less aggressive soft landing, using only O_2 based plasma, can be performed at the end of the etching process.

Platinum processing on top of parylene

Platinum is a noble metal that is difficult to etch and remove from surfaces that are contaminated with it. A custom-designed shielding ring suitable for 4-inch wafers enabled local platinum deposition only on the front side of the wafer. The wafer backside and the edges are free of platinum contamination, enabling further wafer processing using scalable processes and automatized tools available at the EKL facility.

Etching platinum that is deposited on top of the parylene layer is challenging. This is mainly due to the high temperatures that are reached on the surface of the wafer during a sputter etching process using argon-based plasma. In standard, one-step etching processes, the photoresist was heavily cross-linked after etching. It could not be removed entirely from the wafer using methods that are not affecting the exposed parylene layer (e.g., acetone). The two-step platinum etching method, developed in this chapter, guarantees clean photoresist removal. This has been achieved by etching the metal in two sessions, between which the photoresist mask is removed using an O_2 plasma stripper. This approach allows for platinum patterning without the risk of photoresist residues remaining on the metallization. It also prevents the formation of fences, occurring of the shadowing effect, and it does not cause bubbles formation or delamination of parylene. In addition, the increased platinum roughness after the two-step process can potentially improve the adhesion of the second parylene layer to the platinum metallization.

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7

PARYLENE-PLATINUM FLEXIBLE INTERCONNECTS *"TOP STACK" APPROACH*[1]

7.1 INTRODUCTION

State-of-the-art foldable neurostimulation probes are made of biocompatible polymers such as parylene or silicone rubber. Such passive devices with flexible electrodes and interconnects tend to be less invasive due to the application of more body-like materials and their flexibility [1][2][3][4]. The main drawbacks of the current flexible neurostimulation probes are the cumbersome fabrication, including steps like wafer transfer and the limited possibility of electronic component integration. The emerging generation of neurostimulation devices strives to combine a highly integrated system with a flexible and body-friendly interface.

In this chapter, a process that is suitable for the monolithic fabrication of highly integrated semi-flexible neurostimulation devices is developed. The fabrication procedures must be suitable for processing pre-fabricated wafers that contain, for example, custom-designed capacitors. This means that the applied fabrication methods and conditions, like temperature budget, must be compatible with the structures that already exist on the wafer. Moreover, one of the goals of this thesis is to develop a scalable process, and therefore uses only well-established, MEMS compatible processing techniques and equipment.

The process is developed on an example of the implantable deep brain stimulation (DBS) probe designed in Chapter 2. Such probe can be composed only out of materials approved for a long stay in the body by the Food and Drug Association (FDA). The most common materials present in the existing steerable DBS probe are platinum, used for the metallization forming interconnects and stimulation electrodes, and parylene forming the flexible film that forms and encapsulates the flexible metallization [5]. Optionally, silicon and ceramic layers such as Si_3N_4 and SiO_2 can be present in the device. The silicon serves as a mechanical support for the structures or even contains passive devices such as capacitors. The ceramic layers act as an insulator and additional barrier to moisture and chemicals.

The next aspect is the device flexibility, which is especially essential in the case of the DBS probe, designed in Chapter 2, because it enables wrapping of the parylene-based flexible film with embedded metallization into a 1.3 mm diameter needle-shaped cylinder forming the easy to implant DBS probe (Figure 7.1). Furthermore, the DBS design presented in this thesis includes silicon islands for electronic components integration, such as decoupling capacitors and ASICs. For example, the ASIC island is folded to the inside of the DBS probe cylinder at a bending radius of approximately 55 µm, which calls for an ultimate device and interconnects and flexibility.

[1] The chapter is partially based on the work of supervised master student A. Kanhai [11].

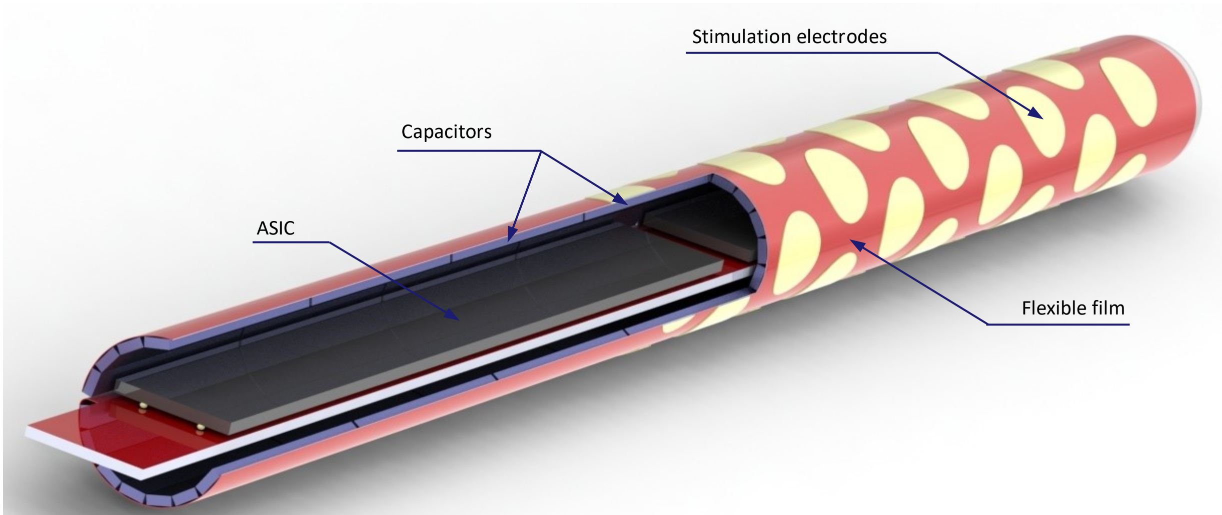

Figure 7.1: 3D model of the Chip-in-Tip concept incorporating two ASICs (chips) and eighty blocking capacitors inside the tip of the 40-electrode DBS probe.

In this chapter, a semi-flexible test device with parylene-platinum-based flexible interconnects and a rigid silicon island is designed and fabricated. The test device structures correspond with the design presented in Chapter 2, and the fabrication flowchart follows the guidelines and best practice methods investigated and summarized in Chapter 6. The test device allows for evaluating the F2R-inspired monolithic fabrication process and the mechanical and electrical properties of the flexible interconnects.

7.2 TEST DEVICE DESIGN

The test device is 3.4 mm wide and 18.4 mm long, and it is composed of a single-metallization parylene-platinum-based flexible film, directly integrated with platinum electrodes and bond pads located on a rigid silicon island (Figure 7.2).

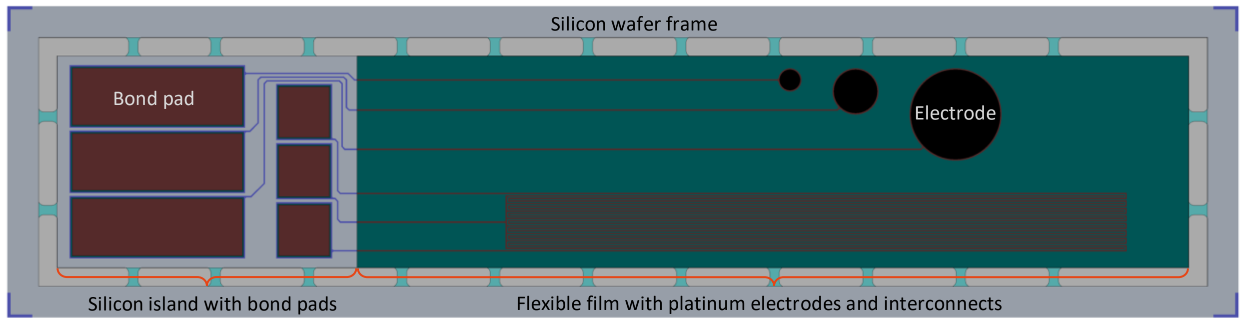

Figure 7.2: Test device with rigid silicon island with bond pads and parylene-platinum-based flexible film containing interconnects and platinum electrodes.

The device contains two test structures used to assess the feasibility of this semi-flexible medical device fabrication process and the interconnects performance. The first structure is a specially developed comb-meander structure that allows for flexible interconnect mechanical characterization and stability assessment using an integrated inter digitated electrode (IDE). The second structure is a set of three platinum electrodes with different diameters that can be used for the electrochemical characterization of the device.

7.2.1 Comb-meander structure

The comb-meander structure is located in the flexible part of the device and is accessible for measurement through the square bond pads located on the silicon island. The 10 cm long platinum structure is composed of 166500 µm long meander (green tracks in Figure 7.3), which is also a part of the open 8-tooth IDE comb (purple tracks in Figure 7.3) running in-between the 8-loop meander. The comb-meander structure is formed from 20 µm wide metal tracks, pitch 40 µm, encapsulated from two sides in a 2.5 µm thick parylene layer. The comb-meander structure is located at a sufficient distance from the exposed metallization of the bond pads, which should not be submerged in the PBS (phosphate-buffered saline) during the reliability tests. The bond pad size and location enable easy handling during manual measurements using a probe station.

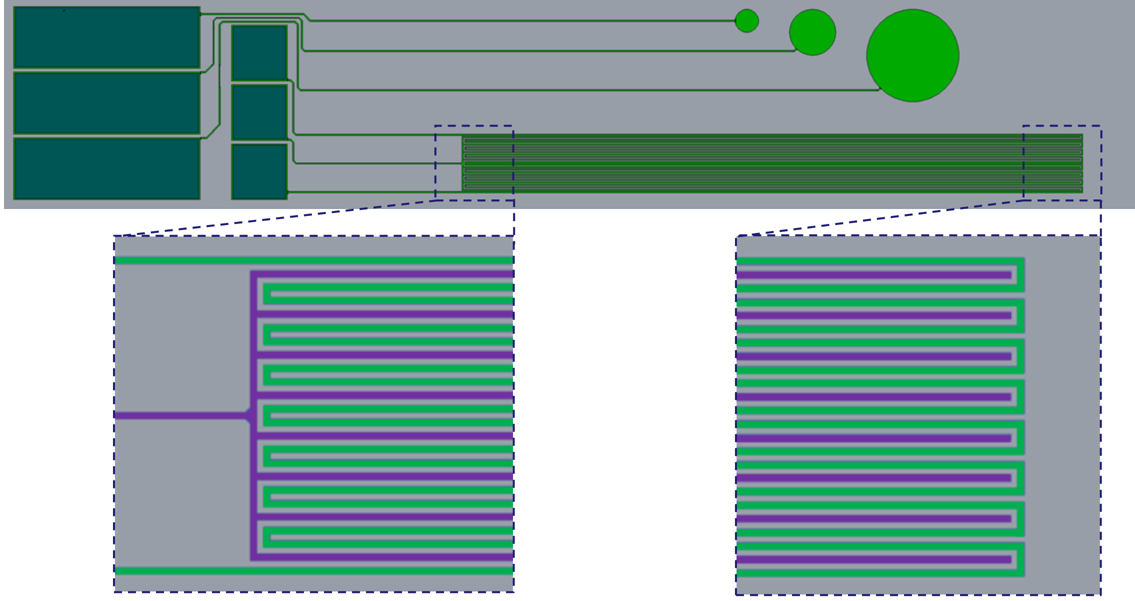

Figure 7.3: The test device with comb-meander structure. The meander is marked in green, while the comb is marked in purple.

The meander is designed to characterize the mechanical properties of interconnects during rolling and bending by measuring the track resistance change during or after mechanical stressing. The comb running in between the meander allows for assessing interconnects stability and reliability during the device soaking in a PBS (phosphate-buffered saline) solution by measuring an impedance change between the two structures.

7.2.2 Electrodes

The three, round platinum electrodes are designed to characterize the electrochemical performance of the device, such as the charge injection performance or the material stability. They are located in the flexible part of the device (Figure 7.2). Each electrode is connected to an individual rectangular bond pad using 20 µm wide interconnects. The optimal surface area for a deep brain stimulation electrode, defined in Chapter 2, is approximately 0.4 mm^2, which can be ensured by 700 µm diameter round electrode. This dimension allows for low electrode impedance and ensures sufficient stimuli delivery, and at the same time prevents a too high local charge injection that might cause irreversible changes to the tissue [6][7][8]. The test device designed in this chapter contains one electrode with a standard diameter of 700 µm, one electrode with a two times smaller diameter of 350 µm, and one electrode with a two times larger diameter of 1400 µm. The variation is intended to be able to study the effect of the electrode

diameter on the electrochemical behavior of the structure. Similarly, as in the case of the comb-meander structure, the electrodes are located at a sufficient distance from the bond pads, which should remain accessible and not be submerged in the PBS solution during the electrode characterization.

7.3 FABRICATION FLOWCHART – “TOP STACK”

During the development of the fabrication flowchart, it is essential to use or optimize only standard manufacturing methods. It ensures the possibility of combining the process with silicon substrates that contain pre-fabricated electronic components such as capacitors or ASICs. Furthermore, the utilization of only standard microfabrication methods ensures the fabrication scalability from 4-inch wafers (in this thesis) to larger diameter wafers.

In this section, the fabrication of the parylene-platinum based flexible interconnects is presented (Figure 7.4). Next, the fabrication results are discussed. Also, some intermediate fabrication results for crucial process steps are presented. The detailed process flowchart that was used in this thesis can be found in Appendix A.

7.3.1 Deposition and patterning of the PECVD SiO_2

The fabrication flow starts with depositing 6 µm thick low-stress PECVD SiO_2 on the backside of the 400 µm thick, 4-inch, double-side polished silicon substrate, followed by depositing 2 µm of low-stress PECVD SiO_2 on the front side of the wafer (Figure 7.4a). The 2 µm SiO_2 layer is a multipurpose layer that serves as an insulator between bond pad pads and silicon, an adhesion enhancing layer for the first parylene layer, and an etch stop layer during the final DRIE.

Next, the 6 µm thick PECVD SiO_2 layer is patterned using the *Backside* mask (Figure 7.4b, Figure 7.5a). The layer is later used as a hardmask during the device release in the backside DRIE process. The mask is patterned already at this stage to minimize wafer flipping and backside processing, as flipping the wafer at a later in the process might damage the parylene layer.

7.3.2 Bottom parylene layer deposition and patterning

Next, the first 2.5 µm thick parylene layer is deposited on both sides of the wafer using the standard A-174 primer. The parylene is removed from the backside of the wafer using a directional O_2 plasma. The parylene on the front side of the wafer is now patterned at the location of bond pads (Figure 7.4c) in an O_2/CF_4-based plasma (recipe #Par2, Table 6.8) using the *Contact to Silicon* mask (Figure 7.5b). It ensures that the bond pads, eventually located on the rigid Si island, are robust enough for performing manual measurements using sharp needle probes or crocodile clips.

7.3.3 Platinum metallization deposition and patterning

In the next step, a stack composed of 20 nm of titanium adhesion-promoting layer and 600 nm of platinum is sputtered onto the parylene at room temperature. The metal layer is patterned using the *Metallization* mask in an ion milling process to form the: electrodes, interconnects, and bond pads (Figure 7.4d, Figure 7.5c). The relatively thick metallization thickness of 600 nm ensures a low impedance of the interconnects and robust and scratch-proof bond pads suitable for wire bonding and the flip-chip processes [9].

7.3.4 Top parylene layer deposition

After the metallization patterning, a second 2.5 µm thick parylene layer is deposited on both sides of the wafer, using the standard A-174 primer, and removed from the backside of the wafer with a directional O_2 plasma (Figure 7.4e). The first and the second layer of parylene have the same thickness, which implies that the metallization lies in the stress-neutral plane of the flexible film. Therefore, it is more resistant to mechanical damage during folding and bending in either direction.

7.3.5 Titanium hardmask deposition and patterning

At this point, a 200 nm thick titanium hardmask is sputter deposited at 25°C and patterned in chlorine-bromine-based plasma using the *Contact to Bond pad/Parylene Patterning* mask (Figure 7.4f, Figure 7.5d). This mask is later used to open the electrodes and the bond pads, and to form the parylene release tabs around the device. The titanium hardmask is patterned before the consequent device release in the DRIE process because patterning the released wafer with the flexible structures can cause alignment and focus issues when using standard lithographic tools.

7.3.6 Backside DRIE etch

Now that the front side of the wafers is prepared for bond pad and electrode opening, the wafer is flipped, and the complete 400 µm thick silicon wafer is etched from the backside. For that, the pre-patterned *Backside* mask and the silicon dioxide etch stop layer are used (Figure 7.4g). During this step, the semi-flexible devices are formed, composed of the flexible parylene-platinum film connected to the rigid silicon islands. The device is thinned down, and the silicon islands are released from the wafer. The etched device remains suspended in the wafer through the flexible film composed of parylene and the remaining SiO_2 etch stop layer. At this stage of the processing, the front side flexible film is not yet patterned, forming a closed layer that prevents helium leakage from the cryo-chuck during the DRIE process.

7.3.7 Top parylene layer patterning

In the next step, the top 2.5 µm of parylene is etched using the *Contact to Bond pad/Parylene Patterning* mask to open the bond pads and the electrodes and form parylene-based release tabs. The etching continues on the edges of the device until the remaining 2.5 µm bottom parylene is removed, landing on the silicon oxide layer (Figure 7.4h). After this, the 200 nm titanium hardmask and the 2 µm thick SiO_2 etch stop layer are wet etched (Figure 7.4i).

At the end of the process, the devices are suspended in the wafer by means of the parylene based release tabs. They can be taken out of the wafer by cutting the tabs along the outline of the device with a blade or a laser. The finished device comprises only five materials: SiO_2, parylene, platinum, titanium, and silicon.

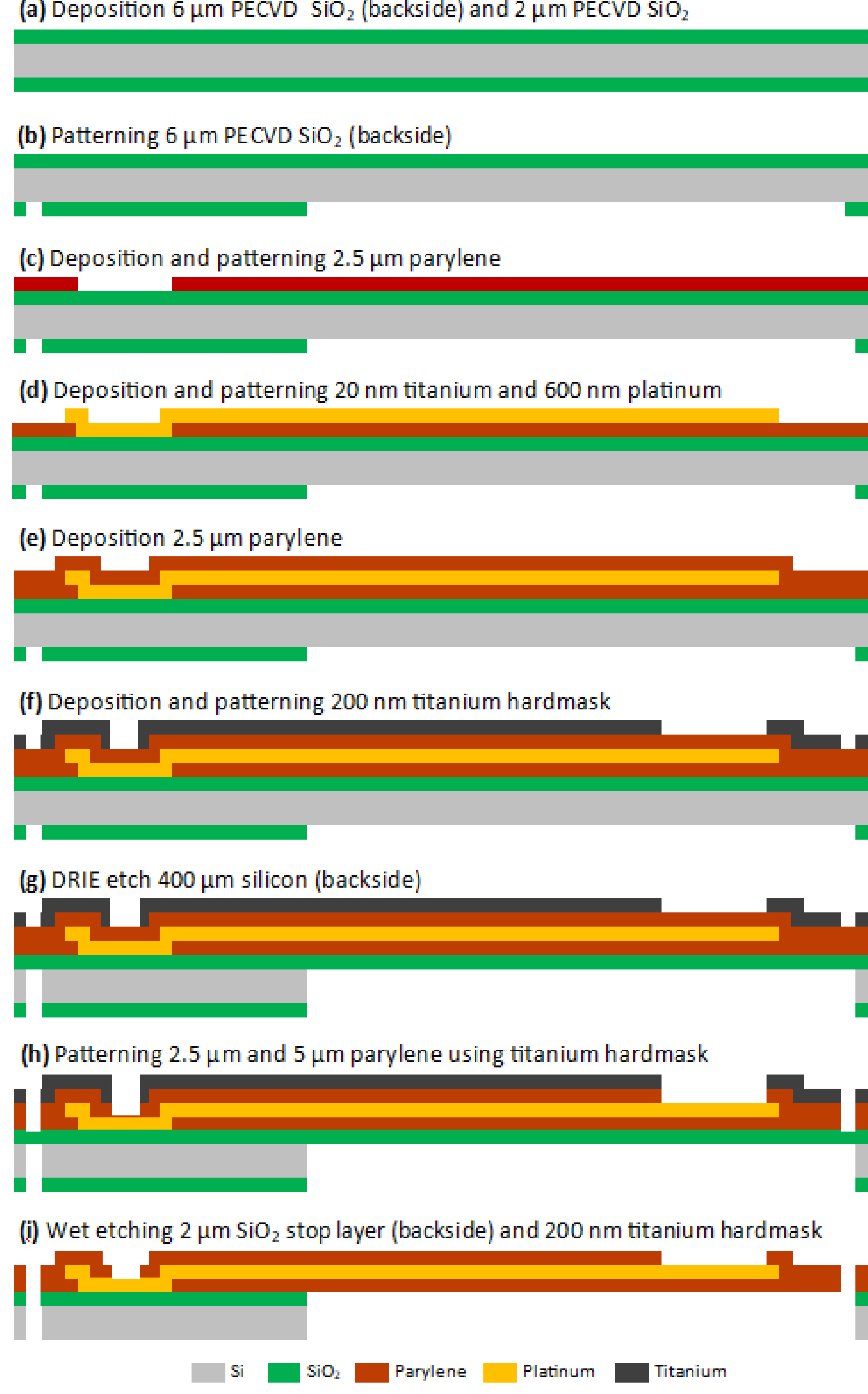

Figure 7.4: The process flow for the fabrication of F2R-based test devices with parylene-platinum flexible interconnects and flexible platinum electrodes using the "top stack" approach.

7.4 MASK DESIGN

A single reticle with four images (masks) was designed to fabricate the test device presented in this chapter (Figure 7.5). The four mask images are:

- *Backside* mask is used to pattern the 6 µm thick SiO_2 hardmask with which the semi-flexible device is released in the final silicon DRIE (Figure 7.5a). The etching is performed from the backside of the wafer, landing on a SiO_2 etch stop layer.
- *Contact to Silicon* mask is used to etch via in the first parylene layer, at the location of the bond pads, before the metallization (platinum) deposition (Figure 7.5b);
- *Metallization* mask is used to pattern the single layer of metallization that forms electrodes, interconnects, and bond pads (Figure 7.5c).
- *Contact to Bond Pad/Parylene Patterning* mask is used to pre-pattern the hardmask (titanium) that is later used to open the electrodes and bond pads, and to pattern the parylene at the very end of the fabrication process (Figure 7.5d).

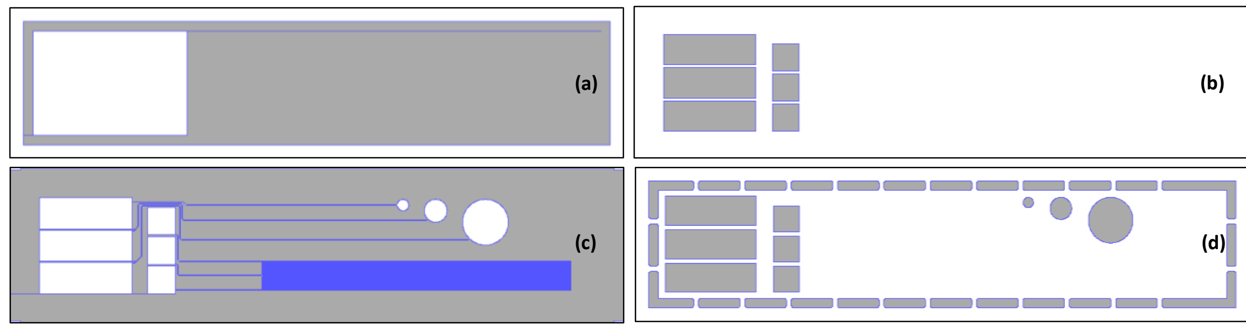

Figure 7.5: The single reticle with four images used to fabricate the test device in the "top stack" approach. (a) Backside. (b) Contact to Silicon. (c) Metallization. (d) Contact to Bond pad/Parylene Patterning.

7.5 DEVICE FABRICATION – RESULTS AND DISCUSSION

The test devices were successfully fabricated. They comprise the flexible comb meander structures and electrodes connected to the rigid silicon island with the bond pads. Figure 7.6 shows the device still suspended in the silicon wafer by the parylene tabs.

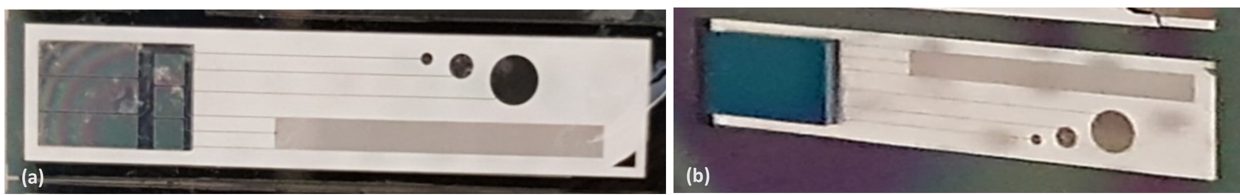

Figure 7.6: Fabricated semi-flexible device with parylene-platinum based interconnects, platinum electrodes, and a rigid silicon island with bond pads. (a) Front side of the wafer. (b) Backside of the wafer.

7.5.1 One-step platinum etching

The platinum metallization in this batch of wafers was patterned in a one-step ion milling process using a 6 µm thick AZ9260 photoresist. To completely remove the photoresist, it was necessary to strip it for three hours in an ultrasonic bath with NMP at 70°C with an additional O_2 plasma flash. The NMP treatment caused local delamination of the parylene from the underlying SiO_2 layer (see Figure 6.24). Because of the impaired adhesion between the device layers, the reliability of the interconnects was not evaluated for these samples.

Moreover, in the later stage of wafers processing, after the second parylene deposition, some roughness around the edge of platinum structures has been observed (Figure 7.7). These are probably small platinum fences remaining after the one-step platinum

patterning process using 6 µm thick AZ9260 photoresist (see Section 6.6.2). The defects became visible in the optical microscope only after the deposition of the second parylene layer that acted like a magnifying glass. In future process iterations, this issue is solved by performing the two-step platinum patterning process developed and described in Section 6.6.3.

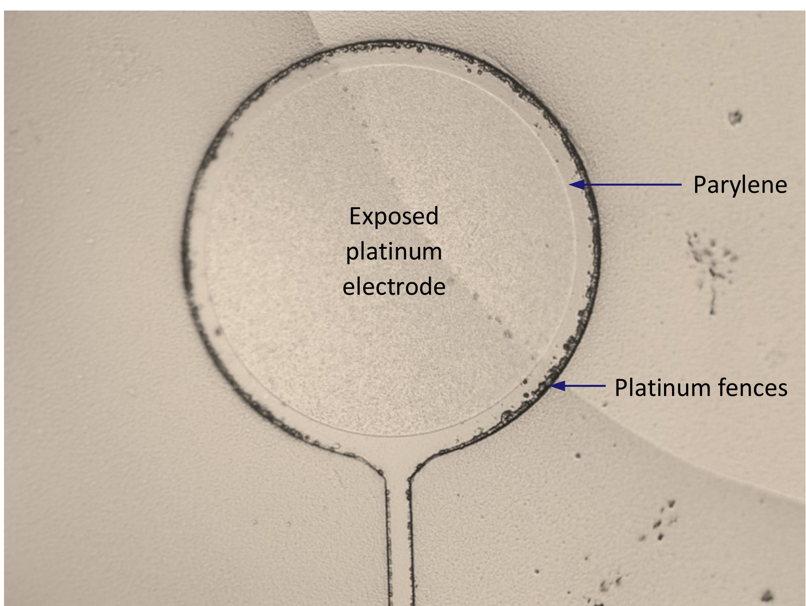

Figure 7.7: Platinum fences around the electrode, buried under a layer of parylene.

7.5.2 DRIE process – Cracking SiO_2 stop layer

During processing the first batches of wafers, the 2 µm silicon oxide etch stop layer was sometimes cracking after the backside DRIE process was complete (Figure 7.8). Severe cracks were occurring only in devices located at the edge of the wafer where they seem to originate from the edges of the device and propagated to the surface of the flexible film. For devices located in the middle of the wafer, the cracks were present around the devices following the line of the release tabs. The cracks are probably due to intrinsic stress present in the layers of the stack.

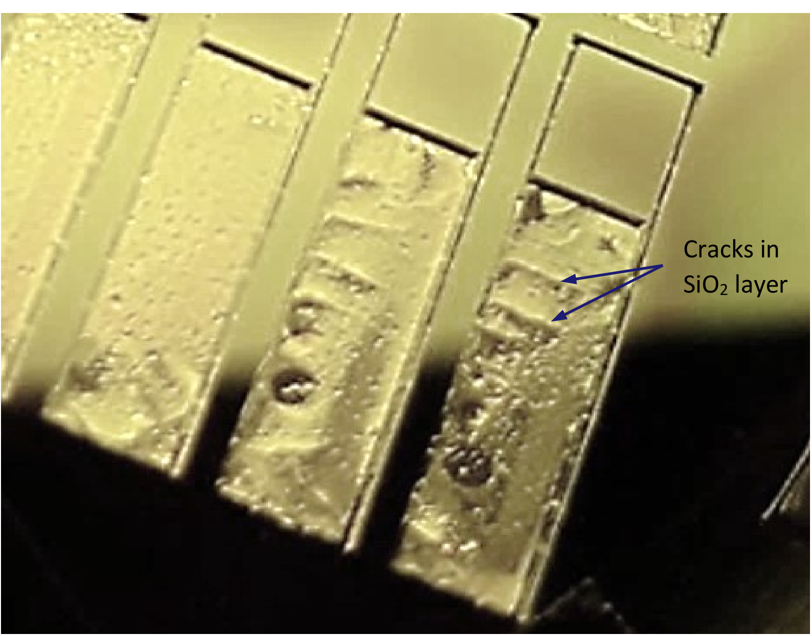

Figure 7.8: Cracking 2 µm SiO_2 stop layer right after the backside DRIE release process.

Tearing of the platinum-containing flexible film during etching should be avoided to prevent contamination of the chuck of the DRI etcher. Therefore etching of the wafers using a carrier wafer alone or a carrier wafer with a thermally conductive adhesive was investigated. Unfortunately, when using the carrier wafer alone, the heat transfer during etching was not sufficient, resulting in large etch rate variations across the wafer and failure of the release process. It was possible to improve the heat transfer and achieve excellent etch rate uniformity by using thermally conductive adhesive Crystalbond™ 555 applied between the process and the carrier wafer. However, the adhesive was altered during the DRIE process, and it was impossible to separate the bonded wafers.

In the future, a short-term solution to the cracking problem could be to move the process to a tool where platinum-containing wafers can be etched without restrictions or to investigate alternative mediums for heat transfer. In the long term, the cracking of the layer should be prevented by, for example, optimizing the device design, adjusting the thickness of the brittle stop-layer and flexible parylene layer, or optimizing the fabrication flow. The long-term solutions were applied to the later developed "parylene last" approach for the fabrication of parylene-based flexible interconnects (Chapter 8).

7.5.3 Curling of the final devices

After completing the "top stack" fabrication process, many devices had the flexible interconnects partially released and curled downward or even torn (Figure 7.9). A clear directionality of the curling to the back has been observed. Such behavior has not been observed in the wafer containing dummy structures with the same parylene thickness but without platinum tracks. This clearly links the curling directly to the presence of patterned platinum on the wafers or indirectly to platinum deposition and patterning processes.

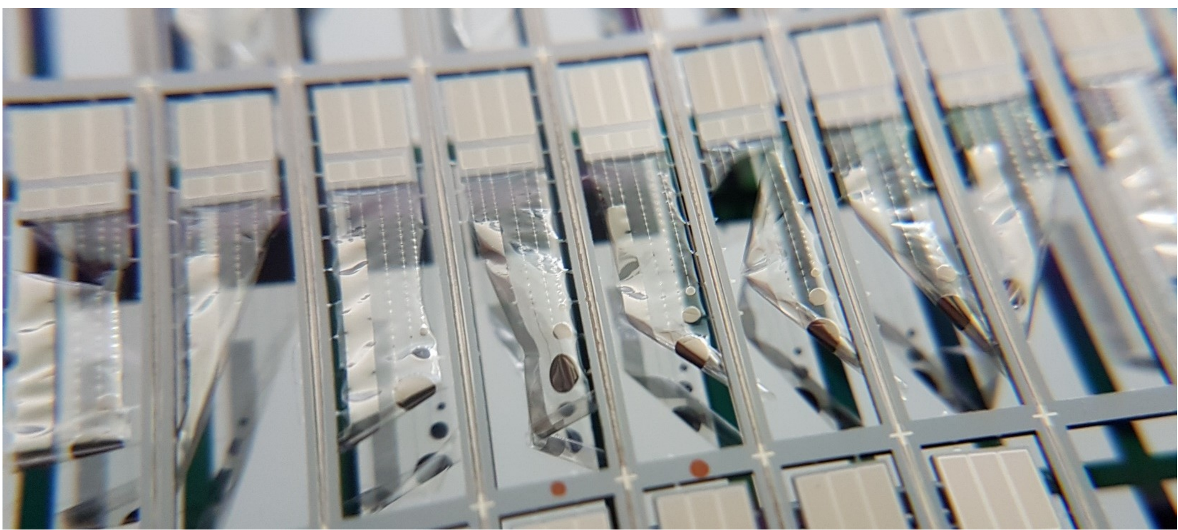

Figure 7.9: Finished semi-flexible devices with curled or torn parylene-platinum flexible interconnects.

A thick film of platinum deposited on a titanium adhesion layer at room temperature can exhibit a significant compressive residual stress in the range of several gigapascals [10]. Such compressive stress can lead to backward curling of the thin, flexible film, especially at the comb-meander structure, where the metallization is densely packed.

In the next iteration of the fabrication process (Chapter 8), the problem of curling devices has been solved by applying approximately two times thicker parylene layer (2 µm x 5 µm) and additional ceramic layers that contribute to the mechanical reinforcement of the flexible film.

7.6 DEVICE EVALUATION

The evaluation of the devices was focused on the mechanical properties and the basic electrical performance of the interconnects using the comb-meander structure. The reliability testing was not performed since the adhesion between the layers was corrupted during the photoresist strip after platinum patterning.

The electrodes on the fabricated devices could not be electrochemically characterized. It was due to the numerous issues occurring during the fabrication process, such as the presence of fences around the platinum structures, layers delamination after resist stripping in NMP, or tearing of the devices and interconnects damage during device separation from the wafer.

7.6.1 Electrical characterization

The electrical conductivity of the interconnects was evaluated by means of the meander structure embedded in the parylene flexible film. The electrical contact was made through the bond pads located on the rigid silicon island. The measurement was performed on a device that was still suspended in the wafer. This was because the devices were curling after releasing them from the wafer frame, and they got either damaged or became difficult to perform the measurements. A four-probe station Cascade MicroTech was used to perform four-point measurements of the meander structure resistance. The measured resistance was equal to 2153 Ω, which is in line with the calculated theoretical meander resistance of 2198 Ω. The theoretical and the measured resistance of the meander are almost identical, which proves that the semi-flexible parylene-platinum based interconnects have been successfully fabricated.

7.6.2 Device rolling and folding

The mechanical properties of the device were first evaluated by rolling the flexible interconnects into a cylinder shape. To ease the handling of the test structure, the rigid part of the device was left suspended in the wafer frame while the flexible part was released from the wafer by cutting the parylene tabs using a sharp blade. The released flexible interconnects were rolled into a diameter of approximately 1 mm using two pairs of tweezers on each side of the film. Then the tweezers were removed, causing a slight unrolling of the film (Figure 7.10a). The resistance of the meander structure was measured before and after the rolling process.

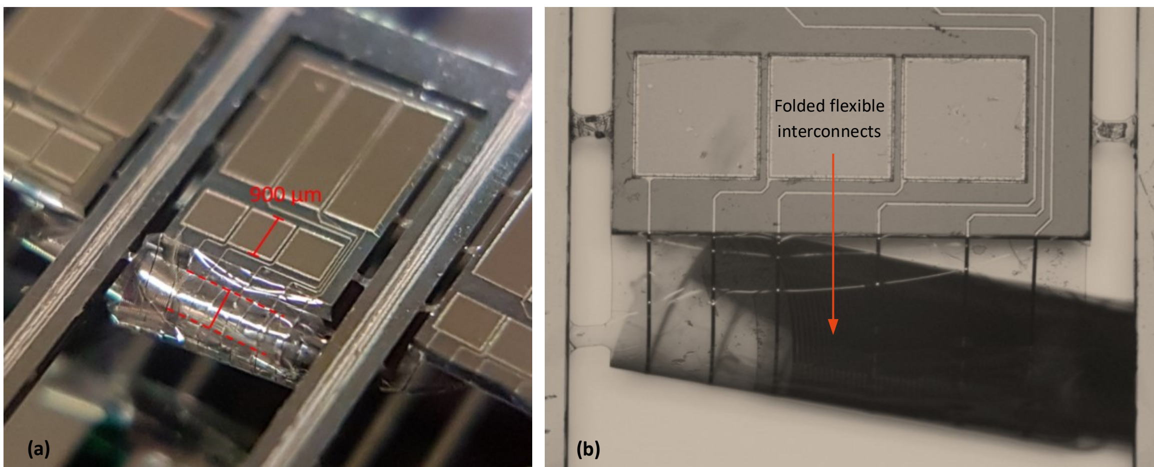

Figure 7.10: (a) The flexible interconnects rolled to a diameter of approximately 1 mm and released. (b) The flexible interconnects rolled and folded to radii ranging from 5 µm to 50 µm.

Next, the rolled interconnects were folded by squeezing the film between the tweezers (Figure 7.10b). This resulted in bending radii ranging from approximately 50 µm for the outer loops and down to 5 µm for the inner loop. Subsequently, the tweezers hold was released, and the resistance of the folded meander structure was measured. The results from the rolling and folding tests are collected in Table 7.1.

Table 7.1: The results of the electrical measurements after the device rolling to 1 mm diameter and folding down to 5 µm radii.

	Before rolling	**After rolling**	**After folding**
Meander resistance [Ω]	2153	2151	2161

The resistance of the meander structure before rolling, after rolling, and after folding did not change significantly. It can be concluded that the electrical performance of the flexible interconnects was not affected by the applied deformations and that the film can withstand bending radii even down to 5 µm.

Optical inspection

After the electrical measurements, the flexible interconnects were unrolled to their original state, and the folding location was investigated optically. In Figure 7.11, a clear mark can be seen at the location where the parylene-platinum-base film was bent down to the smallest radius of 5 µm. A clear fold is only visible in the thin parylene film, which is more prone to plastic deformations. No cracks in the platinum film have been seen also during the inspection using a backside illumination. The consistent electrical measurements also indicate that the platinum interconnects have not been affected.

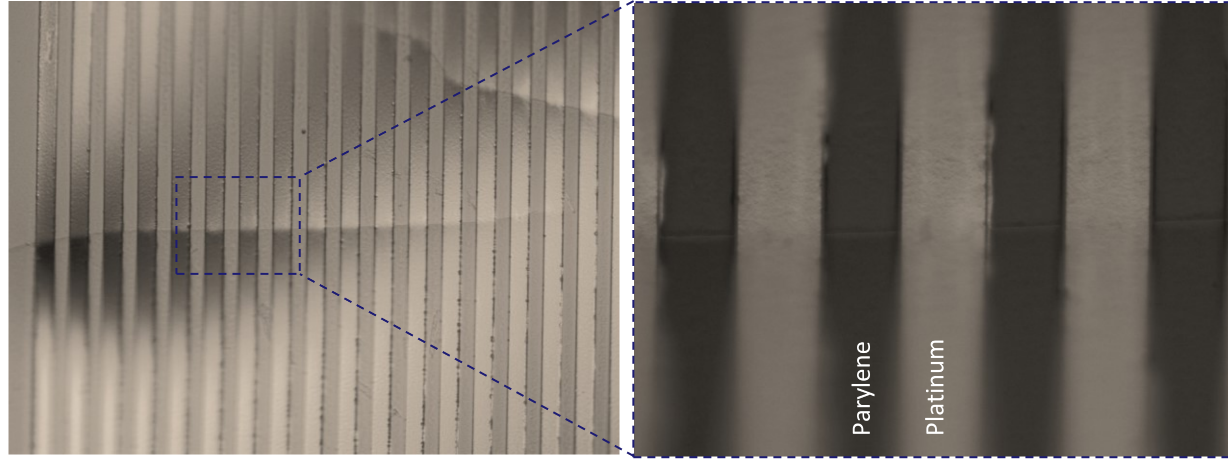

Figure 7.11: The flexible interconnects inspection after the rolling and folding tests. Clear fold in parylene layer. Intact continuity of platinum interconnects.

Even though the electrical performance of the interconnects have not been affected by the fold present in the parylene layer, such permanent device deformation should be avoided. The elastic deformation of the parylene film that probably occurred here might compromise the adhesion between the parylene and the platinum metallization, causing issues with the reliability of the device in the future.

7.7 CONCLUSIONS

The results presented in this chapter show that it is possible to fabricate devices with functional parylene-platinum-based flexible interconnects in a monolithic process using standard microfabrication cleanroom equipment and methods. The scalable process flow closely follows the Flex-to-Rigid process that has been industrialized for smart

catheter application. The newly developed enabling technologies for parylene-based flexible interconnects processing in a cleanroom environment (described in Chapter 6) were successfully incorporated.

Furthermore, it was possible to use a single platinum layer to form all the device structures, and the flexible interconnects without using methods such as wafer transfer, sacrificial layer, or other non-standard fabrication techniques to encapsulate the platinum metallization in the parylene layer.

The electrical conductivity of interconnects is in line with calculated values, and it does not change when the film is subjected to a realistic mechanical strain. The devices could be rolled to a diameter of approximately 1 mm and bend to a radius of 5 µm, meeting the requirements specified for the DBS device (see Chapter 2).

Although a number of test devices have been successfully fabricated, several process issues were identified (e.g., platinum fences, cracking SiO_2 stop layer, or curling of the finished devices. The experience gained during the fabrication of these test devices formed the base for the succeeding device fabrication flow presented in Chapter 8.

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8

CERAMIC-PARYLENE FLEXIBLE INTERCONNECTS *"PARYLENE LAST" APPROACH*[1]

8.1 INTRODUCTION

The long-term reliability of flexible implantable devices is still an interesting research topic in the field of implantable microelectronics. Many have shown that polymer-only (e.g., parylene or polyimide) based encapsulation is not sufficient for neurostimulation probes, whether due to adhesion issues (Section 6.2) or fabrication difficulties (Chapter 7). Current interest is heading towards applying thin ceramic films as an additional barrier material and adhesion promoter between interconnects (e.g., platinum, gold) and the polymer (e.g., parylene) [1][2][3].

In this chapter, a new scalable process for the monolithic fabrication of semi-flexible devices is presented. The goal is to realize flexible interconnects that can be rolled into a diameter of 1.3 mm and bend to approximately 55 µm radius. The parylene based film connects the flexible interconnects with bond pads located on a rigid silicon island, possibly containing prefabricated structures. The new process includes, in addition to parylene, two ceramic materials. A thin stack of SiO_2 and Si_3N_4 layers serves as an additional encapsulation to improve the adhesion of the platinum-titanium-based metallization in the stack. Finally, the parylene layer thickness in this process is increased from 5 µm to 12 µm, which, together with design modifications, ensures the device's robustness during the DRIE silicon etch and during the handling of the final device.

To enable the ceramic encapsulation of the metallization, a novel "parylene last" approach was developed, which ensures a more robust and controlled process. Thanks to the initial encapsulation of interconnects with ceramic layers, it is possible to push the parylene encapsulation steps to the very end of the fabrication process. The absence of the polymer in the early stage of fabrication allows for broader wafer cleaning possibilities, like high-power O_2 plasma. It also significantly increases the process temperature budget from 100°C up to even 400°C.

In this chapter, the flowchart for fabrication of parylene-platinum-based flexible interconnects presented in Chapter 7 is modified so that the ceramic and "parylene-last" encapsulation can be realized in one monolithic flow. The mask design is updated, and some masks are added to aid the "parylene-last" approach. Next, several materials and methods are tested to ensure the readiness of the technology modules necessary for the ceramic-parylene encapsulated device fabrication. Finally, the test device is fabricated, and its mechanical and barrier properties are evaluated in a bending test and by soaking in PBS at 57°C, respectively.

[1] The chapter is partially based on the work of supervised master student D. Wu [27].

In this flow, titanium nitride (TiN) metallization is used. In contrast to the platinum, this layer is available at the EKL facility, where the device fabrication is taking place, and it can be processed in all machines with few restrictions. This allows for a quick feasibility study of the new "parylene last" fabrication approach.

8.2 TEST DEVICE DESIGN

The test device that was presented in Chapter 7 has been updated in this chapter. Similarly, the new device is 3.4 mm wide and 18.4 mm long, and it comprises a comb-meander structure and a set of three electrodes located on a semi-flexible structure (Figure 8.1). In this section, attention is drawn to the changes in the design. For more details regarding the previous device design and its function, see Section 7.2.

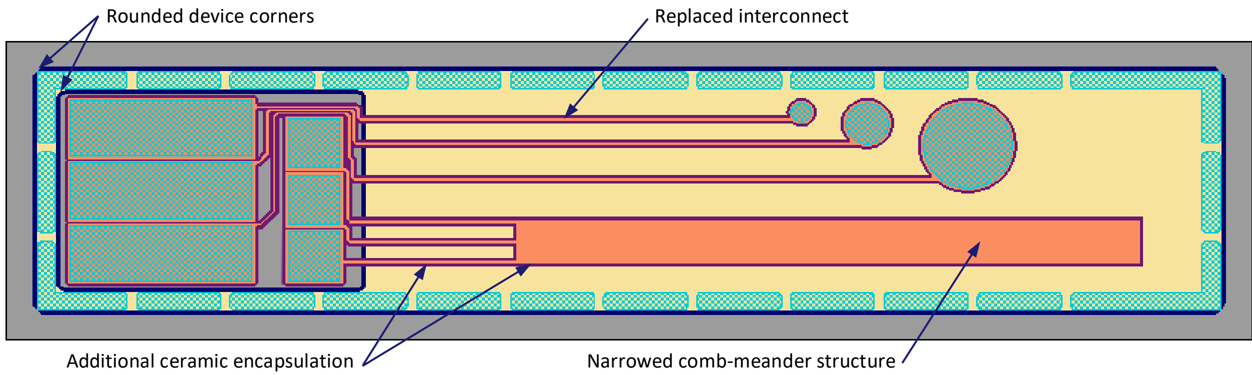


Figure 8.1: The modified test device design comprising rigid silicon island with bond pads and the parylene-platinum-based flexible film containing interconnects and platinum electrodes.

8.2.1 Metallization

The metallization layer still includes three electrodes (with diameters of 350 µm, 700 µm, and 1400 µm), comb-meander structure, interconnects, and bond pads. However, it was modified to minimize device damage during handling that was often occurring in the previous design. First, the 20 µm wide interconnect leading to the smallest electrode is moved away from the flexible-film edge to the distance of 500 µm (previously 375 µm). The position of the interconnects leading to the other two electrodes remained unchanged. Secondly, the comb-meander structure is narrowed to ensure the 500 µm distance from the device's edge (previously 260 µm) and prevent damage to the metallization during device release from the wafer frame. The new comb-meander structure has six instead of eight teethes and loops, and the meander length of approximately 126500 µm (previously 166500 µm). The metallization line width of 20 µm and the pitch of 40 µm, and the size and location of the bond pads remained unchanged.

8.2.2 Ceramic encapsulation

In this chapter, an additional stack of ceramic layers, composed of thin films of SiO_2 and Si_3N_4, is implemented to encapsulate the metallization before the final device encapsulation with parylene is done. The ceramic stack is completely sealing the comb-meander structure and interconnects with the overlay of 50 µm. In the case of the electrodes, only the edges of the structures are sealed. The large area of the electrodes remains open to allow for electrical contact. The structures on the silicon island are completely sealed with ceramic layers, which are re-opened at the bond pads.

8.2.3 Rounded device corners

In the previous process iteration, the flexible film was cracking after the device was released in the DRIE etcher. The cracks were originating at the corners of the device, and they were often progressing through the parylene encapsulation and the metallization layer leading to the device damage. To make the fabrication process more robust, it is essential to prevent cracking of the devices and maintain the top surface of the wafer intact, especially during the backside DRIE release process. To achieve this, the corners of the device have been rounded by modifying the DRIE release mask.

8.3 FABRICATION FLOWCHART - "PARYLENE LAST"

In the previous fabrication process, developed in Chapter 7, the flexible interconnects are encapsulated only in parylene. It was done by depositing the bottom layer of polymer early in the process, then depositing and patterning the metallization directly on top of the first parylene, and finally encapsulating the metallization with the top layer of polymer (Figure 7.4). This method allowed for monolithic fabrication of the device without using wafer transfer techniques. However, the presence of parylene sets the process temperature budget to a maximum of 100°C, and limits the wafer cleaning possibilities.

In the developed in this chapter "parylene last" approach, the parylene deposition has been moved to the very last moment in the fabrication flow – after encapsulating the metallization in the additional stack of ceramic layers. By moving the parylene deposition to a later stage in the fabrication process, it is possible to increase the temperature budget of the fabrication process and permit for the use of more cleaning methods such as high-power O_2 plasma or strong oxidizing solutions. Moreover, by employing the pre-patterned titanium buried mask, used to pattern the top layer of parylene, it is possible to encapsulate in parylene the complete device and not only the metallization.

In this section, the "parylene last" fabrication flowchart developed to realize the ceramic-parylene encapsulated flexible platinum interconnects is presented. The detailed process flowchart that was used in this thesis can be found in Appendix B.

8.3.1 Backside DRIE hardmask and front side etch stop layers

The process flow begins with the deposition of 6 µm PECVD SiO_2 layer on the backside of a 400 µm double side polished wafer. Next, 400 nm PECVD SiO_2 layer is deposited on the front side of the wafer. This layer serves as an insulator between the bond pads and silicon, and as an etch stop layer during the final DRIE process. The SiO_2 layer is thinner than in the previous device iteration (see Section 7.3), 400 nm instead of 2 µm, which should reduce the stress in the layer and prevent cracking of the devices after the DRIE release. At this step, the 6 µm thick PECVD SiO_2 layer is patterned (Figure 8.3a), using the *Backside** mask (Figure 8.4a). This layer is later used as a hardmask during the device release in the backside DRIE process.

The process continues with the deposition and patterning of a 200 nm aluminum etch stop layer on the front side of the wafer (Figure 8.3b) in chlorine-bromine-based plasma using the *Etch Stop* mask (Figure 8.4b). This layer is introduced to protect the ceramic encapsulation from being etched when the 400 µm SiO_2 etch stop layer is removed after DRIE. The aluminum layer can be selectively removed by wet etching at the end of the process.

8.3.2 Ceramic encapsulation and metallization

Next, the stack forming titanium nitride (TiN) metallization encapsulated in a ceramic stack is fabricated (Figure 8.2). The bottom stack of the ceramic encapsulation, composed of 50 nm PECVD Si_3N_4 and 400 nm PECVD SiO_2, is deposited, followed by the deposition of 200 nm of TiN metallization with a 10 nm titanium adhesion layer. The TiN layer is patterned in a chlorine-bromine-based plasma using the *Metallization** mask (Figure 8.4c). The metallization is then encapsulated in the top stack of the ceramic layers composed of 15 nm PECDV Si_3N_4, 400 nm PECVD SiO_2, and 50 nm PECVD Si_3N_4 (Figure 8.3c). The detailed ceramic stack description and deposition methods are described in Section 8.5.3.

Subsequently, the ceramic encapsulation is patterned in a fluorine-based plasma (Figure 8.3d). During this step, vias to electrodes and vias to bond pads are created using the *Encapsulation* mask (Figure 8.4d). In that step, the ceramic stack is also removed from the flexible film areas without the metallization and from the release tabs region around the device.

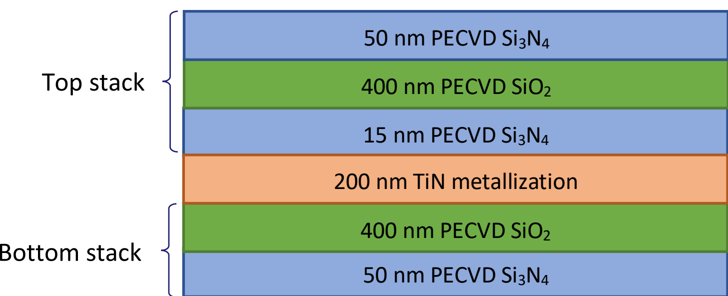


Figure 8.2: The complete stack forming the TiN metallization encapsulated in SiO_2 and Si_3N_4 layers.

8.3.3 Front-side parylene layer and buried titanium hardmask

The 6 µm thick front-side layer of parylene is deposited on both sides of the wafer with the use of the A-174 primer (Figure 8.3e). In this process flow, a 6 µm thick layer of Parylene is used, in contrast to the 2.5 µm parylene layer used in the previous flow (see Section 7.3), to ensure the device's robustness and prevent its failure, especially during manual handling. Subsequently, the parylene is removed from the backside of the wafer using an O_2-based directional plasma. Next, 200 nm thick titanium hardmask is sputter deposited on the front side of the wafer at 25°C, and patterned in a chlorine-fluorine-based plasma (Figure 8.3f) using the *Contact to Bond Pad/Parylene Patterning* mask (Figure 8.4e).

8.3.4 Backside DRIE etch and etch stop layers removal

At this point, the wafer is flipped, and the 400 µm of silicon is DRIE etched from the backside using the pre-patterned 6 µm SiO_2 hardmask and landing on the 400 nm thick silicon dioxide etch stop layer (Figure 8.3g). The rounded corners of the device and the thicker parylene film prevent the membranes from cracking and folding after the DIRE etch. At this point, the flexible film is not patterned yet, and it forms an intact layer that prevents helium leakage from the cryo-chuck during the DRIE process. The devices are suspended in the wafer through a flexible film composed of parylene and the two etch stop layers that are still present on the wafer: SiO_2 and aluminum. The 400 nm thick SiO_2 etch stop layer is now removed in fluorine-based plasma, and subsequently, the 200 nm thick aluminum etch stop layer is wet etched in PES (phosphate-buffered saline) etchant (Figure 8.3h). The bottom part of the ceramic encapsulation is now exposed and ready for the second parylene layer deposition.

8.3.5 Backside parylene deposition and parylene encapsulation patterning

The 6 µm thick backside parylene layer deposition is performed to complete the device encapsulation in a conformal parylene film (Figure 8.3i). This layer has buried the pre-parented titanium hardmask present on the front side of the wafer. At this point, the parylene on the front side of the wafer is etched in a single O_2 plasma-based RIE process. In this step, the 6 µm of parylene is removed from the front side of the wafer, exposing the pre-patterned titanium hardmask that acts as a etch stop layer. Simultaneously, the 6 µm thick front-side parylene layer is patterned using the hardmask to open the bond pads, electrodes and to form the release tabs around the device (Figure 8.3j). Finally, the titanium buried hardmask is removed by submerging the wafer in an ammonia-peroxide-based etchant (Figure 8.3k).

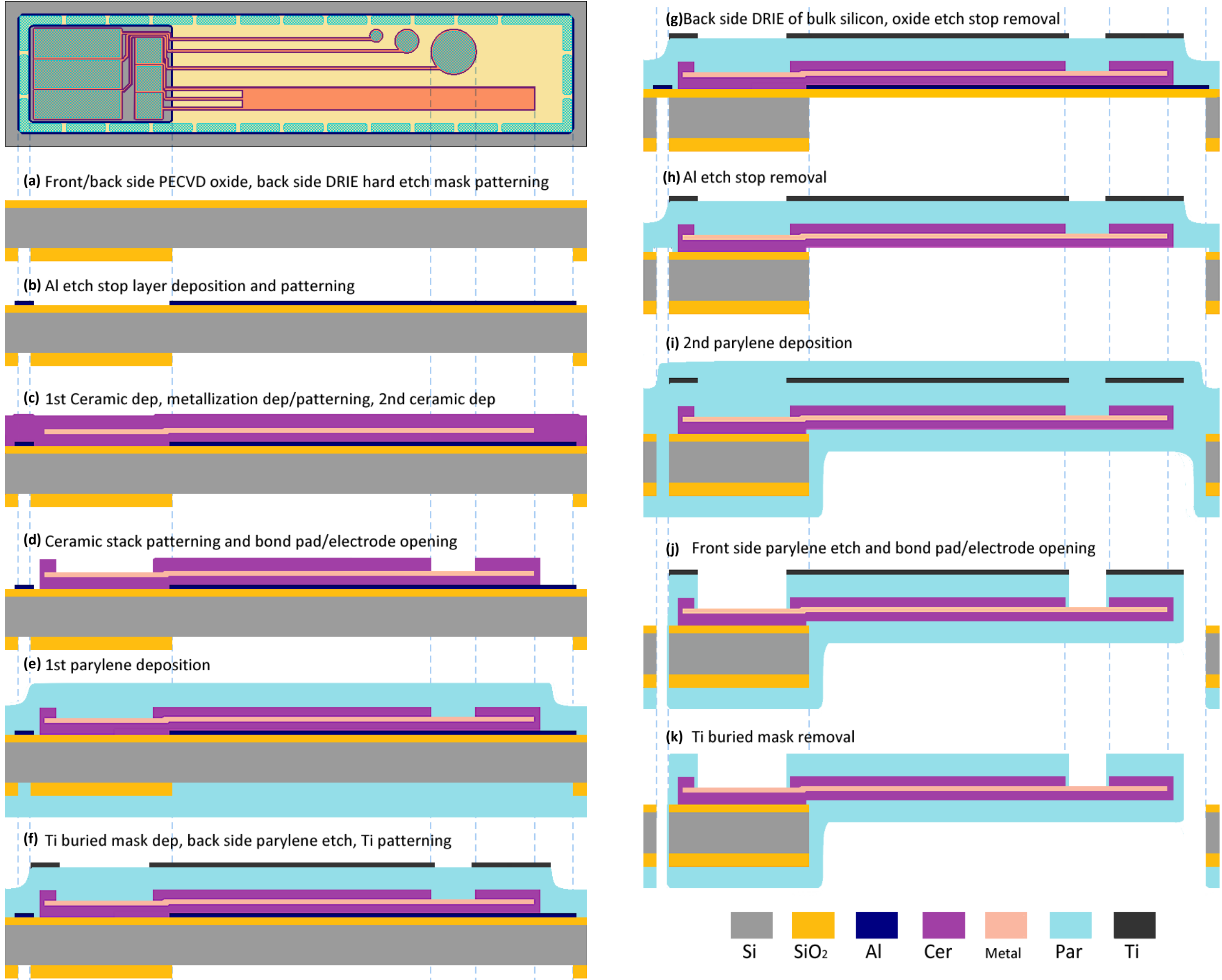


Figure 8.3: The process flow for the fabrication of F2R-based test devices with ceramic-parylene encapsulated flexible interconnects and flexible platinum electrodes using the "parylene last" approach.

After the "parylene last" fabrication process is complete, the devices are suspended in wafers by means of parylene-based release tabs. Each device is completely encapsulated in a conformal 6 µm thick layer of parylene on both sides. The metallization lies in a neutral plane and is additionally encapsulated in a stack of ceramic layers. The titanium nitride bond pads and electrodes are open, allowing for electrical contact.

8.4 MASK DESIGN

To facilitate the ceramic encapsulation of the metallization and execute the "parylene last" approach, a set of four new masks is prepared and completed by one mask reused from the previous design. The new mask set implements the device design updates described earlier in this chapter. Similar to the previous design, the four new masks are placed on one multi-image reticle. The masks used in the "parylene last" fabrication flow are described below:

- *Backside* (modified)* mask is used to pattern the 6 µm thick SiO_2 hardmask through which the semi-flexible device is released in the final silicon DRIE etch (Figure 8.4a). The etching is performed from the backside of the wafer, landing on a SiO_2 etch stop layer. This mask has been modified by rounding off the corners of the release area to prevent cracks in the membrane after the silicon etching process is finished.
- *Etch Stop (new)* mask is used to pre-pattern an etch stop layer (aluminum), which protects the ceramic encapsulation during the removal of the SiO_2 etch stop layer used in the DRIE process (Figure 8.4b). The mask follows the *Backside** mask contour, with an overlay of 20 µm which allows for its complete removal after the SiO_2 etch top layer is removed.
- *Metallization* (modified)* mask is used to pattern the single layer of titanium nitride metallization that forms electrodes, interconnects, and bond pads (Figure 8.4c). In comparison to the previous design iteration, the structures on this mask are moved further away from the edge of the device to prevent their damage during handling. To facilitate this, two loops of the comb-meander structure are removed.
- *Encapsulation (new)* mask is used to pattern the ceramic layers that are encapsulating the metallization (Figure 8.4d). The ceramics is exclusive to the device area. It is removed from the release tabs area around the device, and it is opened at the electrodes and the bond pads location.
- *Contact to Bond Pad/Parylene Patterning (old)* mask is now employed to pre-pattern the hardmask (titanium) used to pattern the parylene layer at the very end of the fabrication process (Figure 8.4e). The two-purpose hardmask is deposited on the front-side parylene layer and later buried under the backside parylene layer.

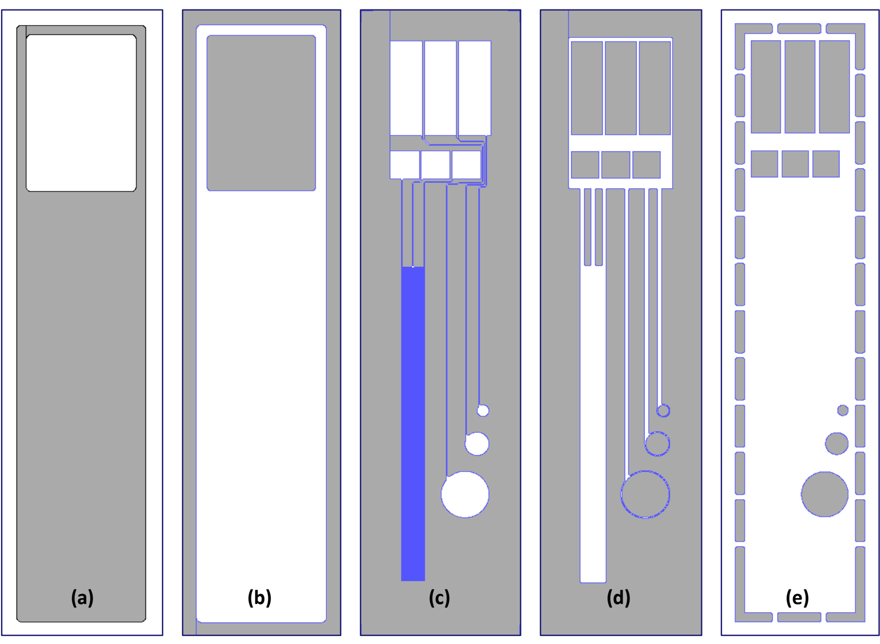


Figure 8.4: The single reticle with four images used to fabricate the test device in the "parylene last" approach. (a) Backside. (b) Etch stop. (c) Metallization*. (d) Encapsulation. (e) Contact to Bond pad/Parylene Patterning.*

8.5 TECHNOLOGY MODULES

Several short-loop experiments have been carried to pre-evaluate the feasibility of the "parylene last" approach presented in this chapter regarding the aluminum etch stop layer, titanium nitride metallization, and ceramic encapsulation. As a result, a number of enabling technology modules compatible with the processing of parylene-based semi-flexible devices have been established. The key points of the developed technology modules are summarized in this section.

8.5.1 Aluminum etch stop layer

The aluminum etch stop layer is introduced in this process to protect the ceramic encapsulation during the removal of the SiO_2 etch stop layer after the DRIE etch of silicon from the backside of the wafer. The layer is deposited and patterned before the ceramic encapsulation process starts, and it is later removed in PES after the SiO_2 etch stop layer has been dry-etched (see Figure 8.3).

For this experiment aluminum has been chosen as a masking material because it can be removed in PES selectively towards exposed materials present in the device, such as the titanium buried hardmask, and it is accessible at the research facility. The available deposition recipes have been evaluated in short-loop experiments. The goal was to select the layer that is pinhole-free, and at the same time, it is as thin as possible to lower the intrinsic stress within the layer and allow for efficient aluminum etch stop removal in PES at the end of the fabrication process.

Deposition parameters

Among available in the Trikon Sigma 204 sputter deposition tool recipes for aluminum deposition, five have been selected and evaluated (Table 8.1). Besides layer thickness variation from 60 nm to 250 nm, the deposition temperature, varying from 25°C to 350°C, was also taken into account. Lower deposition temperature results in smaller grain sizes, and therefore a tighter layer [4][5]. Although other sputter deposition parameters such as power or pressure can influence the layer properties, in case of the selected recipes, they have a much lower impact on the pinhole formation than the other two factors [5].

Table 8.1: Aluminum stop layer deposition parameters and layer evaluation results.

Recipe #	Layer thickness [nm]	Deposition temperature [°C]	Results
1	60	25	Rare defects ~1 μm diameter
2	100	350	Many defects ~400 nm diameter, porous
3	200	25	No defects
4	200	300	No defects
5	250	50	No defects

Samples preparation and evaluation

These five aluminum layers were deposited on wafers with 400 nm thick SiO_2 layer. Subsequently, the wafers were subjected to a fluorine-based direction plasma that is commonly used to etch SiO_2 in a RIE process. The etching was approximately 8 times longer than theoretically required to remove the etch stop layer for the backside DRIE process. This allows for inducing visible defects in the SiO_2 layer etched through the

potential pinholes present in the aluminum layer. Subsequently, the aluminum layer was removed in PES, and the surface of the silicon dioxide layer was inspected in SEM. The results are collected in Table 8.1 and presented in Figure 8.5.

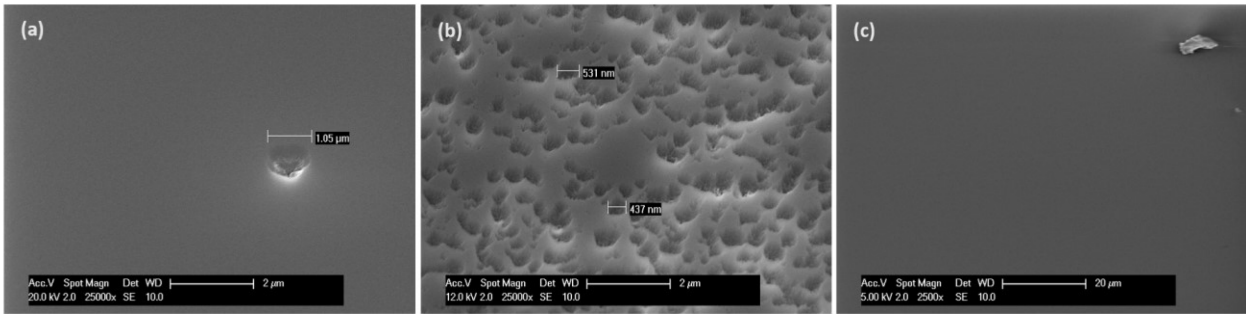


Figure 8.5: SEM images of inspected silicon dioxide layers exposed to fluorine-based plasma through aluminum etch stop layer. (a) The 60 nm aluminum layer deposited at 25°C. Visible single defect. (b) The 100 nm aluminum layer deposited at 350°C. Visible numerous defects. (c) The 200 nm aluminum deposited at 25°C. No visible defects due to exposure to plasma.

Results and conclusions

The 60 nm and 100 nm thick layers of aluminum both have pinholes causing visible defects in the SiO_2 layer underneath the metal mask (Figure 8.5a,b). All the 200 nm and thicker aluminum layers are free of pinholes, and no defects are visible on the silicon dioxide layer (Figure 8.5c). This is regardless of the deposition temperatures of 25°C, 50°C, or 300°C.

The 200 nm thick aluminum layer deposited at 300°C is selected to protect the ceramic layers in the final process flow. This layer is thin enough to be quickly etched in PES, and it is free of pinholes regardless of the elevated deposition temperature. The layer deposited at 300°C is chosen over the layer deposited at 25°C to minimize the effects of potentially unfavorable transformation that can happen during the aluminum annealing in the next step of Si_3N_4 deposition at 400°C.

8.5.2 Titanium nitride metallization

The goal of this chapter is to test the feasibility of the "parylene last" fabrication flow that includes the additional ceramic encapsulation stack of the parylene-based flexible interconnects. For a more straightforward execution of that goal, the fabrication process of the test devices has been modified by exchanging the metallization material from platinum to available in-the-house titanium nitride (TiN). Besides availability, the TiN layer can be processed in a broader range of EKL equipment without contamination-related restrictions.

The TiN is an interesting material, alternative to platinum, for metallization and electrodes of implantable stimulation devices [6][7]. Depending on the layer composition, the bulk TiN can be tuned to have fair electrical properties with the resistivity of approximately 20 µΩ·cm at 20°C [8] (resistivity of platinum is about 10.5 µΩ·cm).

Deposition parameters and layer evaluation

The goal of the short-loop was to find the layer with the lowest resistance and lowest stress to form the flexible interconnect metallization. The low resistance ensures that thin films of metallization can provide sufficient stimulating current while remaining flexible enough to withstand strains in the flexible interconnect. The low stress ensures the mechanical stability of the device and reduces the risk of bulging or curling of the

devices after release. In theory, the lower the sputtering power and N_2 concentration, the more conductive the layer [9].

Three 200 nm thick TiN layers were deposited using recipes with varied deposition power and reactive gases (argon and nitrogen) composition and investigated (Table 8.2). The 10 nm thick titanium adhesion layer and 200 nm thick TiN metallization was sputter deposited at a temperature of 350°C on a wafer with 400 nm of SiO_2 structural layer. The sheet resistance was then measured using a 4-point-probe station CDE ResMap, and the stress was measured using the Flexus 2320-S tool. The stress of the deposited layers was determined by acquiring and comparing the bow and curve information of the wafers from before and after the TiN deposition.

Table 8.2: Titanium nitride deposition parameters and layer evaluation results.

Recipe #	Deposition parameters				Measurements	
	Thickness [nm]	**Ar [%]**	**N_2 [%]**	**Power [kW]**	**Sheet resistance [Ω/square]**	**Stress [MPa]**
1	200	20	70	6	16.41 ± 0.21	212
2	200	20	70	1	84.36 ± 1.42	213
3	200	54	36	6	2.67 ± 0.23	517

Results and conclusions

The sheet resistance and the stress measurement results are collected in Table 8.2. As expected, the layer deposited with the lowest nitrogen concentration of 36% showed the lowest sheet resistance of 2.67 Ω/square. However, this layer has over two times higher stress than the other two layers. The layers that were deposited using N_2 concentration of 70% and showed similar stress of around 200 MPa. However, only the layer deposited at 6 kW has a reasonably low sheet resistance of 16.41 Ω/square. Therefore, it is selected to form the flexible interconnects in this iteration of the device.

8.5.3 Ceramic encapsulation

According to recent publications, the encapsulation of platinum interconnects only in a layer of parylene is not sufficient for long-term implantable devices because it is permeable to moisture [10]. Therefore, in this chapter, the method for flexible metal tracks encapsulation first in thin ceramic layers and then in a flexible parylene layer is investigated. Thin ceramic layers such as SiO_2 and Si_3N_4 can show pseudo-flexible behavior for layer thicknesses below 1 µm [11]. Moreover, ceramic layers such as SiO_2 and Si_3N_4 are known to be pretty resistant to moisture and bodily fluids [12][13], providing an extra barrier to implant encapsulation. The thin ceramic layers of different types (e.g., Si_3N_4 and SiO_2) can be deposited alternately to prevent the moisture from penetrating through pinholes often present in thin, single layer films [5][14]. In addition, the ceramic layers can also serve as an adhesion layer for metallization. The metals common in the IC field, such as aluminum or titanium, tend to have excellent adhesion to ceramics [15][16]. Furthermore, there are many methods available that can potentially ensure excellent adhesion between parylene and ceramics [17].

The short-loop experiments summarized in this section aimed to test the ceramic materials and the feasibility of the ceramic stack fabrication process. The metallization and parylene depositions are omitted to ease the characterization of the individual ceramic layers and their stacks.

Stack properties

To provide additional ceramic-based encapsulation for the platinum-based flexible interconnects in the "parylene last" approach, a stack composed of thin SiO_2 and Si_3N_4 layers was proposed. The layers forming the multilayer stack, their arrangement, and thicknesses, are based on the knowledge and experience of the project partner Medtronic [14]. The bottom part of the stack, lying beneath the metallization, comprises 50 nm PECVD Si_3N_4 and 400 nm PECVD SiO_2. The top part of the stack, deposited on top of the metallization, comprises 15 nm PECDV Si_3N_4, 400 nm PECVD SiO_2, and 50 nm PECVD Si_3N_4. In the final flow, the complete device with flexible interconnects is subsequently encapsulated in parylene (Figure 8.6).

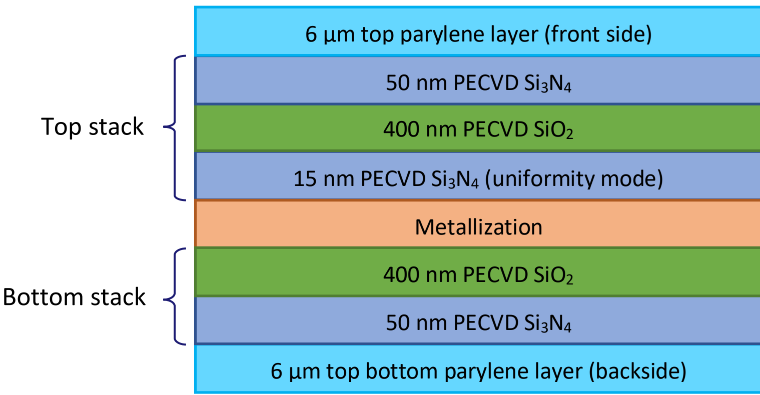


Figure 8.6: The complete flexible interconnect stack realized within the "parylene last" approach. The metallization is encapsulated in alternating thin SiO_2 and Si_3N_4 layers and in a thick parylene layer.

In the stack, the alternating SiO_2 and Si_3N_4 deposition prevent the formation of pinholes that can occur in one of the thin layers from penetrating throughout the complete stack. The optimized thicknesses of each ceramic layer ensure good barrier properties and maintain the flexibility of the complete stack [14]. The first (from the bottom) 50 nm PECVD Si_3N_4 layer forms the first barrier to moisture and chemicals, and it also serves as an adhesion layer for the parylene [18]. The 400 nm thick PECVD SiO_2 layer forms the main barrier to moisture in the stack, and it has a good affinity to the titanium adhesion layer of the metallization. The next layer in the ceramic stack, a 15 nm PECVD Si_3N_4 adhesion layer that belongs to the top stack, is deposited directly on top of the metallization. The Si_3N_4 adheres slightly better to the platinum metallization than the SiO_2 [14][16]. The subsequently deposited layers of 400 nm PECVD SiO_2 and 50 nm PECVD Si_3N_4 form the barrier against moisture and chemicals on the top part of the stack. The layers thicknesses correspond with the analogous layers present in the bottom stack, which ensure that the metallization lies as close as possible to the neutral plane of the flexible interconnect.

Deposition parameters and stack evaluation

All the ceramic layers were deposited on 525 µm silicon substrates at 400°C using the Novellus Concept One PECVD deposition tool. The 15 nm Si_3N_4 layer was deposited using the so-called "uniformity mode". The deposition was performed using recipes available in the tool, selected so that the tensile and compressive stress in individual layers does not exceed 100 MPa or −100 MPa, respectively, and the complete stack stress stays within 0 MPa to maximum 100 MPa (tensile). This is because even the slightest compressive stress in the ceramic encapsulation might compromise the adhesion in the complete interconnects stack [19], and too high tensile stress might lead to device curling and tearing after flexible film release.

The stress in the individual thin-film SiO_2 and Si_3N_4 layers and in the complete ceramic stacks was measured using the FLX 2320-S tool at room temperature. The average stress measurement results are collected in Table 8.3, where positive values indicate tensile stress and negative values indicate compressive stress.

Table 8.3: The results of stress measurements of thin ceramic layers and the ceramic stacks used to encapsulate the metallization in the "parylene last" fabrication flow.

Layer/Stack	Stress [MPa]
15 nm Si_3N_4	−54
50 nm Si_3N_4	−45
400 nm SiO_2	19
50 nm Si_3N_4 400 nm SiO_2 15 nm Si_3N_4	24
400 nm SiO_2 50 nm Si_3N_4	9
50 nm Si_3N_4 400 nm SiO_2 15 nm Si_3N_4 400 nm SiO_2 50 nm Si_3N_4	27

Results and conclusions

Both of the single Si_3N_4 layers showed significant compressive stress. It reached close to 50 MPa. The 400 nm thick SiO_2 layer was clearly in the tensile region, and its initial stress was approximately 20 MPa. Despite the relatively high compressive stress noted for the single Si_3N_4 layers, the average stress of 24 MPa in the top stack, 9 MPa in the bottom stack, and 27 MPa in the complete stack were low and in the preferred tensile region. The compressive stress in the thin Si_3N_4 layers was compensated with the thicker SiO_2 layers present in the stacks, ensuring good adhesion between the interfaces and preventing device deformation after release.

8.6 DEVICE FABRICATION

The semi-flexible devices were successfully fabricated, showing the feasibility of the "parylene last" process and the developed technology modules. After the process, the devices reminded suspended in the wafer by means of parylene tabs (Figure 8.7). The flexible TiN interconnects are encapsulated in a stack of thin ceramic layers, and the complete semi-flexible device is encapsulated in a layer of parylene.

It was possible to complete the "parylene last" fabrication flow for ceramic-parylene encapsulated devices. The wafers remained intact through the backside DRIE release of the flexible film, and no broken devices or cracks in the ceramic layer were observed, neither in the device area itself nor along the edge of the device. This is most probably thanks to the modified rounded device design and the application of a thicker parylene layer. Furthermore, the completed devices can be safely cut out of the wafer frame, and they do not curl or fold after their release (Figure 8.8).

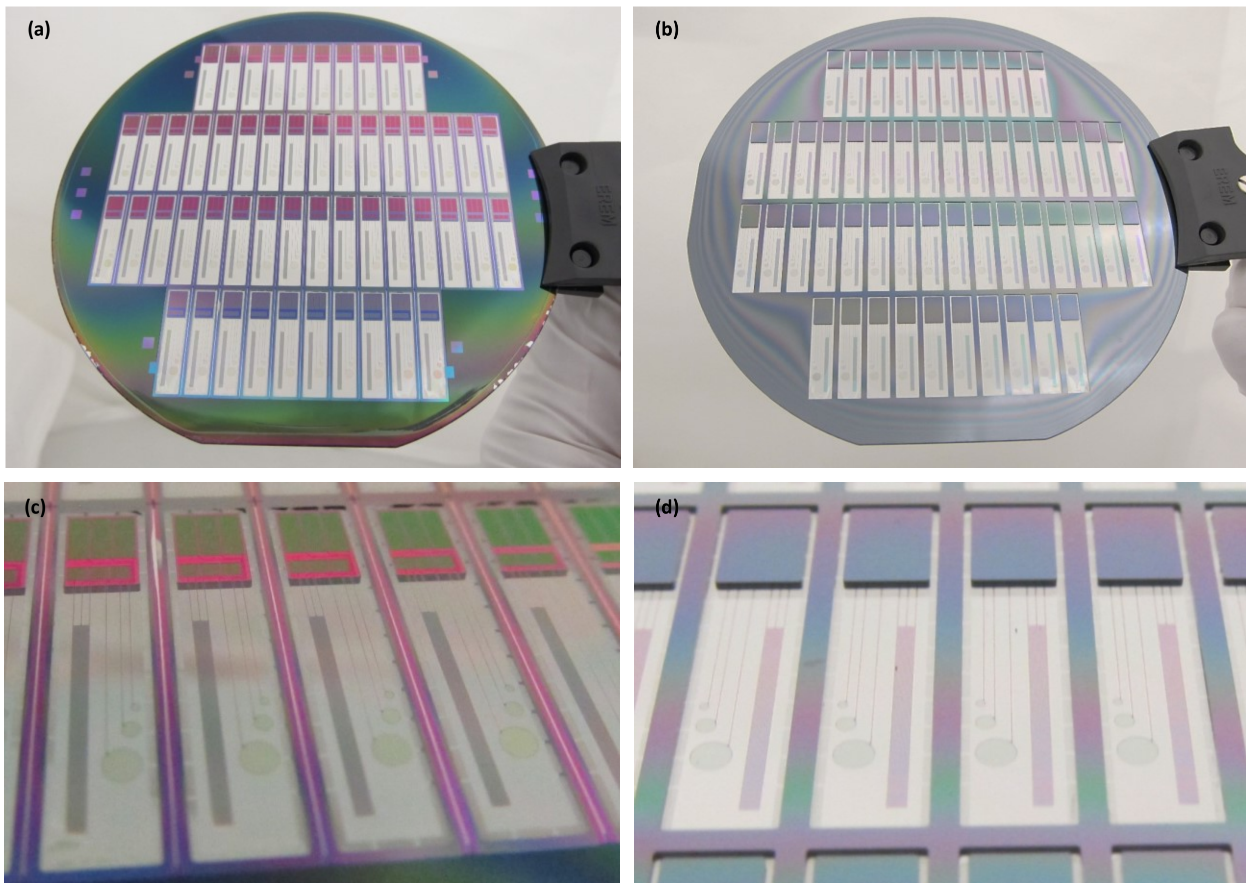


Figure 8.7: Complete wafer with semi-flexible devices fabricated using the "parylene last" process. (a) Front side of the wafer. (b) Backside of the wafer. (c) Zoom-in (front side). (d) Zoom-in (backside).

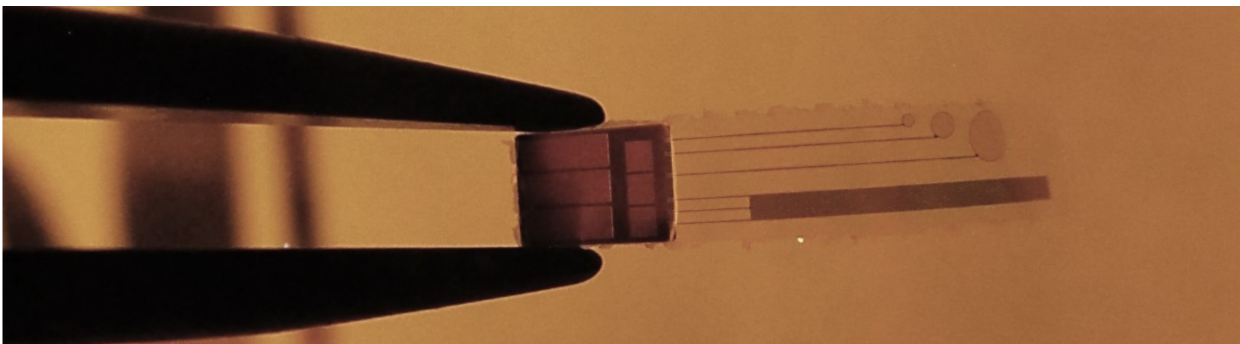


Figure 8.8: A release test device encapsulated in 6 µm of parylene, containing TiN interconnects encapsulated in SiO_2 and Si_3N_4 based ceramic layers stack.

The technology modules developed for the "parylene last" approach were successfully incorporated into the fabrication process without major difficulties. The process steps that require improvement are enclosed in the remainder of this section.

8.6.1 Aluminum etch stop layer

The aluminum etch stop layer, introduced in the "parylene last" process, performed well in protecting the ceramic encapsulation during the dry etching of the SiO_2 etch stop layer. No pinholes or other defects were observed in the ceramic stack after wet aluminum removal in PES. At first, it seemed like the aluminum was removed entirely. However, later in the process, when the titanium mask was removed from the front side of the wafer, aluminum etch stop layer residues were revealed around the edges of the rigid silicon island (Figure 8.9).

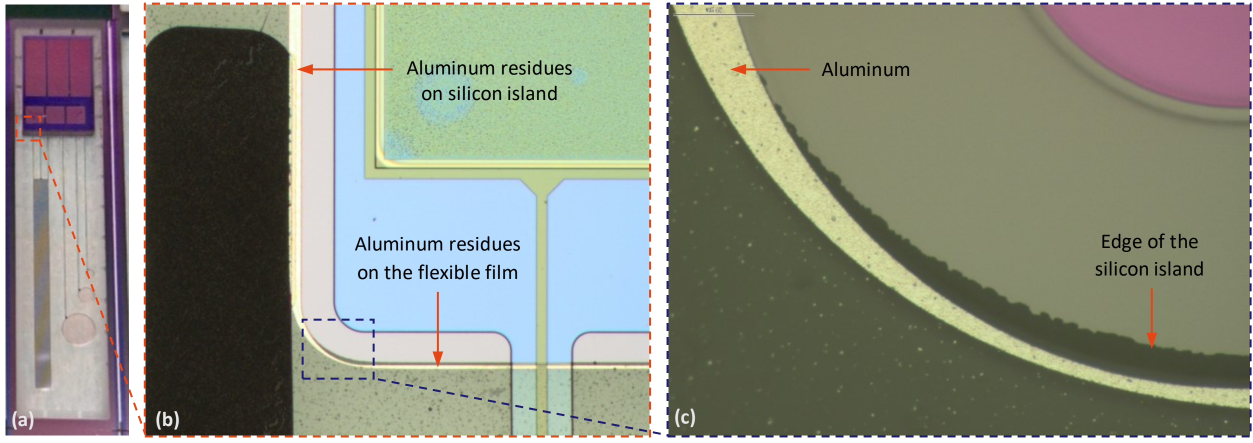


Figure 8.9. (a) The front side of a finished device. Inspected region is marked. (b) Image of the device with aluminum etch stop layer residues on the silicon island and on the flexible film. (c) Zoom-in image.

Upon careful inspection, it was discovered that the aluminum residues occurred in two device regions. On the silicon island, buried under the flexible film, and on the flexible film where silicon was removed during the backside DRIE etch (Figure 8.9b,c).

The aluminum residues on the silicon island could not be etched during significant layer overetch in PES. It seems that the layer overlay of 20 µm is too large or that the typically observed and taken into account 1.5-degree negative slope of the silicon structure is not reproducible. To fix this issue, optimization of the design and the DRIE process is required.

The reason for the etch stop layer residues present on the flexible film is not straightforward as in this region aluminum is not covered with the silicon. Looking at the smooth edge of the remaining aluminum layer, and its profile corresponding with the mask design, it has been concluded that aluminum is not exposed during wet etching. It is possible that the SiO_2 etch stop layer was not completely etched in the directional RIE process because the top of the negatively-sloped silicon island was blocking the plasma (Figure 8.10a,b). Consequently, the remaining SiO_2 layer was masking the aluminum layer during the wet etch process (Figure 8.10c).

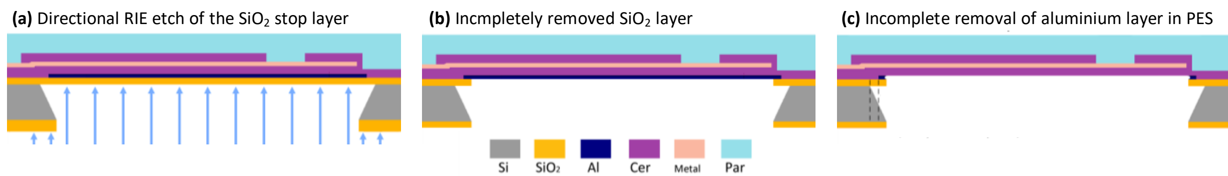


Figure 8.10: The mechanism of aluminum etch stop layer residues formation on the flexible film.

To prevent the aluminum etch stop layer residues on the flexible film, it is advisable to optimize the silicon etch process. The straight slope profile would allow for complete removal of the SiO_2 etch stop layer in an anisotropic RIE process and subsequent complete removal of the exposed aluminum etch stop layer in PES.

8.6.2 TiN metallization

After the fabrication process is finished, the devices with open bond pads and electrodes are suspended in the silicon wafer frame. Figure 8.11a shows the finished device using the backlight. The encapsulated in ceramics and suspended in parylene film comb-meander structure can be seen in Figure 8.11b.

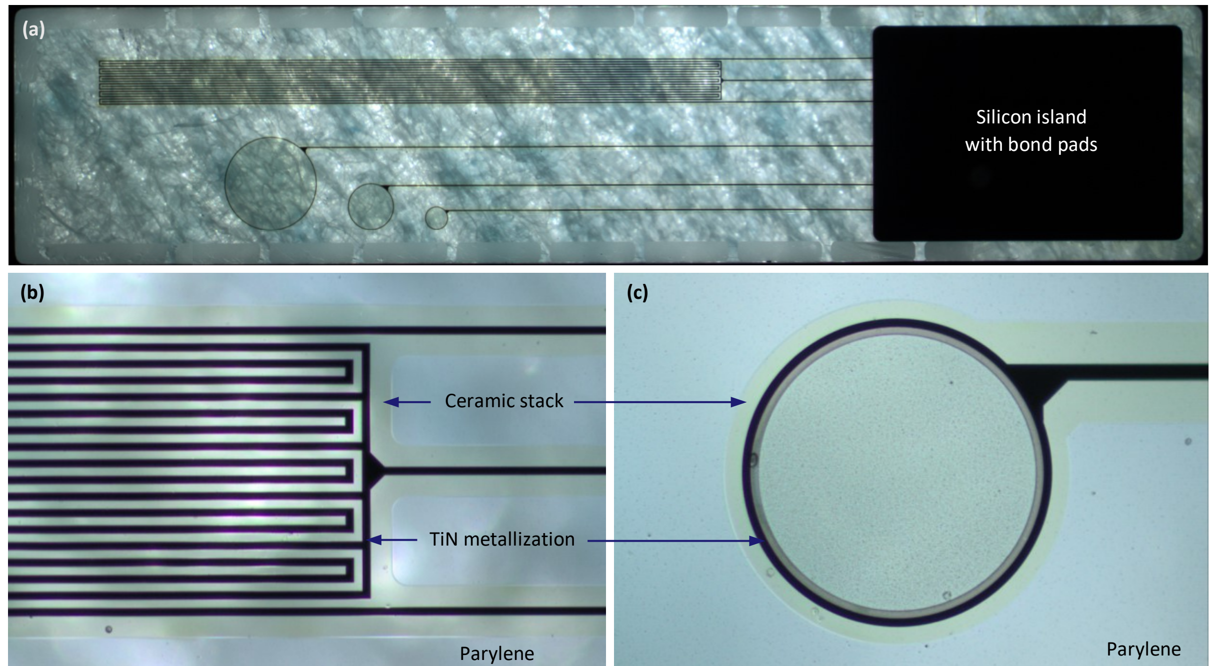


Figure 8.11: (a) Complete test device encapsulated in 6 µm of parylene, containing TiN metallization encapsulated in SiO_2 and Si_3N_4 based ceramic layers stack. (b) The comb-meander structure with visible ceramic encapsulation. (c) The TiN electrode structure. The exposed titanium nitride is removed.

The titanium nitride metallization layer is present on the open bond pads located on the silicon island. This has been demonstrated by making electrical contact on bond pads and through the closed meander circuit. All bond pads located on the silicon island and the meander structure were conductive. However, the open TiN metallization of the electrodes, located on the flexible film, looks transparent (Figure 8.11c), suggesting that the layer has probably been etched away during one of the fabrication steps. It was also not possible to make electrical contact between any of the bond pads and electrodes.

The electrodes and the bond pads went through the same fabrication process. Moreover, on a control wafer that underwent the same fabrication process, except for the silicon etch from the backside, all the structures were conductive, including the electrodes. Therefore, it was concluded that the loss of TiN from open electrodes is linked to substrate flexibility. The TiN can be slowly etched in O_2 plasma [20], and the process can be enhanced by raised substrate temperature. The metallization of the electrodes was most probably etched away during the 45 minutes long parylene etch performed at the end of the fabrication when the electrodes and bond pads are already open. The process was enhanced by insufficient cooling of the suspended in the wafer flexible film. In contrast to the electrodes, the bond pads are located on the silicon island with direct contact to the cooling chuck. In this way, the TiN etch rate can be slower and insufficient to remove the metallization from the bond pads.

8.6.3 Parylene encapsulation

After completing the “parylene last” fabrication process, some wrinkling of the flexible film was observed in devices that were positioned at the edge of the wafer (Figure 8.12). The two sides of the encapsulation stacks were pulled apart with tweezers and inspected with an optical microscope (Figure 8.13). Upon closer inspection, it was found that in the affected devices the top and bottom encapsulation stacks are delaminating from each other. All the structures, including the ceramic encapsulation and the TiN metallization, adhered well to the top parylene layer (Figure 8.13a) but has peeled off

from the bottom parylene layer (Figure 8.13b). The top parylene layer was deposited on the front side of the wafer right after the ceramic layer patterning, whereas the bottom parylene layer was deposited only after the DRIE release of the flexible film and removal of the SiO_2 and aluminum etch stop layers.

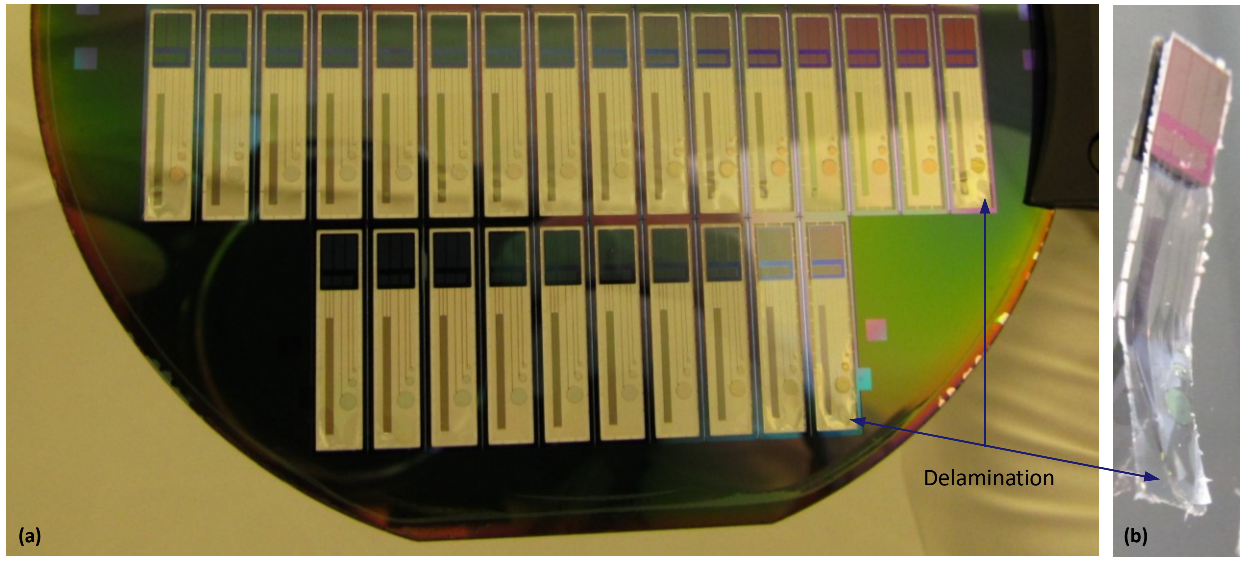


Figure 8.12: Parylene encapsulation delamination on the devices located at the edges of the wafer. (a) Affected devices in a wafer frame. (b) Released device with delaminating parylene layers.

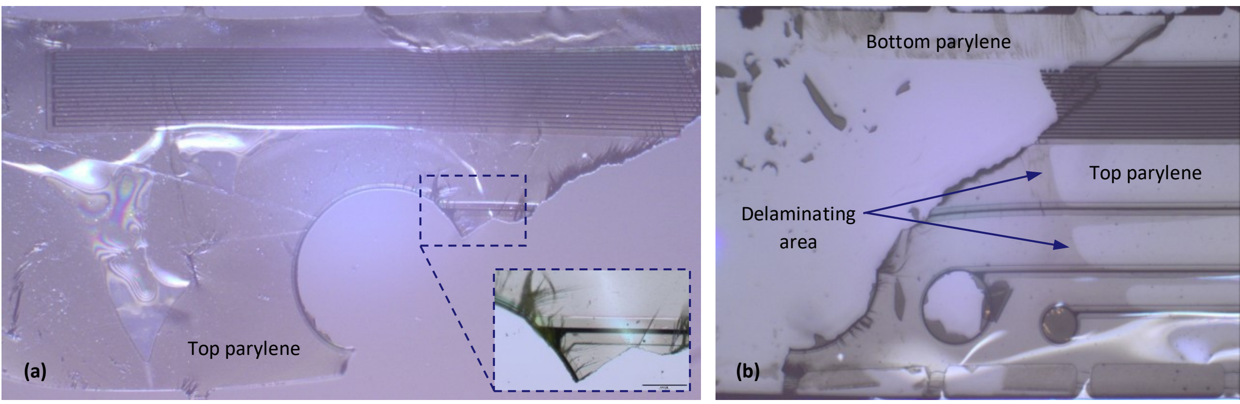


Figure 8.13: Device after peeling delaminating parylene encapsulation layers. (a) The top part of the flexible film with metallization and ceramic encapsulation. (b) Partially peeled top part of the flexible interconnects from the bottom parylene layer.

The adhesion of the bottom parylene layer to the rest of the stack seems impaired only for devices located at the edge of the wafer. In contrast, the devices in the center of the wafer do not show delamination issues. The local adhesion problems can be caused by process steps that show non-uniformity across the wafer and could modify the surface of the wafer before the second parylene deposition. These could happen during the DRIE etch of the silicon, RIE etch of the SiO_2, or the directional O_2 plasma treatment applied before bottom parylene deposition. However, the first two processes do not affect the flexible film directly as it is still protected by the etch stop layers.

Therefore, the most likely reason for the issues with the adhesion of the bottom parylene to the rest of the stack is the directional O_2 plasma treatment that has been performed right before the bottom parylene deposition to clean the flexible film with exposed parylene and Si_3N_4 layers. The O_2 plasma was used to clean the ceramic surface from possible organic contamination that can impair the adhesion and lead to an early device

failure during reliability tests. However, the O_2 plasma treatment can also impair the parylene-to-parylene adhesion [18] by modifying the stack surface to hydrophobic, thereby hindering the working of the A-174 primer that was designed to have a strong affinity to the hydrophilic surfaces.

8.6.4 Conclusions

This section shows the feasibility of the "parylene last" process for the fabrication of semi-flexible devices with flexible interconnects encapsulated in ceramic and parylene. The process allows for significant freedom in designing devices composed of flexible film and rigid silicon islands with crossing-over interconnects. Thanks to the initial metallization encapsulation in ceramics and only later in parylene, the fabrication process became more robust, allowing for a higher temperature budget and more effective cleaning methods. Moreover, in this approach, the complete device and not just interconnects, is encapsulated in parylene. This is achieved by the bottom parylene deposition and contact opening that occurs only after the device release in the DRIE process. The technology modules, developed for the "parylene last" approach, were successfully incorporated into the fabrication process without major difficulties.

Thanks to the application of the alternative TiN metallization in this flowchart, and using the updated rounded design, the feasibility of the "parylene last" process and its compatibility with standard microfabrication tools and techniques have been demonstrated. It was possible to release the devices without cracks or breaks in the wafer surface.

Recommendations

The aluminum etch stop layer has served its purpose in protecting the ceramic layer while etching of the SiO_2 stop layer in the RIE etcher. However, it was not possible to entirely remove the part of the layer covered with the SiO_2. This issue can be solved by adopting the overlay of the aluminum stop layer mask design and by optimizing the silicon etch DRIE process in order to achieve a straight silicon island profile.

The TiN flexible interconnects embedded in the ceramic-parylene-based film were successfully fabricated, resulting in functional metallization and comb-meander structure. However, the exposed metallization on the electrodes was completely removed due to a bad cooling of the flexible film during the O_2 plasma etching of the parylene. These issues emerge from the fact that the fabrication flow used in this chapter has initially been prepared for devices with platinum metallization that is not affected by long O_2 plasma etching. In case if the study should continue using TiN metallization, a flowchart revision is necessary.

The locally observed delamination of the bottom parylene from the rest of the stack was most probably related to the directional O_2 plasma treatment applied to the backside of the wafer right before bottom parylene deposition. An alternative cleaning method involving organic solvents such as acetone or isopropanol spin-cleaning can be applied to overcome this problem in the future.

8.7 DEVICE EVALUATION

The fabricated test devices have been evaluated using the comb-meander structure. First, the electrical and mechanical performance of the ceramic-parylene-based flexible interconnects is assessed using the closed meander circuit. Then, the barrier properties of the ceramic-parylene based encapsulation are evaluated in a body-like solution using the comb and the meander structure that form an open circuit.

The electrodes on the fabricated devices could not be electrochemically characterized because the electrodes have been damaged during the "parylene last" fabrication process, which turned out not to be suitable for the titanium nitride metallization.

8.7.1 Ceramic-parylene-based flexible interconnects

The performance of the flexible interconnects is evaluated in two tests. First, the resistance of the meander is measured right after the devices are released from the wafer. This test is performed to check if the TiN bond pads are properly open and whether the encapsulated interconnects are complete and conductive. Next, the devices are subjected to a bending test. In this test, the flexibility of the ceramic-parylene encapsulated interconnects is assessed.

Resistance of the meander

The resistance of the flexible TiN-based interconnects, encapsulated in ceramic layers and parylene layer, was measured on the meander structure using the Cascade Microtech probe station. Three groups of 5 devices were measured. The measurement results are collected in Table 8.4. All the tested devices were conductive, and the resistance of the meander was in the range from 174 kΩ to 190 kΩ, which is within the expected order of magnitude (calculate measured resistance is 108 kΩ[2]). Device 1 from group 2, which showed resistance of 378 kΩ, is qualified as defected and is excluded from the test pool.

Table 8.4: Results of the TiN interconnects resistance measurements on the meander structure.

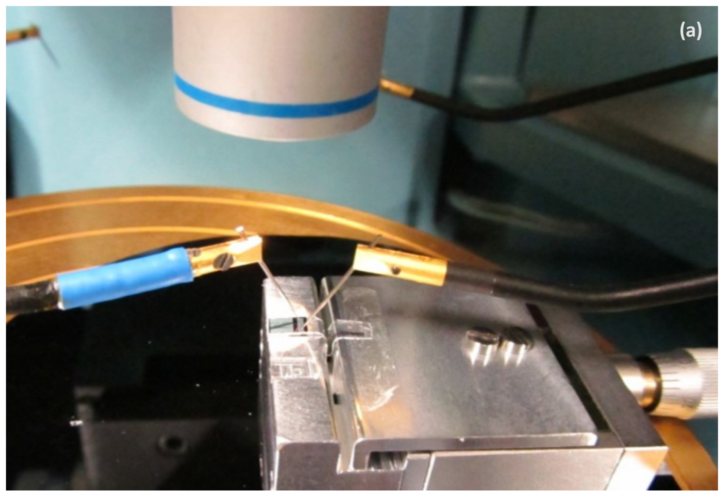
Group 1		Group 2		Group 3	
Device	**Resistance [kΩ]**	**Device**	**Resistance [kΩ]**	**Device**	**Resistance [kΩ]**
1	185	1	378	1	177
2	190	2	189	2	174
3	175	3	186	3	182
4	180	4	180	4	179
5	180	5	178	5	174

Interconnects flexibility

The flexibility of the TiN based interconnects encapsulated in a ceramic-parylene film has been evaluated using a bending test. The test is performed to determine whether the fabricated device can be rolled into a cylindrical shape with a diameter close to 1.3 mm (bending radius of 0.65 mm), and whether the rigid silicon island can be folded inside the cylinder at a radius of approximately 55 µm. The interconnect were evaluated electrically and optically while determining their maximum bending radius.

The resistance of the interconnect was examined via the meander structure using a Cascade Microtech probe station (Figure 8.14b). During the measurement, the I/V curve was drawn using the sweeping voltage in the range from -10 V to 10 V with a step of 0.1 V. The meander resistance was calculated from the curve using Ohm's law.

[2] The measured TiN sheet resistance of 17 Ω/square was used to calculating the theoretical meander resistance.



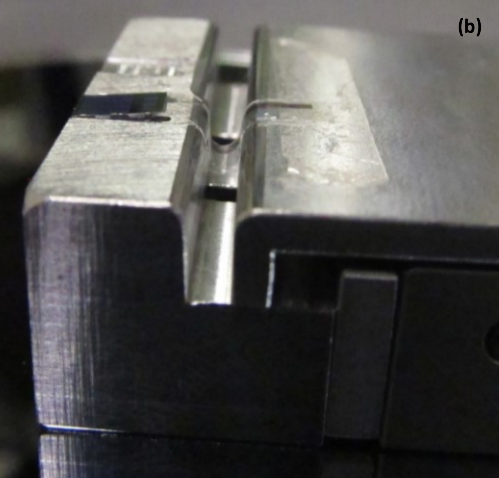


Figure 8.14: (a) The bending tool with a device placed on a probe station during the measurement. (b) Individual device mounted in a bending tool. Sample at an initial bending radius of 1000 µm.

During the bending test, the devices were mounted individually on a custom-made vice-like bending tool with a micrometer screw (Figure 8.14b). By adjusting the micrometer screw, the gap between the vice plates can be decreased. The distance between the plates directly corresponds to the doubled bending radius of the flexible film. During the experiment, the starting bending radius was 1000 µm (gap of 2000 µm), and it was decreased with a variable interval from 250 µm at the beginning of the test to 25 µm towards the end of the test. The resistance of the interconnect was sampled after each change of the bending radius until the moment when the interconnects break. The last bending radius registered before that moment defines the minimum bending radius of the interconnect.

The results of resistance change corresponding with the bending radius are collected in Table 8.5 and plotted in Figure 8.15. In the presented devices, the minimum noted bending radius of 100 µm was noted for device 3. However, most of the examined devices shoved behavior similar to devices 1 and 2 with a minimum bending radius of 125 µm. Moreover, device 3 shoved abnormal behavior expressed with resistance increase below bending radius of 250 µm followed by resistance drop.

Table 8.5: Resistance change in the meander structure corresponding with the bending radius. The infinity symbol "∞" indicates device failure due to broken interconnects.

Bending radius [µm]	Measured resistance [kΩ]		
	Device 1	Device 2	Device 3
1000	175	173	185
750	176	173	190
500	179	171	187
450	177	172	187
400	177	172	185
350	176	172	185
300	178	173	185
250	178	174	187

Bending radius [µm]	Measured resistance [kΩ]		
	Device 1	Device 2	Device 3
225	178	172	197
200	178	173	195
175	179	171	200
150	178	175	207
125	177	174	195
100	∞	∞	197
75	-	-	∞

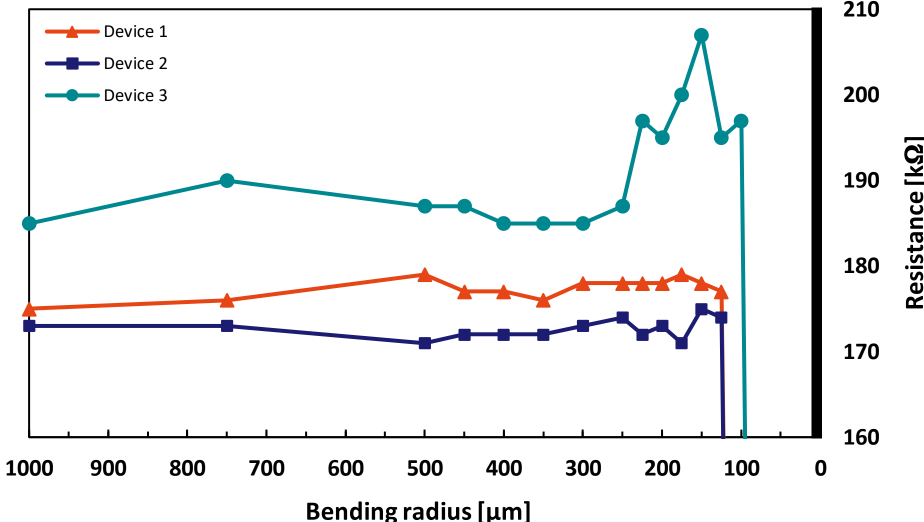


Figure 8.15: Biocompatible interconnects flexibility plotted as a resistance change in the meander corresponding with the bending radius.

Besides electrical measurements performed during the bending test, the influence of the bending on the interconnects was also evaluated optically. For that, several devices have been individually mounted in the bending tool and bent to a radius of 1000 µm or fully folded to a radius of approximately 13 µm. Then the devices were removed from the vice and inspected optically.

Evident creases can be seen in the ceramic-parylene encapsulation of the devices bent to a radius of 1000 µm (Figure 8.16b). The creases extend into the parylene film along with the patterned ceramics. However, no discontinuity in the metal lines is observed (Figure 8.16a), indicating that the interconnects are still functional, which was also demonstrated during the electrical measurements. On the other hand, the fully folded devices to a radius of 13 µm had clear signs of damage on the flexible film and on the TiN metallization (Figure 8.16c).

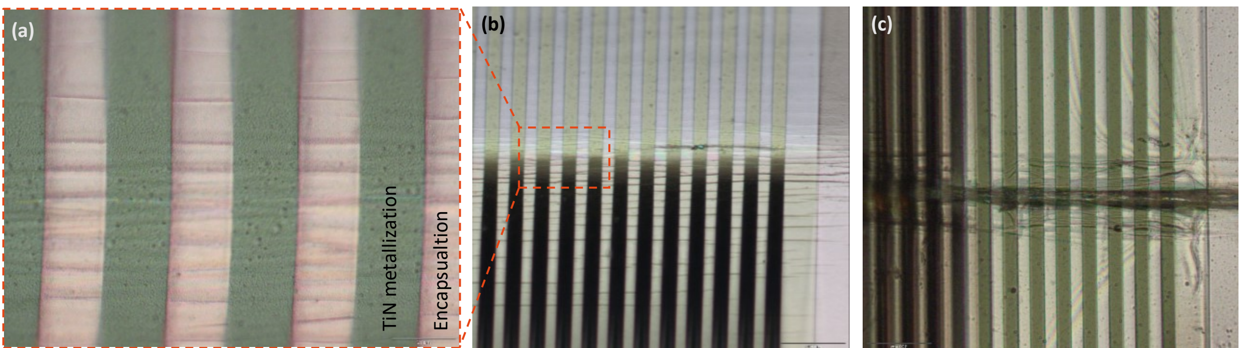


Figure 8.16. Mechanical damage to the ceramic-parylene-based interconnects caused by samples bending to a radius of (a,b) 1000 µm and (c) 13 µm.

Discussion and conclusions

The majority of the fabricated devices (approximately 80%) have been successfully released, and an electrical connection was established, indicating that the developed fabrication process and the devices themselves are robust and functional. It has been shown that the "parylene last" monolithic fabrication of devices encapsulated in the ceramic-parylene layer is feasible. The average interconnects resistance in the released devices is 181 kΩ. The value is within the expected order of magnitude.

It was possible to bend the flexible interconnects to a minimum radius of 125 µm without breaking the devices. Such bending radius is sufficient for the rolling of the device into a 1.3 mm diameter cylinder. However, it is not sufficient to roll the silicon island inside the cylinder at a radius of 55 µm. In general, the ceramic-parylene-TiN-based devices are much less resistant to bending and folding than the parylene-platinum-based interconnects (tested in Chapter 7) that could be folded to a diameter close to 5 µm. The decreased interconnects flexibility is probably related to the mechanical properties of the TiN (Young's modulus 450-590 GPa [21]), which is more brittle in comparison with platinum (Young's modulus 147 GPa [22]), and to the presence of the brittle ceramic layers in the stack.

The irreversible changes were observed in the flexible film bend only to a radius of 1000 µm. The creases observed in the ceramic-parylene stack and the parylene film persist after the bending force is removed. These permanent damages can potentially lead to adhesion issues within the encapsulation layer and raise concerns for device reliability. In the next iteration, the flexibility of the ceramic-parylene encapsulation should be investigated individually to determine whether and under what condition such encapsulation can be applied to implantable devices with flexible interconnects.

8.7.2 Ceramic-parylene-based encapsulation

Encapsulation is one of the most crucial elements of implantable electronics. Its function is to protect the implant against bodily fluids and, more importantly, protect the patient by ensuring device reliability. An encapsulation layer should have excellent barrier properties against bodily fluids and adhere flawlessly to the encapsulated device. This is to avoid corrosion of the encapsulated electronics and the release of possibly harmful substances to the body. In this section, the barrier properties of the ceramic-parylene based encapsulation are preliminarily evaluated in an aging test during which samples are incubated in PBS solution that is commonly used to mimic bodily conditions.

Methods

An accelerated aging test is performed to evaluate the barrier properties of the ceramic-parylene encapsulation. Samples are submerged in a PBS[3] solution and incubated at an elevated temperature of 57°C. The temperature is set below the maximum testing temperature of 60°C recommended for testing of polymeric encapsulation in medical devices specified in the ASTM F1980 norm [23]. The temperature of 57°C is chosen to estimate the accelerated aging duration easily. Increasing the temperature by 20°C above the reference body temperature of 37°C allows for accelerating the aging by approximately four times [24]. This means that aging samples at 57°C for four weeks corresponds to four months of aging at a body temperature of 37°C.

To evaluate the barrier properties of the ceramic-parylene-based encapsulation, the three groups of five devices, which were examined in the previous section, are used. The defective device from group 2 was excluded from the experiment. The samples are mounted on a silicon strip, submerged in the PBS solution, and placed in an incubator set to 57°C (Figure 8.17). Only the flexible film with encapsulated metallization is submerged in the PBS solution to prevent corrosion of the exposed bond pads.

[3] The used PBS solution has pH 7.4 and the following composition: 0.01 M phosphate buffer; 0.0027 M potassium chloride; 0.137 M sodium chloride.

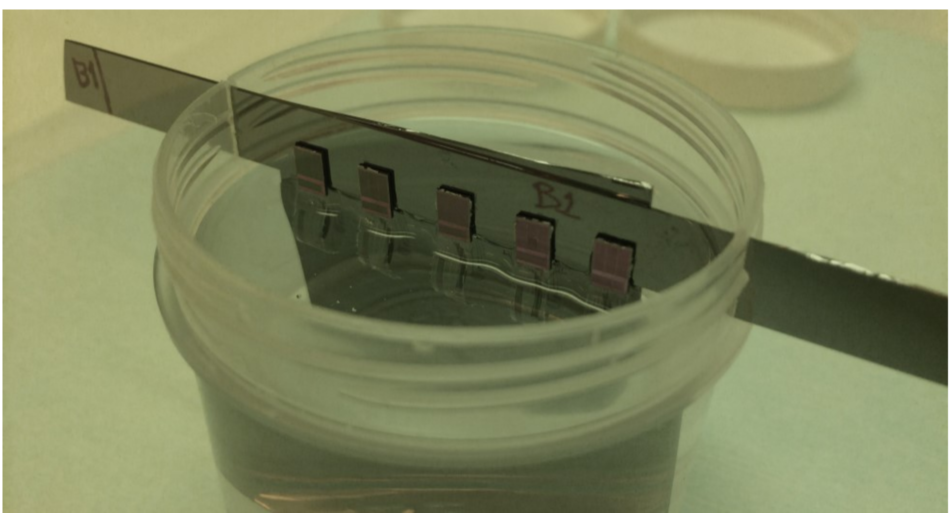


Figure 8.17: Test group of five devices submerged in PBS solution.

All devices are electrically and optically inspected throughout the experiment duration. The electrical measurements are performed both on the closed circuit of the meander structure and on the open circuit of the comb-meander structure. The initial resistance and its changes over time are measured using the Cascade Microtech probe station. During the optical inspection, signs of a discontinuous circuit, layers delamination, or metallization corrosion were searched for. Moreover, the optical inspection was always performed to determine the failure mode.

The increasing resistance of the meander structure indicates, for example, metallization corrosion, whereas infinite resistance of the meander could indicate complete device failure due to, for example, breaking of the metal tracks. The resistance measured between the comb and the meander structure, forming an open circuit, is infinite. A short circuit between the comb and the meander structure indicates device failure due to, for example, the formation of voids filled with condensate that is connecting the two metal tracks.

Before each consecutive test, the tested group is removed from the vial with PBS, rinsed, and shortly dried in the air. The electrical measurements are then performed, and the samples are placed back in the PBS solution. The complete procedure was always performed within 90 minutes, preventing drying of the moisture trapped inside or underneath the encapsulation layers.

During the test, the intervals of testing varied per group, as specified in Table 8.6. Groups 1 was tested more frequently in the early stage of the experiment to detect the moment of device failure. Groups 2 and 3 were tested less frequently to minimize the handling of the devices. For the same reason, the optical inspection was carried out mainly for failed devices to determine the cause of failure and limit the handling of the non-failed devices. Group 1 was subjected to the test one week before group 2, and group 3 was subjected to the test one week after group 2, allowing to apply gained knowledge to the subsequent group.

Meander structure resistance

The resistance of the meander structure was calculated using Ohm's law from the I/V curve acquired during the measurements. The resistance results for all of the examined samples are collected in Table 8.6. An Exemplar I/V curve of device 2 from group 2 after four weeks of aging is shown in Figure 8.18.

Table 8.6: Meander resistance measurements throughout the four-week aging test in PBS at 57°C. The resistance indicating device failure is marked in orange.

Group	Device	Resistance [kΩ]							
		0 hours	6 hours	24 hours	48 hours	1 week	2 weeks	3 weeks	4 weeks
1	1	185	187	$116 \cdot 10^4$	$414 \cdot 10^4$	-	-	-	-
1	2	190	194	191	$464 \cdot 10^4$	-	-	-	-
1	3	175	174	176	182	$149 \cdot 10^4$	-	-	-
1	4	180	180	180	$381 \cdot 10^4$	-	-	-	-
1	5	180	181	181	184	$434 \cdot 10^4$	-	-	-
2	1	Excluded	-	-	-	-	-	-	-
2	2	189	-	-	-	191	191	190	204
2	3	186	-	-	-	$479 \cdot 10^4$	-	-	-
2	4	180	-	-	-	182	183	209	187
2	5	178	-	-	-	178	179	181	$139 \cdot 10^4$
3	1	177	-	-	-	178	179	181	180
3	2	174	-	-	-	174	174	176	174
3	3	182	-	-	-	182	182	182	182
3	4	179	-	-	-	179	179	179	179
3	5	174	-	-	-	174	174	174	173

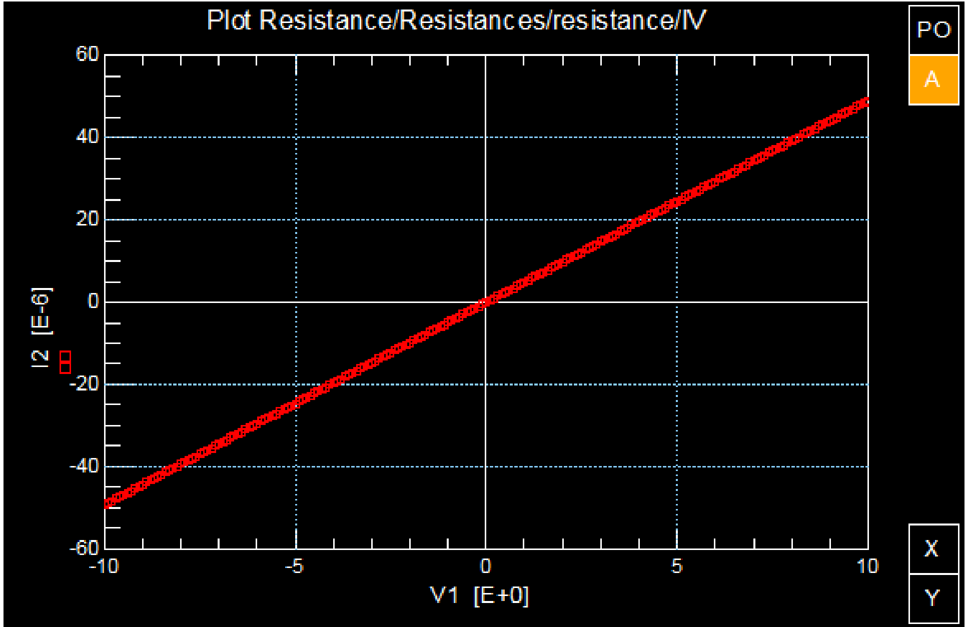


Figure 8.18: The exemplar I/V curve of device 2 from group 2 after four weeks of going at 57°C. The samples express typical linear resistance over the voltage sweep range.

The initial resistance (at 0 hours) of all the meander structures ranges from 174 kΩ to 190 kΩ, indicating a functioning meander circuit. Over the experiment duration, the functioning samples show resistance in a similar range with a slight fluctuation in resistance from measurement to measurement. For properly performing devices, this fluctuation did not exceed 5% on average. Upon device failure, resistance exceeding $100 \cdot 10^4$ kΩ was noted.

The samples in group 1 were tested frequently in the first hours of the experiment, both electrically and optically, to detect early signs of encapsulation failure. All devices in

this group failed within one week of testing. Each time the failure was correlated with the presence of cracks in the region of the flexible film transition to the rigid island (Figure 8.19). However, no signs of voids filled with condensate, delamination, or corrosion have been seen. Because of the specific failure mode, which seems unrelated to the aging test duration, the early devices failure is most likely related to mechanical damage of the interconnects due to frequent device handling.

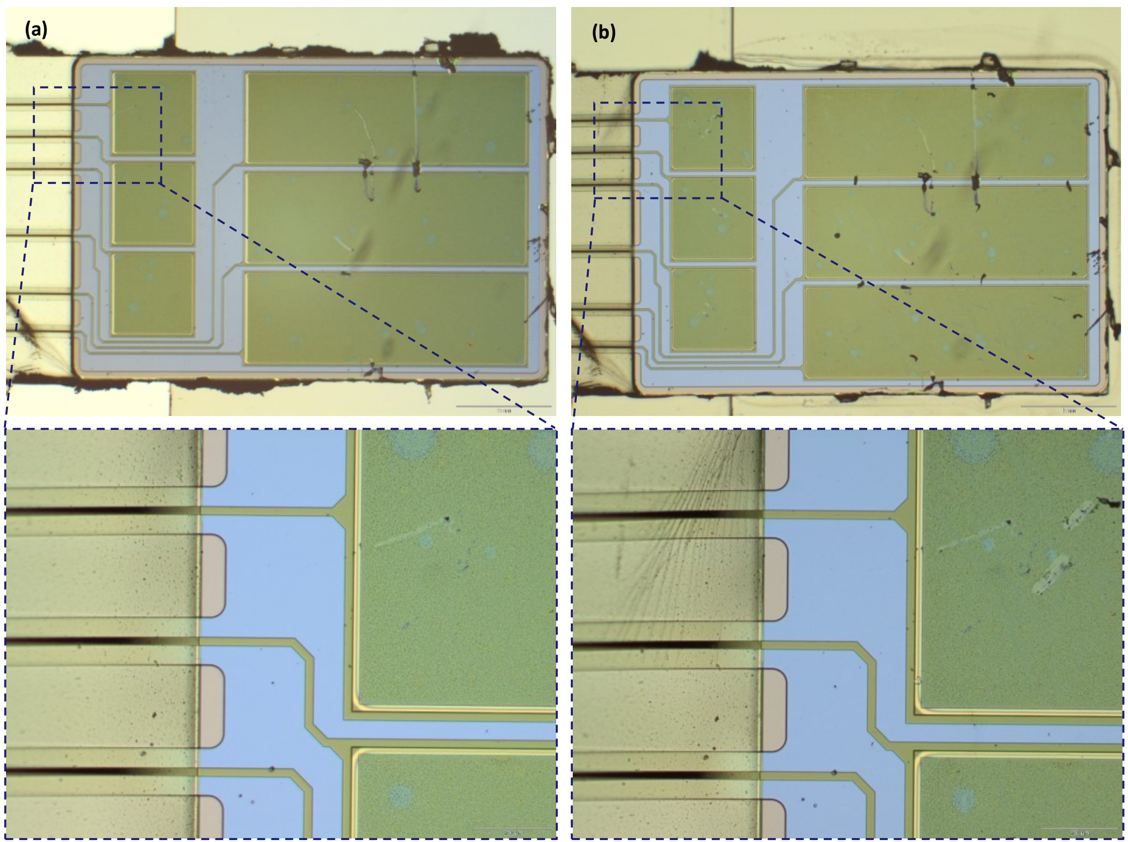


Figure 8.19: Device 1, group 1. (a) At 0 hours. (b) At 6 hours. Visible cracks at the edge of the silicon island.

Group 1 is considered a trial group on which handling and testing procedures were tested. Since the optical evaluation introduces considerable stress and often causes mechanical damage to the comb-meander structure, for groups 2 and 3 the optical inspection was only performed at the beginning and at the end of the experiment. To limit the handling for these groups, the testing interval was increased to one week.

The majority of the devices in test groups 2 and 3 had relatively stable resistance, ranging from 173 kΩ to 204 kΩ, over the test period of 4 weeks of samples aging in PBS at 57°C. Upon optical inspection performed after the testing period, the devices had no signs of delamination, void formation, corrosion, or mechanical damages (Figure 8.20). Devices 3 and 5 from group 2 failed due to mechanical damage after 1 and 4 weeks, respectively. This was confirmed with an optical inspection.

Figure 8.20: Device 2, group 3. No signs of delamination, void formation, corrosion, or mechanical damages.

Comb-meander structure

Throughout the experiment, for none of the examined devices, a short circuit between the comb and meander structure was noted. The measured resistance was always in the 10^9 Ω order of magnitude, indicating an open circuit. No defects induced by the aging test, such as TiN metallization corrosion or condensed moisture between the encapsulating layers, were observed during the optical inspections (Figure 8.20).

Even though no short circuits were observed between the comb and meander structures, it is still possible that condensation occurs, not in between but on the metal lines. To detect this in the early stage, a more sensitive measurement tool, which can detect leakage current in the range of picoamperes, should be used. The threshold for declaring the device failure must be set individually for the device type, but it should not exceed 100 nA [25][26].

Conclusions

The ceramic-parylene-based encapsulation showed promising barrier properties during the four weeks of the accelerated aging test in PBS at 57°C, which can be compared to 16 weeks in body temperature of 37°C. None of the tested semi-flexible devices with TiN metallization showed signs of metal corrosion, layer delamination, or moisture condensation in between the layers. Also, no short circuit was detected between the comb and meander structure at any time, which indicates good adhesion of the ceramic layers directly encapsulating the metal tracks.

During the experiment, three groups of five devices were examined. Group 1 – trail group – was tested more frequently, both optically and electrically. In this group, the handling during the optical examination turned out to cause premature device failures due to cracks in metallization present at the transition from the flexible film to the rigid silicon island.

Ten devices from group 2 and group 3 were examined weekly. For most devices, no aging or failure signs have been observed during the optical and electrical inspection. The comb-meanders circuit remained open, the average resistance measured on the meander structures was and remained 189 kΩ. Few devices from groups 2 and 3 have failed due to mechanical damage caused by device handling, and they have no signs of failure caused by insufficient barrier properties of the encapsulation.

The test devices used in this experiment turned out to be very fragile and prone to mechanical damages during handling. It means that during an extended testing period, common for implantable devices, the samples can get prematurely damaged before the barrier properties of the encapsulation are thoroughly examined. In the next iteration, the test device should be redesigned or reinforced to prevent metallization breakage, especially at the transition from the flexible film to the rigid part of the device.

8.8 CONCLUSIONS

In this chapter, it has been shown that it is possible to fabricate a semi-flexible device encapsulated in the ceramic-parylene layer in a monolithic process using standard microfabrication techniques and equipment. The developed "parylene last" approach allows for a complete device encapsulation in parylene while placing the metallization very close to the neutral plane. Moreover, it is possible to process the wafer with a higher temperature budget, in the range of a couple of hundred degrees Celsius, and use more aggressive wafer cleaning techniques such as two-step nitric acid or O_2 plasma.

The devices were released from the wafer without issues and subsequently subjected to mechanical and electrical evaluation. The resistance of the fabricated flexible TiN interconnects of approximately 181 kΩ is in line with the theoretical value. The minimum bending radius of 125 µm was achieved without extensive process optimization, which means that the device can be easily rolled into a cylinder with a diameter of 1.3 mm, common for DBS devices.

Furthermore, the devices were subjected to an accelerated aging test for four weeks in PBS at 57°C, corresponding to aging at a body temperature for approximately four months. Over the testing period, none of the devices have failed due to the insufficient barrier properties or showed signs of corrosion, delamination, or condensation of moisture at and of the interfaces present in the flexible film.

As intended, developed in this chapter "parylene last" process for fabrication of implantable, flexible devices is compatible with pre-processed wafers that might contain capacitors or ASICs. Moreover, the process is based on the F2R platform that, unlike the wafers transfer method, uses release tabs to neatly hold the device in a wafer frame after the device fabrication is completed.

Recommendations

During the fabrication of the semi-flexible devices using the "parylene last" approach and consequent devices evaluation, several improvement points have been identified:

- The DRIE process that is applied to release the device has been optimized to be suitable for parylene containing wafers. Further optimization of the DRIE process is required for two main reasons. First, to fabricate less fragile devices, with less sharp (rounded or tapered) edge of the silicon island at the interface of the flexible film with the rigid silicon island. Second, the aluminum etch stop layer should be removed entirely after device release. The slope of the silicon island edge and the aluminum etch stop layer design (overlay) must be carefully aligned to achieve this goal.
- The adhesion of the second layer of parylene to the stack has to be improved. For that, alternative methods of adhesion enhancement and cleaning (e.g., short sputter etching) applied to the ceramic and parylene interface have to be investigated to find a suitable treatment for all exposed materials.
- The semi-flexible device with a large flexible area is somewhat fragile and difficult to handle. The laser cutting can be applied as a safer way of removing the devices out of the wafer frame. In the testing phase, the device handling can be minimized by using a semi-automatic setup, where a wired sample is mounted in a viol with PBS solution through the complete duration of the experiment. The electrical measurements can be automatized and done in-situ without removing the sample from the vial and repeatedly making electrical contact with the bond pads.
- The "parylene last" process was initially designed for wafers containing platinum. The replacement of the metallization with the TiN allowed for monolithic fabrication of the proof of concept device. However, some of the process steps were not suitable for processing wafers with TiN metallization. If devices with such metallization are of interest in the field of implantable electronics, the flowchart should be reviewed and adapted to this material.
- The replacement of the platinum interconnects with the TiN ones enabled the efficient demonstration of the “parylene last” process feasibility. However, to accurately investigate whether the ceramic-parylene encapsulation qualifies for use in long-term implantable electronics with platinum-based electrodes and metallization, it is necessary to fabricate and test the devices in such a configuration.

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9
CONCLUSIONS

9.1 CONCLUSIONS

In this thesis, a set of enabling technologies has been developed for manufacturing and packaging highly integrated neurostimulation deceives. The key findings are collected related to the design and inter-facility fabrication of the “Chip-in-Tip” deep brain stimulator (DBS) probe containing parylene-platinum-based interconnects.

- Integration of active electronics in the tip of implantable or minimally invasive devices can greatly reduce wire count, reduce manufacturing costs, and increase device reliability. In the case of developed in this thesis “Chip-in-Tip” DBS device, integration of ASICs and decoupling capacitors in the tip of the probe also contributes to the increased stimulation resolution achieved by increasing the number of electrodes. Such directional brain stimulation reduces the treatment side effects and helps target more specific regions in the brain and related to them complex disorders (Chapter 2).
- The realization of the advanced implantable and minimally invasive devices requires the heterogeneous integration of high-quality outsourced components (e.g., ASICs) or process steps (e.g., capacitors pre-fabrication). They have to be brought together in a microfabrication environment that allows for the processing of non-standard CMOS-incompatible materials. This process requires complex planning and steps alignment between the involved manufacturing sites, such as in the case of trench capacitors integration (Chapter 4).
- The modified Flex-to-Rigid (F2R) miniaturization platform, allowing for precise silicon islands separation by, for example, using sealable trenches technology (Section 4.3) or a novel cavity-BOX substrate (Section 4.4), and incorporating parylene-platinum-based interconnects, is very suitable for the fabrication of advanced minimally invasive implantable devices.
- Parylene processing in a microfabrication cleanroom is possible, but it requires careful processing because of the limited parylene cleaning methods and the low-temperature budget (Chapter 6). Moreover, special precautions have to be taken if double side wafer processing is required (e.g., F2R-bassed DBS process) to prevent polymer layer contamination or mechanical damage. Finally, after the conformal double-side parylene deposition, the layer often has to be removed from one side of the wafer and its edges (e.g., “Chip-in-Tip” DBS fabrication flow).
- The interconnection scheme based on parylene and platinum only is difficult to realize in a monolithic planar fabrication flow where many different interfaces are present. Series of adhesion treatments were tested in Chapter 6 without satisfying results.
- The interconnection scheme based on parylene, ceramic layers, and titanium nitride is reliable and can be realized in a monolithic planar fabrication flow, which has been demonstrated in Chapter 8. The developed fabrication flow can also be adopted for platinum-based metallization.

- Developing a complete integration flow for manufacturing advanced implantable devices, like the “Chip-in-Tip” DBS probe, is very complex. In this thesis work, the enabling technologies for the fabrication of the DBS device were developed and preliminarily tested. To realize a functioning, implantable DBS probe, extensive development and testing of the individual components and process steps are required.

9.2 CONTRIBUTIONS

Along with developing specific design and fabrication flow designated for the “Chip-in-Tip” DBS probe, most of the technologies presented in this thesis are also applicable to the broad field of microfabrication.

- A process flow has been developed for the double-sided encapsulation of the semi-flexible F2R structures in parylene. The “parylene last” process incorporates additional metallization encapsulation in ceramic layers (Si_2O and Si_3N_4), and titanium buried mask to fabricate stress-free interconnects lying in a neutral plane (Chapter 8).
- A process for fabrication of high aspect ratio (HAR) sealable trenches using a meshed hardmask was developed (Section 4.2). It allows for etching deep trenches through the meshed SiO_2 mask and subsequent sealing of the trenches with a silicon dioxide layer. In this thesis, the process was used to separate capacitor islands in the DBS fabrication flow (Section 4.3).
- It was demonstrated that the cavity-BOX layer in a novel SOI substrate could be used as a buried hardmask. Applying the advanced substrate can significantly simplify the F2R process, and it can be used to simplify the fabrication of other complex MEMS devices. In this thesis, the process was used to separate capacitor islands in the DBS fabrication flow (Section 4.4).
- The methodology of parylene processing in a microfabrication cleanroom using standard techniques was developed (Chapter 6). This includes guidelines for two-sided wafer processing, wafer cleaning and maintaining its cleanliness, parylene patterning, and one-sided parylene removal. The parylene structures can be patterned, resulting in a straight edge slope in O_2 plasma or a positive edge slope in O_2/CF_4 plasma.
- The two-step process for deposition and patterning of platinum interconnects on top of a parylene layer was developed (Section 6.6.3). The process is safe for the parylene layer, and it allows for the complete removal of a photoresist mask after the platinum etching and prevents the shadowing effect or formation of the fences.
- A fully platinum-based biocompatible flip-chip process was developed together with project partner Fraunhofer IZM (Chapter 3). It allows for bonding chips with platinum bond pads using platinum stud bumps. Furthermore, a complete parylene-based underfill has been applied to this process.
- The design, processing methods, and logistics allowing for direct integration of outsourced silicon-based capacitors onto an F2R-based DBS structure were realized (Chapter 4). The methods were proposed for electrical isolation of the capacitors to realize the semi-flexible device structure (Section 4.3 and Section 4.4). Furthermore, the method was proposed for wrapping the semi-flexible DBS structure into a cylinder-shaped probe without inserting additional mechanical support (e.g., titanium rod) inside the device (Chapter 5).

9.3 RECOMMENDATIONS

In this thesis, a number of enabling technologies have been developed to realize the highly integrated “Chip-in-Tip” DBS probe. Further, two manufacturing methods have been proposed and preliminarily tested for the fabrication of foldable structures with biocompatible interconnects. Even though some test devices were already successfully fabricated using these methods, there is still a need to optimize the developed processes and validate whether they are suitable for scalable fabrication of long-term implantable devices such as the DBS probe. The interesting key points that can be addressed as a follow-up on this research are listed.

- It is not a problem to combine in one fabrication flow process module such as capacitor fabrication, F2R processing, or flip-chip, done in different facilities. However, within one process module, all process steps and materials should be available in one facility. In this thesis, the platinum deposition and patterning (part of the F2R module) was done in another facility than the rest of the process, which resulted in a significantly prolonged testing and fabrication phase, and unavoidable logistics difficulties.
- The „parylene last” process is a very promising approach for the realization of fully parylene encapsulated semi-flexible structures. However, further process optimization will be required with respect to the backside DRIE release process and subsequent aluminum etch stop layer removal, the deposition procedure of the second parylene layer, and the titanium buried mask deposition, patterning, and removal.
- In this thesis work, due to process and material limitations in the research facility (EKL cleanroom), platinum metallization was replaced with titanium nitride in the final process flow (Chapter 8). To realize interconnects approved for long-term implantable devices, the titanium nitride metallization should be replaced with platinum in the final „parylene last” process flow, followed by extensive reliability testing.
- The feasibility of the platinum-based flip-chip process was demonstrated. However, extensive testing with respect to the platinum stud bump adhesion to the platinum bond pad, the strength of the platinum-based flip-chip bond, the conformity of the parylene underfill, and the bonded structures reliability and biocompatibility will be necessary before this method can be considered as a new interconnection technology for implantable devices.
- Although separate process modules such as capacitor integration, F2R processing, ASIC flip-chip bonding, DBS device wrapping, and lead extinction attachment have been proposed, a complete process integration will be necessary to demonstrate the “Chip-in-Tip” DBS concept feasibility.
- The process flows presented in this thesis are all based on the food and drug administration (FDA) approved parylene C substrate. However, parylene C has a very low glass transition temperature of about 100°C, which was sometimes exceeded in the proposed process flows. Although this did not seem to have apparent consequences, the implications of the parylene C processing at higher temperatures should be further investigated. As an alternative, it is worth investigating the new type of parylene AF4 that offers a wider temperature process window of up to 450°C. However, its biocompatibility still has to be established.

APPENDIX A

"TOP STACK" FABRICATION FLOWCHART

Deposition and patterning of the PECVD SiO_2

- Silicon substrate: 4-inch; 400 µm thick; DSP (Double Side Polished)
- Deposition (backside): 6.0 µm PECVD SiO_2; Novellus #ZeroStressOxide; 400°C
- Lithography (alignment markets):
  - Coating (EVG 120; HMDS; 1.4 µm AZ3012);
  - Exposure (ASML PAS 5500 stepper; COMURK mask; 140 mJ/cm^2 energy);
  - Development (EVG 120; MF322; PEB[1] at 115°C; HB[2] at 100°C)
- Etching (alignment markers): 140 nm silicon; Trikon Omega 201 #URK-NPD (dry)
- Cleaning line: TePla #04 + HNO_3 100% (Si) + HNO_3 69% (Si) + SemiTool (rinse and dry)
- Deposition: 2.0 µm PECVD SiO_2; Novellus #ZeroStressOxide; 400°C
- Lithography (DRIE hardmask, backside):
  - Coating (EVG 120; HMDS; 4.0 µm AZ3027);
  - Exposure (ASML PAS 5500 stepper; *Backside* mask; 500 mJ/cm^2 energy);
  - Development (EVG 120; MF322; PEB at 115°C; HB at 100°C)
- Etching (DRIE hardmask, backside): 6.0 µm PECVD SiO_2; Drytek 384T #StdOxide (dry)
- Cleaning line: TePla #04 + HNO_3 100% (Si) + HNO_3 69% (Si) + SemiTool (rinse and dry)

Bottom parylene layer deposition and patterning

- Deposition: 2.5 µm parylene C; SCS LabCoater; Pretreatment (TePla O_2 plasma flash); Promoter (A-174 Silane; in-situ)
- Etching (backside): 2.5 µm parylene; Trikon Omega 201 #Par1 (dry; O_2)
- Lithography (contact to silicon):
  - Coating (EVG 120; 6.0 µm AZ9260);
  - Exposure (ASML PAS 5500 stepper; *Contact to Silicon* mask; 675 mJ/cm^2 energy; −3.0 µm focus);
  - Development (manual; AZ400K)
- Etching (contact to silicon): 2.5 µm parylene; Trikon Omega 201 #Par2 (dry; O_2/CF_4)
- Cleaning: acetone spin-cleaning; EVG 101

Platinum metallization deposition and patterning

- Deposition: 20 nm titanium (adhesion layer) and 600 nm platinum; sputtered (PInS); carrier wafer with shielding ring
- Lithography (metallization):
  - Coating (EVG 120; 1.4 µm HPR504);
  - Exposure (ASML PAS 5500 stepper; *Metallization* mask; 120 mJ/cm^2 energy; −0.3 µm focus);
  - Development (manual; AZ; reflow in a convection oven at 125°C for 30 minutes)
- Etching (metallization): 600 nm platinum and 20 nm titanium; ion-milling with argon (PInS)
- Cleaning: acetone-spin cleaning + NMP ultrasonic cleaning at 75°C + O_2 plasma flash

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[1] PEB – Post Exposure Bake. [2] HB – Hard Bake.

Top parylene layer deposition

- Deposition: 2.5 µm parylene C; SCS LabCoater; Pretreatment (TePla O_2 plasma flash); Promoter (A-174 Silane; in-situ)
- Etching (backside): 2.5 µm parylene; Trikon Omega 201 #Par1 (dry; O_2)

Titanium hardmask deposition and patterning

- Deposition: 200 nm titanium; sputtered; Trikon Sigma 204; 25°C
- Lithography (titanium hardmask):
  - Coating (manual; 3.1 µm AZ3027);
  - Exposure (ASML PAS 5500 stepper; *Contact to Bond Pad/Parylene Patterning* mask; 420 mJ/cm^2 energy);
  - Development (manual; MF322; PEB at 95°C)
- Etching (titanium hardmask): 200 nm titanium; Trikon Omega 201 #TinTiSvo (dry)
- Cleaning (photoresist): acetone spin-cleaning; EVG 101

Backside DRIE etch

- Etching (release, backside): 400 µm silicon; Rapier Omega i2L (dry)

Top parylene layer patterning

- Etching (parylene patterning): 2.5 µm / 5.0 µm parylene; Alcatel GIR 300 (dry; O_2)

Hardmask and stop layer removal

- Etching: 200 nm titanium hardmask and 2 µm PECVD SiO_2 stop layer; BOE (wet); 7 min.

APPENDIX B

"PARYLENE LAST" FABRICATION FLOWCHART

Backside DRIE hardmask and front side SiO_2 etch stop layer

- Silicon substrate: 4-inch; 400 µm thick; DSP (Double Side Polished)
- Deposition (backside): 6.0 µm PECVD SiO_2; Novellus #ZeroStressOxide; 400°C
- Lithography (alignment markets):
  - Coating (EVG 120; HMDS; 1.4 µm AZ3012);
  - Exposure (ASML PAS 5500 stepper; COMURK mask; 140 mJ/cm^2 energy);
  - Development (EVG 120; MF322; PEB[1] at 115°C; HB[2] at 100°C)
- Etching (alignment markers): 140 nm silicon; Trikon Omega 201 #URK-NPD (dry)
- Cleaning line: TePla #04 + HNO_3 100% (Si) + HNO_3 69% (Si) + SemiTool (rinse and dry)
- Deposition: 400 nm PECVD SiO_2; Novellus #ZeroStressOxide; 400°C
- Lithography (DRIE hardmask, backside):
  - Coating (EVG 120; HMDS; 4.0 µm AZ3027);
  - Exposure (ASML PAS 5500 stepper; *Backside** mask; 500 mJ/cm^2 energy);
  - Development (EVG 120; MF322; PEB at 115°C; HB at 100°C)
- Etching (DRIE hardmask, backside): 6.0 µm PECVD SiO_2; Drytek 384T #StdOxide (dry)
- Cleaning line: TePla #04 + HNO_3 100% (Si) + HNO_3 69% (Si) + SemiTool (rinse and dry)

Front side aluminum etch stop layer

- Deposition: 200 nm aluminum; sputtered; Trikon Sigma 204; 300°C
- Lithography (aluminum etch-stop):
  - Coating (EVG 120; HMDS; 1.4 µm AZ3012);
  - Exposure (ASML PAS 5500 stepper; *Etch Stop* mask; 150 mJ/cm^2 energy);
  - Development (EVG 120; MF322; PEB at 115°C; HB at 100°C)
- Etching (aluminum etch-stop): 200 nm aluminum; Trikon Omega 201 #Al675TMP (dry)
- Cleaning line: TePla #04 + HNO_3 100% (Me) + HNO_3 69% (Me) + SemiTool (rinse and dry)

Ceramic encapsulation and metallization

- Deposition: 50 nm PECVD Si_3N_4; Novellus #xxnm_Std_Sin; 400°C
- Deposition: 400 nm PECVD SiO_2; Novellus #ZeroStressOxide; 400°C
- Deposition: 10 nm titanium (adhesion layer) and 200 nm TiN; sputtered; Trikon Sigma 204 #Ti10_TiN200_STD_6kW; 350°C
- Lithography (metallization):
  - Coating (EVG 120; HMDS; 1.4 µm AZ3012);
  - Exposure (ASML PAS 5500 stepper; *Metallization** mask; 150 mJ/cm^2 energy);
  - Development (EVG 120; MF322; PEB at 115°C; HB at 100°C)
- Etching (metallization): 200 nm TiN and 10 nm titanium; Trikon Omega 201 #TinTiSvo (dry)
- Cleaning line: TePla #04 + HNO_3 100% (Me) + HNO_3 69% (Me) + SemiTool (rinse and dry)
- Deposition: 15 nm PECVD Si_3N_4; Novellus #xxnm_Std_Sin; 400°C; uniformity mode

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[1] PEB – Post Exposure Bake. [2] HB – Hard Bake.

- Deposition: 400 nm PECVD SiO_2; Novellus #ZeroStressOxide; 400°C
- Deposition: 50 nm PECVD Si_3N_4; Novellus #xxnm_Std_Sin; 400°C
- Lithography (encapsulation):
  - Coating (EVG 120; HMDS; 2.1 µm AZ3012);
  - Exposure (ASML PAS 5500 stepper; *Encapsulation* mask; 200 mJ/cm^2 energy);
  - Development (EVG 120; MF322; PEB at 115°C; HB at 100°C)
- Etching (encapsulation): 50 nm PECVD Si_3N_4, 400 nm PECVD SiO_2, 15 nm PECVD Si_3N_4, 400 nm PECVD SiO_2, 50 nm PECVD Si_3N_4; Alcatel GIR 300 (dry; CF_4, SF_6, O_2)
- Cleaning line: TePla #04 + HNO_3 100% (Me) + HNO_3 69% (Me) + SemiTool (rinse and dry)

Front-side parylene layer and buried titanium hardmask

- Deposition: 6.0 µm parylene C; SCS LabCoater; Pretreatment (TePla O_2 plasma flash); Promoter (A-174 Silane; in-situ)
- Etching (backside): 6.0 µm parylene; Trikon Omega 201 #Par2 (O_2/CF_4)/#Par1 (O_2)
- Deposition: 200 nm titanium; sputtered; Trikon Sigma 204; 25°C
- Lithography (titanium hardmask):
  - Coating (EVG120; 3.1 µm AZ3027);
  - Exposure (ASML PAS 5500 stepper; *Contact to Bond Pad/Parylene Patterning* mask; 420 mJ/cm^2 energy);
  - Development (EVG120; MF322; PEB at 95°C)
- Etching (titanium hardmask): 200 nm titanium; Trikon Omega 201 #TinTiSvo (dry)
- Cleaning (photoresist): acetone spin-cleaning; EVG 101 + O_2 plasma flash; Alcatel GIR 300

Backside DRIE etch and etch stop layers removal

- Etching (release, backside): 400 µm silicon; Rapier Omega i2L (dry)
- Etching (backside): 400 nm PECVD SiO_2; Alcatel GIR 300 (dry; CF_4, SF_6, O_2)
- Etching (backside): 200 nm aluminum; PES (wet); 20°C

Backside parylene deposition and parylene encapsulation patterning

- Deposition: 6.0 µm parylene C; SCS LabCoater; Pretreatment (TePla O_2 plasma flash); Promoter (A-174 Silane; in-situ)
- Etching (parylene patterning): 6 µm/12 µm/18 µm parylene; Alcatel GIR 300 (dry; O_2)

Hardmask and stop layer removal

- Etching: 200 nm titanium hardmask; (wet; 1xH_2O : 1xH_2O_2 31% : 1xNH_4OH 28%); 3 min

SUMMARY

The progress in the field of neurostimulation is impressive, both from a technical as well as from a therapeutic point of view. Nowadays, the electrical stimulation of the nervous system can be used to induce or suppress muscle responses. Additionally, it can also influence hearing, vision, immune system response, pain perception, and even mental state. The number of medical conditions that can be treated using existing or completely new neurostimulation devices is continuously growing. Moreover, well-targeted electrical neuromodulation can help reduce the whole-body side effects, typical for traditional medication therapies. However, the potential of neurostimulation therapy is limited by the relatively slow development of the accompanying technologies. Most commercial neurostimulation implants still consist of a pulse generator encapsulated in a bulky titanium case and lengthy extension cords. Moreover, in some cases, such as deep brain stimulation (DBS), the resolution of the stimulation is also an issue that can cause severe side effects. In this thesis work, a technology platform for the manufacturing and packaging of advanced neurostimulation implants has been developed to enable further bioelectronics miniaturization and improve the stimulation resolution. These goals have been achieved in close collaboration with the InForMed project partners involved in finalizing the joint design, preparing the inter-facility fabrication process, and supplying off-the-shelf technology modules.

In the first part of this thesis (Chapter 2), the Chip-in-Tip concept was developed to realize a directional, 40-electrode DBS probe with a high stimulation resolution. The design facilitates a less complex implantation procedure and ensures overall implant miniaturization and improved robustness. It is achieved by integrating multiplexing ASICs (chips) and DC blocking capacitors directly into the tip of the neurostimulation device (DBS probe) in a monolithic inter-facility fabrication process based on the Flex-to-Rigid (F2R) platform. The presented design, integration process, and biocompatible packaging strategies can be applied to the miniaturization and scalable fabrication of long-term neurostimulation devices.

The second part of the thesis focuses on the development of technologies that enable the integration of components and the subsequent device packaging. In Chapter 3, a biocompatible flip-chip process is described to integrate the multiplexing ASICs onto a semi-flexible DBS structure. The flip-chip process uses non-standard platinum stud bumps on platinum bond pads. Subsequently, two materials were used to underfill the 30 µm gap between the bonded devices: medical-grade silicone rubber and parylene C. The latter allows for the underfilling of the structure with no visible voids. The presented biocompatible flip-chip technology is suitable for a wide range of implantable devices, contributing to the further miniaturization of bioelectronic devices. Moving the ASICs inside the tip of the DBS probe requires bringing the decoupling capacitors into the tip to ensure patient safety. For that, an inter-facility PICS3 trench capacitor integration process was developed in Chapter 4. The joint design and mutual fabrication resulted in a foldable DBS structure with capacitor islands that can be wrapped around the circumference of the probe. Two methods were developed to enable precise component separation: the Flex-to-Rigid platform technology in combination with sealable trenches; and a custom cavity-BOX SOI substrate with a pre-patterned BOX layer that can simplify the fabrication of all kinds of MEMS devices where precise separation of structures is required. A manual tool with a two-strip clamping system was prototyped in Chapter 5, and used for the rod-free wrapping of the foldable device to form a 1.3 mm diameter probe. The probe was subsequently filled with a low-viscosity medical-grade

epoxy providing mechanical strength and securing all the components in place. After automation, the wrapping tool can be applied to the assembly of other foldable devices. The demonstrated component integration approach enables using high-quality components and achieving exceptional device performance without compromising the process robustness or device dimensions.

Parylene C is widely used in various flexible bioelectronic devices. However, there is little experience with the (monolithic) fabrication of parylene-based devices in a microfabrication cleanroom. In the third part of this thesis (Chapter 6), several aspects of parylene processing were investigated. First, the adhesion between the layers in parylene-platinum based flexible interconnects was evaluated by soaking the samples in PBS at 55°C for up to 10 days and using an adopted cross-cut test. The preliminary tests showed that it would technically be possible to fabricate devices with platinum-based flexible interconnects encapsulated in parylene. However, more research is needed to realize biocompatible flexible interconnects suitable for long-term implantable devices since the adhesion of parylene to platinum after the soaking test was poor regardless of the applied pre-treatment of the platinum. Secondly, a best practice was developed to maintain a clean parylene surface (e.g., shielding rings, edge tweezers) and to clean the parylene-coated wafers (e.g., mild O_2 plasma, acetone spin-clean) during a two-sided fabrication process. Excellent surface cleanliness is essential, especially when fabricating soft-encapsulated implantable devices. Thirdly, a controllable and selective RIE process for parylene patterning was established. The micron-sized parylene structures can be precisely patterned in an O_2 plasma using a thick photoresist, aluminum, or titanium as a masking layer. Adding a small fraction of CF_4 (approximately 6%) to the O_2 plasma allows for the etching of parylene structures with a positive slope, ensuring better step coverage of the subsequently deposited metallization layer. Finally, a two-step argon-based sputter etch process with intermediate photoresist mask removal was developed to pattern platinum on top of parylene. The method prevents photoresist mask residues, fence formation, shadowing effects, and does not cause parylene degradation. The presented methods are universal and form a good base for parylene processing in other microfabrication environments.

In the last, fourth part of this thesis (Chapter 7 and Chapter 8), the developed parylene processing methods were applied for the monolithic fabrication of biocompatible flexible interconnects. Platinum interconnects encapsulated only in a parylene layer were fabricated using the “top stack” approach (temperature budget of ~100°C). These interconnects are highly flexible, allowing for a minimum bending radius of 5 µm (stack thickness). However, they are also very fragile, and therefore their reliability needs further evaluation. For the next iteration of the process, a “parylene last” approach was developed to fabricate interconnects with TiN metallization encapsulated in ceramic layers (SiO_2, Si_3N_4) and parylene. In this approach, the parylene deposition step is moved to the very end of the process. It allows for fabricating robust devices that do not show any signs of corrosion or delamination in an accelerated lifetime test equivalent to four months in the human body. The 12 µm thick TiN-based interconnects are less flexible, allowing for a minimum bending radius of 125 µm. The “parylene last” approach enables increasing the process temperature budget to around 400°C and using standard microfabrication techniques (e.g., PECVD deposition, high-power O_2 plasma). It can be used for the monolithic fabrication of robust and reliable biocompatible flexible interconnects that can be applied to a wide range of advanced implantable devices.

SAMENVATTING

De vooruitgang in het veld van neurostimulatie is indrukwekkend, zowel vanuit een technisch als therapeutisch oogpunt. Tegenwoordig kan de elektrische stimulatie van het zenuwstelsel worden gebruikt om spierreacties op te wekken of te onderdrukken. Aanvullend daarop kan het ook het gehoor, het gezichtsvermogen, de reactie van het immuunsysteem, de pijnperceptie en zelfs de mentale toestand beïnvloeden. Het aantal medische aandoeningen dat kan worden behandeld met bestaande of nieuwe neurostimulatoren groeit voortdurend. Bovendien kan goed gerichte elektrische neuromodulatie bijwerkingen van de stimulatie, typisch bij traditionele medicatietherapieën, helpen verminderen. Echter, het potentieel van neurostimulatietherapie wordt beperkt door de relatief trage ontwikkeling van de bijbehorende technologieën. De meeste commerciële implantaten voor neurostimulatie bestaan nog steeds uit een pulsgenerator in een omvangrijke titanium behuizing en lange geleidingsdraden. Bovendien is in sommige gevallen, zoals bij diepe hersenstimulatie (deep brain stimulation, DBS), de resolutie van de stimulatie ook een probleem dat ernstige bijwerkingen kan veroorzaken. In dit proefschrift is een technologieplatform ontwikkeld voor de productie en verpakking van geavanceerde neurostimulatie-implantaten om verdere bio-elektronische miniaturisatie mogelijk te maken en de stimulatieresolutie te verbeteren. Deze doelen zijn bereikt in nauwe samenwerking met de EU ECSEL JU InForMed-projectpartners die betrokken zijn bij het afronden van het gezamenlijke ontwerp, het voorbereiden van het fabricageproces tussen de faciliteiten en het leveren van kant-en-klare technologiemodules.

In het eerste deel van dit proefschrift (Hoofdstuk 2), is het Chip-in-Tip-concept ontwikkeld om een directionele DBS-sonde met 40 elektroden te realiseren met een hoge stimulatieresolutie. Het ontwerp maakt een minder complexe implantatieprocedure mogelijk en zorgt voor de algehele miniaturisatie van het implantaat en een verbeterde robuustheid. Dit wordt bereikt door multiplexing ASIC's (chips) en gelijkstroom-blokkerende condensatoren rechtstreeks in de punt van de neurostimulator (DBS-sonde) te integreren in een monolithisch interfacilitair fabricageproces op basis van het Flex-to-Rigid (F2R) platform. Het gepresenteerde ontwerp, integratieproces en de biocompatibele verpakkingsstrategieën kunnen worden toegepast op de miniaturisatie en schaalbare fabricage van permanent geïmplanteerde neurostimulatoren.

Het tweede deel van het proefschrift richt zich op de ontwikkeling van technologieën die de integratie van componenten en de daaropvolgende circuitomhulling mogelijk maken. In hoofdstuk 3 wordt een biocompatibel flip-chip-proces beschreven om de multiplex-ASIC's te integreren in een semi-flexibele DBS-structuur. Het flip-chip-proces maakt gebruik van niet-standaard platina-bumps op platina-bondpads. Vervolgens zijn twee materialen gebruikt om de opening van 30 µm tussen de chips op te vullen: siliconenrubber van medische kwaliteit en paryleen C. Het laatste zorgt voor een ondervulling van de structuur zonder zichtbare holtes. De gepresenteerde biocompatibele flip-chip-technologie is geschikt voor een breed scala aan implanteerbare circuits en draagt bij aan de verdere miniaturisering van bio-elektronische circuits. Het verplaatsen van de ASIC's naar de punt van de DBS-sonde vereist ook het verplaatsen van de ontkoppelingscondensatoren naar de punt om de veiligheid van de patiënt te waarborgen. Daarvoor is in hoofdstuk 4 een interfacilitair PICS3-condensatorintegratieproces ontwikkeld. Het gezamenlijke ontwerp en de onderlinge fabricage resulteerden in een opvouwbare DBS-structuur met condensatoreilanden die rond de omtrek van de sonde kunnen worden gewikkeld. Er

zijn twee methoden ontwikkeld om nauwkeurige componentenscheiding mogelijk te maken: de Flex-to-Rigid platformtechnologie in combinatie met afsluitbare sleuven; en een speciaal cavity-BOX SOI-substraat met een voorgevormde BOX-laag die de fabricage van allerlei MEMS-circuits kan vereenvoudigen waar een nauwkeurige scheiding van structuren vereist is. Een handmatig gereedschap met een klemsysteem met twee stroken is in hoofdstuk 5 als prototype ontwikkeld en gebruikt voor het vormvrij omwikkelen van het flexibele circuit om een sonde met een diameter van 1.3 mm. De sonde is vervolgens gevuld met een laagviskeuze epoxy van medische kwaliteit die mechanische sterkte biedt en alle componenten op hun plaats houdt. Na automatisering kan het wikkelgereedschap worden toegepast voor de montage van andere flexibele circuits. De gedemonstreerde benadering van de componentintegratie maakt het mogelijk om hoogwaardige componenten te gebruiken en uitzonderlijke circuit prestaties te bereiken zonder afbreuk te doen aan de robuustheid van het proces of de afmetingen van het implantaat.

Parylene C wordt veel gebruikt in verschillende flexibele bio-elektronische circuits. Er is echter weinig ervaring met de (monolithische) fabricage van op paryleen gebaseerde circuits in een microfabricage-cleanroom. In het derde deel van dit proefschrift (Hoofdstuk 6) zijn verschillende aspecten van paryleenverwerking onderzocht. Ten eerste is de hechting tussen de lagen in op paryleen-platina gebaseerde flexibele verbindingen geëvalueerd door de monsters tot 10 dagen in PBS bij 55°C te weken en een goedgekeurde cross-cut-test te gebruiken. De eerste tests tonen aan dat het technisch mogelijk is om circuits te fabriceren met op platina gebaseerde flexibele verbindingen ingekapseld in paryleen. Echter, meer onderzoek is nodig om biocompatibele flexibele verbindingen te realiseren die geschikt zijn voor langdurig implanteerbare circuits, aangezien de hechting van paryleen aan platina na de inweektest slecht was, ongeacht de toegepaste voorbehandeling van het platina. Ten tweede is een “best practice” ontwikkeld om een schoon paryleenoppervlak te behouden (bijv. afschermringen, randpincet) en om de paryleen-gecoate wafers (bijv. mild O_2-plasma, aceton-spin-clean) te reinigen tijdens een tweezijdig fabricageproces. Uitstekende oppervlaktereinheid is essentieel, vooral bij het fabriceren van implanteerbare circuits met een zachte inkapseling. Ten derde is een controleerbaar en selectief RIE-proces voor het patroneren van paryleen vastgesteld. De paryleenstructuren ter grootte van een micrometer kunnen nauwkeurig in een O_2-plasma worden gefabriceerd met een dikke fotoresist, aluminium of titanium als maskeringslaag. Door een kleine fractie CF_4 (ongeveer 6%) aan het O_2-plasma toe te voegen, kunnen paryleenstructuren met een positieve helling worden geëtst, waardoor een betere stapdekking van de vervolgens afgezette metallisatielaag wordt gegarandeerd. Tot slot is een tweestaps, op argon gebaseerd, sputter-etsproces ontwikkeld met tussentijdse verwijdering van fotoresistmaskers om platina bovenop paryleen te vormen. Deze methode voorkomt resten van het fotoresistmasker, vorming van randen, schaduweffecten en veroorzaakt geen beschadiging van het paryleen. De gepresenteerde methoden zijn universeel en vormen een goede basis voor paryleenverwerking in andere microfabricage-omgevingen.

In het laatste, vierde deel van dit proefschrift (Hoofdstuk 7 en Hoofdstuk 8), zijn de ontwikkelde paryleenverwerkingsmethoden toegepast voor de monolithische fabricage van biocompatibele flexibele verbindingen. Platina-interconnecties die alleen in een paryleenlaag zijn ingekapseld, zijn vervaardigd met behulp van de "topstack"-benadering (temperatuurbudget van ~ 100°C). Deze verbindingen zijn zeer flexibel, waardoor een minimale buigradius van 5 µm (stapeldikte) mogelijk is. Echter, ze zijn ook erg kwetsbaar en daarom moet hun betrouwbaarheid nader worden geëvalueerd.

Voor de volgende iteratie van het proces is een "parylene last"-benadering ontwikkeld om verbindingen te maken met TiN-metallisatie ingekapseld in keramische lagen (SiO_2, Si_3N_4) en paryleen. Bij deze benadering wordt de paryleenafzettingsstap naar het einde van het proces verplaatst. Dit maakt het mogelijk om robuuste circuits te fabriceren die geen tekenen van corrosie of delaminatie vertonen in een versnelde levensduurtest gelijk aan vier maanden in het menselijk lichaam. De 12 µm dikke op TiN gebaseerde verbindingen zijn minder flexibel, waardoor een minimale buigradius van 125 µm mogelijk is. De "parylene last"-benadering maakt het mogelijk om het procestemperatuurbudget te verhogen tot ongeveer 400°C en gebruik te maken van standaard microfabricagetechnieken (bijv. PECVD-depositie, hoogvermogen O_2-plasma). Het kan worden gebruikt voor de monolithische fabricage van robuuste en betrouwbare biocompatibele flexibele verbindingen die kunnen worden toegepast op een breed scala aan geavanceerde implanteerbare circuits.

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List of Publications

Journal articles

- **M. Kluba**, J. Li, K. Parkkinen, M. Louwerse, J. Snijder, and R. Dekker, "Cavity-BOX SOI: Advanced Silicon Substrate with Pre-patterned BXO for Monolithic MEMS Fabrication," Micromachines, vol. 12, no. 4, 2021, doi: 10.3390/mi12040414.
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Conference contributions

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Co-supervised master theses and internships

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- A. Kanhai, "Flexible parylene-platinum based electrodes and interconnects," Master thesis, 2018
- C. Mountain, "Developing C-BOX in SOI wafers for the next generation of the F2R platform," Internship, 2018
- S. Kawasaki, "Silicon based devices for smart assessment of cellular stiffness," Master thesis, 2017
- A. Kanhai, "Adhesion of Parylene and Platinum," Internship, 2017

BIOGRAPHY

Name: **Marta Maria KLUBA**

Born: 22nd June 1986

Oświęcim, Poland

Mobile: +31 (0)634 132 458

E-mail: klubam@gmail.com

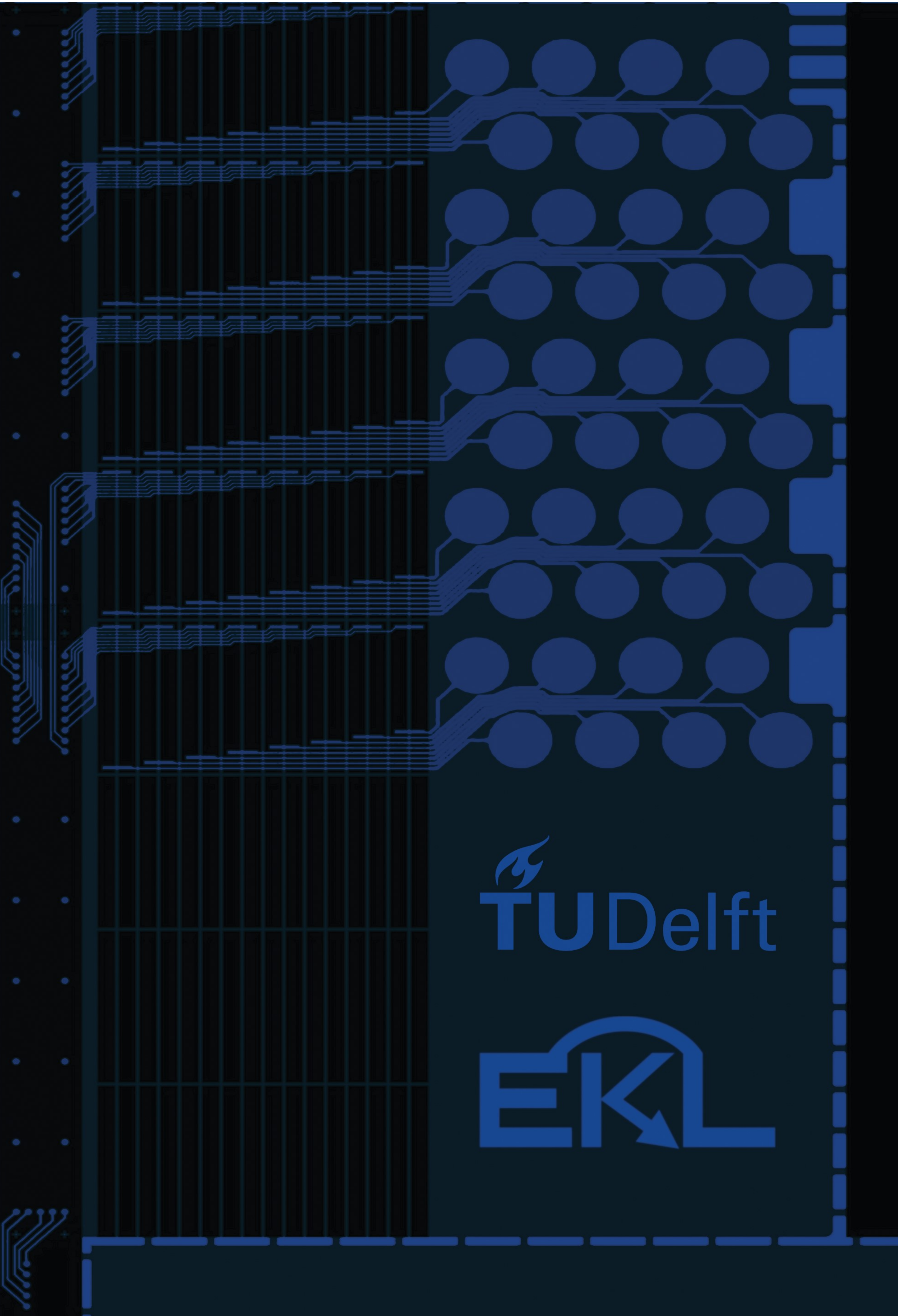
Marta obtained her master's degree in Chemical Technology and her bachelor's degree in Biomedical Technology from the AGH University of Science and Technology in Cracow (AGH-UST, Poland) in 2010 and 2012, respectively. In 2009 Marta joined the Erasmus exchange program, and she studied for half a year at the Delft University of Technology (TU Delft).

In 2011, Marta won a scholarship for the European Master program (CEMACUBE), during which she obtained a double-degree in Biomedical Engineering from the University of Groningen (RUG, The Netherland) and the Aachen University (RWTH Aachen, Germany) in 2014. She conducted her master's research at the Delft Institute of Prosthetics and Orthotics (DIPO, The Netherlands).

After graduation, she started working at the micro-manufacturing facility of the TU Delft (Else Kooi Laboratory, former DIMES Technology Centre) as a junior process engineer. Here, Marta gained her knowledge and experience in the field of microfabrication.

In 2015, she was successfully appointed as a PhD candidate by Professor Ronald Dekker and started her research on flexible, implantable bioelectronics at the Department of Microelectronics (TU Delft, The Netherlands). Her research was done as part of the InForMed project, a European initiative aimed at bringing medical technologies and devices to the market. During her PhD, Marta collaborated with and guided a team of experts from industrial and academic institutions such as Fraunhofer IZM, Murata, Okmetic, and Philips Research.

Marta is currently working as a process engineer at Else Kooi Laboratory (EKL, The Netherlands). Besides fabrication processes development and control, she is also involved in process logistics and in direct contact with customers.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