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A 16 MHz CMOS *RC* Frequency Reference With ± 90 ppm Inaccuracy From -45 °C to 85 °C

Çağrı Gürleyük¹, Member, IEEE, Sining Pan¹, Member, IEEE, and Kofi A. A. Makinwa¹, Fellow, IEEE

Abstract—This article presents a 16-MHz *RC* frequency reference implemented in a standard 180-nm CMOS process. It consists of a frequency-locked loop (FLL) in which the output frequency of a digitally controlled oscillator (DCO) is locked to the frequency-phase characteristic of a Wien bridge *RC* filter. Since it is made from on-chip resistors and capacitors, the filter's characteristic is temperature dependent. To compensate for this, the control signal of the DCO is derived by digitizing the filter's output phase and combining it with the digital output of a Wheatstone bridge temperature sensor. After a two-point trim, this digital temperature compensation scheme achieves an inaccuracy of ± 90 ppm from -45 °C to 85 °C. The frequency reference draws 220 μ A from a 1.8 -V supply, with a supply sensitivity of $0.12\%/V$ and a 320 -ppb Allan Deviation floor for a 10 -s stride.

Index Terms—CMOS, digitally controlled oscillator (DCO), digital frequency-locked loop (FLL), integrated frequency reference, *RC*.

I. INTRODUCTION

ACCURATE frequency references are used in electronic systems for timing, communication, and synchronization purposes. Nearly a century after their introduction [1], frequency references based on quartz crystal resonators dominate the market due to their excellent accuracy and high quality factor. However, they are incompatible with CMOS technology and require hermetically sealed packages, making them quite bulky compared with most systems-on-chip.

Recently, alternatives to quartz crystal resonators have emerged in the form of MEMS [2] and bulk acoustic wave (BAW) [3] resonators. These can achieve similar (or higher) levels of stability and accuracy and can be packaged with CMOS circuitry to realize compact frequency references. Achieving further size reductions will then require the realization of accurate frequency references in standard CMOS.

CMOS frequency references are usually based on *LC* and *RC* oscillators. Although frequency references based on the thermal diffusivity of silicon have also been reported [4], they dissipate milliwatts of power and only achieve ± 1000 ppm inaccuracy from -55 °C to 125 °C after a one-point trim.

In contrast, recent *LC* references achieve ± 120 ppm inaccuracy from -50 °C to 170 °C after a one-point trim [5], and even ± 50 ppm inaccuracy after a two-point trim [6], [7]. However, limitations on the size and quality factor of on-chip inductors constrain *LC* oscillators to GHz frequencies and thus milliwatts of power consumption. In contrast, *RC* oscillators can operate at much lower frequencies and thus consume much less power [8]–[20]. However, unlike inductors, the temperature dependence of on-chip resistors is a function of doping. As a result, *RC* frequency references exhibit larger spread, larger and significantly nonlinear temperature dependency, and worse stability than their *LC* counterparts.

To improve their accuracy, *RC* frequency references require temperature compensation schemes capable of mitigating the nonlinear temperature coefficients (TCs) of on-chip resistors. Composite resistor schemes, which combine resistors with complementary TCs, only achieve limited first-order cancellation, resulting in inaccuracies of $> \pm 1000$ ppm. In [9], the combination of complementary TCs is achieved via pulse-density modulated resistors, resulting in accurate linear compensation. This yields an inaccuracy of ± 500 ppm after a two-point trim, limited by the residual nonlinear TCs of the resistors. In [8], a digital compensation scheme is proposed that can address the nonlinear TCs, in which the output phase of two *RC* filters is digitized and then combined to cancel their complementary TCs. Such dual-*RC* frequency references achieve inaccuracies of ± 200 ppm from -45 °C to 85 °C after a two-point trim and batch calibration [8], [11]. However, since the output of each filter depends on both frequency and temperature, they require an extensive initial batch calibration at several temperatures. A simpler approach involves the use of a temperature sensor to compensate for the nonlinear TC of an on-chip filter [4]. In [4], this approach was used to compensate for the TC of an electro-thermal filter. However, the combination of sensor inaccuracy and the relatively high TC (~ 3000 ppm/°C) of the filter limited the resulting inaccuracy to ± 1000 ppm from -55 °C to 125 °C.

This article describes a 16-MHz frequency reference that combines a low-TC *RC* filter and a Wheatstone bridge (WhB) temperature sensor [22]. With a simple linear temperature compensation scheme, it achieves ± 400 ppm inaccuracy from -45 °C to 85 °C after a two-point trim. This improves to ± 90 ppm with a nonlinear temperature compensation scheme based on a fixed sixth-order correction polynomial whose coefficients are determined by an initial batch calibration.

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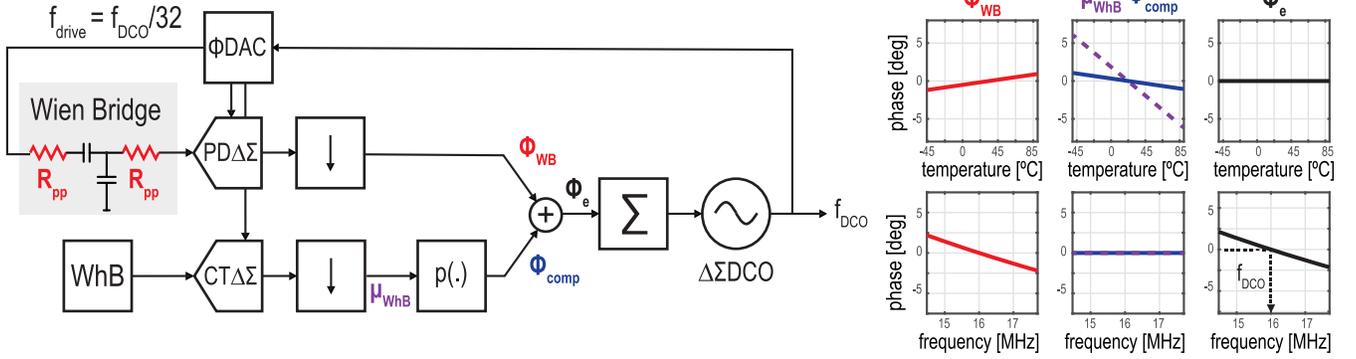


Fig. 1. Block diagram of the RC frequency reference, showing the temperature compensated digital FLL and the simulated temperature and frequency dependence of the phase signals.

This article is organized as follows: Section II describes the architecture of the proposed frequency reference architecture. Section III describes its circuit-level implementation. Measurement results are shown in Section IV, and the circuit's performance is compared to the state-of-the-art. Finally, conclusions are drawn in Section V.

II. SYSTEM ARCHITECTURE

Fig. 1 shows the block diagram of the proposed RC frequency reference. It consists of a digital frequency-locked loop (FLL) in which the output frequency f_{DCO} of a delta-sigma digitally controlled oscillator ($\Delta\Sigma\text{DCO}$) is locked to a frequency-dependent but temperature-independent phase shift, ϕ_e shown in Fig. 1.

The required phase-shift ϕ_e is realized by compensating for the temperature dependency of the frequency-dependent phase shift of an on-chip Wien Bridge (WB) filter ϕ_{WB} shown Fig. 1. The choice of a WB filter represents a trade-off between phase sensitivity and the number of passive components required. Furthermore, being a band-pass filter, it effectively rejects low-frequency (power-supply) noise components in the DCO's output. This is a significant advantage over a polyphase filter [11], which only requires four passive components, but is an all-pass filter.

The phase shift ϕ_{WB} of a WB filter is given by

$$\phi_{\text{WB}}(f, T) = -\tan^{-1}\left(\frac{R_{\text{pp}}(T)^2 C^2 (2\pi f)^2 - 1}{3R_{\text{pp}}(T)C(2\pi f)}\right) \quad (1)$$

where C is a temperature-independent on-chip MIM capacitor and $R_{\text{pp}}(T)$ is the resistance of a temperature-dependent p-poly resistor. The latter can be expressed by

$$R_{\text{pp}}(T) = R_0(1 + \text{TC}_1(T - T_0) + \text{TC}_2(T - T_0)^2 + \dots) \quad (2)$$

where TC_1 and TC_2 are the first- and second-order TCs of the resistor. The center frequency of the WB at T_0 can then be written as

$$f_0 = \frac{1}{2\pi R_0 C}. \quad (3)$$

As in [8], the phase-shift of the WB filter is digitized by a second-order phase-domain delta-sigma modulator

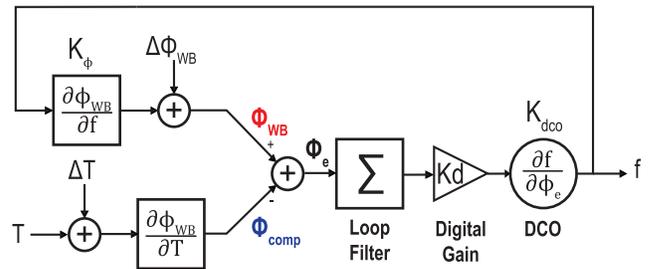


Fig. 2. Simplified linear model of the temperature compensation scheme.

($\text{PD}\Delta\Sigma\text{M}$). Due to the TC of R_{pp} , its decimated output ϕ_{WB} will be both frequency- and temperature-dependent (Fig. 1). To compensate for this, die temperature is determined by a WhB temperature sensor, whose output is digitized by a continuous-time delta-sigma modulator ($\text{CT}\Delta\Sigma\text{M}$) [22]. Its decimated output μ_{WhB} is temperature-dependent, but frequency-independent (Fig. 1). By using a polynomial mapping function, $p(\cdot)$, μ_{WhB} can then be mapped to the inverse of ϕ_{WB} , resulting in ϕ_{comp}

$$\phi_{\text{comp}} = -\phi_{\text{WB}}|_{f=f_{\text{DCO}}} = p(\mu_{\text{WhB}}). \quad (4)$$

The resulting compensated phase error, ϕ_e , crosses 0 at the intended target frequency f_{REF} . Due to the infinite dc gain of the digital accumulator, f_{DCO} will lock to f_{REF} at steady state.

A. Inaccuracy Analysis

The overall accuracy of the proposed frequency reference can be analyzed with the help of the simple linear model shown in Fig. 2. Here, the WB is modeled as a frequency to phase converter that introduces phase errors $\Delta\phi_{\text{WB}}$ due to component spread. Similarly, the WhB is modeled as an ideal temperature sensor with additive errors ΔT .

The DCO output frequency is converted to phase via the frequency sensitivity of ϕ_{WB} , which is given by

$$K_\phi = \left. \frac{\partial\phi_{\text{WB}}}{\partial f} \right|_{\substack{f=f_0 \\ T=T_0}} = -\frac{4\pi}{3} R_0 C. \quad (5)$$

The WhB then temperature compensates this phase via the compensation polynomial $p(\cdot)$. Neglecting the higher-order

TCs of $R_{pp}(T)$, the temperature sensitivity of the output phase of the WB is given by

$$\left. \frac{\partial \phi_{WB}}{\partial T} \right|_{f=f_0} = -\frac{2}{3} TC_1. \quad (6)$$

The contribution of $\Delta \phi_{WB}$ to the output frequency error, Δf , in the steady-state condition, where $\phi_e = 0$, is

$$\phi_e = 0 = \Delta f \frac{\partial \phi_{WB}}{\partial f} + \Delta \phi_{WB} \quad (7)$$

$$\Delta f = \Delta \phi_{WB} \frac{\partial f}{\partial \phi_{WB}} = \Delta \phi_{WB} \frac{-3}{4\pi R_0 C}. \quad (8)$$

From (8), the variance of the output frequency, σ_f^2 , due to the variance of phase spread, σ_ϕ^2 , is then

$$\frac{\sigma_f}{f_0} = \left| \frac{\Delta f}{\Delta \phi_{WB}} \right| \frac{1}{f_0} \sigma_\phi = \frac{3}{2} \sigma_\phi. \quad (9)$$

This result indicates that phase errors in the WB filter, e.g., errors due to component spread, will manifest themselves as output frequency errors. As in [8], these can be effectively reduced by a two-point trim.

Similarly, the contribution of ΔT to the output frequency error, Δf , in the steady-state condition is

$$\phi_e = 0 = \Delta f \frac{\partial \phi_{WB}}{\partial f} - \Delta T \frac{\partial \phi_{WB}}{\partial T} \quad (10)$$

$$\Delta f = \Delta T \frac{\partial \phi_{WB}}{\partial T} \frac{\partial f}{\partial \phi_{WB}} = \Delta T \frac{TC_1}{2\pi R_0 C}. \quad (11)$$

The variance of the output frequency, σ_f^2 , due to the variance of temperature error, σ_T^2 , is then given by

$$\frac{\sigma_f}{f_0} = \left| \frac{\Delta f}{\Delta T} \right| \frac{1}{f_0} \sigma_T = |TC_1| \sigma_T. \quad (12)$$

As expected, this result shows that the TC of the WB should be minimized to suppress the contribution of temperature sensor inaccuracy to errors in the output frequency.

A similar analysis for a dual-RC frequency reference [8] where two WB sensors with temperature errors $\sigma_{T_{1,2}}^2$ and resistor TCs $TC_{1,2}$ yields the following:

$$\frac{\sigma_f}{f_0} = \frac{\sqrt{\sigma_{T_1}^2 + \sigma_{T_2}^2}}{\left| \frac{1}{TC_1} - \frac{1}{TC_2} \right|}. \quad (13)$$

In contrast to (12), the contribution of temperature errors to frequency error is determined by the TCs of two different types of resistors. Ideally, resistors with complementary TCs of similar magnitude should be used. This limits the applicability of the dual-RC architecture in processes where only a low-TC resistor is available.

B. Bridge and Sensor Design

To maximize frequency reference accuracy, the WB was realized with p-type polysilicon resistors (TC = -200 ppm/°C, lowest in the chosen process) and MIM capacitors (TC = -30 ppm/°C). As a result, the inaccuracy of the WhB temperature sensor, typically less than 0.2 °C [22], will only cause frequency errors in the order of ~ 50 ppm.

To optimize its energy efficiency, the temperature sensitivity of the WhB temperature should be maximized. In [22], this was done by using silicided-diffusion resistors (TC₁ = 3300 ppm/°C) and n-polysilicon resistors (TC₁ = -1500 ppm/°C). In this work, however, to ensure that the accuracy of the frequency reference is limited by the spread of only two types of resistors, the n-poly resistors were replaced by p-poly resistors.

C. Frequency Control Loop Design

The FLL dynamics can be approximately modeled as a single-pole system due to the dominant very low-frequency pole introduced by the digital accumulator. For this single-pole approximation to hold, all nondominant poles (including the DSM integrators and any filtering in the DCO) should be considerably higher than the intended loop bandwidth. In addition, the digital loop filter has to operate at a significantly higher sample rate than the loop bandwidth.

To approximate the FLL bandwidth, the digital accumulator in Fig. 2 can be replaced by a normalized continuous-time integrator with $H(s) = 1/s$. The blocks are replaced by their small-signal sensitivities, where K_{dco} is the digital-to-frequency sensitivity of the DCO, K_d is a digital gain, and K_ϕ is the frequency-to-digital sensitivity of the WB readout defined in (5). Then, the transfer function of the noise in the phase readout ($n_{\phi_{WB}}$ injected at $\Delta \phi_{WB}$) to the output frequency has a low-pass characteristic

$$\frac{f}{n_{\phi_{WB}}} = \frac{K_{DCO}}{s - K_d K_\phi K_{DCO}}. \quad (14)$$

Conversely, the transfer function of the noise injected after the loop accumulator (i.e., DCO phase noise) to the output frequency has a high-pass characteristic

$$\frac{f}{n_f} = \frac{s K_{DCO}}{s - K_d K_\phi K_{DCO}}. \quad (15)$$

The bandwidth of both transfer functions is defined by the frequency sensitivity of the WB, the phase-to-frequency sensitivity of the DCO, and the digital gain, K_d . Making the digital gain programmable thus allows the overall loop bandwidth to be flexibly set.

The FLL needs to be fast enough to track thermal transients, which will depend on the thermal time constant of the die and its packaging. Furthermore, a higher loop bandwidth has the benefit of attenuating the oscillator's low-frequency offset and noise. For stability, however, the bandwidth of the loop is limited to a fraction of its sampling rate. In this design, the loop bandwidth is set to around ~ 50 Hz, which is enough to compensate for thermal transients [20] and some of the oscillator's $1/f$ noise, but not enough to filter out the majority of the oscillator's wideband noise.

III. CIRCUIT DESIGN

A. $\Delta \Sigma$ Modulator Readouts

The DFLL locks its output frequency to the digitally temperature-compensated phase shift of the WB. As shown in Fig. 3, the WB phase and the WhB output are digitized

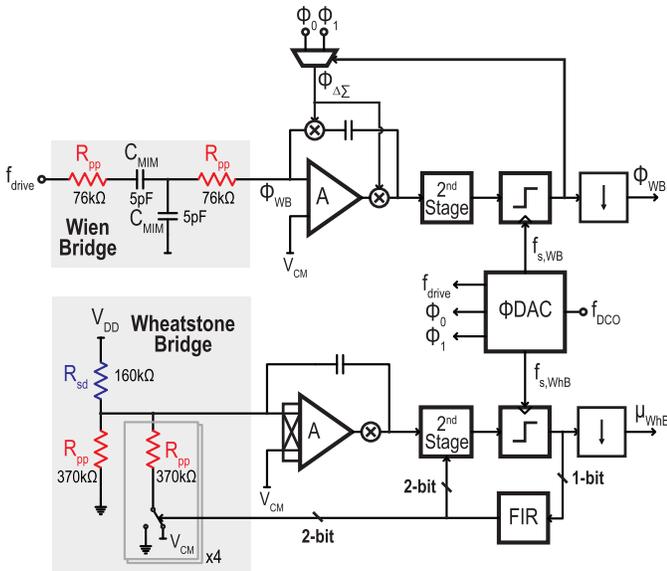


Fig. 3. Simplified single-ended schematic diagrams for the WB and WhB $\Delta\Sigma$ modulator readouts.

by a phase-domain delta-sigma modulator (PD $\Delta\Sigma$ M) and a CT $\Delta\Sigma$ M).

The PD $\Delta\Sigma$ M [21] utilizes a two-stage feed-forward architecture with a 1-bit quantizer and an integrated synchronous demodulator. The fully differential WB is constructed with $R_{pp} = 76 \text{ k}\Omega$ and $C_{MIM} = 5 \text{ pF}$. The WB is driven at $f_{drive} = f_{DCO}/32 = 500 \text{ kHz}$. The phase of its output current is then detected by a chopper demodulator embedded in the feedback loop of the first integrator. This also mitigates the offset and $1/f$ noise of the first-stage amplifier [21]. The choppers are driven by phase references $\phi_0 = 90^\circ$ and $\phi_1 = 90^\circ + 11.25^\circ$ at f_{drive} , to accommodate the expected phase variation of the WB filter. As in [21], the second stage of the modulator is a switched-capacitor integrator. Finally, a 1-bit quantizer generates the digital output bitstream. The gain of the $\Delta\Sigma$ loop drives the average input current of the first integrator to zero, which ensures that the selected phase references are, on average, in quadrature with ϕ_{WB} . Thus, the bitstream output of the PD $\Delta\Sigma$ M is a digital representation of the WB phase shift.

The CT $\Delta\Sigma$ M [22] employs a second-order feed-forward architecture with a 1-bit quantizer and 2-bit (four-tap) FIR DAC. The WhB employs p-poly $R_{pp} = 370 \text{ k}\Omega$ ($TC_1 = -200 \text{ ppm}/^\circ\text{C}$) and silicided-diffusion $R_{sd} = 160 \text{ k}\Omega$ ($TC_1 = 3300 \text{ ppm}/^\circ\text{C}$) resistors. The 2-bit DAC also employs p-poly resistors. The modulator's loop gain drives the error current flowing into the first integrator to 0, which ensures that the bitstream, on average, will represent the temperature-dependent ratio of the WhB and DAC resistors. Choppers mitigate the offset and $1/f$ noise of the first-stage amplifier. The second stage is a switched capacitor integrator, with a feedback path to compensate for the delay introduced by the FIR-DAC.

Compared to [8] the combined power of the two $\Delta\Sigma$ Ms is reduced to $100 \mu\text{W}$ from $320 \mu\text{W}$, via the scaling of the bridge resistors and using power-optimized first-stage amplifiers [21].

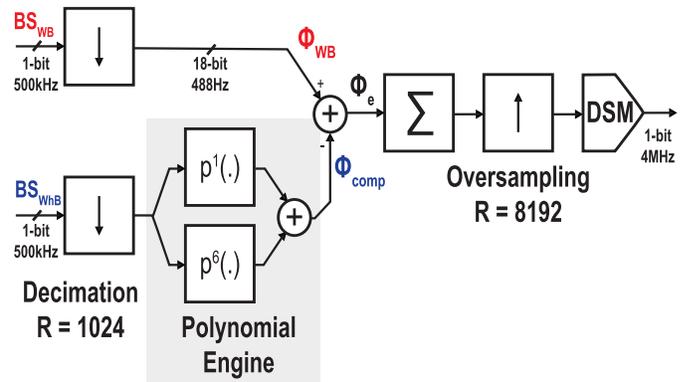


Fig. 4. Block diagram of the digital loop filter and temperature compensation.

B. Digital Loop Filter and Temperature Compensation

The bitstream outputs of the two modulators are applied to the digital loop filter (DLF), where they are decimated and then subtracted (Fig. 4). The resulting error signal ϕ_e is then applied to a digital accumulator whose output drives a DCO.

The 500-kHz input bitstreams are decimated by second-stage CIC filters [23]. A decimation factor of 1024 sets the sampling rate of the DLF to 488 Hz, which is $\sim 10\times$ larger than the loop bandwidth. The CIC output words are quantized to 18 bits before polynomial processing, ensuring that any additional quantization error is well below the readouts' noise floor.

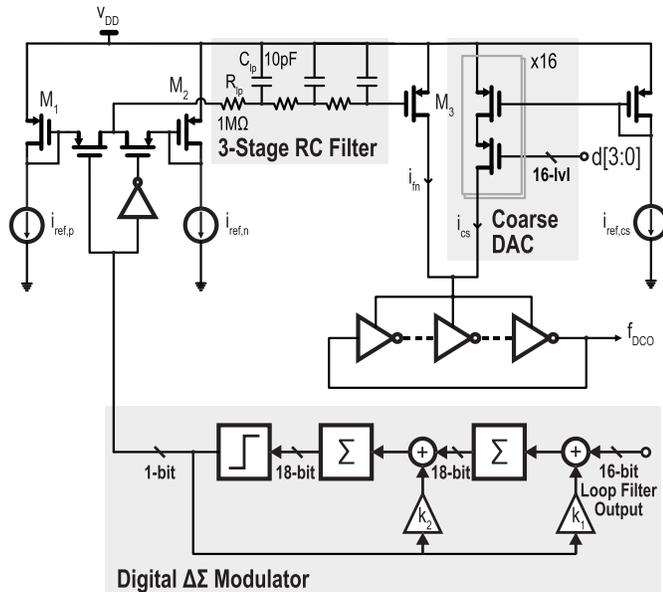
The polynomial engine processes the decimated output of the WhB $\Delta\Sigma$ M and realizes the function p , where $p(\mu_{WhB}) = \mu_{WB}$. The block implements a sixth-order polynomial with 20-bit programmable coefficients. Only the coefficients a_0 and a_1 are utilized in the two-point only mode, implementing a linear fit p^1 . In the two-point (per-sample) + batch mode (single polynomial for all samples), a parallel p^6 branch is added. In the actual implementation, both branches are mathematically combined into a single sixth-order polynomial and loaded to the coefficient engine.

Finally, the loop integrator output is converted to a 1-bit, 4-MHz bitstream that drives the DCO through a digital $\Delta\Sigma$ modulator after oversampling, detailed in Section III-C.

C. $\Delta\Sigma$ Digitally Controlled Oscillator

The 16-MHz output frequency of the DCO (Fig. 5) is divided down and used to drive the WB and all the other system components, including the $\Delta\Sigma$ M readouts and the DLF.

As mentioned in Section II-C, since the DCO is in a high-gain feedback loop, the requirements on its own frequency accuracy are relaxed. However, the loop bandwidth is only about 50 Hz, and so it does not suppress the DCO high-frequency noise, which then determines the overall jitter performance. As a result, a high-resolution DCO is required. In addition, its control range must be wide enough to cover the effect of PVT variations on its center frequency, and it must have a monotonic transfer function to maintain stability. To meet these requirements, a segmented coarse/fine structure

Fig. 5. Schematic diagram of the $\Delta\Sigma$ DCO.

architecture is adopted. In [8], a 5-bit current steering and a 13-bit fine $R - 2R$ DAC were combined, but the latter occupied significant area, resulting in a total DCO area of 0.35 mm^2 . In this work, the fine DAC is implemented by a 1-bit DAC driven by a digital $\Delta\Sigma$ modulator (D $\Delta\Sigma$ M). This provides intrinsic monotonicity in a much smaller (analog) area of 0.05 mm^2 , a $7\times$ reduction.

Fig. 5 shows the schematic diagram of the $\Delta\Sigma$ DCO. The programmable output frequency (16 MHz) is provided by a 9-stage single-ended current-starved ring oscillator controlled by two coarse/fine current DACs. The coarse control is achieved by a 4-bit current-steering DAC ($i_{cs} = 50 \mu\text{A}$ nominal), covering the expected $\pm 40\%$ process variation around the center frequency and remains static during operation. The nominal coarse code is determined manually for each batch in an initial characterization and used for all samples. The fine control is achieved with the combination of a digital $\Delta\Sigma$ modulator (D $\Delta\Sigma$ M) and a 1-bit current steering DAC ($i_{fn} = 18 \mu\text{A}$ nominal) with an integrated low-pass filter, covering the expected $\pm 7.5\%$ frequency variation due to temperature and supply voltage variations.

Compared to [8] the DCO power is reduced to $120 \mu\text{W}$ from $450 \mu\text{W}$, via the scaling of the ring oscillator core at the cost of worse open-loop noise. The closed-loop operation of the FLL relaxes the DCO noise requirements and yields a lower power design.

The digital $\Delta\Sigma$ modulator (implemented on the FPGA) employs a two-stage feedback architecture with 18-bit digital integrators. It oversamples the 16-bit MSBs of the loop filter output (operating at $500 \text{ kHz}/1024$) by a factor of 8192, resulting in a sampling rate of 4 MHz. To filter out the modulator's quantization noise, a third-order cascaded RC low-pass filter is used. The filter has a 4 kHz corner frequency, which results in a residual quantization error of < 30 ppm.

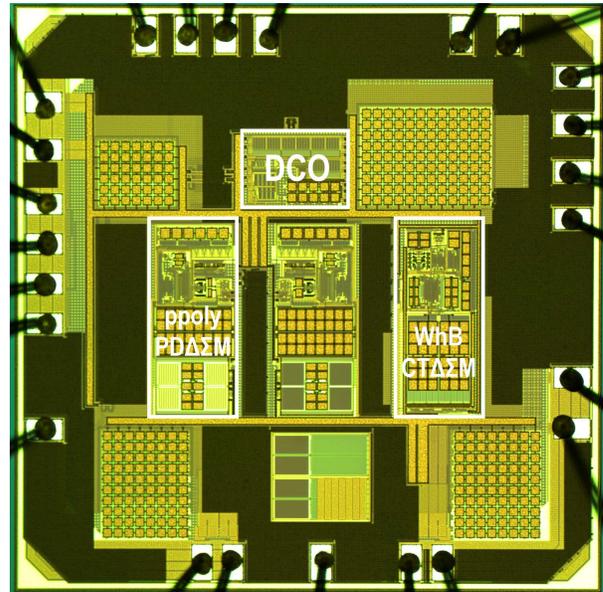


Fig. 6. Die micrograph of the RC frequency reference.

The bitstream selects drives the filter by selecting two diode voltages (M_1 and M_2) generated by two reference currents, $i_{ref,p}$ and $i_{ref,m}$. The reference generator is based on an n -poly resistor whose TC partially compensates for the TC of the ring oscillator. The filter's output voltage is converted back to a current by M_3 and then applied to the ring oscillator core. Although the overall digital code to frequency characteristic of the resulting DCO is not linear, its monotonicity is guaranteed by design. This nonlinearity is not significant enough to impact loop dynamics in this design.

IV. MEASUREMENT RESULTS

The RC frequency reference (Fig. 6) was implemented in a TSMC $0.18 \mu\text{m}$ standard CMOS process. The total active area is 0.3 mm^2 , where WB + PD $\Delta\Sigma$ M and WhB + CT $\Delta\Sigma$ M occupy 0.125 mm^2 each and the $\Delta\Sigma$ DCO occupies 0.05 mm^2 . Digital components of the DFLL (decimation filters, temperature compensation, loop filter, and the digital $\Delta\Sigma$ M) were realized off-chip in an FPGA. An area-optimized version [10] of the digital design is estimated to consume 0.1 mm^2 area in the same process. The 20 samples from a single batch were packaged in ceramic DIL24 packages.

The WB + PD $\Delta\Sigma$ M and WhB + CT $\Delta\Sigma$ M both dissipate about $50 \mu\text{W}$ from a 1.8-V supply. The $\Delta\Sigma$ DCO (excluding the digital $\Delta\Sigma$ M) dissipates $120 \mu\text{W}$ from a 1.8-V supply. Simulations (post-synthesis) show that the off-chip digital would consume about $60 \mu\text{W}$ if implemented in the same process.

The trimming procedure consists of three sequential steps. A first temperature measurement is conducted to determine the values of the $\Delta\Sigma$ M outputs in the closed-loop FLL configuration. Then, from the obtained values, the trimming polynomials are calculated. Finally, another temperature measurement is conducted where the polynomials calculated in

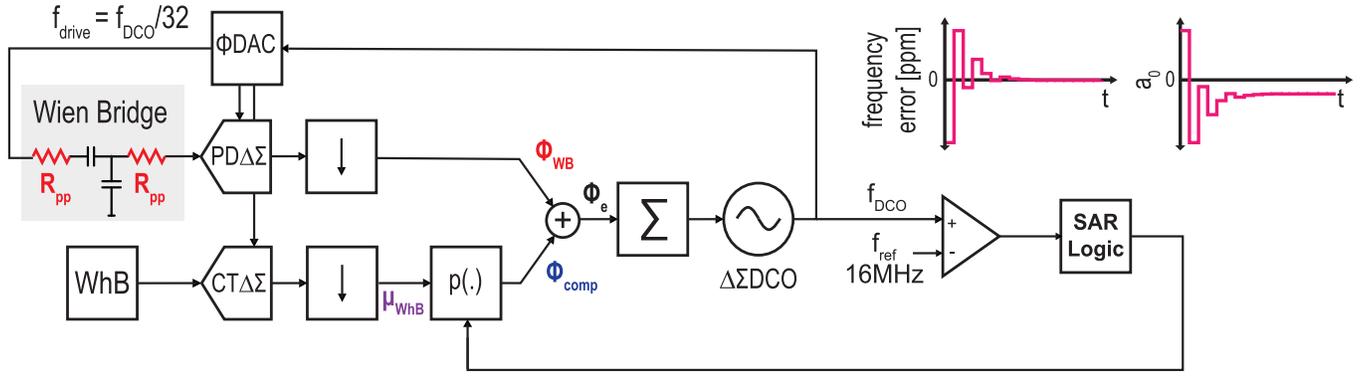


Fig. 7. Block diagram of the RC frequency reference under the trimming setup showing the convergence of the output frequency to the target reference as the coefficient a_0 is trimmed.

step 2 are loaded into the FLL, and frequency reference error is measured.

To start the trimming process, the FLL was placed in closed-loop and the a_1 coefficient of the first-order polynomial (p^1) was set to the value expected from simulations. Using the expected value of a_1 during trimming reduces the temperature sensitivity of the output frequency, alleviating the requirement for high temperature-stability during measurement. Using a SAR algorithm a_0 was then tuned, by comparing the DFLF output frequency to the 16-MHz target (Fig. 7). The 18 steps were sufficient to ensure that the residual error in the DFLF output frequency is <10 ppm, at which point the final values for a_0 and μ_{WhB} are recorded.

Since the input of the DLF is 0 at steady state, the WB output μ_{WB} can be calculated from the recorded values of a_0 and μ_{WhB} . Fig. 8(a) and (b) shows the measured WhB output μ_{WhB} and the calculated μ_{WB} for each sample. The two outputs are similarly nonlinear functions of temperature. Fig. 9(a) shows a plot of μ_{WB} versus μ_{WhB} , together with the first-order polynomial (p^1) that passes through the points obtained at -35°C and 75°C . p^1 constitutes the linear (two-point trim) component of the temperature compensation polynomial and as shown in Fig. 9(b) results in only a small frequency error. To achieve higher accuracy, a sixth-order polynomial (p^6) was fitted to the average residual error, $\mu_{\text{WB}} - p^1(\mu_{\text{WhB}})$, of all samples. p^6 is the same across all samples and constitutes the batch component of the temperature compensation.

It is important to note that nowhere in the characterization and trimming steps was a temperature measurement utilized. Thus, in contrast to [8], a temperature sensor during characterization is not required, which increases the industrial potential of the trimming scheme.

Following the extraction of the temperature compensation polynomials p^1 and p^6 , the samples were characterized again over the target range from -45°C to 85°C in two modes: linear and higher-order temperature compensated. In the linear scheme, only p^1 (different for each sample) was loaded into the polynomial engine. Fig. 10 shows that the linear temperature compensated frequency reference achieves ± 385 ppm frequency accuracy (20 samples), resulting in a residual TC of 5.7 ppm/ $^\circ\text{C}$. The similarity in the characteristics of the residual

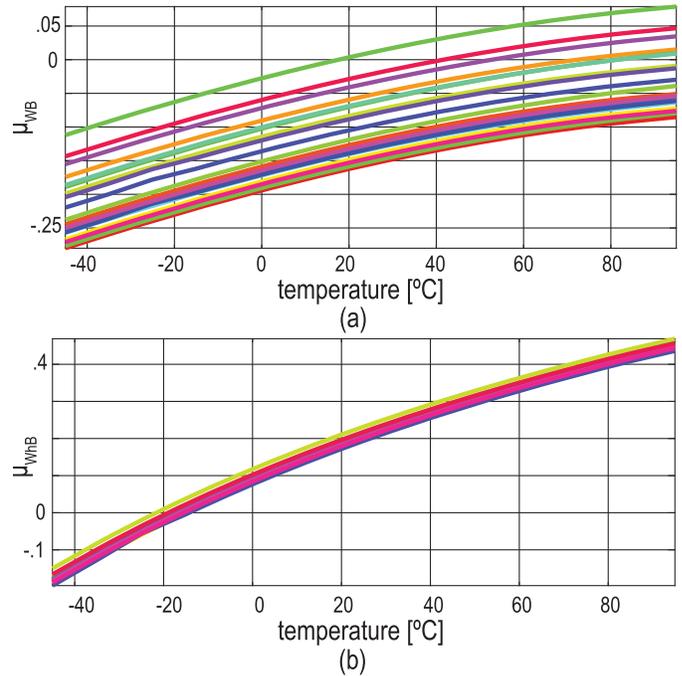


Fig. 8. Measured bitstream average μ_{WhB} for the WhB + CT $\Delta\Sigma$ M and μ_{WB} for the WB + PD $\Delta\Sigma$ M over temperature for each sample.

error in Fig. 9(b) and the frequency error in Fig. 10 highlights the resolution achieved during the trimming procedure. In the higher-order temperature compensated mode, p^6 (same for all samples) was added to p^1 (different for each sample) and loaded into the polynomial engine. Fig. 11 shows that the higher-order temperature compensated frequency reference achieves ± 90 ppm frequency accuracy (20 samples), resulting in a residual TC of 1.3 ppm/ $^\circ\text{C}$ (box method).

To verify the robustness of the proposed temperature compensation to process variation, 8 samples from a second batch were characterized. Fig. 12 shows the frequency error estimated from the linear compensation residuals for the two batches. To maintain $<\pm 100$ ppm inaccuracy of the higher-order temperature compensation, samples from each batch require p^6 to be characterized from a statistically significant set from each batch. The expected frequency inaccuracy

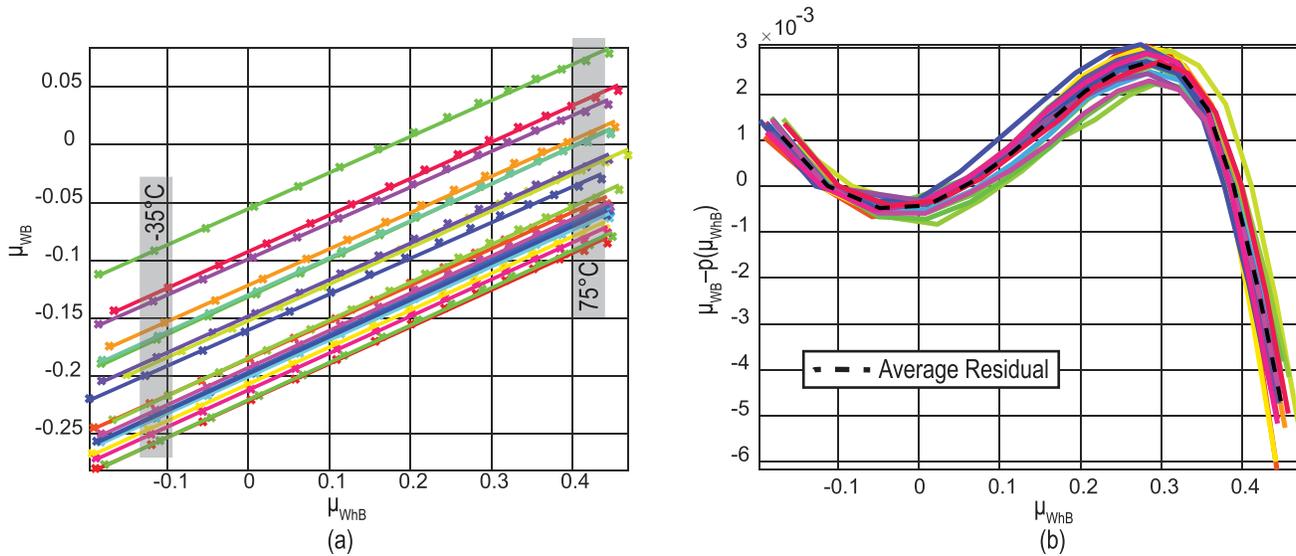


Fig. 9. (a) Measured (markers) WB bitstream output, μ_{WB} , mapped to the measured WhB bitstream output, μ_{WhB} , and the first-order fit using the two highlighted trimming points at -35 °C and 75 °C (straight line) (b) Residual output of the temperature compensation after the first-order fit is removed and the average residual.

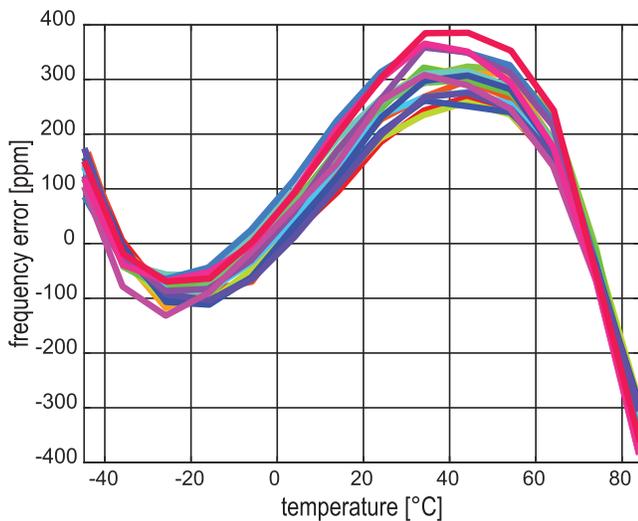


Fig. 10. Inaccuracy of the 2-point temperature compensated frequency reference.

increases to ± 200 ppm if the p^6 from one batch is used in the second. On the other hand, linear compensation (p^1) is robust to process variations and guarantees $< \pm 400$ ppm inaccuracy.

For supply sensitivity characterization, the 1.8-V nominal power supply voltage was varied between 1.6 and 2 V. The worst-case sample shows a 500 ppm frequency shift, resulting in a voltage coefficient of 0.12%/V.

Fig. 13 shows the period jitter of the frequency reference to be 39 ps and the open-loop $\Delta\Sigma$ DCO (driven by a constant input digital $\Delta\Sigma$ M) to be 37 ps, indicating that the DCO dominates the period jitter of the system. The increase in closed-loop jitter is attributed to the DCO noise transfer function's peaking characteristic to the FLL output. By using the frequency reference as the reference oscillator of a low-bandwidth PLL system, much of the DCO high-frequency

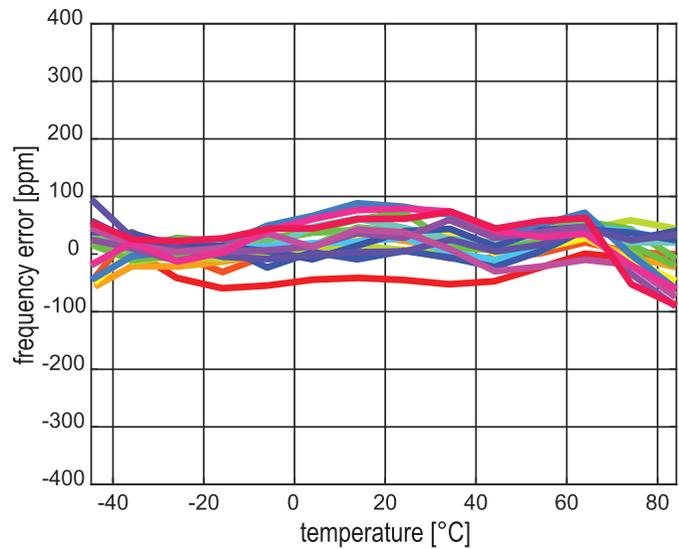


Fig. 11. Inaccuracy of the 2-point and higher-order batch temperature compensated frequency reference.

jitter can be filtered out. Fig. 14 shows the results of an Allan Deviation measurement. The frequency reference achieves 320 ppb in an 8-s stride, which is a significant improvement on the 20 ppm of the open-loop $\Delta\Sigma$ DCO.

Table I summarizes the performance of the frequency reference with both compensation schemes and compares it with state-of-the-art high-accuracy RC frequency references. The high-power consumption of this work is mainly due to the chosen $\Delta\Sigma$ DCO architecture and its low jitter requirement. With a straightforward linear temperature compensation, the frequency reference achieves ± 400 ppm inaccuracy, which, moreover, is robust to batch-to-batch variations. With the higher-order temperature compensation scheme, the proposed

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO THE PRIOR ART

	This Work	[8]	[9]	[10]	[11]	[12]	[13]	[14]
Process [nm]	180	180	65	180	65	180	180	65
Frequency [Hz]	16M	7M	32M	16M	28M	2M to 40M	24M	100M
Power [W]	220u ¹	775u ¹	34u	88u ¹	142u	2.9m	200u	101u
Area [mm ²]	0.3 ²	1.59 ²	0.18	0.14 ²	0.06	1.04	0.17	0.07
# of Trim. Points	2	2+Batch	2+Batch	2	1+Batch	2+Batch	2	3
Inaccuracy [ppm]	±385	±90	±170	±530	±400	±200	±170	±140
T Range [°C]	-45 to 85	-45 to 85	-45 to 85	-45 to 85	-45 to 85	-25 to 85	-40 to 150	-40 to 95
Supply sensitivity [%/V]	0.12	0.18	0.0082	0.2	0.29	0.49	0.03	0.008
Supply Range [V]	1.6 to 2.0	1.7 to 2.0	1.1 to 3.3	1.6 to 2.0	0.85 to 1.05	0.85 to 1.4	1.8 to 5.0	1 to 1.4
# of Samples	20	12	6	18	12	1	>200	20
Period Jitter [ps]	39.9	23.8	24.4	10.2	7	-	-	13.3
ADEV [ppm]	0.32	0.33	2.5	0.35	2	63	-	1.6

¹ Does not include the power of the off-chip digital blocks

² Does not include the area of the off-chip digital blocks

³ Worst case TC computed as $\mu+6\sigma$ from $\mu=3.3\text{ppm}/^\circ\text{C}$ mean and $\sigma=2.45\text{ppm}/^\circ\text{C}$ standard deviation over 200 samples

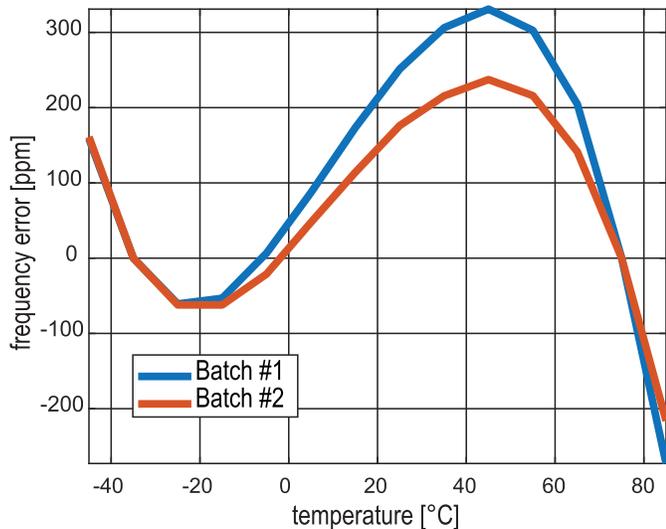


Fig. 12. Average frequency error estimations from two batches, showing shifted nonlinear residual frequency error curves.

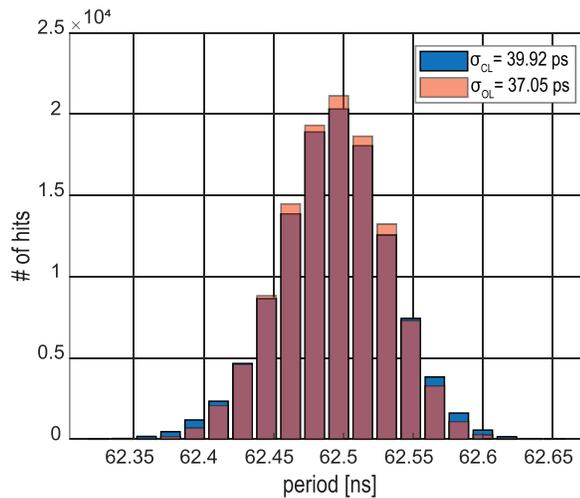


Fig. 13. Period jitter of the closed-loop and open-loop frequency reference.

frequency reference achieves an inaccuracy of ± 90 ppm, which is the best result reported for an RC frequency reference.

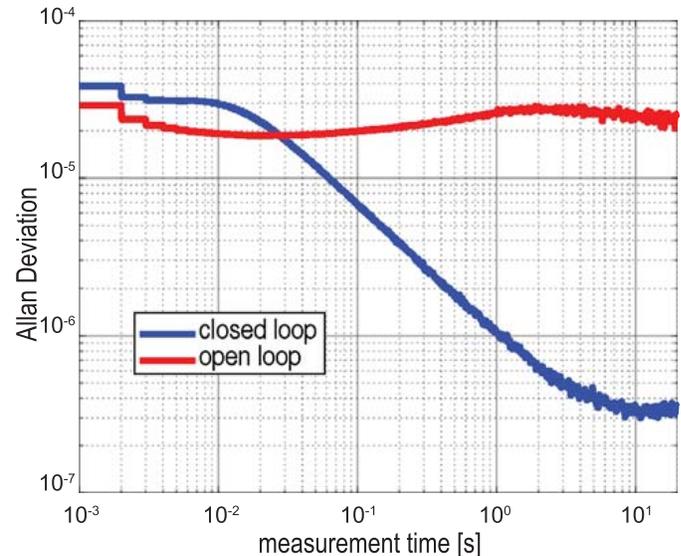


Fig. 14. Allan deviation of the closed-loop and open-loop frequency reference.

V. CONCLUSION

This article presents a 16-MHz RC frequency reference realized in a $0.18\text{-}\mu\text{m}$ CMOS process that utilizes a FLL with digital temperature compensation. The phase response of an integrated RC filter (WB) is compensated with a resistor-based temperature sensor (WhB) and used to realize an accurate on-chip time constant. The frequency of an inaccurate DCO is locked to this time constant through a digital FLL. This scheme achieves better accuracy (± 90 ppm over 20 samples), lower power, lower area, and comparable long-term stability compared to state-of-the-art. Characterization of two batches shows that the methodology applies to standard CMOS production. By demonstrating $< \pm 100$ ppm inaccuracy for the first time, this work asserts the viability of integrated RC frequency references as fully integrated solutions.

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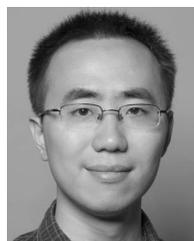
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