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High-Power Digital Transmitters for Wireless Infrastructure Applications (A Feasibility Study)

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***Abstract*— Fully digital transmitters (DTXs) have the potential of replacing analog-intensive transmitter (TX) line-ups in future massive multiple-input and multiple-output (mMIMO) systems since they hold the promise of higher system integration level and energy efficiency. DTX operation so far has been limited to low RF output powers. This article introduces a concept that enables high-power DTX operation. A DTX demonstrator targeting both high output power and high efficiency is realized as a proof of concept. It is based on a custom V_T-shifted laterally-diffused MOS (LDMOS) technology, which is utilized to implement a segmented high-power output stage operated in class-BE. A low-voltage high-speed 40-nm CMOS controller drives the individual output stage segments at gigahertz rates. Measurements show the promising results for the proposed high-power DTX concept and provide valuable lessons for future DTX implementations.**

***Index Terms*— Class-E, CMOS, digital predistortion (DPD), digital transmitter (DTX), efficient, GaN, high-power RF, laterally-diffused MOS (LDMOS), mixing power digital-to-analog converter (DAC), polar.**

I. Introduction

THE introduction of massive multiple-input and multiple-output (mMIMO) communication systems has increased the need for low-cost, highly integrated, and energy-efficient transmitter (TX) line-ups. Unfortunately, today's analog-intensive TX architectures suffer from poor integration while having severe linearity/efficiency tradeoffs. Moreover, their standby power dissipation in low data traffic situations remains high, which is a big concern given the operational costs of mMIMO systems. Fully digital-TX (DTX) line-ups can, in theory, provide lower standby power, improved integration, higher functionality (e.g., independently controllable Doherty branches), and (re)configurability (e.g., changing operating frequency or upconversion scheme without changing core hardware) at reduced design logistics and costs. However, DTX works published so far use almost exclusively advanced high-speed CMOS/silicon on insulator (SOI) technologies with low breakdown voltages for their active devices, limiting the maximum achievable RF voltage and RF power. As a result, all reported fully integrated DTX CMOS/SOI implementations are limited to 2–3 W of peak RF output power [1], [2]. Furthermore, since CMOS/SOI technologies are optimized for digital applications and have limitations in their active devices and metal stack, they can only offer moderate drain efficiencies, e.g., below 55% [2]. Hybrid DTX approaches, using combinations of CMOS/SOI with a high-voltage/high-power RF technology (e.g., laterally-diffused MOS (LDMOS) or GaN), are less frequently reported. This approach yields two main difficulties: first, to obtain a high enough gate–source voltage swing to activate the (LDMOS/GaN) RF power device, as an RF power technology is optimized for drain efficiency and linearity, yielding a high threshold voltage (V_T), and second, to effectively switch their (very) large input capacitance C_{GS} (typically tens of pF).

To avoid these difficulties, DTX hybrid approaches often use an analog interface to drive the final output stage. For example, in [3], a DTX is used to drive a common-gate GaN power amplifier (PA) output stage in current mode, which yields scaling limitations toward higher frequencies and power levels (above 10 W becomes very challenging). Also, digital-intensive implementations of envelope elimination and restoration (EER) [4] and out-phasing TX line-ups [5] have been reported. In [5], the output stages are driven fully digital using dedicated high-breakdown CMOS devices [6], which requires the input capacitance of the output stage to be fully charged and discharged for every RF cycle by the preceding driver. As such, the digital operation of the RF output stage demands a constant input/drive power, which in deep power back-off can be even larger than the desired RF output power itself. As a result, the overall system efficiency will be low when handling signals with a high peak-to-average power ratio (PAPR). In addition, using a large output stage, which is always hard-driven in its totality, can cause dynamic range limitations [7].

This work proposes a low-voltage DTX controller in combination with a segmented (V_T-shifted) FET-based high-power output stage. Such a combination can enable true

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DTX operation, which is perfectly scalable to high power levels. More importantly, the controller's power consumption is (linearly) proportional to its RF output voltage, enabling high TX system efficiencies that can offer dramatic power savings in standby or low traffic conditions. This article explores the feasibility of such a high-power DTX approach with its underlying technology and design challenges (Sections II and III), providing an extended, more detailed description of the work published in [8]. Section IX gives the DTX realization and its static and dynamic measurement results, demonstrating its high output power and system efficiency. Furthermore, it shows that modulated signals can be handled within the constraints of the technology, interconnect, and assembly methods used in the DTX prototype. The primary goal of this article is, however, to provide the reader with the (costly) lessons learned designing world first >10-W segmented power DTX, yielding a set of clear guidelines and directions for developing a new, improved generation of power DTX line-ups that can replace power-hungry analog-intensive TX line-ups in future mMIMO systems. For this purpose, this article starts with the underlying hardware challenges, which are tackled in a step-by-step approach.

II. Power-DTX Technology Considerations

In a power-DTX line-up, the (segmented) RF output stage will use binarily quantized driving signal(s) that will put the output stage (segments) in either "ON" or "OFF" mode. Achieving high efficiency from an RF output stage requires an n-type FET device in LDMOS or an HEMT device in GaN technology. The driver of this output stage needs to provide very fast charging and discharging of the input capacitance of the RF output stage to guarantee digital switch-mode operation. A class-D driver using complementary devices is typically considered the most logical candidate to perform this action. In LDMOS or GaN technologies, unfortunately, there are no p-type devices available with adequate performance.

Consequently, the driver needs to be implemented in (a separate) high-speed CMOS or SOI technology. Given this topology, the RF output stage and its (off-chip) class-D driver can be modeled by switching elements with resistance, as shown in Fig. 1(b). Here, the driver's equivalent resistances are denoted by R_{dr}, with the additional subscripts n and p for nMOS and pMOS devices, respectively. The RF output stage's ON-resistance is denoted by R_{ON}. Since two different integrated circuits (ICs) in technologies are used, protection against electrostatic discharge (ESD) and interconnect parasitics need to be considered as well. In Fig. 1(b), these are modeled by shunt capacitances ($C_{\mathrm{ESD1,2}}$) and series inductor (L_{bond}) and resistor (R_{bond}).

Considering the ON/OFF activation of the RF output stage, a resonant switch-mode PA (SMPA) operating class seems to be the most logical choice to achieve high energy efficiency. In view of this, class-E is favored over (inverse) class-F operation since it is challenging to realize harmonic open conditions for a high-power device with a large output capacitance (e.g., approximately 0.3 $\mathrm{pF\,W^{-1}}$ for LDMOS technology). Furthermore, class-E stands out with a theoretical drain efficiency

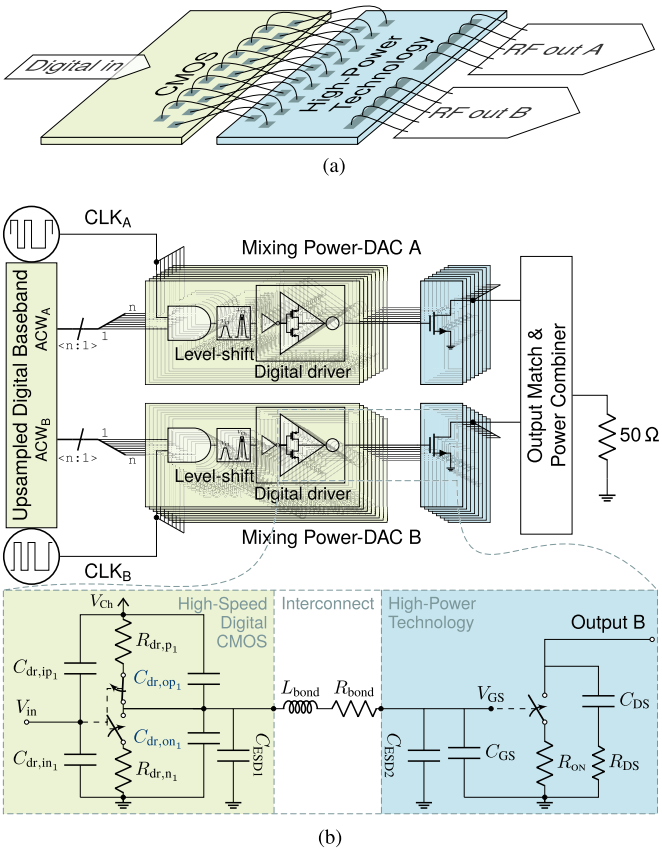


Fig. 1. Conceptual diagrams of (a) proposed RF high-power mixing-DAC configuration using a CMOS controller and a gate-segmented high-power output stage. (b) Top-level diagram of the proposed power DTX, with below the circuit diagram of a single (digital) segment of the mixing power-DAC, showing in detail the parasitics of the final stage of the tapered buffer chain and its connection to a gate segment of the high-power output stage.

of 100% while benefiting from a simple circuit topology [9]. Practical implementations, however, will be restricted in their peak drain efficiency by limitations imposed by the used technology in relation to the targeted operating frequency and output impedance level in terms of f_T/f_0 and R_L/R_{ON}. Namely, these ratios need to be large for high drain efficiency at peak output power [10].

A. Segmentation of the RF Output Stage

SMPA operation such as class-E is often entirely focused on peak power performance. However, when dealing with modulated signals with high PAPRs, the control of the output power in an energy-efficient manner from a driver's perspective is needed. This can be achieved by using segmentation of the output stage [11], [12]. In low-power DTX implementations, this is done by putting many (scaled) unit cells in parallel, together with their embedded activation logic. This approach can be followed for both polar- [13] and Cartesian-oriented [14] DTX architectures. In this work, however, we focus on high-power DTX operation, which uses separate dies for the CMOS controller and power stage(s), blocking the use of advanced unit cells. To minimize layout and implementation parasitics as well as facilitate high output power and efficiency, segmentation of the gate width (W_G) of the power output stage itself

is used. In such a gate-segmented power device (Fig. 1), all drain fingers are directly connected in parallel, and all sources are connected to the ground through a highly doped substrate plug (LDMOS) or ground vias (GaN). Output power control is obtained by activating more gate segments, controlled by an amplitude code word (ACW), scaling the effective R_{ON} (when operated in triode mode) or the effective g_m (when operated in the saturation mode). R_{ON} control offers the highest theoretical efficiency (e.g., in class-E) but yields a nonlinear ACW–RF-output transfer. The latter can be handled by adopting a dedicated (nonlinear) segmentation technique [11] or by using digital predistortion (DPD) [15], [16]. In theory, g_m scaling can provide linear DTX operation [17], but this approach relies on a transconductance class of operation, yielding constraints in efficiency while being potentially more sensitive to variations of the driving voltage of the gate segments (see also Sections IX-B and IX-C).

B. Threshold Voltage Optimization

RF power FET technologies are typically optimized for their dominant high-volume application, namely, base station Doherty operation. These are primarily analog Doherty PAs, with an output stage gain ranging from 13 to 22 dB and supply voltages ranging from 28 to 50 V, based on gain, stability, and bandwidth considerations. In these applications, emphasis is placed on efficiency enhancement in power back-off operation, in combination with smooth AM–AM and AM–PM behaviors. Practical implementations aim to accomplish this by selecting the appropriate gate bias voltages to put the main device in class-AB and the peak device(s) in class-C operation. This design strategy has resulted in LDMOS and GaN technologies with high threshold voltages (V_T), e.g., a V_T above 2 V for LDMOS, and below -2 V for GaN, while the V_{GS} voltage swing in these analog applications is in the order of 3 to 5 V_{pp} at the maximum drive level. In contrast, in digital-oriented high-speed CMOS technologies, the supply voltage is limited to 1–2 V. In the targeted high-power DTX, the limited CMOS driver voltage should be sufficient to switch the LDMOS or GaN output stage (segments) between the "ON" and "OFF" state. For GaN, this is somewhat more complicated since large negative voltages are required to turn the device completely OFF. Consequently, for this purpose, dedicated high-voltage CMOS devices and a related design technique have been developed [18]. It is not practical to establish complete output stage switching with standard LDMOS or GaN devices when using commercially available high-speed CMOS technologies. Therefore, V_T of RF power technologies for DTX applications needs to be reduced.

LDMOS technologies can offer some flexibility for lowering the threshold voltage. Therefore, in this work, we use a 0.4-µm 28 V LDMOS technology, combined with a high-speed digital controller based on 40-nm CMOS technology. The downshifting of the LDMOS V_T can be done by selecting different doping concentrations or using thinner gate oxides. This is a delicate process since various other performance parameters, such as ruggedness (the ability to withstand a stress condition without degradation or failure [19]), need to

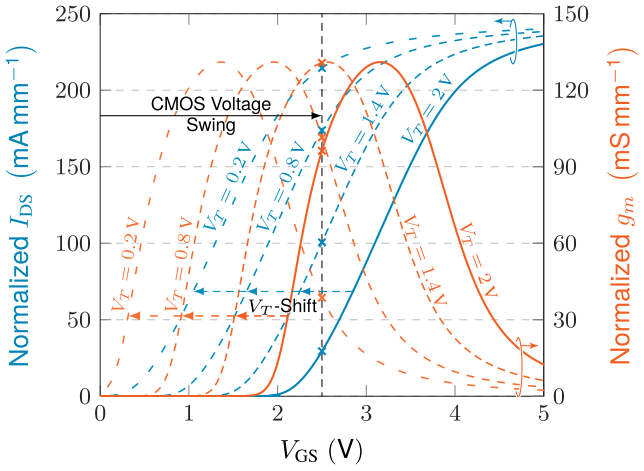


Fig. 2. LDMOS I_{DS} and g_m curves normalized per mm when $V_{DS} = 28$ V for different V_T-shifts to lower voltage levels (shown in dashed line). The solid lines illustrate the nominal LDMOS technology as typically used for analog base station implementations.

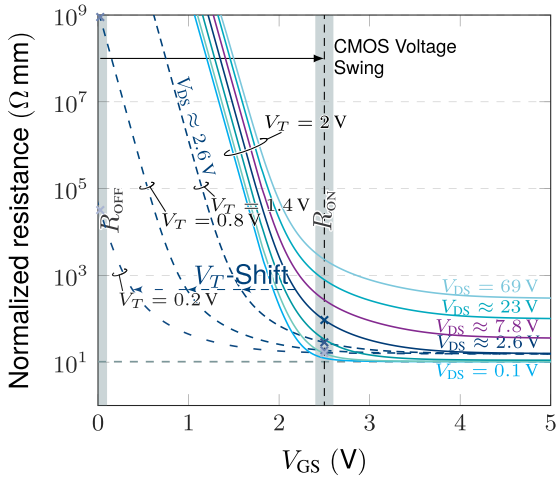


Fig. 3. Modeled drain ON/OFF resistance shown versus V_{GS} for different values of V_{DS}.

stay satisfied. Furthermore, when shifting the V_T down, the LDMOS process technology is no longer calibrated, so there will be uncertainty in the actual realized V_T. To relax the LDMOS V_T-shift, thick-oxide CMOS devices are selected to implement 2.5 V drivers for the LDMOS output stage segments and their tapered buffer chains. Logically, these devices are slower than the low-voltage high-speed standard 40 nm CMOS devices, which we use in the control logic. The design considerations for the tapered buffer chains are discussed in Section VI.

Fig. 2 shows the drain current (I_{DS}) and transconductance (g_m) versus gate voltage (V_{GS}) for the considered LDMOS technology. We observe that V_T of 0 V allows to switch the device entirely "ON" and "OFF" using a 2.5-V driver signal. However, choosing a very low value for V_T causes a drop in R_{OFF} (Fig. 3), which also affects the peak drain efficiency. This is most prominent in power back-off operation when a part of the DTX segments will be deactivated. Consequently, the optimum LDMOS V_T for a power-DTX implementation

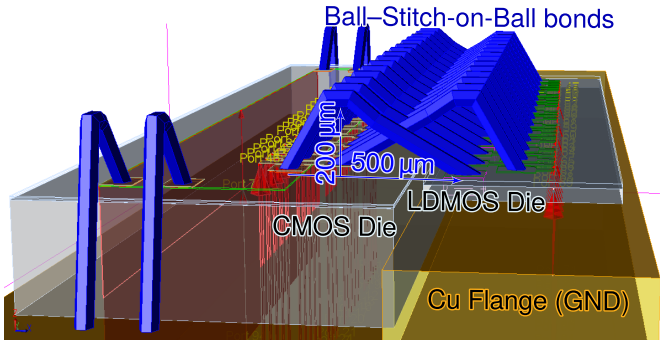


Fig. 4. Modeled bond-wire configuration used for the connection of the CMOS controller to the LDMOS power die.

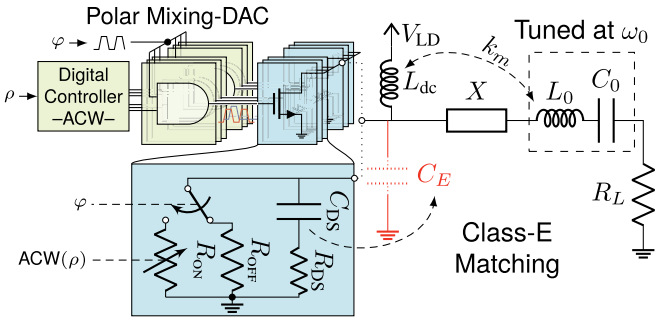


Fig. 5. Digital polar class-E DTX configuration using output stage segmentation. The digitally controlled segments can be modeled as a single switch with an ACW-controlled R_{ON}.

ranges from 0.4 to 1.4 V. For the remainder of this article, we will assume $V_T = 0.8$ V. When the details of the power-DTX line-up have been determined, this V_T choice is reevaluated in Section VIII.

III. High-Power-DTX Line-Up Definition

Since the realization of a power-DTX prototype is costly, our aimed demonstrator (Fig. 1) must support various DTX operation conditions for testing purposes. Thus, its architecture is intended to support both polar and Cartesian operation, of which the latter demands two baseband-to-RF upconverting TX line-ups. This dual TX line-up topology can also be used to support testing of two-way Doherty or out-phasing prototypes in the future. Consequently, the output stage segments are grouped in two independently controlled switch banks. Furthermore, the output stage(s) of the power-DTX must be flexible in their operating class and compatible with a rectangular (digital) drive signal. The nominal supply voltage V_{LD} of the LDMOS technology is 28 V. The standard LDMOS die size for power devices is 4.9 mm, which we adopt as the maximum LDMOS die width in this work. The number of interconnections between the CMOS and LDMOS dies has been maximized to allow as many DTX segments as possible, to reach maximum DTX resolution and dynamic range. This is achieved by using the minimum available bond-wire pitch of 80 µm, in combination with staggered bond pads and 25-µm-diameter gold bond wires with ball–stitch-on-ball bonding to minimize bond-wire loop height (Fig. 4).

Wedge–wedge bonds with 50-µm-diameter aluminum wires with a definable loop shape are used at the output of the LDMOS die to achieve low output losses and a predictable connection to the output matching network on a printed circuit board (PCB). This requires a minimum bond-wire pitch for these aluminum wires at the output of 130 µm and a bond bar on the LDMOS of at least 167 µm wide. The minimum trace width on the PCB is 100 µm for a 35-µm-thick copper layer. Finally, to make our feasibility study of interest to future DTX-based mMIMO base stations, the power-DTX prototype should operate up to at least 3-GHz transmit frequency while being capable of delivering at least 20 W of RF output power with high system efficiency. For this purpose, we will explore the following high-power DTX single-ended polar class-E technology demonstrator, with its conceptual diagram given in Fig. 5.

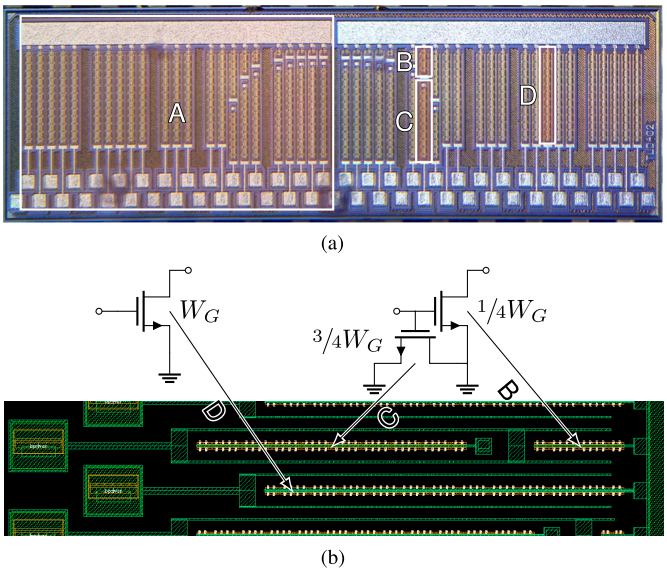


Fig. 6. Layouts of the segmented LDMOS power die. (a) Micrograph of the die (4.9 mm × 1.6 mm) having a total gate width ($W_{G,tot}$) of 41.472 mm distributed over two switch banks (the surrounding box indicates the left switch bank A), each bank featuring seven binary-weighted segments, (B) indicates such a binary segment with dummy device (C), and 15 unary segments representing 4 bit, denoted by D. (b) Layout detail showing the use of a dummy LDMOS device (C) for equalizing $C_{in} = C_{ESD2} + C_{GS} + C_{GG,dummy}$. Here, the second MSB binary segment is shown below a unary segment.

IV. Dimensioning of the Segmented RF Output Stage

When assuming $V_T = 0.8$ V and a drive signal swing of 2.5 V, the modified LDMOS technology has $I_{DS,max} \approx 0.17$ A mm (Fig. 2). This current density is somewhat limited by the lower voltage swing from the CMOS driver. Furthermore, in the class-E operation, the supply voltage needs to be lowered to 20 V to avoid breakdown, lowering the output power capability [20]. Due to requirements on the effective R_{ON} and to allow for some design flexibility (e.g., use of Cartesian operation, requiring I and Q banks, or flexibility to use operating classes with lower output power capability, such as digital class-C [17], in later implementations), we assume doubling of the minimum bank size with respect to an analog Class-B implementation at $V_{LD} = 28$ V for 20-W RF output

power, giving a minimum LDMOS total gate width $W_{G,\mathrm{tot}} \geq$ 33.6 mm, which is split over the two banks [Fig. 6(a)]. The maximum number of segments is limited by the number of interconnections between the CMOS controller and the LDMOS output stage. Naive division (i.e., neglecting things as pad sizes and bank spacing) of the available die size of 4900 μm by the minimum bond-wire pitch of 80 μm yields 62 interconnections in total, so 31 is for a single bank. Fully thermometer coding would yield a too small dynamic range for the DTX to sufficiently handle modulated signals. Therefore, a hybrid approach was selected, resulting in 15 unary segments (4-bit resolution) and 7 binary-weighted segments for each bank. The size of the least significant binary bit is limited by the minimum W_G of the LDMOS device. The least significant binary-weighted segment was doubled to make use of the remaining space, allowing some extra redundancy in testing, yielding an overall segment (bond) pitch of 83.5 μm. The above makes the summed gate width of all binary-weighted segments equal to that of a single unary segment. Therefore, $W_{G,\mathrm{tot}} = 2 \times 16 W_G$, where W_G is the gate width of a unary segment. To comply with the output power requirement, $W_G \geq 1.05$ mm, which, for this LDMOS technology, is spread over two gate fingers per segment.

Aside from the LDMOS gate capacitance, the loading capacitance for an LDMOS segment driver also consists of ESD protection diodes on both dies. To reduce the disproportionate ESD contribution and to have W_G that is decently divisible by 2, W_G was increased to 1.296 mm, yielding a unary segment loading capacitance of $C_L = C_{\mathrm{ESD1}} + C_{\mathrm{ESD2}} + C_{\mathrm{GS}} \approx 0.81\ \mathrm{pF} + 0.50\ \mathrm{pF} + 1.10\ \mathrm{pF} = 2.41\ \mathrm{pF}$ and $W_{G,\mathrm{tot}} = 41.472$ mm. This gives a total LDMOS output capacitance of $C_{\mathrm{DS}} \approx 12.3$ pF when $V_{\mathrm{DS}} = 28$ V. The use of binary-weighted segments raises the issue that C_{GS} reduces by a factor of 2 with each binary step. To avoid delay mismatches caused by different loading of the segment drivers, the lower C_L of these binary segments is compensated by adding dummy LDMOS devices [Fig. 6(b)], with both source and drain tied to ground. Following this strategy, the total driver-connected W_G of a binary segment is targeted to be equal to that of a unary segment.

V. Class-E Output Match

With the LDMOS power die defined, next, we will consider the class-E output matching network. In a polar class-E TX, the segmented output stage can be modeled as a switch that toggles between the effective R_{ON} and R_{OFF}, in parallel with the output capacitance C_{DS}, which is the sum of all segments' output capacitances (Fig. 5). The ACW in this polar configuration provides the amplitude information ρ and defines the number of activated LDMOS segments. The clock phase φ controls the switching moment of these segments. The capacitance C_{DS} is used as the class-E shunt capacitance C_E. Its equivalent series resistance R_{DS} relates to the losses that occur when an RF signal is applied at the output of the LDMOS segments, a condition of particular interest when dealing with Doherty or high frequency operation. The resistance R_{OFF} models the static losses due to the output stage's bias. Class-E operation is extensively analyzed in the literature, where the zero voltage switching (ZVS) criterion is the critical requirement in reaching 100% drain efficiency [9]. A set of class-E normalization equations can be defined, where L_{dc} can range from finite to infinite[1] [21], [22]

$$q = \frac{1}{\omega_0 \sqrt{L_{\mathrm{dc}} C_E}} \tag{1}$$

$$K_C = \omega_0 C_E R_L \tag{2}$$

$$K_X = \frac{X}{R_L} \tag{3}$$

$$K_P = \frac{P_{\mathrm{RFout}} R_L}{V_{\mathrm{LD}}^2}. \tag{4}$$

A technology-dependent upper frequency for class-E is given by

$$f_{\mathrm{max},E} = \frac{I_{\mathrm{DSmax}}}{\alpha_E C_E V_{\mathrm{LD}}} \tag{5}$$

where α_E is a constant dependent on the subclass of class-E operation determined by the value q, ranging between 56 and 31. For the LDMOS technology used, $f_{\mathrm{max}\,E}$ is between 510 and 920 MHz for $V_{\mathrm{LD}} = 20$ V. Beyond this frequency, the ZVS criterion cannot be met anymore and the active device operates partly in saturation rather than purely in its triode region. This shifts its operating class to the continuum between transconductance and switch mode, also called class-BE operation [23], [24]. Since our targeted operating frequency is 3 GHz for our power LDMOS DTX, the class-BE operation is used for its design.

VI. DTX Drivers

In the power-DTX concept, the relatively large input capacitance (C_{in}) of the LDMOS segments are driven by rectangular activation signals. This voltage swing needs to be high enough to sufficiently activate the LDMOS segments, while rise and fall times need to be short to guarantee the energy-efficient operation of the output stage. To achieve this, a level shifter and a chain of inverters using thick-oxide devices of increasing size are used to bring the digital drive signal from the core logic to the input of the LDMOS output stage [Fig. 7(a)]. This inverter chain, referred to as a "tapered buffer chain," has a power/speed tradeoff, influencing the overall performance of the power-DTX, justifying a more detailed investigation.

The CMOS tapered buffer chain can be analyzed using linearized resistances, capacitances, and their related propagation delays [25]. The definitions of these linearized circuit elements in the context of this article are given in Appendix B. Minimizing the rise and fall times mainly depends on the propagation delay per stage, rather than having a low delay for the entire chain. This propagation delay can be analyzed for a single DTX segment, as shown in Fig. 7. The interconnect parasitics between the CMOS controller chip and LDMOS power die are neglected since the operating frequency is (significantly) lower than the resonance frequency of L_{bond} and $C_{\mathrm{ESD2}} + C_{\mathrm{GS}}$, and $R_{\mathrm{bond}} \ll R_{\mathrm{dr}}$. Here, R_{dr} is

[1] Acar *et al.* [21], [22] also defined K_L to determine L_{dc}, but its calculation is straightforward from q and K_C.

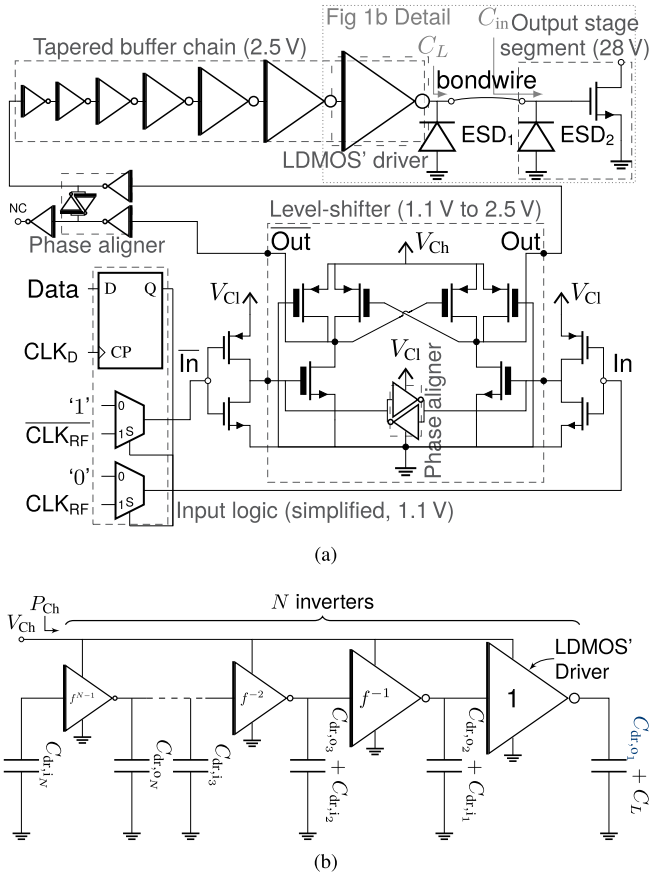


Fig. 7. (a) DTX segment, including the level-shifter circuit with phase aligner for going from the 1.1-V domain with low-voltage high-speed standard CMOS devices to the 2.5-V domain, which uses thick-oxide devices. A tapered buffer chain based on the thick-oxide devices is used to drive the capacitive input of the LDMOS segments with sufficient switching speed. (b) Tapered buffer chain with its parasitics in more detail.

the equivalent switch resistance of the inverter functioning as the LDMOS' driver that (dis)charges the capacitive load C_L. Here, a low switch resistance R_{dr} means a bigger (thus "faster" or 'stronger') driver. Then, each consecutive inverter is a factor f smaller (seen from the load toward the input of the chain) and the overall effective fan-out is then defined as $F = C_L/C_{dr,i_N}$; the total number of stages becomes $N(f) = \lceil \log_f F \rceil + 1$. This implies a technology-dependent maximum driver speed as $\lim_{f\downarrow 1} N(f) \to \infty$. However, in practical implementations, there is a tradeoff between power consumption and driver speed, which can be captured in the following (see Appendix B):

$$C_{seg} = C_L + \frac{C_L}{f}(1+\gamma)\frac{1-f^{-N}}{1-f^{-1}}. \tag{6}$$

This yields a power dissipation in the CMOS controller per segment of $P_{seg} = f_0 C_{seg} V_{Ch}^2 + P_{const}$. The "constant" segment power dissipation (P_{const}), originating from continuous running RF input clocks, the level shifter, and static leakage currents, is extremely small compared to the dynamic power dissipation and will be neglected onward. Since P_{seg} is proportional to the total capacitance in the overall segment line-up, rather than only the input capacitance of the LDMOS (unary) element and ESDs (C_L), we can define the capacitance multiplication factor

$$M = \frac{C_{seg}}{C_L}. \tag{7}$$

This factor M is useful for defining the DTX system efficiency, comparable with more conventional RF power technology parameters such as drain efficiency (η_D) and the operating power gain (G_P), and its role is discussed in more detail in Section VII-B. The factor M and the effective fan-out f are derived analytically, resulting in

$$M \approx \frac{f+\gamma}{f-1} \tag{8}$$

$$f = \gamma \frac{\ln(2) R_{dr_1} C_L}{t_{p0}}. \tag{9}$$

VII. Power-DTX From a System-Level Perspective

A. Driver Power Consumption

A power-DTX configuration has many segments whose activation is controlled by the ACW. The related "activated" capacitance is given as $C_{act} = N_{act} C_{seg}$, with N_{act} the number of activated segments. When assuming equal segment sizing, this leads to a linear dependence of the tapered buffer chains consumed power P_{Ch} on the ACW

$$P_{Ch} = f_0 \frac{\text{ACW}}{2^{N_b}-1} C_{tot} V_{Ch}^2 \tag{10}$$

where N_b is the number of bits of the ACW and C_{tot} is the summed capacitance of all segments, including the LDMOS input capacitance, ESDs, and the capacitance of the entire digital tapered buffer chains.

B. Line-Up Efficiencies

The voltage-to-power transfer of the LDMOS segments makes the classical efficiency definitions based on the "operating power gain" (G_P) useless. However, when considering the power consumption of the tapered buffer chain, the (system) efficiencies of interest can be defined similar to those of analog PAs, starting with the drain efficiency of the LDMOS output stage

$$\eta_D = \frac{P_{RFout}}{P_{LD}} \tag{11}$$

where P_{RFout} is the measured DTX output power and P_{LD} is the power supplied by the LDMOS supply (V_{LD}). Furthermore, the total efficiency of the LDMOS output stage

$$\eta_T = \frac{P_{RFout}}{P_{dr} + P_{LD}} \tag{12}$$

in which $P_{dr} = f_0 N_{act} C_L V_{Ch}^2$ relates to the capacitive switching loss caused by the activated LDMOS output segments itself (i.e., it does not include the remaining switching losses of the tapered buffer chain). Note that P_{dr} should not be confused with the (almost zero) input power $P_{in,LDMOS}$ in a conventional impedance matched RF situation where the input capacitance of the LDMOS device is resonated out, although

they serve a similar function in the expression. Finally, the system efficiency is defined as

$$\eta_S = \frac{P_{\text{RFout}}}{P_{\text{Ch}} + P_{\text{LD}}} = \frac{P_{\text{RFout}}}{M \cdot P_{\text{dr}} + P_{\text{LD}}} \tag{13}$$

in which M is the capacitance multiplication factor for the driver chain as defined in (7). In this way, the DTX and its system efficiency can be easily evaluated while using the driver's speed, which sets the rise and fall times, as a free design parameter. Consequently, the required number of stages in the tapered buffer chain follows as a result and not as a predefined constraint. This allows, for example, to include only the final driver stage with an LDMOS segment in the simulation setup and use the M value (based on the CMOS controller technology under consideration) to include the power consumption of the remaining tapered buffer chain. Note that in this latter approach, C_{dr,o_1} of the final driver is already included. Consequently, in this particular case, M needs to be replaced by M', which can be calculated as

$$M' = M\frac{C_L}{C_{\text{dr},o_1} + C_L} = M\frac{f}{f+\gamma} \approx \frac{f}{f-1}. \tag{14}$$

C. Stability

Due to its complementary digital topology, the drivers for the LDMOS output segments have a very low output impedance compared to a (pre)driver in a traditional analog TX line-up. Furthermore, it fixes its output voltage to a "high" or "low" state. As a result, stability problems of the RF output stage, as present in analog implementations, are entirely eliminated. Moreover, when the LDMOS segments are driven to be fully "ON" or "OFF," their related transconductance (gain) in these conditions is very low (see Fig. 2), again contributing to stable behavior of the output stage.

D. Frequency Agility

The drivers transfer the (phase-modulated) rectangular voltage to the LDMOS gate segments. Consequently, no (frequency-dependent) impedance matching at the input of the LDMOS output stage is used, yielding frequency-agile operation for the entire DTX line-up within the speed limitations of the tapered buffer chain. In fact, if the maximum operating frequency is not limited by the interconnect between the CMOS controller and LDMOS die, only the LDMOS output capacitance combined with the applied output matching network defines the frequency transfer of the DTX line-up.

VIII. Optimization of the DTX Line-Up

With above definitions in place, we can optimize our power-DTX drain and system efficiencies for class-BE operation at various V_T values of the LDMOS segments. For this purpose, the equivalent resistance of the LDMOS' driver is modeled by R_{dr}. Selecting the R_{dr} value affects the switching speed of the LDMOS segments and, as such, the LDMOS drain efficiency. Furthermore, the chosen R_{dr} value automatically sets the required size of this driver for given CMOS technology, as specified by (9). The empirical constants extracted from the thick-oxide device models in the CMOS 40-nm technology, including layout parasitics, are found to be: $t_{p0} = 10.76$ ps, $\gamma = 1.092$, and $t_{\text{step}_1}/t_{p_1} = 0.736$. Also, here, we assume the number of stages N in the related tapered buffer chain to be continuous. Finally, the output matching network (Fig. 5) is assumed to be lossless.

Using the theory of Sections V and VII-B, the normalized class-E design parameters (see Table I) have been determined by numerical optimization for each V_T point in the graph of Fig. 8 to maximize the related efficiencies and output power. Interestingly, for low V_T, also, the optimum R_L ($\propto K_C$) is low, which can be explained by the increased maximum current capability of the LDMOS. For this condition, also, the optimum value for R_{dr} drops, implying that the driver provides faster rise and fall times to reach high drain efficiency. This low R_{dr} comes at the cost of an increased P_{Ch}, which can be

TABLE I

Class-(B)E Design Sets and Driver Sizes Used for Generating the Datapoints of Fig. 8

V_T	V_{LD}	q	K_C	K_X	R_{dr}	M
2.00	28.00	0.983	7.189	1.167	10.31	3.781
1.67	28.00	0.987	7.996	0.960	12.69	2.809
1.33	28.00	1.017	8.169	0.500	15.44	2.289
1.00	28.00	1.296	0.209	−2.280	14.43	2.441
0.80	28.00	1.368	0.155	−3.071	14.39	2.448
0.60	27.11	1.407	0.137	−3.265	14.67	2.401
0.40	25.75	1.448	0.122	−3.398	14.62	2.410
0.20	24.58	1.486	0.111	−3.426	14.46	2.436
0.00	23.50	1.525	0.102	−3.365	13.84	2.548

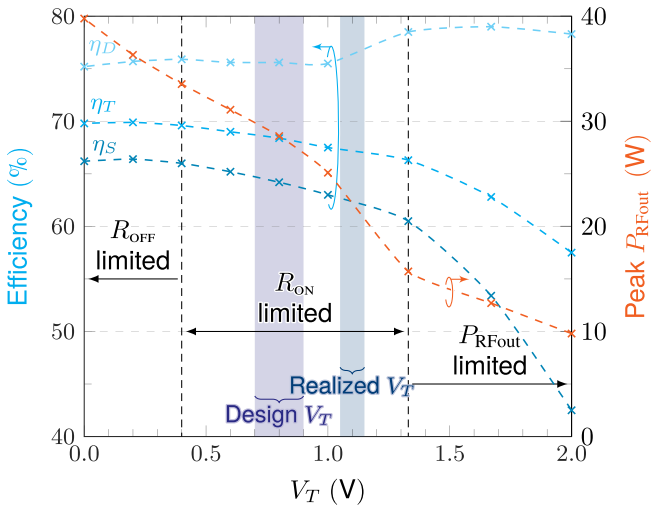


Fig. 8. Theoretical full power-DTX performances for the optimized class-BE designsets for varying values of V_T of the applied LDMOS technology. The design parameters used to generate this graph are: $L_{\text{bond}} = 0.6$ nH, $R_{\text{bond}} = 0.2\ \Omega$, $Q_{L_0} = 10$, $k_m = 0.2264$, $f_0 = 3$ GHz, $d = 50\%$, and $V_{\text{Ch}} = 2.5$ V; the remaining parameters depend on V_T and are given in Table I.

afforded from a system efficiency perspective since P_{RFout} is also higher for low V_T. For high V_T, the RF output power is severely limited, and rise and fall times need to be sufficiently short to achieve any respectable output power at all. This also requires a low R_{dr}, further decreasing the achievable system efficiency.

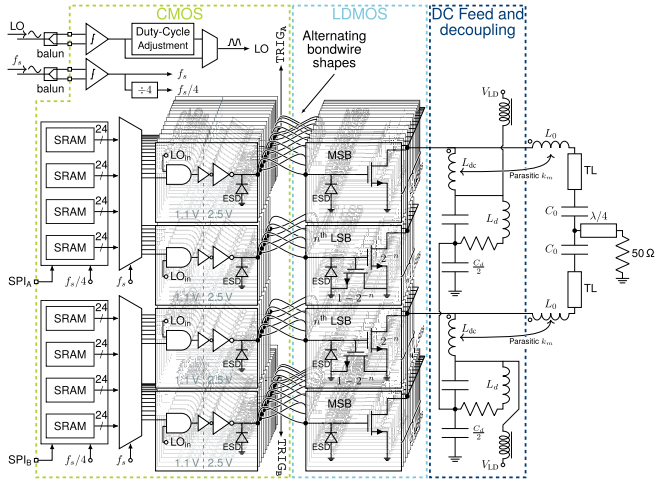
It appears from Fig. 8 that a customized LDMOS technology, having a threshold voltage of $V_T = 0.2$ V, yields the optimum system efficiency. However, such a low V_T requires very high doping concentrations in the LDMOS fabrication process, impacting other device parameters such as ruggedness. Therefore, based on practical considerations, V_T of 0.8 V is targeted in this work. However, since this V_T value deviates significantly from the standard LDMOS process flow, it comes in practice with some uncertainty. To handle this V_T uncertainty in the demonstrator, duty-cycle (d) and supply voltage (V_{LD}) adjustment is used in the testing phase of the power-DTX (see Appendix A). The DTX is reoptimized for the targeted $V_T = 0.8$ V with the output matching network now including realistic losses. This results in an optimum $R_{\mathrm{dr}} = 16.87\ \Omega$ requiring $f = 2.88$ and $N = 7.5$ for the number of driver stages, yielding a capacitance multiplication factor $M = 2.114$ ($M' = 1.532$). The simulation result of the power consumption of the CMOS controller using these values is shown in Fig. 10 and will be discussed in more detail with the measurement results in Section IX-A.

With the design study above, the high-power DTX configuration is defined within the technology options available. Within this project, targeted DTX peak output power (larger than 20 W) and a peak system efficiency (close to or above 60%) seem feasible.

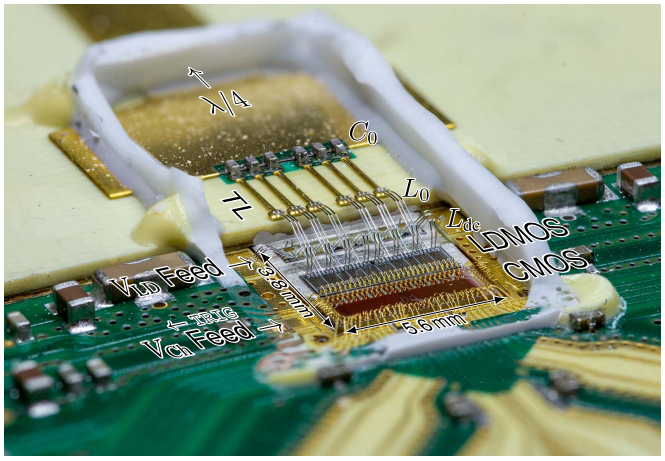
IX. DTX Demonstrator Realization and Verification

The TSMC 40-nm CMOS controller and custom 0.4-µm 28-V low-V_T LDMOS power die have been fabricated, targeting the optimum design values discussed previously. The DTX's detailed schematics and a photograph of its implementation are shown in Fig. 9. The single-ended class-BE output matching network, centered around $f_0 = 2.1$ GHz, was implemented using discrete capacitors, bond wires, and PCB transmission lines as inductances, and a quarter-wave transformer to match R_L to 50 Ω. Layout parasitics in the CMOS tapered buffer chain decreased relatively with the smaller stages, allowing for a slightly increasing the effective fan-out along the tapered buffer chain, resulting in a chain of seven stages. The controller features additional trigger outputs for synchronization and testing purposes. These "TRIG" outputs are driven using identical drivers as used for the LDMOS gate segments. The dc-based verification of the realized LDMOS V_T-shift indicated V_T of 1.1 ± 0.05 V. This is higher than intended, but the availability of on-chip duty-cycle control and flexibility in the LDMOS supply voltage can handle this deviation (see Appendix A).

The thickness of the CMOS controller IC is 300 µm, and the LDMOS die has been thinned to 50 µm (also see Fig. 4). Both dies are glued on a modified copper flange, minimizing the



(a)



(b)

Fig. 9. Realized power-DTX configured for polar operation with the single-ended 2.1-GHz class-BE output matching. The prototype features a CMOS 40-nm controller and a V_T-shifted segmented LDMOS output stage, featuring two switch banks that take their ACW data from time-multiplexed on-chip memory. The power-DTX prototype also has extra trigger output pins to monitor its output independent of the LDMOS die. (a) Schematic. (b) Photograph with the ceramic cap removed.

bond-wire inductance between the CMOS controller and the LDMOS power dies. In addition, grounded pads were placed on the LDMOS power die to provide current return paths to the CMOS drivers through bond wires. The interconnecting bond wires between the CMOS driver and LDMOS power die inputs are placed in alternating directions to minimize the mutual inductance (see Fig. 4). The flange is placed as a PCB inset on a larger aluminum heatsink, adding mechanical support for the PCB.

A. Dynamic Power Consumption of the Controller

First, the simulated 2.5-V power consumption of the CMOS controller (simulated $M' \cdot P_{\mathrm{Ch}}$) is compared to the measured data, as shown in Fig. 10. The fluctuations resulting from the hybrid unary and binary-weighted implementation of the segments with equalized input capacitances are clearly visible (see Section IV and Fig. 6). Apart from this, the power dissipated does show the overall linear proportionality with

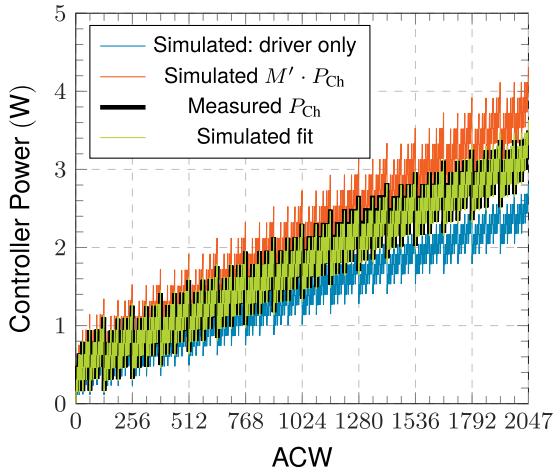


Fig. 10. Simulated drive power including $C_{dr,o1}$, this power is multiplied by the theoretically calculated $M' = 1.532$ to provide the total power consumption of the driving drive chain, which is compared to its actual measured values.

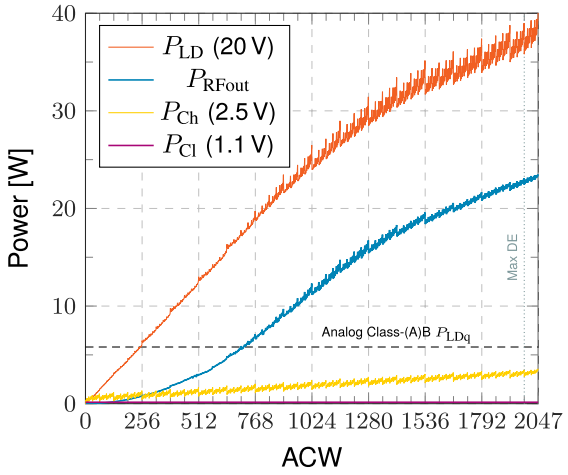


Fig. 11. Measurement of the fully digital-TX line-up ($W_{G,tot} = 41.472$ mm, 11 bit) in static pulsed CW operation at 2.1 GHz using 15% duty cycling to lower thermal effects and $V_{LD} = 20$ V. The RF output power (P_{RFout}), the total dc power consumed by the segmented LDMOS devices (P_{LD}), the dc power consumed by the driver (2.5-V domain), the static dc power of the low-voltage (1.1-V) CMOS circuitry, and (dashed line) the static quiescent dc power for an LDMOS device with the same $W_{G,tot}$ when operated in an analog class-AB bias condition for linearity are plotted.

ACW. We can compare the simulated P_{Ch} with the total controller power consumption needed to drive the LDMOS segments using an empirical fit for the capacitance multiplication factor $M' = 1.291$, which is 15.7% lower than what was theoretically predicted in Section VIII. This can be attributed to the slightly more aggressive scaling in the implemented tapered buffer chain, resulting in a seven-stage chain, and the fact is that the (nonlinear) device capacitances are not 100% charged and discharged each cycle. Still, the accuracy of this estimation can be observed from its almost perfect correlation with the measured power dissipation of the 2.5-V supply domain. Furthermore, if the ESD capacitances could have been avoided, the required drive power would have been a factor 2.2 lower given the same driver speed (see Section IV). The above suggests that close to perfect scaling of the consumed DTX power with the RF output signal is in reach.

B. Digital-to-RF Transfer of the Power-DTX

The digital-to-RF transfer is confirmed by performing static power measurements versus ACW using a power meter. A 30-dB attenuator was included in the measurement setup to protect the instruments, whose losses have been deembedded. Pulsed continuous wave (CW) measurements are performed using a 15% time duty cycle to reduce thermal effects. The optional RF duty-cycle adjustment is first bypassed, so the RF duty cycle in these measurements is close to 50%. For ACW = 1920, peak drain and system efficiencies occur (see Fig. 11), being 62.6% and 58.1%, respectively.

The total power balance at maximum ACW is shown in Fig. 12, showing that the static power consumption basically only occurs in the low-voltage domain (1.1 V) and is a tiny fraction of all the powers involved. This is in strong contrast with an analog-oriented TX line-up biased for linear class-AB operation. The related quiescent current would, in combination with a typical LDMOS supply, result in static power consumption (P_{LDq}) of 5.8 W for an LDMOS device of

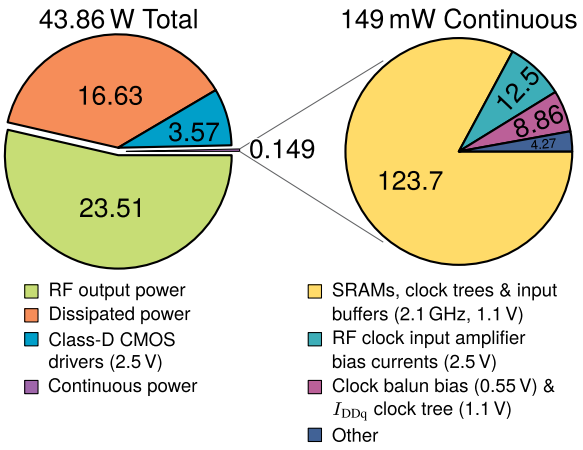


Fig. 12. Dynamic and static dc power consumption breakdown in the implemented DTX at peak RF output power conditions (ACW = 2047).

comparable size. This level is indicated in Fig. 11 by the dashed line.

As indicated in Section VIII, the efficiency and output power can be optimized by changing the RF duty cycle and supply voltage (see Appendix A). Using $V_{LD} = 20$ V, the best peak system efficiency measured was 60.4% using an RF duty cycle (d) of 43%, with a maximum output power of 18.5 W and a drain efficiency of 66.7%. Maximum output power was observed for $V_{LD} = 28$ V and $d = 50\%$, being 29.8 W. Due to the nonlinear LDMOS C_{DS} and higher switching losses, the drain and system efficiencies under these conditions were 40.0% and 38.1%, respectively. This downward trend was already expected from simulations regarding the postproduction tuning (see Fig. 20).

Furthermore, CW efficiency measurements with varying V_{LD} have not been done, as the demonstrator sample used for these measurements was damaged after finishing these

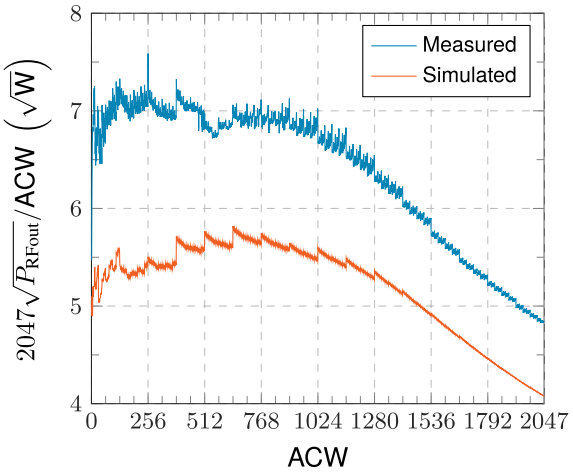


Fig. 13. Simulated and measured static DTX transfers compared, normalized to the ACW (ACW–AM/ACW). Both clearly show the effect of the hybrid unary and binary-weighted implementation of the segments, especially when switching to a unary weighted segment (every 128 ACWs).

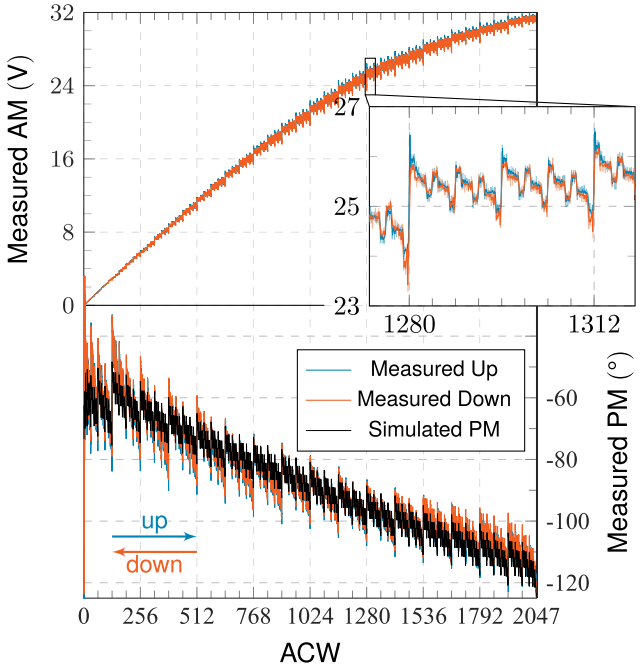


Fig. 14. Measured dynamic response for a linear ACW triangle-shaped envelope signal, centered around 2.1 GHz with the f_s and VSA analysis bandwidth set both to 525 MHz, leading to a cycle time of 62.4 µs. The ramp down is flipped and placed over the ramp up to enable comparison. This shows some hysteresis in the form of overshoots when going up and undershoots when going down. For reference, also, the simulated static ACW–PM is plotted, adjusted for the delay of the full tapered buffer chain and resistive supply variation (see also Fig. 17).

peak power measurements. This was caused by lacking a proper shutdown procedure for the power-DTX in this set of measurements, as the DTX could go from full power to zero in a single sample when downloading new amplitude data to the SRAMs or when aborting a measurement. Such a sudden change in the related dc current can cause large V_{DS} spikes, even over a moderate bias feed inductance. The remaining measurements in this article were done before this breakdown or performed on a different prototype sample. To avoid damaging these remaining samples, further CW measurements or measurements using $V_{\mathrm{LD}} = 28$ V were avoided.

In Fig. 13, the simulated and measured static (CW, with stepped ACW, using a power meter) digital-to-RF transfer of the entire DTX system is given for $V_{\mathrm{LD}} = 20$ V and $d = 50\%$, in terms of the square root of the RF output power ("AM") normalized by the ACW. The simulation setup used includes all known parasitics and imperfections in the realized power-DTX demonstrator. The first parasitics to be included are the mutual inductances of the staggered bond-wire array between the CMOS controller and LDMOS output stage, and limited bond-wire quality factor, by using an S-parameter EM model for the bond wires (see Fig. 4). The effective self-inductance ranges from 490 to 620 pH with a coupling factor up to 0.52, depending on bond-wire location within the array. This coupling is stronger between the first and third bond wires than between the first and second bond wires, due to their staggered orientation. The remaining parasitics to be included are lumped component parasitics, as well as the underestimated C_{GS} of the drain–source short-circuited dummy LDMOS devices included in the binary segments as compensation capacitances, yielding a 15% higher dummy C_{GS} value than intended one. This deviation was caused by the used compact model of the LDMOS device, which was optimized for analog transconductance operation and, therefore not for the $V_{\mathrm{DS}} = 0$ V condition. It can be concluded from the simulations at low ACW that the impact of the mutual inductances of the bond wires between the CMOS and LDMOS dies is quite pronounced. Activating the thermometer segments at every 128 ACWs yields small jumps, except for the first two transitions. This is caused by aforementioned mutual coupling, which increases the effective RF drive voltage (V_{GS}) of an LDMOS segment when neighboring segments are activated, yielding an unwanted bit-to-bit interaction in the output power. In this simulation, the unary-weighted segment located the farthest away from the grouped binary-weighted segments [see Fig. 6(a)] is activated first. After ACW $\approx$ 1024, the DTX starts to enter compression, evident from the transfer decreasing in magnitude.

Our forgoing driver analysis assumed that the LDMOS input capacitance of the segments remains perfectly constant, independent of what happens at the drain terminal of the RF output stage. However, C_{GS} is dependent on the operating region of the LDMOS device. In addition C_{GD} undergoes the Miller multiplication and also appears at the input of the segment. Although, in RF-oriented LDMOS technologies, C_{GD} is very small, this yields some dependence on the output operating condition. These effects modulate the effective loading capacitance of the LDMOS' driver and its delay, appearing as (additional) ACW–PM distortion in the DTX line-up.

In Fig. 14, the measured (dynamic) ACW–AM/PM curves are shown for a triangular (linear) ACW ramp, measured using a spectrum analyzer in the vector signal analyzer (VSA) mode. For this purpose, the baseband sampling rate f_s is reduced to 525 MHz, an integer factor 4 lower than the RF center frequency, to be within the VSA's baseband sampling rate. Every SRAM value directly corresponds to one demodulated

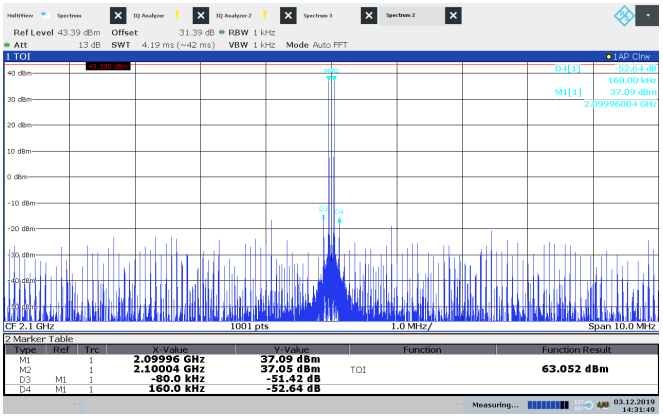


Fig. 15. Measured spectrum of the 80-kHz two-tone signal, showing an $IM_3 \leq -51.4$ dBc after static DPD, only using the unary segments with pulse density modulation.

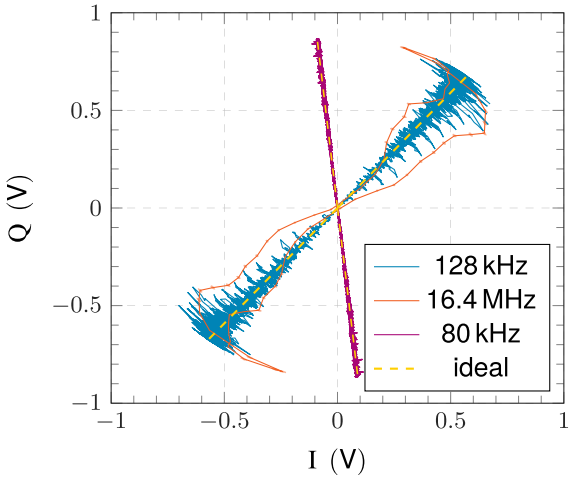


Fig. 16. Measurements using a 2.1-GHz two-tone test with varying tone spacing: downconverted IQ-constellations, after static DPD, showing hysteresis/memory effects for 16.4 MHz tone spacing. For reference, also, measured constellations using 128 kHz tone spacing and the 80-kHz tone spacing only using the unary segments with pulse density modulation are shown (with arbitrary phase reference).

IQ sample, and every ACW value is repeated eight times in the memory, giving a cycle time of 62.4 µs. For reference, the simulated static ACW–PM curve is also plotted. In this simulation, only the final stage of the tapered buffer chain was included (see Section VII-B) to aid simulation speed and convergence. To compensate for the delay variation of the full chain due to the resistive supply variation (IR-drop, see Fig. 17) and thus additional ACW–PM variation, the on-chip V_{Ch} is used to adjust the simulated curve. The overall difference between simulated and measured ACW–PM can be attributed to the aforementioned use of a compact model of the LDMOS device, optimized for analog transconductance operation, not including the severe C_{DS} nonlinearty when operating close to $V_{\mathrm{DS}} = 0$ V. The nonmonotonic behavior of the binary-weighted segments can be clearly seen in this measurement. The triangular ramp up and down have been folded on top of each other to compare them. Doing so, some memory effects also become visible. Namely, the ramp up has some overshooting when switching to a higher ACW value, while in the ramp down, undershooting happens when switching to a lower ACW value; at ACW = 1280, a unary-weighted segment is being switched ON/OFF, and at ACW = 1312, an 2^{-2}-weighted segment is switched ON/OFF. This hysteresis/memory effect is attributed to timing glitches, which are caused by delay differences due to C_L mismatch in the binary-weighted LDMOS devices.

C. Power-DTX Operation With Modulated Signals

For measurements with modulated signals, the power-DTX was used in its polar operation mode, and a Keysight M8190A AWG was used to provide the phase-modulated RF clock centered around $f_0 = 2.1$ GHz. The on-chip duty-cycle adjustment circuit was found to generate some spectral dirt caused by its analog control. Therefore, it was bypassed, and hence, $d = 50\%$. Static DPD [using a lookup table (LUT)] has been applied to compensate for the ACW–AM and ACW–PM DTX nonlinearities. This approach was attempted first for the full range of possible ACWs; however, the ACW–PM variations introduced by the use of the binary-weighted segments could not be compensated such that the effective number of bits (ENOB) was increased. Clearly, the dynamic effects in our DTX prototype dominate here, and henceforth, only the unary-weighted segments are used. To compensate for the reduced resolution and still improve the DTX's dynamic range and noise floor, pulse density modulation techniques using the remaining least significant bit were applied. Using this approach, a two-tone signal with a narrow tone spacing of 80 kHz was generated and measured (Fig. 15), yielding $IM_3 \leq -51.4$ dBc.

When moving to signals with video bandwidths larger than 10 MHz, the linearity degraded more than what theoretically can be expected based on the ENOB and sampling speed. In particular, two tones with a tone spacing of 16.4 MHz proved to be problematic. Closer inspection indicated that a resonance in the dc feed of the CMOS controller caused this linearity degradation. This resonance hypothesis is confirmed, by measuring the related on-chip driver voltage V_{Ch} through the TRIG test pin outputs with an oscilloscope. These TRIG pins were included in the DTX demonstrator to increase its testability [see Fig. 9(a)]. The on-chip driver supply should ideally be constant at 2.5 V. However, it showed around 240-$\mathrm{mV_{pp}}$ variation with the two-tone envelope frequency. It proved not possible with the current hardware demonstrator to correct this defect. Besides the quality of the driver supply decoupling, the supply variation also depends on the resistance in the dc supply path, which in our setup (cables, PCB, bond wires, and on-chip interconnect) is estimated to be 94 mΩ in total. Due to the considerable overall propagation delay (t_{ptot}) of the tapered buffer chain and its dependence on the supply voltage (V_{Ch}), any variation in the controller's supply voltage will cause an unwanted phase change in the DTX output, yielding unwanted phase modulation.

The resulting ACW–PM distortion is confirmed by the measured downconverted IQ-constellation diagram for this 16.4-MHz two-tone (Fig. 16), which strongly deviates from the ideal straight line. The variation in delay due to V_{Ch} variations

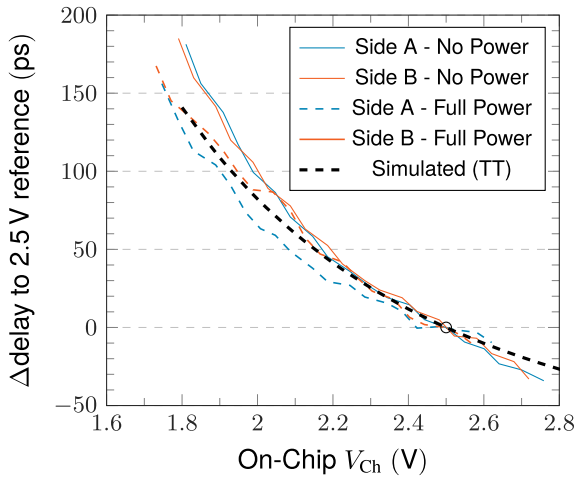


Fig. 17. Change in propagation delay of the CMOS tapered buffer chain compared to the $V_{Ch} = 2.5$ V reference case versus the measured V_{Ch}, which includes the IR-drop (averaged measurements, and the $\pm 1\sigma$ measurement variation is 14.4 ps). Thick dashed line: the simulated propagation delay.

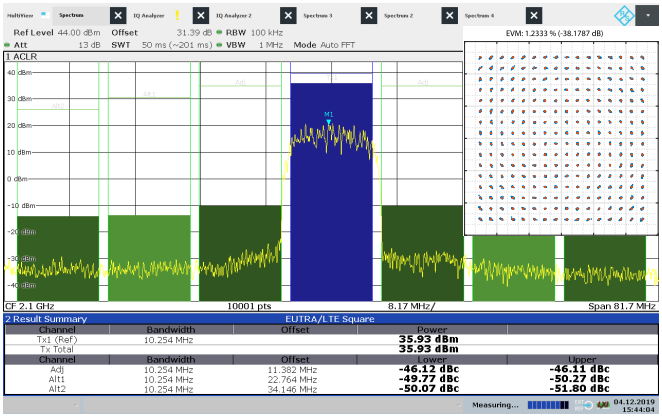


Fig. 18. Measured spectrum and constellation of the 10-MHz 256-QAM signal, showing an ACLR = 46.1 dBc and EVM = 1.2% after static DPD.

was also measured using an oscilloscope by putting a square wave in the SRAM for the TRIG pins and comparing the delay between its rising edge and a reference marker of the AWG. The measured and simulated results for the buffer chain are shown in Fig. 17, showing a decreasing delay with increasing (on-chip) supply voltage. All delays are referenced to the nominal $V_{Ch} = 2.5$ V case, for which the simulated tapered buffer chain delay is $t_{ptot} = 605.8$ ps. It can be seen that the measured delay differences follow the simulated values very well. This confirms that indeed, a dc supply resonance around 16 MHz causes the phase deviations in the RF output. Henceforth, we restrict ourselves to lower bandwidths in the following measurements.

In Fig. 18, the measured result for a 10.254-MHz 256-QAM signal around a carrier of $f_0 = 2100$ MHz is shown. The baseband sampling rate has been multiplied by 5/8 to $f_s = 1312.5$ MHz, to comply with the 2^{15} baseband samples in the SRAM and to have the video bandwidth just below the supply resonance. The signal was filtered by an root raised cosine (RRC) with a roll-off factor of $\alpha = 0.22$, and static (memoryless) DPD was applied (again only using an LUT for the unary-weighted segments with pulse density modulation for the LSB). This yielded for a signal with 7.2-dB PAPR, a measured adjacent channel leakage ratio (ACLR) of −46.1 dBc, and an rms error vector magnitude (EVM) of 1.2% (−38.2 dB, averaged over 4096 constellation points). The average output power was 3.9 W, with average drain and system efficiencies at 28.1% and 25.6%, respectively.

X. Discussion

This work aims to explore the feasibility of high-power fully DTXs that allow for high integration and low (static) standby power. Within the design constraints of today's LDMOS and CMOS technologies, our first high-power DTX demonstrator achieved decent performance in terms of output power and energy efficiency, which are the main objectives of this study. Although the dynamic range of the DTX, in terms of its implemented number of bits, could not be fully reached, reasonable linearity figures (IM_3, ACLR, and EVM) could be obtained for a complex modulated TX signal with not too large bandwidths. This bandwidth was mainly restricted by unfortunate resonance in the driver supply bias. However, other (lower power) DTX work [26] shows that large bandwidths (>300 MHz) with good linearity are in reach using a fully digital approach.

The measured performance of the presented DTX is summarized in Table II and compared to "high-power" prior-art solutions. In [1] and [2], fully integrated digital solutions are demonstrated; Diddi *et al.* [3] showed a hybrid digital/analog solution and McCune *et al.* [4] showed a digital-intensive EER solution. The work presented offers a 10× higher output power compared to these works while also providing higher (system) efficiency and comparable or better modulated performance. The work presented in [5] can be regarded as a digital-intensive PA and is added for completeness. In contrast to our proposed DTX concept, this solution is not based on a segmented output stage. Therefore, the operation of its two amplifier branches is limited to constant envelope and thus requires constant drive power limiting the achievable system efficiency [6].

Overall, valuable lessons for future power DTX implementations were learned from this study, which we summarize in the following.

1) Use fully saturated operation for the output stage segments, i.e., low g_m. Doing so minimizes the dependence of the DTX bit-to-RF transfer on the actual drive voltage offered to the gate of these segments (V_{GS}). This requires a relatively low V_T for the power stage.
2) Avoid mutual inductance in digital-to-RF-power die interconnections to stay away from bit-to-bit interaction.
3) Reduce delay variation in the driver chain due to variation of the on-chip voltage (V_{Ch}) by adopting the following strategies.
   a) Take the CMOS controller supply decoupling extremely serious even when it is supposed to be "just" a digital circuit.
   b) Make the tapered buffer chain as short as possible (lower t_{ptot}, so lower absolute variation with V_{Ch}).

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART DTXS AND DIGITAL PAS

	This work			RFIC'16 [1]	PAWR'16 [2]	JSSC'17 [3]	IMS'17 [4]	IMS'11 [5]
Technology	40 nm CMOS + LDMOS			180 nm CMOS SOI + GaN	180 nm CMOS SOI	130 nm CMOS	GaN	65 nm CMOS + GaN
Architecture	Polar DTX			Broadband Polar DTX	Polar Doherty DTX	Multi-Phase SC-PA	Broadband EER DTX	Outphasing PA
f_c (GHz)	2.1			0.9	0.9	1.8	2.1	1.95
Supply (V)	1.1/2.5/20		1.1/2.5/28	1.7/4.1/15	1.7/4.1	3	17	1.2/5.0/26
P_{max} (W)	18.5[1]	23.5[2]	29.8[3]	2.8[4]	2.0	0.398	2.5	19
Peak Drain Efficiency (%)	66.7[1]	62.6[2]	40.0[3]	57.7	55.4	n/a	51.7[4,5]	68.5[4]
Peak System Efficiency (%)	60.4[1]	58.1[2]	38.1[3]	n/a	n/a	24.9	n/a	n/a
Bandwidth (MHz)	n/a	10	n/a	5.0	No dynamic signals used	10	4.0	3.84
Signal Type		256-QAM		16-QAM		64-QAM LTE	256-QAM	WCDMA
EVM (%)		1.2		n/a		3.5	1.1[4,6]	n/a
$ACLR_1$ (dBc)		−46.1		−36.6		−30.3	−44[4,6]	−47

[1]43 % LO duty-cycle [2]Uncorrected LO duty-cycle (≈ 50 %) [3]Maximum output power [4]Estimated from figure [5]EER stack efficiency [6]No DPD

4) Use a finer (multilevel) thermometer coding, resulting in better linearity and ENOB [similar to digital-to-analog converters (DACs)].
5) Duty-cycle control should be implemented in a very robust way to avoid jitter; therefore, analog duty-cycle control loops can be best avoided.
6) Based on its digital amplitude data, the DTX can go from full power to zero in a single sample, yielding a very rapid change in the supply current, which, due to the always present self-inductance in the dc bias network, can cause a large overvoltage condition on the RF output stage that can be easily damaged. Thus, soft shutdown in a testing phase is essential.

In future implementations, when optimized LDMOS/GaN technology and high-density interconnect (such as high-density flip-chip) are available, the effective DTX resolution (ENOB) and related linearity and bandwidth can be drastically increased by using more and smaller segments. Also, the overall DTX system efficiency would benefit strongly from avoiding interdie ESD protection, which results in (unnecessary) additional capacitive loading of the CMOS drivers. In such a situation, the overall TX system efficiency will closely approach the drain efficiency of the RF power technology used.

XI. CONCLUSION

World's first bits-in-RF-out, fully digital mixing-DAC with an output power above 10 W has been presented as a proof of concept, focusing on output power and energy efficiency. Depending on the operating mode, the RF output power varied from 18.5, 23.5, and 29.8 W, with associated system efficiencies of 60.4%, 58.1%, and 38.1%, respectively. Compared to prior-art DTX implementations, a 10× improvement in output power has been achieved while yielding a record high peak system efficiency. Equally important is the almost perfect scaling of its total power consumption with the RF output voltage delivered. Namely, it is this property that will enable significant energy savings when applied in mMIMO base stations. Within the technology constraints for this demonstrator, encouraging results were also obtained for modulated signals, showing an ACLR of −46.1 dBc and an rms EVM of 1.2% for a 10-MHz 256-QAM signal and an $IM_3 \leq -51.4$ dBc for an 80-kHz two tones. Although these are promising results, more work is still needed. Namely, efficiency enhancement techniques, such as Doherty or (mixed-mode) outphasing, need to be applied to improve average efficiency. Furthermore, to improve linearity, future DTX implementations should offer a higher number of effective bits. This can be achieved by improving the dc supply decoupling of the digital controller to avoid any V_{GS}–I_{DS} variation as well as minimizing g_m in the "ON"-state by even better shaping the $I_{DS}(V_{GS})$ relation of LDMOS or GaN technologies used in the segmented output stage for the available driver voltage swing. Finally, more advanced interconnect schemes need to be applied between the CMOS controller and the segmented output stage, yielding lower interconnect parasitics while allowing more thermometer bits. When these issues are addressed, high-power DTX solutions are ready to take over conventional analog solutions and will offer higher system integration and higher functionality at lower costs and lower energy consumption.

APPENDIX A
POSTPRODUCTION TUNING OF THE DTX

The DTX demonstrator hardware and its class-BE output matching network were designed together while assuming V_T of 0.8 V. To deal with the uncertainty in realized V_T, the postproduction tuning possibilities of the DTX demonstrator are evaluated next. Lowering the duty cycle d gives the output stage more time in the "OFF"-state, resulting in a lower drain voltage at the switching moment, yielding lower switching losses.

Assuming $V_T = 0.8$ V and varying both d and V_{LD} results in the efficiency dependencies, as shown in Fig. 19. Note that the drain efficiency can be slightly improved by decreasing d to 40%. Decreasing d further degrades the efficiency due to the finite rise and fall times of the driver. The impact of V_T is evaluated in Fig. 20 for $d = 50\%$, showing that, in general, the drain efficiency increases for lower values for V_{LD}. However, since the peak output power also drops, while P_{Ch} for peak output power remains constant, the overall system efficiency

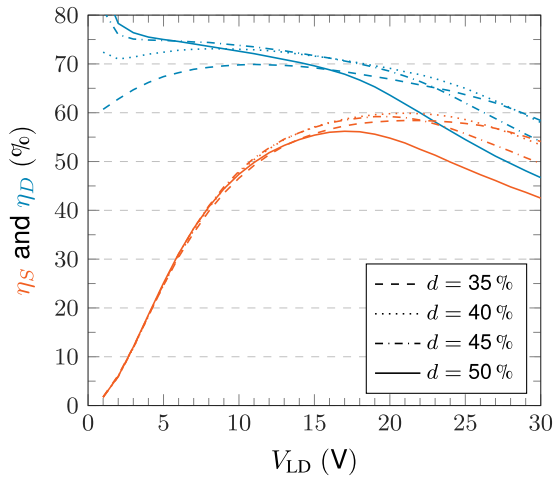


Fig. 19. System and drain efficiencies versus V_{LD} with postproduction duty-cycle adjustment, assuming a realized V_T of 0.8 V.

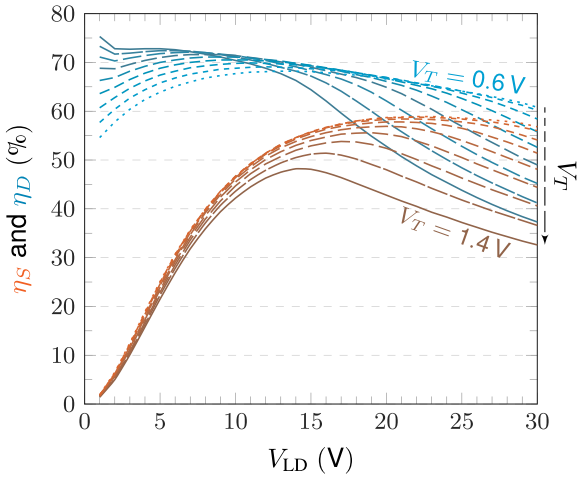


Fig. 20. System and drain efficiencies versus V_{LD} for potential realized V_T-shifts, assuming a duty cycle of 50%.

drops. Decreasing V_T results in more output power, yielding higher system efficiencies. For higher values of V_{LD}, aside from more switching-related losses, the nonlinear LDMOS C_{DS} changes to a lower value, resulting in a mismatch with the desired class-BE loading, also causing a decrease in drain efficiency.

Appendix B
Derivation of the Chain Capacitance

From the definition in [25], the equivalent switch resistance R_{dr} is defined as the resistance that discharges the capacitive load C_L from V_{Ch} to $V_{\mathrm{Ch}}/2$ in the same time as a fully modeled nMOS device would or charges from 0 to $V_{\mathrm{Ch}}/2$ in case of a pMOS device. The related propagation delay for a step input is $t_p = \ln(2)\, R_{\mathrm{dr}}(C_{\mathrm{dr},o_1} + C_L)$. To have the same delay for low-to-high $t_{pH\to L}$ and high-to-low $t_{pL\to H}$, the nMOS and pMOS should have the same equivalent resistance $R_{\mathrm{dr}_1} = R_{\mathrm{dr},p_1} = R_{\mathrm{dr},n_1}$ [Fig. 1(b)]. The effective input and output capacitances of the k^{th} CMOS inverter in the chain (numbering starting from the load) are then given by $C_{\mathrm{dr},i_k} = C_{\mathrm{dr},ip_k} + C_{\mathrm{dr},in_k}$ and $C_{\mathrm{dr},o_k} = C_{\mathrm{dr},op_k} + C_{\mathrm{dr},on_k}$, respectively [Figs. 1(b) and 7(b)]. Furthermore, the technology-dependent self-loading factor is defined as $\gamma = (C_{\mathrm{dr},o_k}/C_{\mathrm{dr},i_k})$.

Then, from [25, eqs. (5.30) and (5.37)], $t_{p,\mathrm{step}_k} = t_{p0}(1 + (f_k/\gamma))$ and $t_{p_k} = t_{p,\mathrm{step}_k} + \eta t_{p_{k+1}}$. Defining the tapered buffer chain such that the propagation delays and effective fan-outs are constant (i.e., $t_{p_k} = t_p \forall k$ and $f_k = f \forall k$) results in

$$t_p(1-\eta) = t_{p,\mathrm{step}} \tag{15}$$

and therefore

$$f(t_p) = \gamma\left(\frac{t_p}{t_{p0}}[1-\eta] - 1\right). \tag{16}$$

Note that $1 - \eta = t_{p,\mathrm{step}}/t_p$, which can be empirically determined for a buffer chain with $f = 1$, resulting in

$$f(t_p) = \gamma\left(\frac{t_p}{t_{p0}}\frac{t_{\mathrm{step}_1}}{t_{p_1}} - 1\right). \tag{17}$$

Then, filling in $t_p = \ln(2)R_{\mathrm{dr}}(C_{\mathrm{dr},o_1} + C_L) + \eta t_p = \ln(2)R_{\mathrm{dr}}(C_{\mathrm{dr},o_1} + C_L)/(1-\eta)$ and $C_{\mathrm{dr},o_1} = t_{p0}/(\ln(2)R_{\mathrm{dr}_1})$, which results in (9).

The total segment capacitance is the sum of the load capacitance and all the effective (including intrinsic) inverter input and output capacitances

$$C_{\mathrm{seg}} = C_L + C_{\mathrm{dr},o_1} + C_{\mathrm{dr},i_1} + \cdots + C_{\mathrm{dr},o_N} + C_{\mathrm{dr},i_N} \tag{18}$$

$$= C_L + \frac{C_{\mathrm{dr},o_1} + C_{\mathrm{dr},i_1}}{f^0} + \cdots + \frac{C_{\mathrm{dr},o_1} + C_{\mathrm{dr},i_1}}{f^{N-1}} \tag{19}$$

$$= C_L + C_{\mathrm{dr},i_1}(1+\gamma)\sum_{k=0}^{N-1} f^{-k} \tag{20}$$

giving (6) by the sum of a geometric series and that $C_{\mathrm{dr},i_1} = C_L/f$. Then, by the definition of M [see (7)] and substituting in $N = \log_f F + 1$, it gives

$$M = 1 + \frac{1+\gamma}{f}\left(\frac{fC_L - C_{\mathrm{dr},i_N}}{(f-1)C_L}\right). \tag{21}$$

By assuming $C_L(f-1) \gg C_{\mathrm{dr},i_N}$ the last factor can be approximated by $f/(f-1)$, giving (8).

An additional assumption made here is that the total number of stages N is allowed to be fractional. Logically, the latter cannot be implemented and should be rounded up. However, this estimation is adequate since the smallest inverter stage will have a negligible capacitance compared to the final stage.

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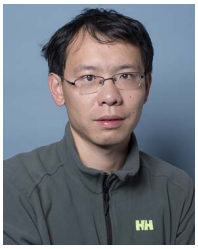

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