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A −107.8 dB THD+N Low-EMI Multi-Level Class-D Audio Amplifier

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Abstract

This paper describes a class-D audio amplifier with a multi-level output stage that reduces both EMI and idle power. High loop gain, and thus high linearity, are enabled by a relatively high (4.2 MHz) switching frequency, which relaxes the requirements on its output LC filter. Fabricated in a 180nm BCD technology, it can drive 14 W into an 8-Ω load with state-of-the-art performance: −107.8 dB THD+N, 91 % peak efficiency, and 7 mA quiescent current. It meets the CISPR 25 Class 5 radiated emission standard with a low-cost 580 kHz LC filter, improving the state-of-the-art by 5.8x.

Introduction

Due to their high power efficiency, Class-D amplifiers (CDA) have largely replaced their class-AB counterparts in mobile and consumer applications. In automotive applications, however, the more stringent EMI standards often require a bulky LC filter with a low cutoff frequency (≤ 100 kHz), thus increasing system size, cost and weight [1, 2]. Furthermore, low idle power is a must, since tens of channels may be needed. In addition, high linearity is always desired for good sound quality. The proposed multi-level CDA addresses all of these challenges.

Multi-Level Output Stage

In order to mitigate EMI, various multi-level output stages have been proposed. In [3], the output stage uses two external capacitors per channel in a bridge-tied-load (BTL) configuration and requires complex charge balancing circuitry. The output stage in [4] is sensitive to the timing mismatch of the gate driving signals, which increases gate driver complexity. In [5], the proposed 7-level output stage requires two extra power supplies capable of sourcing large load currents, which significantly increases system cost.

In this paper, a multi-level output stage is proposed that significantly reduces EMI and minimizes switching activity in idle operation without the need for extra flying capacitors, complex circuitry or extra supplies. A gate charge reuse technique further reduces idle power. Fig. 1 shows the proposed multi-level output stage in a BTL configuration. It consists of an NLDMOS-based H-bridge ($M_{H/L,\ P/N}$) and two sets of back-to-back NLDMOS transistors ($M_{CM1/2,\ P/N}$) that connect the output nodes to a mid-rail voltage PVCM. An on-chip linear regulator, which only consumes 7% of the idle power, regulates PVCM and smoothly brings the output to mid-rail at start-up. To ensure low common-mode (CM) EMI, the output stage switches differentially, establishing a mid-rail CM level and inheriting the two output states of AD modulation. A 3rd state, with zero differential output, can be established by using $M_{CM1/2,P/N}$ to short the outputs. It is important to note that in this state, no load current is supplied by PVCM (Fig. 1). During idle operation, the output stage is mainly in this state, minimizing switching activity and idle power. This offers significant advantage over two-level CDAs [1, 2], where switching loss and ripple current loss (especially when using small inductors) can lead to excessive power consumption. To save area, M_{CM1} and M_{CM2} are smaller than M_H and M_L. Despite their much higher series on-resistance (3x that of M_H and M_L), they only degrade peak efficiency by ~0.5%, as $M_{H/L,P/N}$ carry most of the load current at high output power levels.

Fig. 2 shows the gate driving circuitry featuring gate charge reuse. $M_{H,P/N}$ and $M_{CM2,P/N}$ are driven by floating 4V supplies, derived from the bootstrap voltage V_{BST} [1]. C_{CM} acts as a charge buffer, allowing the gate charging currents of $M_{CM1,P/N}$, sourced by PVDD, to be reused for the gates of $M_{L,P/N}$.

Closed-Loop Class-D Amplifier

As shown in Fig. 3, the proposed multi-level output stage is driven by a fully differential 3rd-order loop filter [1]. An RC oscillator built around an active integrator generates a fully differential 2.1 MHz triangle wave. Two comparators implement a multi-level PWM scheme (Fig. 4) by comparing the inverted and non-inverted triangle waves to the loop filter output. In contrast to other schemes [1, 3], this PWM scheme does not produce quantization noise in the AM band, making its AM EMI less sensitive to component mismatch in the LC filter. The high switching frequency enables an 800 kHz loop bandwidth and > 82 dB loop gain over the audio band. A 2-bit trimming scheme ensures that the loop filter's RC time constants are robust to process spread.

Measurement Results

In a 180 nm BCD process, the proposed CDA occupies an active area of 5mm^2 (Fig. 5), of which the output stage occupies 1.8mm^2. Despite the high switching frequency, it only draws 7 mA from a 14.4 V supply during idle operation, thanks to the multi-level architecture and gate-charge reuse technique. A small LC filter (470 nH, 160 nF) attenuates output switching tones. Fig. 6 shows the CDA's measured output waveform, proving minimal switching activity for zero input. As shown in Fig. 7, it achieves a noise-limited THD+N of −99.7 dB for a 1 kHz input when driving 1W into an 8-Ω load. At 10 W, this improves to −107.8 dB (Fig. 8). For a 4-Ω load, a THD+N of −102.6 dB is measured at 17.3 W. As shown in Fig. 9, the measured peak efficiency (10% THD) is 91% and 87% for 8-Ω and 4-Ω loads, respectively. Fig. 10 shows the EMI measurement setup, in which the CDA is connected to a 12V battery supply and a 4-Ω load using 1.5 m-long unshielded cables. Fig. 11 shows the radiated emission measured per the CISPR 25 Class 5 standard from 150 kHz to 1 GHz. With a 580 kHz LC filter, the CDA passes the test with a 5.7 dB margin. Table I compares this work with other state-of-the-art two-level [1, 2] and multi-level [3-5] CDAs. This design achieves the best THD+N, enables a 5.8x higher LC-filter cutoff frequency when compared to another automotive-compliant CDA [2], and obtains the lowest idle current per channel when compared to other CDAs switching at ≥ 2 MHz [1, 2].

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[4] P. Siniscalchi et al., *JSSC*, 2009. [5] J. Lee et al., *ISSCC*, 2017.

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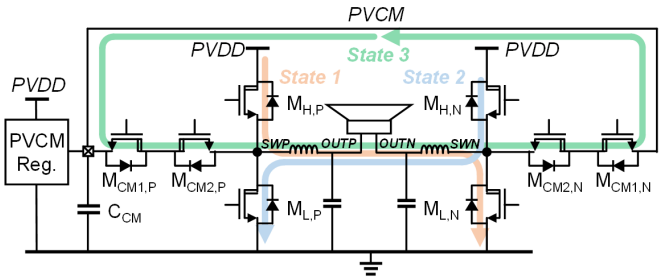

Fig. 1. Simplified schematic of the proposed 3-level output stage.

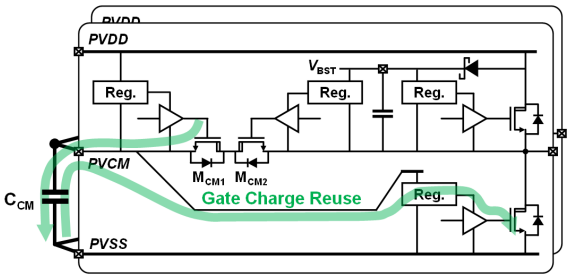

Fig. 2. Gate drivers in the proposed 3-level output stage.

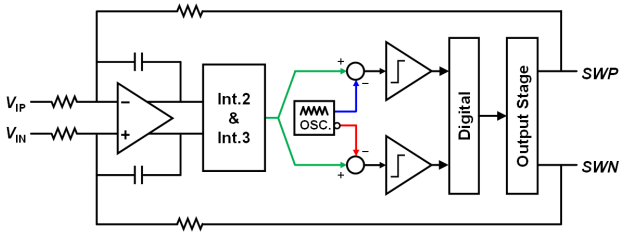

Fig. 3. Architecture of the closed-loop class-D amplifier.

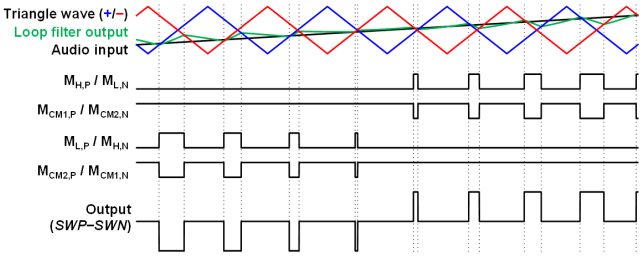

Fig. 4. Timing diagram of multi-level PWM generation.

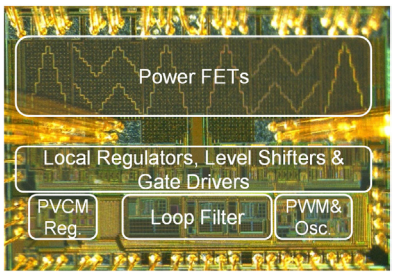

Fig. 5. Die micrograph.

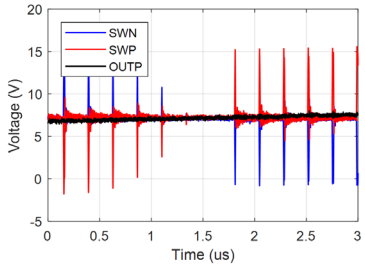

Fig. 6. Output waveform before LC filter (SWP, SWN) and after (OUTP).

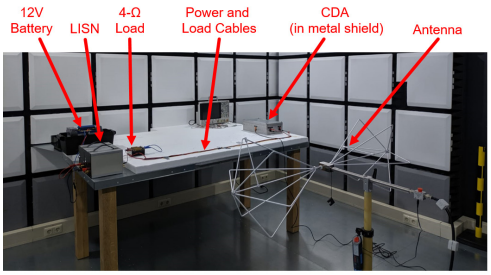

Fig. 10. EMI measurement setup.

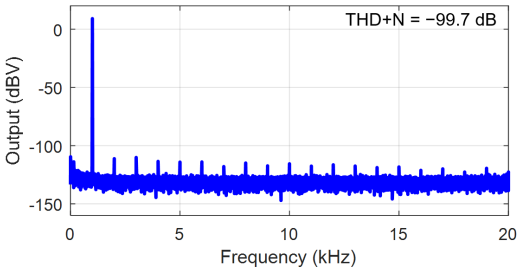

Fig. 7. FFT at 1W output driving 8-Ω load.

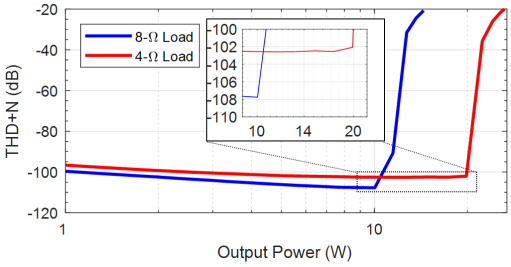

Fig. 8. THD+N vs. Output Power.

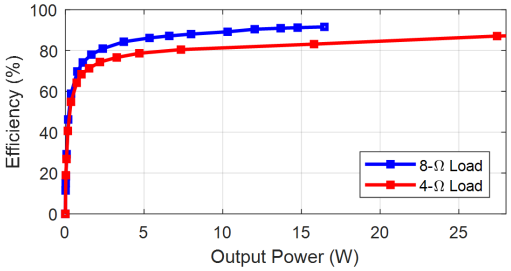

Fig. 9. Efficiency vs. Output Power.

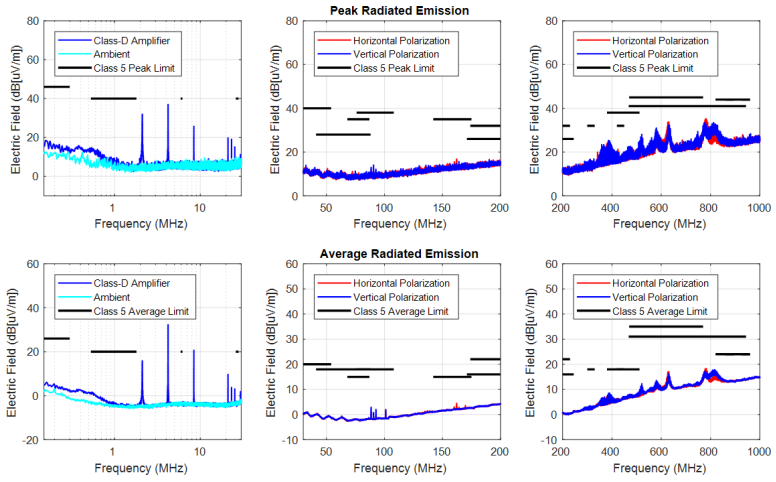

Fig. 11. Measured radiated emission at 12 W output power (4-Ω load).

Table. I. Performance summary and comparison.

	This Work		[1]	[2]	[3]	[4]	[5]
Architecture	PWM 3 Level		DSPWM 2 Level	PWM 2 Level	PWM 5 Level	PWM 3 Level	PWM 7 Level
f_{SW} (kHz)	4200		2000	2100	165~660	250	700
f_{LC} (kHz)	580		100	88	N.A.	-	N.A.
I_Q (mA) / Channel	7		17	~40	2.8	-	3.5
P_{IDLE} (mW) / Channel	94		245	N.A.	70	-	N.A.
Supply Voltage (V)	14.4		14.4	14.4	24	12	2.5~5
R_L (Ω)	8	4	4	4	4	8	8
$P_{OUT,MAX}$ (W)	14	28	28	27	70	10	10
Efficiency	91%	87%	91%	86%	90%	90%	91%
Min. THD+N (1kHz) (%)	0.0004	0.0007	0.0008	~0.015	0.003	0.1	0.0023
SNR (dB-A)	109.7		109	N.A.	N.A.	-	106
DR (dB-A)	111.2		N.A.	N.A.	110	-	N.A.
EMI standard	CISPR 25 Class 5		CISPR 25 Class 5*	CISPR 25 Class 5	N.A.	FCC Class B	N.A.

*Only 150 kHz ~ 30 MHz reported