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A 28-W, −102.2-dB THD+N Class-D Amplifier Using a Hybrid ΔΣM-PWM Scheme

Shoubhik Karmakar, *Graduate Student Member, IEEE*, Huajun Zhang, *Graduate Student Member, IEEE*, Robert van Veldhoven, *Senior Member, IEEE*, Lucien J. Breems, *Fellow, IEEE*, Marco Berkhout, *Member, IEEE*, Qinwen Fan, *Senior Member, IEEE*, and Kofi A. A. Makinwa, *Fellow, IEEE*

***Abstract*— This article presents a 28-W class-D amplifier for automotive applications. The combination of a high switching frequency and a hybrid multibit ΔΣM-PWM scheme results in high linearity over a wide range of output power, as well as low AM-band EMI. As a result, only a small (150-kHz cutoff frequency), and thus low-cost, *LC* filter is needed to meet the CISPR-25 EMI average limit (150 kHz–30 MHz) with 10-dB margin. At 28-W output power, the proposed amplifier achieves 91% efficiency while driving a 4-Ω load from a 14.4-V supply. It attains a peak THD+N of 0.00077% (−102.2 dB) for a 1-kHz input signal.**

***Index Terms*— ΔΣM, audio power amplifier, class-D amplifier, electro-magnetic interference (EMI), hybrid, pulsewidth modulation (PWM).**

I. Introduction

THE trend toward more and more audio channels in modern automobiles is driving the development of highly efficient audio amplifiers with small system size and a low bill-of-materials. Compared with their class-AB counterparts, class-D amplifiers are well suited for such applications due to their high power efficiency (∼90%), which makes their thermal management lighter and cheaper.

Compared with class-AB amplifiers, one drawback of class-D amplifiers is the presence of high-frequency switching activity at their outputs. While this is not necessarily an issue in mobile devices [1], it can be quite detrimental to automotive applications. The long cables connecting such amplifiers to their power supplies and speakers can act as antennas for high-frequency switching signals, causing unacceptable levels of electro-magnetic interference (EMI). Consequently, automotive class-D amplifiers are subject to stringent EMI standards, the most common being CISPR-25 [2].

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EMI is especially problematic when it falls in the AM band (535–1605 kHz). In conventional class-D amplifiers, which are based on fixed-frequency pulsewidth-modulation (PWM), the PWM carrier frequency (f_{PWM}) is generally set below 500 kHz to avoid AM-band interference. However, bulky *LC* filters with low cutoff frequencies (f_{LC} between 20 and 40 kHz) are then required to suppress the resulting PWM tones (harmonics of f_{PWM}), leading to significant increases in system size and cost.

In a bid to achieve higher *LC* cutoff frequencies, while meeting the same EMI standards, and without altering f_{PWM}, additional measures are required. Examples of these are the use of multilevel or multiphase PWM architectures [3]–[8]. The multiphase architecture described in [3], reduces the ripple current in the speaker cables and, therefore, lowers EMI. However, this is at the cost of two extra inductors per channel, significantly increasing system bulk and cost. Multilevel output stages [5], [6], can also reduce PWM tones by decreasing the voltage swing across the switching nodes. The 7-level output stage in [5] uses each half of an H-bridge output stage to realize two extra levels, thereby reducing PWM tone energy. However, it requires an extra power supply capable of sinking and sourcing large load currents, which significantly increases system size and cost. Similarly, Høyerby *et al.* [6] realizes one extra level per half H-bridge, at the cost of two external flying capacitors. In general, both multilevel and multiphase architectures also require larger power stages and, hence, more die area to implement the additional low ohmic output switches.

A more cost-effective way to satisfy EMI requirements and relax *LC* cutoff frequency is to increase f_{PWM} beyond the AM band [9]. Since the unity gain frequency of a stable class-D amplifier must be less than f_{PWM}/π [10], increasing f_{PWM} enables higher loop gain in the audio band (20 Hz–20 kHz), which, in turn, results in better suppression of output-stage non-linearity. However, increasing f_{PWM} means that the output stage will have to reproduce narrower pulses. Due to its finite slew rate, however, sufficiently narrow pulses will not be able to swing from rail to rail, thus causing extra non-linearity.

To avoid the narrow pulses produced by conventional PWM, pulse-density-modulation (PDM), using a 1-bit delta–sigma modulator (ΔΣM), can be used [11]. The minimum pulsewidth will then be defined by the modulator's sampling frequency (f_S), which can be optimized to prevent slew-rate

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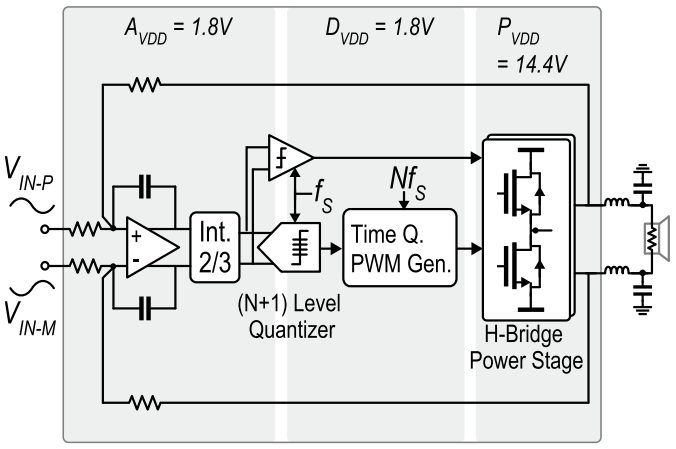

Fig. 1. Simplified block diagram of the fully differential CDA.

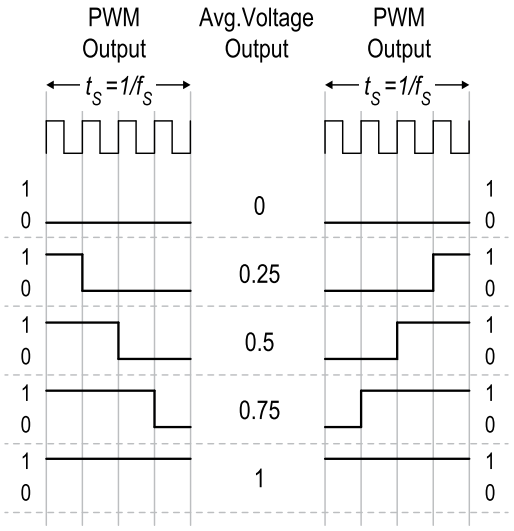

Fig. 2. Generation of time-quantized PWM pulses using a higher clock rate.

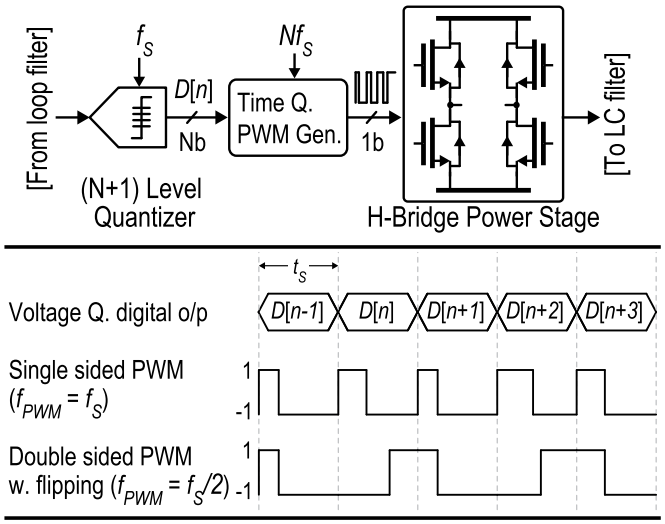

Fig. 3. Time-domain signal path from quantized digital outputs to normalized PWM signals.

distortion, while still being high enough to achieve high loop gain, and thus high linearity. However, a 1-bit $\Delta\Sigma$M will typically have a limited stable input range, and its out-of-band (OOB) quantization noise will cause EMI. Simply increasing f_S to reduce the OOB noise in the AM band will drastically increase the modulator's average switching frequency and, therefore, increase the amplifier's switching losses proportionally. In [11], adding hysteresis to the quantizer of a $\Delta\Sigma$M lowers the average switching frequency. However, it will still generate excessive AM-band EMI. Moreover, its loop filter must be dynamically switched from 7th order (for low in-band quantization noise) to 2nd order (to maintain large-signal stability), which complicates its design and degrades large-signal linearity.

This article, an extension of [12], describes a class-D amplifier that employs a hybrid $\Delta\Sigma$M-PWM architecture to limit the minimum pulsewidth applied to the output stage, as well as the resulting AM-band EMI. An overview of the fully differential, analog-input class-D amplifier is shown in Fig. 1. It consists of a 3rd order loop filter, followed by a multilevel quantizer, whose output is then applied to a pulsewidth modulator that drives a 2-level output stage. A prototype achieves the state-of-the-art linearity over a wide output power range, while meeting the CRISPR-25 standard with a relaxed *LC* filter, and no additional off-chip components.

This article is organized as follows. Section II introduces the proposed architecture and describes its benefits and challenges. Sections III and IV describe the implementation of the low- and high-voltage blocks, respectively, at the circuit level. Measurement results and comparisons are given in Section V, and the conclusions are summarized in Section VI.

II. Modulator Architecture

Compared with their 1-bit counterparts, multilevel $\Delta\Sigma$Ms have several advantages, such as reduced OOB noise and a larger stable input range. However, as discussed in the introduction, multilevel output stages are expensive in terms of both silicon area and off-chip components.

In this work, a multilevel $\Delta\Sigma$ to PWM convertor drives an H-bridge in a bid to achieve the best of both worlds. An $(N + 1)$-level quantizer converts the loop filter output into a multilevel digital output, which is then converted into a two-level signal by a PWM generator that outputs a series of 1s and 0s at a higher clock frequency $f_{\mathrm{CLK}} = N \cdot f_S$ [13]. The case when $N = 4$ is illustrated in Fig. 2, where five different two-level PWM pulses with a period t_S result in five different average values that can each be assigned to one level of a 5-level quantizer. The main considerations that inform the choice of N and f_S are the *LC* filter cutoff frequency and its tolerance, the desired in-band SQNR, and the narrowest pulsewidth that the output stage can faithfully reproduce. Each of these considerations will be discussed in detail below.

A. Modulation Scheme and Sample-Rate-f_S

The signal path from the N-level quantizer to the high-voltage output stage is shown in Fig. 3, along with the normalized time-domain signals. Based on the quantizer's output, the PWM generator serially outputs the appropriate bits at f_{CLK}. As shown in Fig. 2, there are two ways of generating

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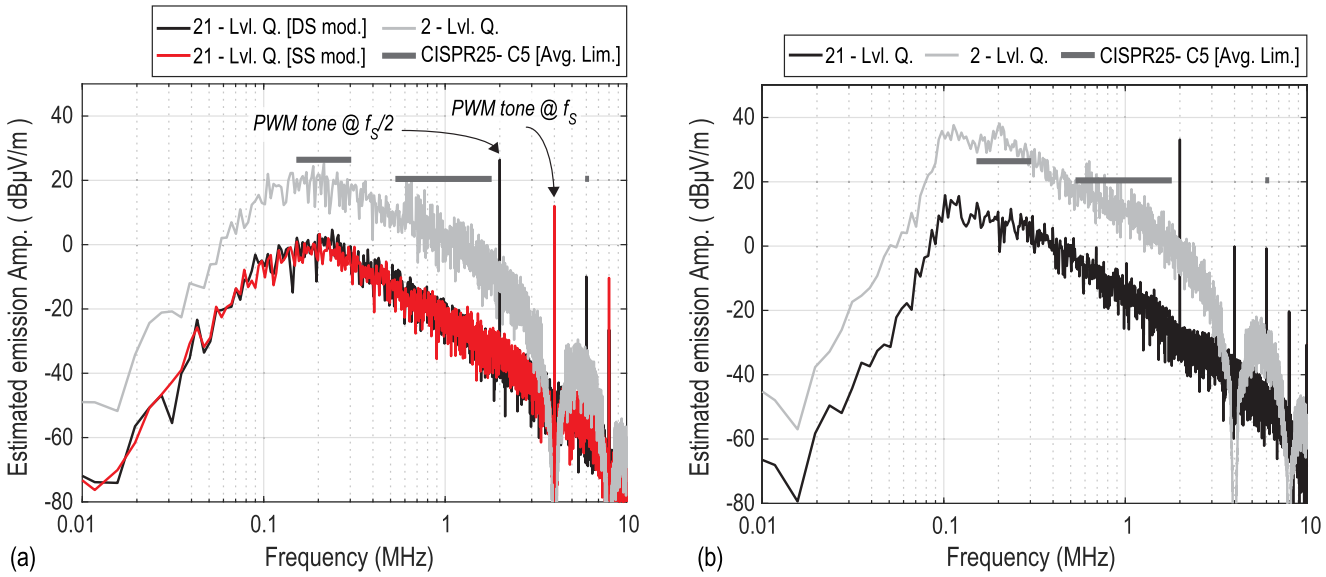

Fig. 4. Simulated estimates out-of-band emission. (a) Comparison of the various modulation schemes. (b) Effect of ±15% *LC* mismatch on both the 21-level (DS) hybrid modulation and the conventional 2-level ΔΣM.

the same average value in one sample period. Consistently generating all the 1s (or 0s) first results in a single-sided (SS) uniformly sampled PWM (UPWM) signal at a carrier frequency $f_{\mathrm{PWM}} = f_{\mathrm{S}}$ [14]. By alternately reversing the order of the bits, however, a double-sided (DS) signal can be generated, which halves f_{PWM}, together with the associated switching activity and switching losses. The resulting DS-UPWM signal, with the input sampled at twice the modulation frequency ($f_{\mathrm{S}} = 2f_{\mathrm{PWM}}$), is sometimes also referred to as asymmetric uniform-sampling [15]. In this design, to ensure some margin between the edge of the AM band and the PWM tone, while not incurring excessive switching losses, f_{PWM} is set to 2 MHz, and so $f_{\mathrm{S}} = 4$ MHz with DS modulation.

B. EMI, LC Filter Cutoff Frequency-f_{LC} and Tolerance

Since EM emissions are mainly caused by common-mode (CM) signals, the H-bridge is driven by AD modulated signals [16], [17]. The transitions of each half bridge are in anti-phase, which maintains a constant CM voltage at the output nodes. However, mismatch and timing skews in the two halves lead to some differential mode (DM)-to-CM leakage. Moreover, the use of non-twisted differential cables will cause extra DM-to-CM EMI leakage.

Fig. 4(a) shows the simulated EMI spectrum for different modulation schemes with a relaxed *LC* filter cutoff frequency ($f_{\mathrm{LC}} = 100$ kHz). A conventional 2-level ΔΣM generates a PDM output with a large amount of OOB noise. By increasing the number of quantization levels and using the hybrid modulation technique, the OOB noise is reduced and converted into PWM tones. In this design, $f_{\mathrm{CLK}} = 80$-MHz clock results in 21 levels, which significantly reduces the OOB noise and positions the PWM tone at 2 MHz. Also, by using DS instead of SS modulation, the amplifier switches at half the frequency for the same OOB noise.

It is worth pointing out that while the 2-level ΔΣM appears to (just) satisfy the EMI requirements, this is not the case if *LC* filter tolerances (up to ±15%) are considered. As shown in Fig. 4(b), this results in significantly more DM-to-CM EMI leakage. Under the same conditions, however, the 21-level hybrid modulator still satisfies the EMI requirements with an acceptable margin. Furthermore, f_{LC} can be made even higher, if tighter component tolerances can be guaranteed. While the amplifier's power supply connections also produce EMI, local supply decoupling is enough to reduce this to negligible levels.

Compared with [3] and [10], the increased switching frequency means that high in-band loop gain can be achieved even with a 3rd order loop filter. As a result, the 21-level modulator achieves an in-band SQNR of ∼122 dB and a maximum stable amplitude (MSA) to ∼97% FS, which are both significantly larger than the 1-bit case. The end result is a thermal-noise limited design with a high dynamic range.

C. Pulsewidth Limitation and Quantizer Non-Uniformity

The multilevel voltage and time quantization described above uniformly distribute 21 bipolar steps (0.1 FS each) across the full scale both in the voltage and time domain. The minimum pulsewidth (12.5 ns) is then determined by $f_{\mathrm{CLK}} = 20 \cdot f_{\mathrm{S}} = 80$ MHz. In our design, however, the finite slew rate of the HV output stage and the propagation delay of the driving logic limit minimum pulsewidths to about 16 ns (typical), which worsens across PVT (Section IV). This can be accommodated by decreasing either N or f_{S}, at the expense of more OOB noise.

Since audio signals typically have a high crest factor (7–25 dB) [18], [19], they rarely reach FS levels. Therefore, a more pragmatic approach is to make the quantizer nonuniform at high input levels. This can be done by removing the quantization levels of ±[0.8;0.9]FS, as illustrated in Fig. 5,

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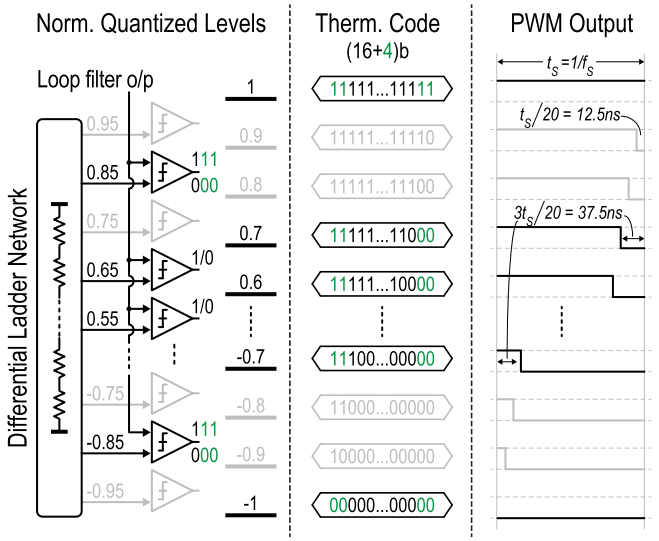

Fig. 5. Limiting the pulsewidth at extremely high modulation index by making the quantizer nonuniform.

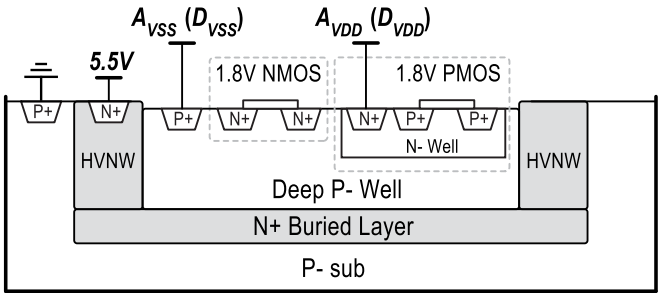

Fig. 6. Simplified cross section of the HV N-well used for 1.8-V device isolation.

thus relaxing the minimum pulsewidth requirement by 3x to 37.5 ns. Removing these levels reduces the total number of levels from 20 to 16. To keep the same average output values, the outputs of the two extreme comparators of the flash quantizer are, therefore, 0/1 padded (indicated in green), maintaining a throughput of 20 bits for the $20 \cdot f_S$ main clock. Although this tradeoff lowers the linear modulation range slightly (to ∼93%), the increased OOB noise (due to the increased step size) is negligible for signals close to FS.

III. Low-Voltage Circuits

The digital logic and analog circuits such as loop-filter integrators and quantizer are built using area and power efficient 1.8-V devices. However, due to bond-wire inductance, the high switching currents in the output stage can cause substantial substrate bounce (in the order of several volts). To prevent unwanted substrate coupling, sensitive low-voltage blocks are placed in high-voltage N-wells biased at 5.5 V. As shown in Fig. 6, deep P-wells within the N-wells serve as the local ground (A_{VSS}/D_{VSS}) for their respective supply domains.

A. 17-Level Quantizer

As illustrated earlier [Fig. 5(b)], a flash ADC is well-suited for implementing the quantizer. Since it directly outputs a thermometer code that can simply be transmitted to the output stage, the loop delay is kept minimum. Although it is much more power hungry than e.g. an SAR ADC, its power contribution is negligible compared with that of the power stage. Dual-difference comparators [20] were used to implement the quantizer. Non-linearity in the quantizer itself arises due to mismatch in the unit elements of the ladder and the individual offsets of the 16 comparators. Of these two, the ladder references have a 3σ spread of ∼400 μV, while the offset spread is within ∼40 mV. The gain of the quantizer is optimized to limit the swing of the loop filter output and ensure high linearity, while having a sufficiently large LSB step size ($V_{\mathrm{LSB}} \sim 102$ mV) to relax the offset requirements of the comparators. Extensive simulations confirm the absence of bubble errors over PVT. In the worst case, the loop gain preceding the quantizer is high enough to maintain an SQNR above 120 dB.

To compare the performance of the hybrid architecture with that of a 1-bit $\Delta\Sigma$M with the same loop filter, a 1-bit comparator was incorporated in parallel.

B. Fully Differential 3rd Order Loop-Filter

As shown in Fig. 7(a), the modulator employs a 3rd order filter. An NTF with optimally placed zeros and an out-of-band gain of 1.8 results in high MSA, low OOB quantization noise, and high loop-gain across the entire audio band [20].

The loop filter is realized as a cascade of highly linear active-*RC* integrators in a feedback (CIFB) configuration. Direct input feed-ins to the first two integrator's output suppress the audio band component at their outputs and significantly relax their linearity requirements. Due to their low-voltage coefficients, p-poly resistors and high density MIM capacitors are used to realize the various *RC* time constants. The noise in the audio band is primarily dominated by the 1st integrator, with the input resistors R_{IN} (=20 kΩ) accounting for ∼52% of the total noise, while OTA_1 and the feedback resistors R_{FB} add another ∼43%. The input resistance is a compromise between noise considerations and the requirements on the driving capability of a preceding DAC. The feedback resistors set a closed loop gain of 8× (18 dB). To compensate for *RC* process spread, (∼30%), the capacitors are made 2-bit trimmable that are trimmed manually (once) by observing the OOB-shaped noise content.

The OTAs [Fig. 7(b)] employ a 2-stage feedforward topology to provide the required gain. A capacitively coupled input feedforward path to the second stage ensures sufficient phase margin and high GBW [21]. Together, the three integrators draw 1.8 mA from the analog supply ($A_{\mathrm{VDD}} = 1.8$ V). After trimming, the filter's overall loop gain at 20 kHz is >76 dB across PVT, as shown in Fig. 8.

It is worth mentioning that the high loop gain also suppresses the adverse effects of clock jitter, which manifests itself in the output pulses as duty cycle errors and degrades audio performance [22]. In this design, up to 1 $\mathrm{ns_{RMS}}$ clock jitter ($f_{\mathrm{CLK}} = 80$ MHz) can be tolerated to maintain 120-dB SQNR.

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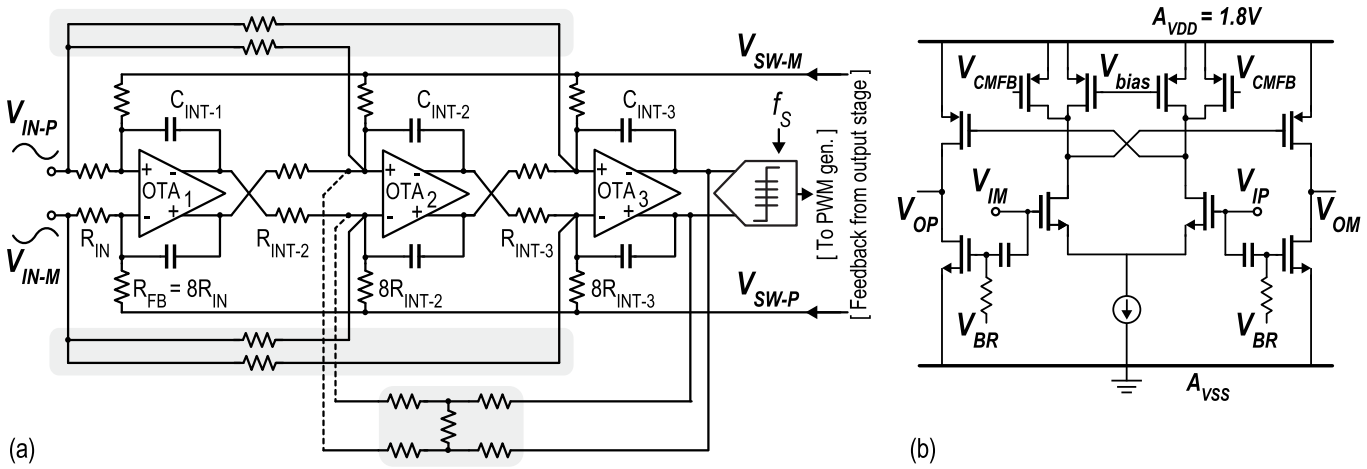

Fig. 7. (a) Simplified schematic of the fully differential loop filter. (b) Simplified schematic of the OTA.

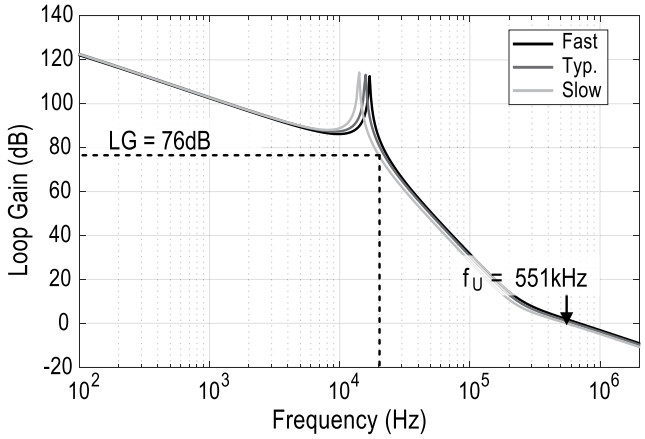

Fig. 8. Loop gain of the loop filter across process after trimming.

IV. Output Power Stage

The output power stage consists of a fully differential H-bridge structure and is capable of driving a 4-Ω BTL, along with associated driving circuits. Fig. 9 shows the circuit with half of it depicted in detail. The primary output switches are laterally diffused 20-V NMOS (N-LDMOS) transistors. The output power stage is responsible for >95% of the total quiescent power consumed in the chip.

Several factors contribute to the overall power dissipation in the output power stage [19], [23]; the dominant ones include conduction loss due to the on resistance of the output transistors (R_{ON}) and switching loss due to charging/discharging of gate capacitances (C_G). At high power levels, conduction loss dominates due to large signal current. Therefore, all output transistors ($M_{H/L}$) are sized for an R_{ON} of ∼100 mΩ at 100 °C to obtain an efficiency ∼90% close to FS. Meanwhile, the gate charge loss accounts for ∼18% of the total losses. It is not worth increasing the output transistor size to further reduce R_{ON}, as this would result in a large die area and higher idle power consumption, which is dominated by switching loss.

While all the high-voltage LDMOS devices have a high $V_{DS,MAX}$ rating, the sensitive nature of their gate oxides limits the maximum allowable V_{GS} to 5.5 V. To ensure that the gate voltages will never exceed this limit, linear voltage regulators are used to generate a localized 4.8-V supply to power all the circuits associated with driving the output switches [24]. This also provides sufficient de-coupling from supply and ground bouncing.

A. Linear Voltage Regulators

Since R_{ON} is relatively insensitive to V_{GS} variations, provided it has sufficient overdrive (>∼3 V), a closed-loop regulation for the gate-driver supply [24] is not required. A more area/power efficient solution, which avoids an HV error amplifier for every regulator, is to use an open-loop structure, as shown in Fig. 10(a). All the regulators share a common 1.2-V reference in the low-voltage section to derive a local 4.8-V reference using 1:1 current mirrors and scaled resistors (R, 4R). V_{4R} gets further reflected across an output decoupling capacitor (C_{Decoup}) of 12 pF, by maintaining equal current densities across M_{1-3}, providing a regulated output voltage $V_{REG} = V_{4R}$. The push–pull source-follower architecture provides a low output impedance, which, together with a C_{Decoup}, result in a relatively clean V_{REG} by sinking/sourcing large transient currents during switching activities.

Fig. 10(b) shows the output waveforms of both the high/low side regulators ($V_{REG-HS/LS}$) together with the V_{GS} of the high-/low-side output switches and the switching node V_{SW}. The typical case and variations across PVT are represented in black and gray, respectively. V_{REGs} exhibits a transient fluctuation within 250 mV across PVT, and thus guaranteeing safe operation of the output devices and associated circuits. Random mismatch in the resistors and current mirrors causes an additional variation of ∼180 mV (3σ) in V_{REG} [Fig. 10(c)], which results in a negligible R_{ON} spread of ∼1 mΩ.

The low-side regulators are powered directly from the high-voltage rail (P_{VDD}), while the boot-strapped voltages (V_{BS-X}) are generated by using internal Schottky diodes (D_S) and off-chip capacitors (C_{BS}) to power the high-side regulators. All HV LDMOS devices are realized in large isolation N-wells to achieve their ratings, making them area inefficient for small aspect-ratio transistors. Hence, wherever appropriate

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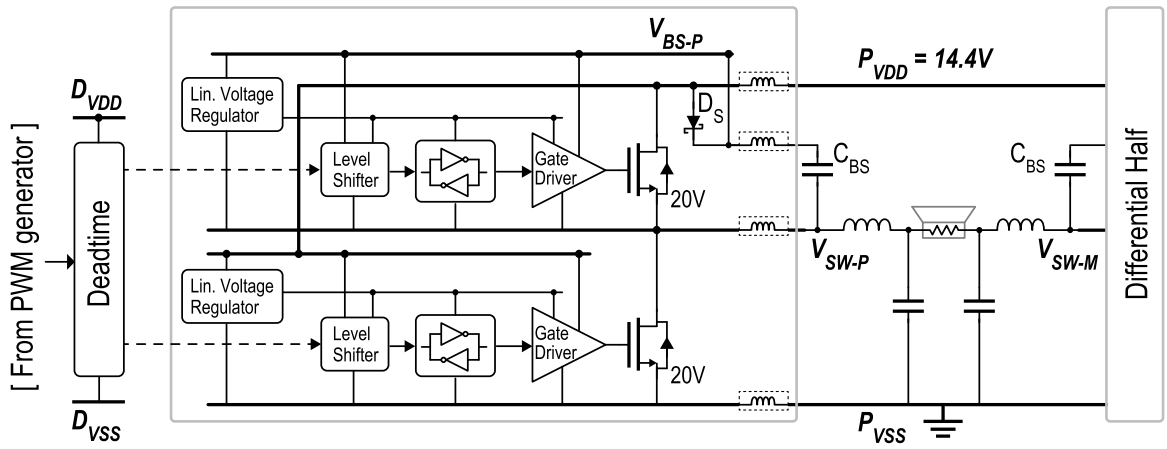

Fig. 9. Block diagram of the output power stage together with bonding wires.

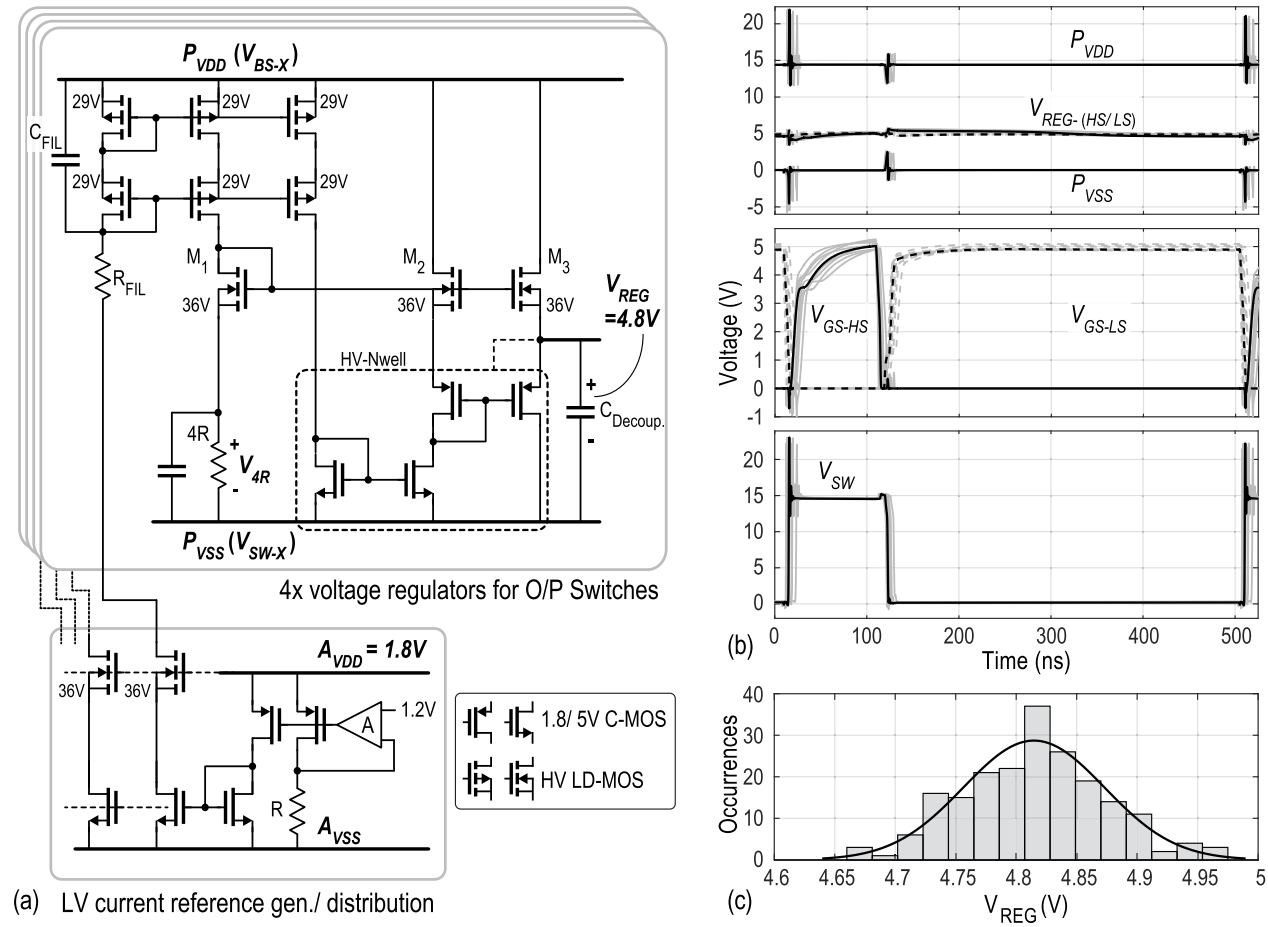

Fig. 10. (a) Schematic of the linear voltage regulators for the gate-driving circuits. (b) Output waveforms of the regulated voltage, V_{GS} of the switches and the output switching node, across process and temperature. (c) Monte Carlo spread in V_{REG} due to component mismatch.

($V_{DS} < 5$ V), low-voltage (5 V) devices are used. These are clubbed together in a single floating HV N-well [indicated by the black-dashed boxes in Fig. 10(a)], with the deep P-well acting as the local reference ground.

B. Level Shifters and Gate Drivers

Level shifters are used to transmit the signals from the digital domain ($D_{VDD} = 1.8$ V) to their respective high-voltage domains. High immunity from supply and ground bouncing can be attained by using a two-step approach similar to [24]. As shown in Fig. 11, complimentary digital signals, initially referred to a relatively clean D_{VSS}, are first up-shifted to $P_{VDD}(V_{BS})$ and then down-shifted to the output transistor's reference node P_{VSS} (V_{SW}). The fully differential structure and large headroom between D_{VSS} and $P_{VDD}(V_{BS})$ and between $P_{VDD}(V_{BS})$ and P_{VSS} (V_{SW}) makes this signal transmission robust to high common-mode ringing and prevents output latch errors. A pulsed constant bias current, with a typical

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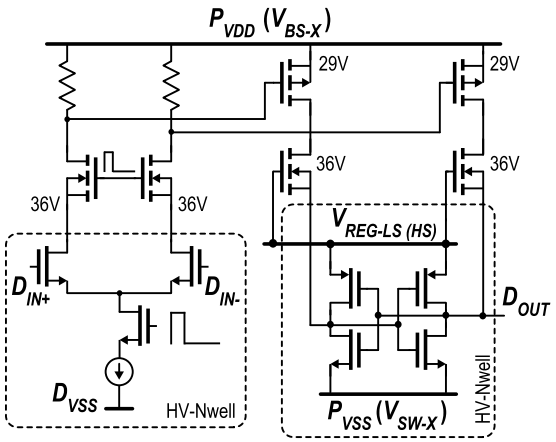

Fig. 11. Schematic of the two-step level shifter.

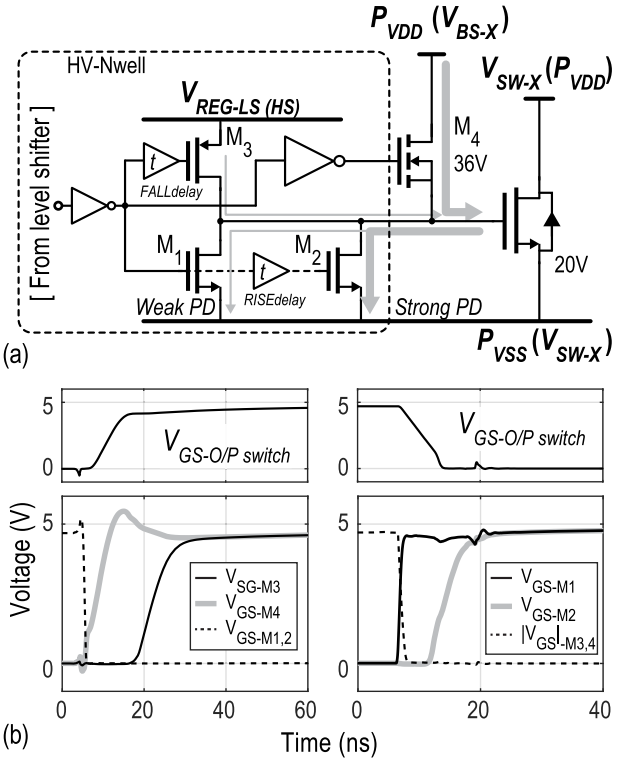

Fig. 12. (a) Schematic of the gate driver. (b) Associated gate driving signals and delays for turn-ON/OFF phases.

on duration of 15 ns, enables the level shifter shortly before a switching signal arrives at $D_{IN+/-}$, resulting in low average quiescent current (number).

Gate drivers, as shown in Fig. 12(a), are required to reliably charge/discharge the gates of the output transistors. In general, the pull-down strength of a gate driver has to be sufficiently larger than the pull-up strength to avoid cross conduction [25]. However, simply using a strong pull-down would cause an excessive amount of ringing due to large di/dt in the parasitic inductances of the bonding wire. To avoid this situation, a weak pull-down (M_1) first discharges the gate, after which, the stronger pull-down (M_2) is activated. The associated gate-driving signals are illustrated in Fig. 12(b). For charging

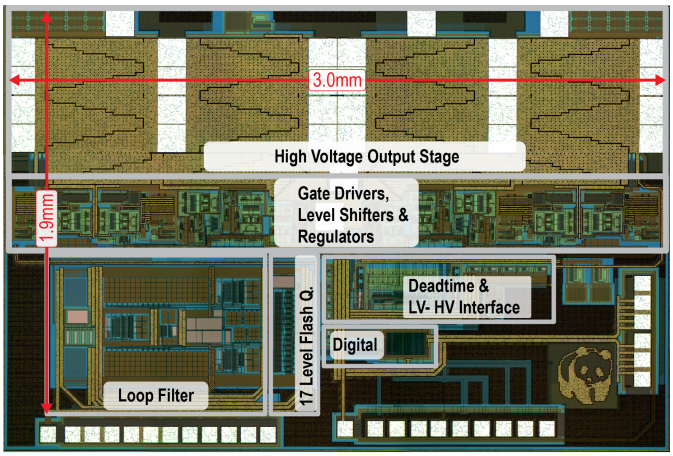

Fig. 13. Die micrograph.

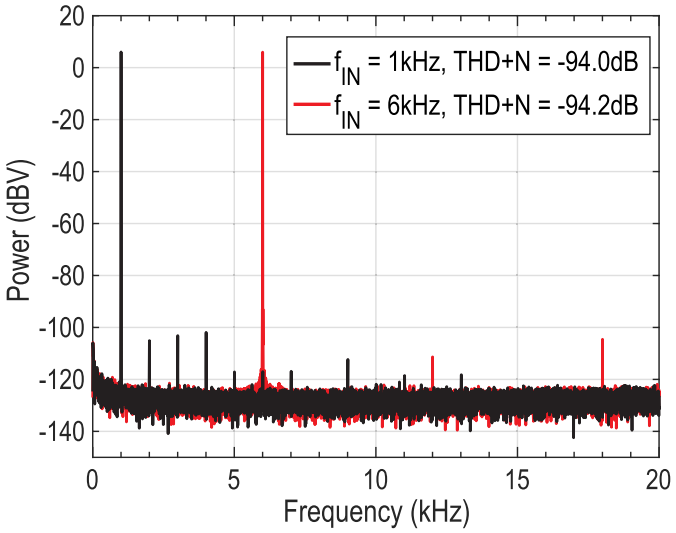

Fig. 14. FFT at 1-W output power across a 4-Ω load.

the gate, a pull-up using a 36-V N-LDMOS (M_4) is first activated to charge to gate up to roughly V_{REG}-V_T directly from P_{VDD} (V_{BS}). A PMOS (M_3) is then turned on to supply the remaining charge from the regulator. This reduces the regulator loading, reducing the transients on its output voltage. A minimal dead time of 7 ns (with ∼±15% variation across process and temperature) ensures no cross-conduction without causing a noticeable degradation in audio performance.

V. Measurement Results

The prototype hybrid class-D amplifier is realized in a TSMC 180-nm BCD bulk process, as shown in Fig. 13. It occupies an active area of 4.8 mm^2, with the high-voltage switches in the output power stage taking up 40% of the area, while the loop filter, whose area is dominated by the integration capacitors, takes up another 27%. The amplifier can drive a 4-Ω load and is powered from three separate supplies: A_{VDD} / D_{VDD} = 1.8 V, and P_{VDD} = 14 V. The main external components are the supply de-coupling capacitors (2 × 100 uF) and the *LC* filter with a cutoff frequency f_{LC} = 100 kHz (L = 2.2 μH, C = 1.15 μH).

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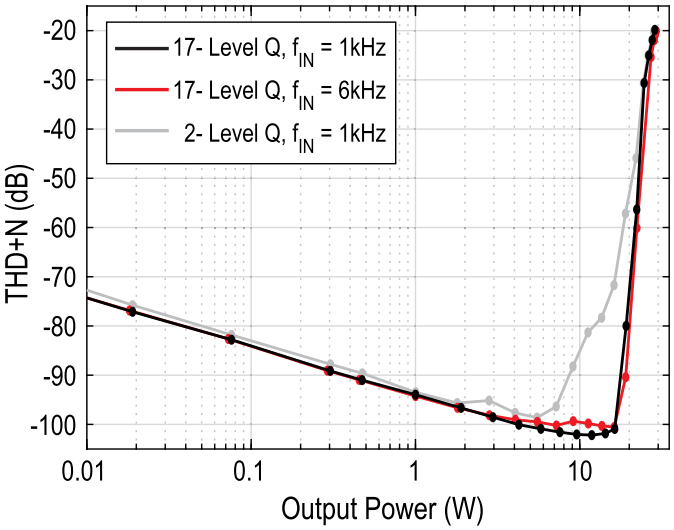

Fig. 15. THD+N across output power.

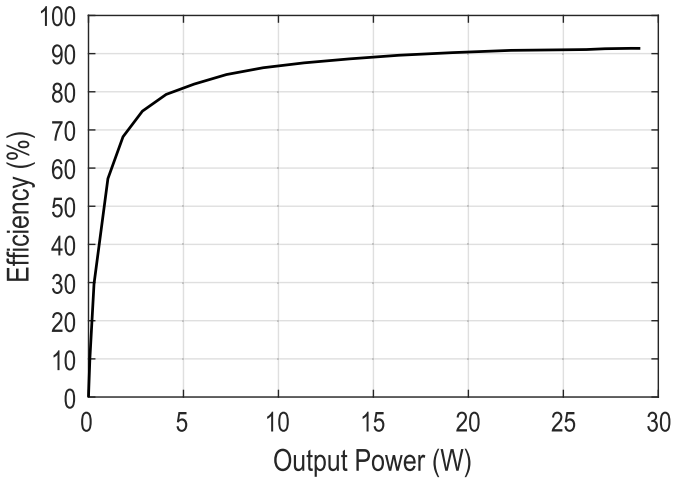

Fig. 16. Efficiency of the amplifier across output power.

During idle-channel operation, the amplifier draws 17 mA from P_{VDD}, which is primarily due to gate charging losses, and conduction losses due to the ripple current.

Audio measurements were done using an Audio Precision APX-555 in combination with an AES17 filter. Fig. 14 shows that the measured performance when a 4-Ω load is driven at 1 W. A noise-limited THD+N of −94.0 and −94.2 dB is achieved at input frequencies of 1 and 6 kHz, respectively. Across output power levels (Fig. 15), the amplifier achieves a peak THD+N of −102.2 and −100.5 dB, for input frequencies of 1 and 6 kHz, respectively, while maintaining a THD+N < −80 dB for output power levels as high as 20 W. When a 1-bit quantizer is used, the ΔΣ modulator overloads at significantly lower power levels (>8 W). In the 17-level mode, the amplifier has an A-weighted output noise of 31-μV_{RMS} and a dynamic range of 110.6 dB (A-wt.).

Fig. 16 shows the measured efficiency of the amplifier across output power levels. It attains a peak efficiency of 91% at its full power of 28 W and maintains an efficiency of >90% beyond 20 W.

EMI measurements were carried as per the CISPR-Class 5 standard [2] using a 12-V battery supply and a 4-Ω load

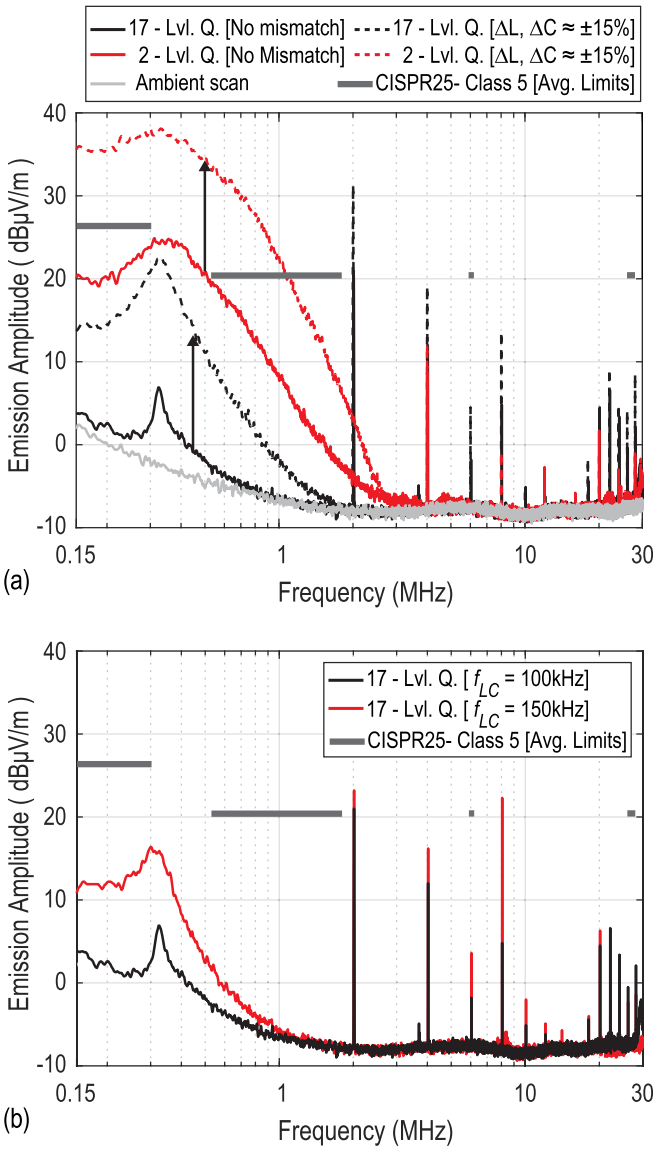

Fig. 17. Measured EMI of the class-D amplifier. (a) With and Without ±15% mismatch in L and C and a mean $f_{LC} = 100$ kHz. (b) Effect of further relaxing the *LC* cutoff frequency to $f_{LC} = 150$ kHz (without mismatch).

connected to the amplifier using 1.5-m long unshielded and untwisted cables. Fig. 17(a) shows the average radiated emission in the 150-kHz–30-MHz frequency band for different modes and scenarios. In the absence of mismatch in off-chip *LC* components, both the multilevel and 2-level modes are able to satisfy the EMI limits. However, there's hardly any margin for the 2-level mode. To assess the effect of component tolerances and mismatch, additional series/parallel combination of Ls and Cs was used to induce a ±15% mismatch over a nominal $f_{LC} = 100$ kHz. In this case, while the emission for the 2-level mode exceeds limits, the 17-level mode still maintains 6-dB margin. In the case of tighter component tolerances, the cutoff frequency may be relaxed further, as shown in Fig. 17(b), where an f_{LC} of 150 kHz without mismatch still maintains 10 dB of margin.

Fig. 18 shows the measured PSRR of the amplifier when its supply is perturbed by a 1 V_{RMS} sine wave, swept across

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORKS

Parameter	This work	[3]	[5]	[6]	[9]	[11]	[26]
Modulation Scheme	**Hybrid ΔΣ-PWM (Analog In.)**	PWM [MP] (Digital In.)	PWM [ML] (Analog In.)	PWM [ML] (Analog In.)	PWM (Digital In.)	ΔΣ (Analog In.)	PWM (Digital In.)
Supply	**14.4V**	25V	2.5-5V	24V	14.4V	12V	8-20V
Load	**4Ω**	4Ω	8Ω	4Ω	4Ω	6Ω	8Ω
THD+N (f_{IN} = 1kHz, P_O = 1W)	**0.002%**	0.004%	~0.0025%	~0.0095%	0.02%	~0.0032%	0.0029%
Peak THD+N (f_{IN} = 1kHz)	**0.00078%**	~0.0037%	0.0023%	0.003%	~0.015%	~0.0032%	0.0013%
Output Noise (A wt.)	**31uVrms**	34uVrms	-	-	42uVrms	50uVrms	20.5uVrms
$P_{O\text{-}MAX}$ (10% THD)	**28W**	80W	10W	70W	27W	10W	20 W
Efficiency	**91%**	>90%	91%	90%	86%	88%	90%
Switching Freq.	**2.0MHz**	0.4MHz	0.7MHz	0.165-0.6MHz	2.1MHz	< 0.7MHz	0.4MHz
Comp. Count [L, C] /Values	**2L, 2C** **2.2µH, 1.1uF**	4L, 2C -	- -	- -	2L, 2C 3.3µH, 1uF	2L, 2C 15µH, 1uF	2L, 2C -
LC filter cutoff	**100kHz**	~40kHz	-		88kHz	41kHz	-
Quiescent Current	**17mA**	12mA	3.5mA	2.9mA	~40mA		20.52mA
PSRR (20-20kHz)	**70-62dB**	~100-60dB (88dB@100Hz)	~88dB (@217Hz)	-	~75-57dB	~68-39dB	80-50dB
Area/ Channel	**4.8mm²**	-	6.4mm²	6.7mm²	-	10.1mm²	-
Process	**180nm BCD**	140nm BCD SOI	180nm BCD	180nm BCD	-	600nm BCD	180nm BCD

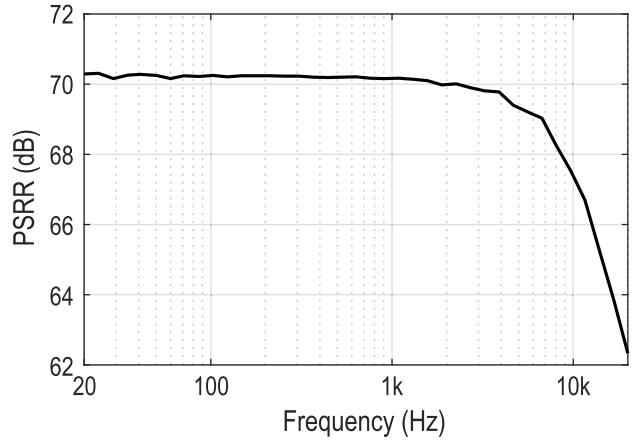

Fig. 18. PSRR of the amplifier across supply perturbation frequency.

frequency. At low frequencies, the PSRR is 70 dB and is mainly limited by the matching of the resistors. Toward the edge of the audio band, a PSRR > 60 dB is maintained.

A comparison of the performance of this amplifier with other state-of-the-art designs is shown in Table I.

VI. CONCLUSION

A class-D amplifier incorporating a hybrid ΔΣM-PWM modulation scheme is presented. Multilevel quantization using ΔΣM followed by time-quantized PWM generation drastically reduces the out-of-band EM emission compared with a 1-bit ΔΣM class-D amplifier, allowing the use of a relaxed *LC* cutoff frequency with relaxed component tolerances. A high loop gain, enabled due to the high sample rate, together with a robust output stage that delivers well-defined quantized pulses, ensures high linearity of the amplifier across a wide output power range. Overall, the class-D amplifier achieves the state-of-the-art performance with a peak THD+N of −102.2 dB and a peak efficiency greater than 90%. In addition to [12], it is shown that the *LC* cutoff frequency can be pushed as high as 150 kHz to satisfy the CISPR-25 average EMI limit [150 kHz–30 MHz], while still maintaining some margin.

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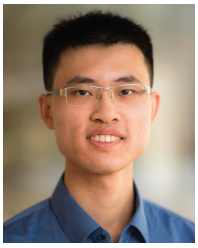

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