A CMOS Resistor-Based Temperature Sensor with a 10fJ·K2 Resolution FoM and 0.4°C (30) Inaccuracy from -55°C to 125°C after a 1-point Trim

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3.6 A CMOS Resistor-Based Temperature Sensor with a 10fJ·K² Resolution FoM and 0.4°C (3σ) Inaccuracy From −55°C to 125°C After a 1-point Trim

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Energy efficiency and accuracy are important specifications of CMOS temperature sensors. BJT-based sensors achieve state-of-the-art accuracy [1], while Wheatstone-bridge (WhB) sensors achieve lower accuracy but state-of-the-art energy efficiency [2,3]. This paper presents a WhB sensor that is read out by an energy-efficient continuous-time delta-sigma modulator (CTDSM). Compared to [2,3], the modulator achieves better energy efficiency with the help of a return-to-CM (RCM) DAC and an OTA with a tail-resistor linearization scheme. Moreover, better accuracy is achieved by embedding the DAC in the bridge and by using more sensitive silicided-diffusion resistors instead of silicided-poly resistors. Compared to the state-of-the-art [3], the proposed sensor achieves a 2× improvement in resolution FoM (10fJ·K²), and a 2× improvement in inaccuracy (0.4°C (3σ) from -55°C to 125°C after a 1-point trim).

As shown in Fig. 3.6.1, the WhB is made from resistors R_p and R_n with positive and negative temperature coefficients (TCs). As in [2,3], it is read out by a CTDSM, which balances the bridge via a multi-level resistor DAC, thus forcing the average error current (I_{err}) to zero. A multi-level DAC reduces the swing of I_{err}, which reduces the power dissipation of the modulator's 1st integrator, and the size and area of its integration cap C_{int} [2,3]. To minimize spread, the DAC resistors are of the same type as the R_n resistors and also have a negative TC. To balance the bridge, however, some of the DAC resistors (R_{DAC1}) will be connected in parallel with the R_p resistors, reducing the sensitivity of the bridge, and hence, its energy efficiency.

In this design, the DAC resistors are switched to the common-mode voltage V_{CM} of the bridge when they are not required for bridge-balancing (Fig. 3.6.1, bottom). Compared to [3], this RCM approach preserves bridge sensitivity, and improves its energy efficiency by ~30%. Furthermore, since their values are now quite similar, the R_n and R_{DAC} resistors can be merged into a single array with 6 unit elements (all 370kΩ), leading to better matching and greater accuracy. As in [2,3], R_p (105kΩ) is a silicided resistor, while R_{DAC} is made from non-silicided n-poly.

As shown in Fig. 3.6.2, the CTDSM consists of a 2nd-order modulator with a FIR-DAC [3]. V_{CM} is realized by connecting unused DAC resistor pairs together. Compared to a return-to-open approach, this equalizes the rising/falling edges of the DAC currents, mitigating ISI and thus preventing quantization noise (Q-noise) folding. Both the modulator's feedforward stabilization and the FIR-DAC's delay-compensation are realized by a switched-capacitor (SC) 2nd-stage [3]. To make optimum use of the modulator's dynamic range, R_p is trimmed (3b) to compensate for process spread [3], and only 4 of the 6 unit elements of R_{DAC} are switched.

To maximize its energy efficiency, the 1st integrator should employ a single-stage OTA, so that its thermal noise is fully defined by its bias current. However, this OTA must also be linear enough to handle the output of the FIR-DAC without incurring Q-noise folding, as this will degrade the CTDSM's noise floor [4]. Simulations show that a conventional current-reuse OTA would then require significantly more (4×) bias current than that indicated by thermal-noise considerations alone.

Much better linearity can be achieved by replacing the OTA's tail current sources with tail resistors [5]. Assuming that the MOSFET pairs are in weak inversion, the optimum tail resistance R_{tail} is equal to $nV_T/(2I_{tail})$. This temperature-dependent resistance can be emulated by combining a fixed resistor with a PTAT biasing circuit, resulting in a 22dB improvement in HD3 ($I_{out} = 0.4 \cdot I_{tail}$) over PVT. The actual OTA employs an energy-efficient current-reuse topology (Fig. 3.6.3). As in [6], it is biased via R_b and capacitively-coupled to the WhB via C_b. Chopping enables the amplification of the bridge's DC output signal, and also suppresses the OTA's offset, even-order distortion and 1/*f* noise. To minimize the noise contribution of the biasing network, its time constant ($C_b \cdot R_b$) should be kept well below the chopping frequency (f_{chop} = 125kHz). To do this, a delay-line-based pulse generator is used to duty-cycle R_b at $2 \cdot f_{chop}$, thus boosting its effective resistance by >500×. As a result, the area of C_b (2pF) and R_b (700kΩ) is quite small (<4×0.002mm²). From simulations, the OTA has 80dB gain, and consumes 9μA at room temperature (RT), which is 1.8× less than the opamp in [3]. Compared to the WhB (17μA at RT), it contributes only 25% of the input-referred noise. The 2nd stage is also built around a standard current-reuse OTA. It also has 80dB gain, but consumes only 1μA.

Four sensors were fabricated on the same die in a standard 0.18μm CMOS process (Fig. 3.6.7), two with silicided-poly/n-poly WhBs, and two with silicided-diffusion/n-poly WhBs, the latter having a somewhat (~10%) higher TC. Ambient temperature drift is rejected by differential measurements on each pair of sensors. Each sensor consumes 30.5μA (27.5μA analog, 3μA digital) from a 1.8V supply, and occupies 0.11mm². To save area, C_{int1} (27pF, MIM) is located directly above the WhB (0.06mm²). The four sensors share two clock-generation circuits (0.003mm² each, input clock of 2MHz, BS at 500kHz). For flexibility, the sinc² decimation filters are implemented off-chip.

After ceramic DIL packaging and mounting in good thermal contact with a large metal block, 20 samples from one wafer (40 sensors for each type) were characterized in a temperature-controlled oven. With the same R_p trimming code, the residual spread from sample to sample is less than ±3% of full scale at RT (Fig. 3.6.4, left). After an individual 1st-order fit and a fixed 5th-order polynomial systematic nonlinearity removal, the silicided-poly/n-poly WhB achieves an inaccuracy of 0.15°C (3σ) over the military temperature range (Fig. 3.6.4, top middle). With a single-point trim that exploits the correlation between the fitting coefficients [2], the inaccuracy is 0.6°C (Fig. 3.6.4, top right). For the silicided-diffusion/n-poly bridge, however, the inaccuracy is even smaller: 0.1°C after a 1st-order fit and 0.4°C after a single-point trim. The measured supply sensitivities of the two types of bridges are roughly the same (~0.04°C/V from 1.4 to 2V at RT), and are mainly determined by the voltage-dependent R_{on} of the DAC switches.

FFTs of the sensor's bitstream output are shown in Fig. 3.6.5 (top). Shorting the tail resistors in both the OTA and its biasing circuit leaves the OTA's biasing current unchanged, but increases its non-linearity. The resulting Q-noise folding causes an ~3dB increase in the modulator's noise floor. The sensor's resolution is derived by computing the standard deviation of the difference in the output of two identical sensors from the same die. Over a 1s interval, the silicided-poly/n-poly bridge achieves 160μK_{rms} resolution in an 8ms conversion time (Fig. 3.6.6, bottom), while the silicided-diffusion/n-poly bridge achieves 150μK_{rms}, due to its higher sensitivity.

Figure 3.6.6 summarises the performance of the proposed FIR-DAC WhB sensor and compares it with state-of-the-art BJT [1], resistor [2,3] and MEMS [7]based sensors. It achieves the best FoM, improving on the state-of-the-art [3] by 2×. Compared to previous resistor-based sensors, it is 1.5× more accurate after a 1st-order fit, or 2× after a correlation-based 1-point trim. This level of performance makes this sensor quite competitive in embedded applications where both high resolution and good accuracy are required.

References:

[1] B. Yousefzadeh et al., "A BJT-Based Temperature-to-Digital Converter with ±60 mK (3σ) Inaccuracy from –55 °C to +125 °C in 0.16-μm CMOS," *IEEE JSSC*, vol.52, no. 4, pp. 1044-1052, Apr. 2017.

[2] S. Pan, K. A. A. Makinwa, "A 0.25 mm²-Resistor-Based Temperature Sensor With an Inaccuracy of 0.12°C (3σ) From -55°C to 125°C," *IEEE JSSC*, vol. 53, no. 12, pp. 3347-3355, Dec. 2018.

[3] S. Pan, K. A. A. Makinwa, "A Wheatstone Bridge Temperature Sensor with a Resolution FoM of 20fJ·K²," *ISSCC*, pp. 186-187, Feb. 2019.

[4] P. Sankar, S. Pavan, "Analysis of Integrator Nonlinearity in a Class of Continuous-Time Delta-Sigma Modulators," *IEEE Trans. Circuits Syst. II*, vol. 54, no. 12, pp. 1125-1129, Dec. 2007.

[5] R. Sehgal et al., "A 13mW 64dB SNDR 280MS/s Pipelined ADC Using Linearized Integrating Amplifiers," *IEEE JSSC*, vol. 53, no. 7, pp. 1878-1888, July 2018.

[6] B. Gönen et al., "A Low Power Continuous-Time Zoom ADC for Audio Applications," *IEEE Symp. VLSI Circuits*, pp. C224-225, June 2019.

[7] M. H. Roshan et al., "A MEMS-Assisted Temperature Sensor With 20-μK Resolution, Conversion Rate of 200 S/s, and FOM of 0.04 pJK²," *IEEE JSSC*, vol. 52, no. 1, pp. 185-197, Jan. 2017.

 978-1-7281-3205-1/20/$31.00

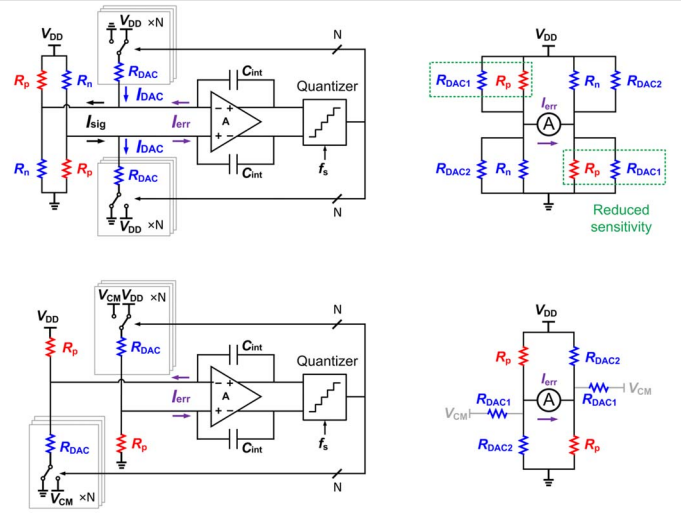

Figure 3.6.1: Conventional multi-bit CTΔΣ readout of a Wheatstone bridge sensor (top left); proposed readout scheme with an embedded RCM DAC (bottom).

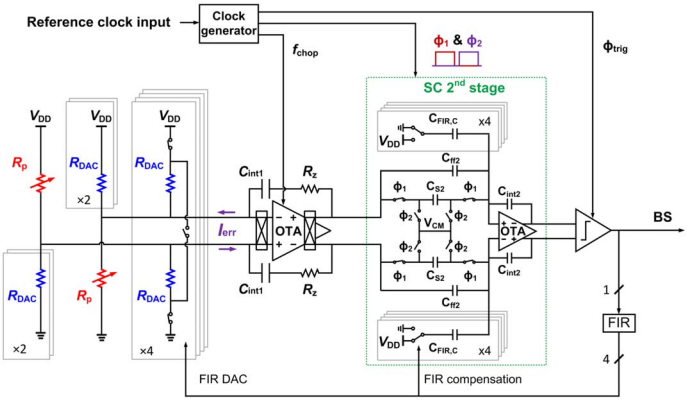

Figure 3.6.2: Simplified system block diagram.

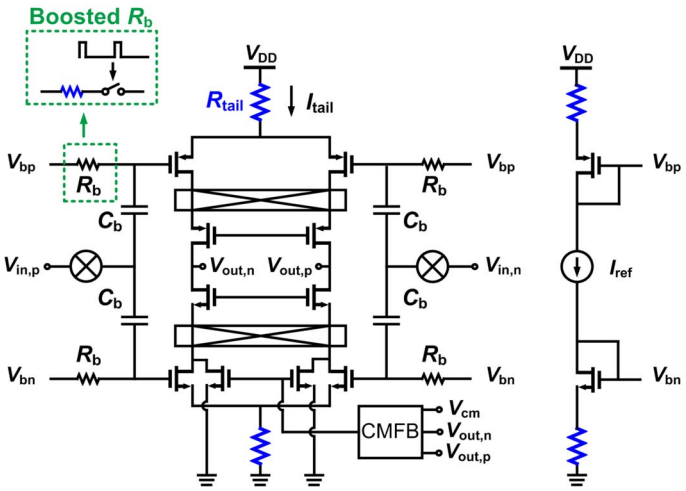

Figure 3.6.3: Simplified diagram of the chopped capacitively-coupled 1st-stage OTA with robust biasing and tail resistor linearization.

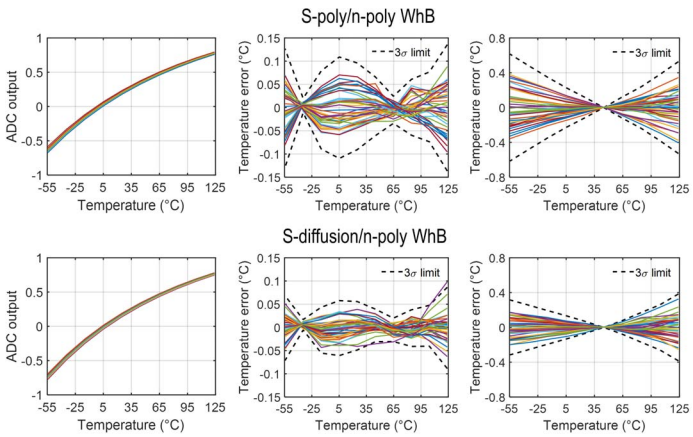

Figure 3.6.4: Sensor characteristic (left); temperature inaccuracy after a 1st-order-fit and a 5th-order systematic nonlinearity removal (middle) or a correlation-based 1-pt trim (right).

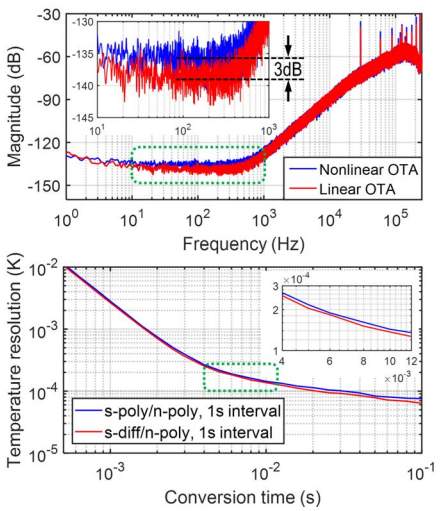

Figure 3.6.5: Bitstream spectra (20s interval, Hanning window, 10× averaging) with tail resistors enabled/disabled (top); resolution vs. conversion time (bottom).

	[6]	[1]	[2]	[3]	This work	
Sensor type	Dual-MEMS Resonator	BJT	Resistor WhB	Resistor WhB	**Resistor WhB S-poly/n-poly**	**Resistor WhB S-diff/n-poly**
CMOS Technology	0.18µm	0.16µm	0.18µm	0.18µm	**0.18µm**	
Area [mm²]	0.54	0.16	0.25	0.12	**0.11**	
Temperature range	-40°C to 85°C	-70°C to 125°C	-55°C to 125°C	-55°C to 125°C	**-55°C to 125°C**	
3σ inaccuracy [°C] (Trimming points)	--	0.06 (1)	0.12 (2 *) 1.0 (1)	0.14 (2 *) 0.8 (1)	**0.15 (2 *) 0.6 (1)**	**0.1 (2 *) 0.4 (1)**
Supply voltage [V]	1.6	1.6	1.8	1.8	**1.8**	
Supply sensitivity [°C/V]	--	0.01	0.02	0.03	**0.04**	
Power consumption [µW]	13000	7	94	79	**55**	
Conversion time [ms]	5	5	5	10	**8**	
Resolution [mK]	0.02	15	0.29	0.16	**0.16**	**0.15**
Resolution FoM [fJ·K²] **	40	7300	40	20	**11**	**10**

* 1st order fit. ** FoM = Energy / Conversion x (Resolution)².

Figure 3.6.6: Performance summary and comparison with previous work.

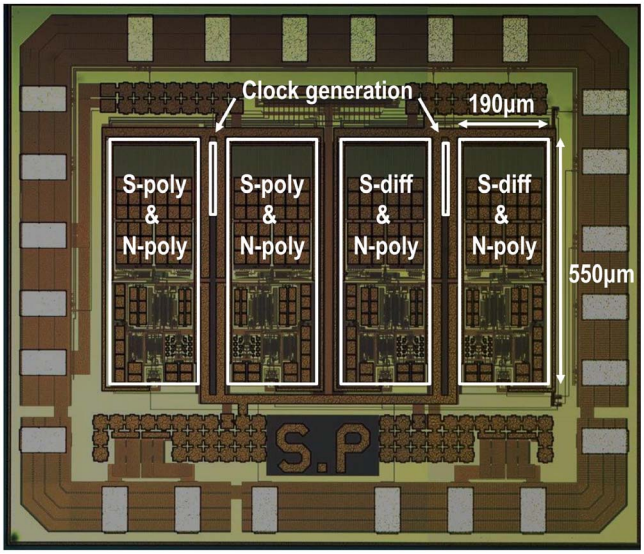

Figure 3.6.7: Die micrograph of the fabricated chip.

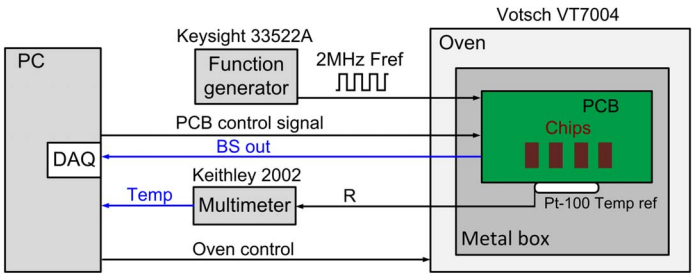

Figure 3.6.S1: Measurement setup.

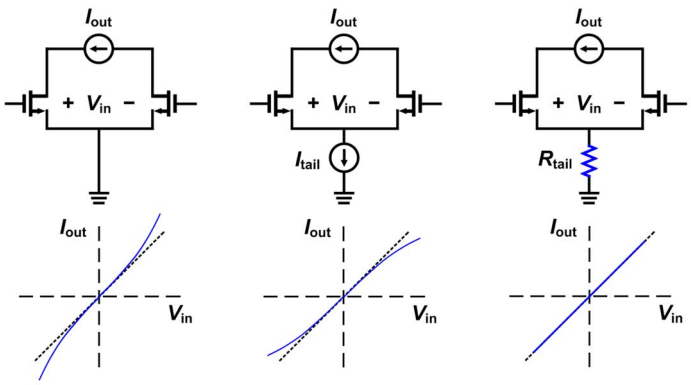

Figure 3.6.S2: OTA linearity with zero tail impedance (left), infinite tail impedance (middle) and the optimum tail resistance (right).

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