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A 3.2mW SAR-assisted CTΔΣ ADC with 77.5dB SNDR and 40MHz BW in 28nm CMOS

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Abstract

This paper presents a SAR-assisted Continuous-time Delta-Sigma (CTΔΣ) ADC, which combines the energy efficiency of SAR ADCs with the relaxed driving requirements of CTΔΣ ADCs, as well as similar anti-alias filtering. When clocked at 2.4GHz, the ADC achieves 77.5dB SNDR in 40MHz BW. It consumes 3.2mW, resulting in a state-of-the-art Walden FoM of 6.5fJ/cs and a Schreier FOM of 178.5dB.

Introduction

Multi-standard receivers for BLE and WIFI require energy efficient (<10fJ/cs) ADCs with > 40MHz BW, and > 70dB DR to maintain linearity in the presence of strong blockers. Although a SAR-assisted pipeline ADC can convert such BWs with excellent energy efficiency [1], a power-hungry anti-alias filter (AAF) is then required to drive its 4pF sampling capacitors with sufficient linearity [1]. Moreover, to relax the AAF requirements, oversampling is often used at the expense of higher power dissipation. In comparison, CTΔΣ ADCs have relaxed driving requirements and inherent anti-alias filtering, but are less energy efficient [2-3]. This paper presents an ADC that combines the best of both worlds. It achieves 77.5dB SNDR in a 40MHz BW, >40dB anti-alias filtering, consumes 3.2mW, and has an input capacitance of only 21fF.

SAR-Assisted CTΔΣ ADC Architecture

Fig. 1 shows the block diagram of the SAR-assisted CTΔΣ ADC. The first stage is built around a coarse 5b-SAR ADC. A 5b-DAC converts its digital output (Y0) to the analog domain, where it is subtracted from a delayed version of the input signal to generate a residue (ε). An all-pass filter (APF) implements the delay, which is designed to match the $1.5*T_{CLK}$ latency of the 5b SAR-DAC path [4]. The residue (SAR ADC quantization noise, non-linearity and sampling images) is then filtered (LPF), amplified (inter-stage gain G), and digitized by a CTΔΣ ADC. The final output (Yout) is obtained by combining Y1 and Y0 in a digital compensation filter Hd(z). This models the combined transfer function H(s) of LPF, G and the signal transfer function (STF) of the ΔΣ ADC. After summing Y1 and Y0', aliasing components and SAR ADC related errors are cancelled.

Any mismatch between H(s) and Hd(z) will allow some of the residue to "leak" into Yout. To minimize this, Hd(z) can be trimmed via a digitally-programmable delay (ΔT) and gain (G). This suppresses the residue by > 42dB, pushing it below the overall ADC's thermal-noise floor. To minimize first stage latency (path1), the SAR ADC employs a non-interleaved architecture and processes 1b per conv.-cycle to avoid the extra delay incurred by look-up tables or decoders. By clocking the SAR ADC at half the sampling rate (fs) of the ΔΣ ADC, overall ADC power can then be reduced by ~25%. Furthermore, the SAR ADC's rail-to-rail capability maximizes the overall ADC's input dynamic range [5], while the use of half-LSB dither mitigates its tonal behavior.

The inter-stage gain (G) reduces the ΔΣ ADC's input-referred noise contribution. To minimize overall ADC power, G should be greater than ~7.5V/V. However, if G is too high, the ΔΣ modulator will become unstable in the presence of full-scale (FS) out-of-band blockers. The frequency response from the input of the ADC to the input of G is shown in Fig. 2, assuming an ideal SAR ADC. Depending on their relative phases, the outputs of the APF (path0) and the SAR-DAC (path1) will either cancel or complement each other, resulting in either a frequency response notch or a 6dB peak. The latter is attenuated by the LPF (f_{-3dB} ~ 65MHz), making the system robust to out-of-band blockers. To match the SAR ADC delay, the APF adds two 338MHz RHP zeros and one 338MHz pole. The APF/LPF combination ensures that the ΔΣM remains stable for G <11V/V, even for a worst-case FS 700MHz blocker. The aliased residue components caused by higher frequency (> 800MHz) blockers, can then be suppressed by incorporating a simple 1st order LPF (70MHz) into a preceding stage.

Fig. 3 shows a detailed block diagram of the ADC. A single amplifier realizes the APF, LPF and the inter-stage gain. Its input RC network defines the APF, while its RC feedback network defines the LPF and the inter-stage gain. An inverter-based amplifier is used for low power and low noise (Fig. 4). Since it only processes the SAR ADCs errors, its linearity requirements are relaxed. The 5b-DAC employs resistors, which sink/source current from the supply (0.9V) and ground. It consists of 31 slices (Fig. 4) directly connected to the output of the SAR through 5 D-FFs. The data (Y0) is available at the start of the SAR's sampling phase (SP). During SP, the switches (S1-S4) are open, ensuring that the DAC settles by the end of SP without introducing further delay in path1. The SAR ADC, DAC and ΔΣM are driven by 100ps pulses derived by a pulse generator from an external 2.4GHz clock. As a result, the ADC's operation is robust to PVT and duty-cycle variation.

The ΔΣM (Fig. 3) consists of a 4th-order feed-forward (FF) loop filter, a 1-bit quantizer and a R-DAC (Fig. 4). To reduce its power dissipation, the loop filter consists of two single-opamp biquad stages, whose coefficients have been optimized for the low gain (<25dB) inverter-based amplifiers (Fig. 4). The FF and ELD coefficients are implemented by splitting the input pair of a StrongArm comparator [5]. The comparator is triggered at the end of the SAR sampling phase (SP). When its output becomes valid, a decision detector starts the reset phase and updates the ELD signal through a D-FF. The data for the ΔΣM's DAC, like that of the 5-bit DAC, is then also available during SP.

Measurement Results

The ADC occupies 0.025mm^2 in 28nm CMOS (Fig. 6) and dissipates 3.2mW from a 0.9V supply (708μW SAR, 777μW DAC, 585μW Amplifier, 697μW ΔΣM, 414μW pulse gen.). To compensate for PVT variation, the supply voltage of the amplifiers and the capacitors used in the ΔΣM/APF/LPF (5-bit arrays) are calibrated at start-up. As in [7], Hd(z) is foreground-calibrated by adjusting its delay and gain in ~20ps ($2.4\%*T_{CLK}$) and ~0.4% steps, respectively. Fig. 5 (top) shows the measured spectra with and without a -0.13dBFS 18.5MHz input tone. Fig. 5 (bottom) shows the measured spectra with two -6.2dBFS 17.8 MHz and 19.6MHz tones. The ADC then exhibits a peak SNDR of 77.5 dB at -0.13dBFS and an IM_3 of -76.7dBc. Fig. 6 shows the measured SNDR versus input amplitude, which corresponds

to a DR of 78.2dB. Table I summarizes the ADC's performance and compares them to the state of the art. Although its energy efficiency is similar to that of a state-of-the-art SAR ADC [1], its CT implementation ensures easier drivability and superior anti-alias filtering, similar to that of CTΔΣ ADCs.

References

[1] Y. Lim et al., VLSI 2017 [2] S. Loeda et al., JSSC 2016 [3] Y. S. Shu et al., ISSCC 2013 [4] H. Shibata et al., JSSC 2017 [5] P. Cenci et al., ESSCIRC, 2017 [6] Y. Dong et al., JSSC 2014 [7] R. Rutten et al, ESSCIRC, 2006.

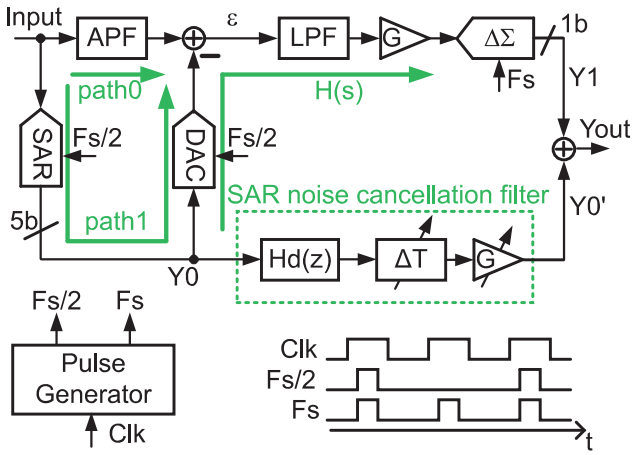

Fig. 1: Block diagram of the SAR-Assisted CTΔΣ ADC with timing diagram.

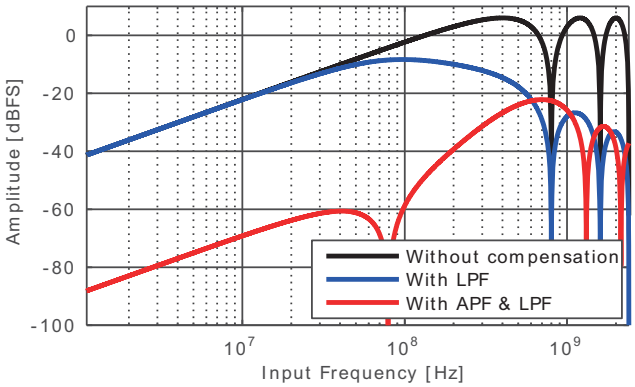

Fig. 2: Frequency response from the input of the ADC to the input of the gain stage with full scale (0.9V) input signal and ideal SAR ADC @ 1.2GS/s.

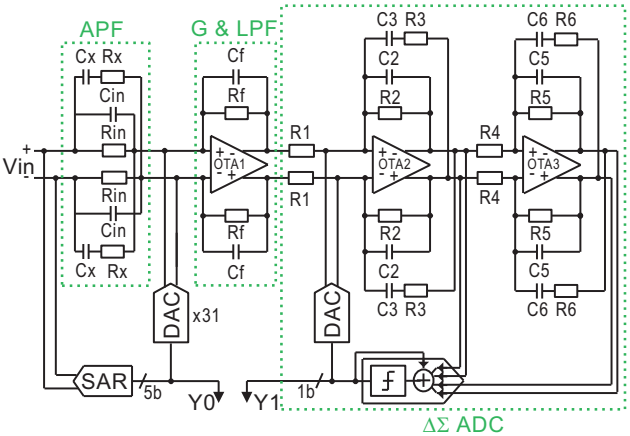

Fig. 3: Schematic of the SAR-Assisted CTΔΣ ADC with APF delay compensation, G&LPF stage, and 4th order ΔΣM with feed-forward and ELD coefficients integrated in the quantizer.

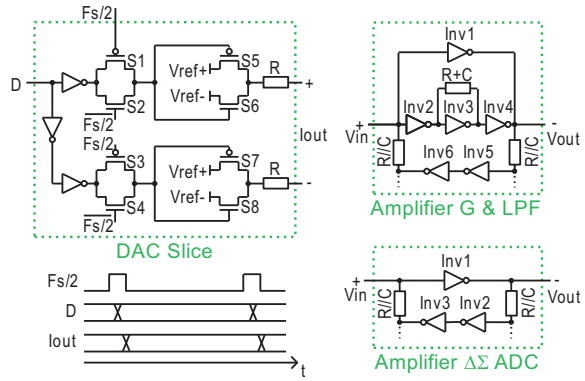

Fig. 4: Schematic of the R-DAC with timing diagram(left). Half-circuit schematic of the amplifiers (G&LPF on top-right, ΔΣ on bottom-right).

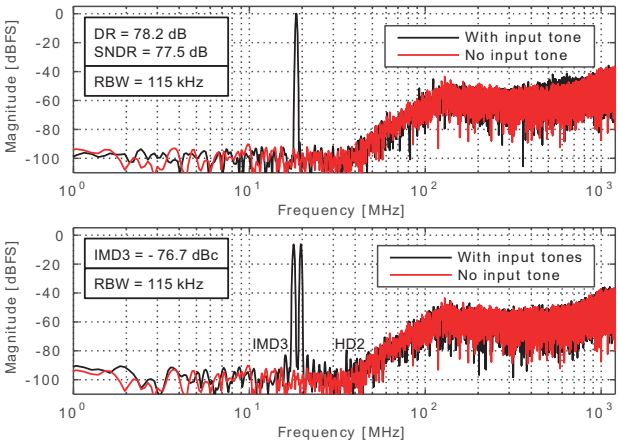

Fig. 5: Measured output spectra with a 0.85 V @ 18.5 MHz input tone (top) and with two 0.434 V @ 17.8 & 19.5 MHz input tones (bottom).

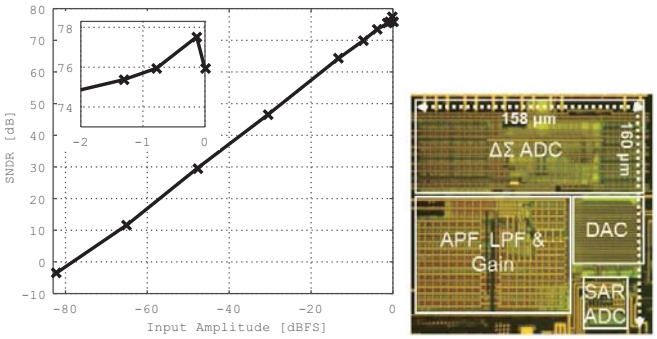

Fig. 6: Measured SNDR vs. Input amplitude (Left). Micrograph of the SAR-Assisted CTΔΣ ADC in 28 nm CMOS (Right).

Table I. Comparison with state-of-the-art ADCs with similar BW and resolution.

	This work	[1]	[2]	[3]	[5]	[6]
ADC Architecture	**SAR-Assisted CTΔΣ**	SAR-Assisted	CTΔΣ	CTΔΣ	0-3 MASH	CT pipeline
Technology [nm]	**28**	40	40	28	28	28
Active Area [mm2]	**0.025**	0.068	0.0194	0.08	0.9	5.1
Supply Voltage [V]	**0.9**	1.1	-	-	0.9/1.8/-1	-
Sampling Rate [GHz]	**2.4**	0.1	2.4	0.64	3.2	9
Power [mW]	**3.2**	2.3	5.25	3.9	235	2330
OSR	**30**	1	30	17.7	30	4
Bandwidth [MHz]	**40**	50	40	18	53.3	1125
Sampling Cap. [fF]	**21**	4000	-	-	-	-
Anti-aliasing filtering [dB]	**42**	X	-	-	-	-
DR [dB]	**78.2**	-	67.8	78.1	88	73
SNR [dB]	**-**	73.3	-	-	83.1	64
SNDR [dB]	**77.5**	73.2	66.9	73.6	71.4	63
ENOB [bits]	**12.58**	11.9	10.8	11.9	11.6	10.17
FOMS [dB]	**178.5**	176.6	162.7	170.2	155.5	153.3