A 5800-μ m ²Resistor-Based Temperature Sensor with a One-Point Trimmed Inaccuracy of ±1.2 °c (3σ) From-50 °c to 105 °c in 65-nm CMOS

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A 5800-μm^2 Resistor-Based Temperature Sensor With a One-Point Trimmed Inaccuracy of $\pm$1.2 °C (3σ) From $-$50 °C to 105 °C in 65-nm CMOS

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***Abstract*—This letter describes a compact resistor-based temperature sensor intended for the thermal monitoring of microprocessors and DRAMs. It consists of an *RC* poly phase filter (PPF) that is read out by a frequency-locked loop (FLL) based on a dual zero-crossing (ZC) detection scheme. The sensor, fabricated in 65-nm CMOS, occupies 5800 μm^2 and achieves moderate accuracy [$\pm$1.2 °C (3σ)] over a wide temperature range ($-$50 °C to 105 °C) after a one-point trim. This is 2× better than the previous compact resistor-based sensors. Operating from 0.85 to 1.3-V supplies, it consumes 32.5-μA and achieves 2.8-mK resolution in a 1-ms conversion time, which corresponds to a resolution FoM of 0.26 pJ·K^2.**

***Index Terms*—CMOS temperature sensor, dual zero-crossing (ZC) detection, frequency-locked loop (FLL), one-point trim, *RC* poly phase filter (PPF), resistor-based temperature sensor.**

I. Introduction

Compact temperature sensors are required for the thermal monitoring of microprocessors and DRAMs [1]–[4]. In microprocessors, they provide information about on-chip thermal gradients and hot spots, which helps to maintain performance and reliability [2]. In DRAMs, they control the self-refresh period, which in turn, determines standby power [3]. To avoid wasting expensive die area, sensors intended for thermal monitoring in nanometer CMOS should be compact (<0.01 mm^2). They should also be fast enough (~1-ms conversion time) to track on-chip temperature gradients. Finally, to reduce calibration costs, they should only require a one-point trim to achieve moderate accuracy.

For thermal monitoring, resistor-based temperature sensors are attractive, because they can operate at low-supply voltages and are highly energy efficient [4]–[8]. Of the available resistors in CMOS processes, silicided poly resistors are well suited for temperature sensing due to their relatively high temperature coefficient (TC ~ 0.3 %/K), low-voltage dependency, and low 1/*f* noise [4]–[6]. In the previous work, such resistors have been incorporated in Wheatstone bridges and read out by the continuous-time ADCs, resulting in high energy-efficiency but large area (0.25 mm^2) [6]. More compact sensors have been realized by incorporating resistors into Wien-Bridge filters (0.0068 mm^2) [7], *RC* networks (0.01 mm^2) [8], or poly phase filters (PPFs) (0.007 mm^2) [4]. However, these typically require two-point trimming to achieve inaccuracies below $\pm$1 °C.

This letter presents a compact resistor-based temperature sensor in 65-nm CMOS. It is based on a PPF whose temperature-dependent phase shift is digitized by a zero-crossing (ZC) detector and then read out by a frequency-locked loop (FLL). The FLL employs a *dual ZC detection scheme*, which improves accuracy by reducing the impact of the ZC detector offset. As a result, the sensor requires only one-point trimming to achieve a 3σ inaccuracy of $\pm$1.2 °C from $-$50 °C to 105 °C.

This letter is organized as follows. The sensor's architecture is described in Section II, together with an analysis of its main error sources and the resulting circuit implementation. Section III presents measurement results. Finally, the conclusion is presented in Section IV.

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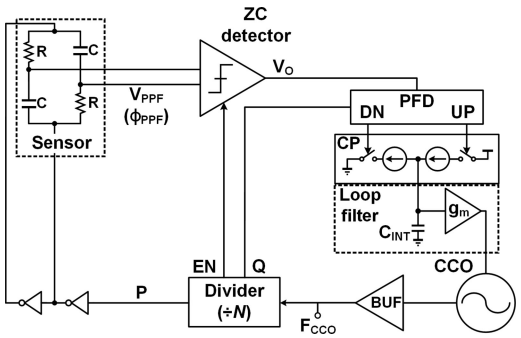

Fig. 1. Architecture of the proposed PPF-based temperature sensor.

II. PPF-Based Temperature Sensor

A. Sensor Architecture

A block diagram of the proposed sensor is shown in Fig. 1. As in [4], its temperature-sensing element is a PPF that incorporates a silicided poly resistor. The PPF is driven by an in-phase signal (P), generated by dividing the output frequency F_{CCO} of a current-controlled oscillator (CCO) by N, while a quadrature-phase signal (Q) drives a digital phase/frequency detector (PFD). A ZC detector then detects the ZCs in the PPF's output V_{PPF}, which represent its temperature-dependent phase shift ϕ_{PPF}. Depending on the phase difference between the detector output V_O and Q, the PFD generates up or down pulses which are converted by a charge pump (CP) into current pulses that drive a loop filter (integration capacitor C_{INT}). The filter's output then regulates the CCO frequency via the g_m stage. At steady state, the resulting FLL maintains ϕ_{PPF} at $-90°$, and so F_{CCO} is locked to N times the center frequency ($f_{PPF} = 1/2\pi RC$) of the PPF.

B. Spread Analysis

Fig. 2 highlights the main error sources of the proposed sensor: resistor spread, ZC detector offset V_{OS}, and CP mismatch. From simulations, an inaccuracy of $\pm$0.2 °C can be achieved with a 1000-μm^2 70-kΩ resistor. The combined error of the other blocks should then be less than $\pm$0.8 °C to obtain a worst-case total inaccuracy of $\pm$1 °C.

The offset V_{OS} causes phase errors in the detected ZCs of V_{PPF}, which translate into temperature-sensing errors. As shown

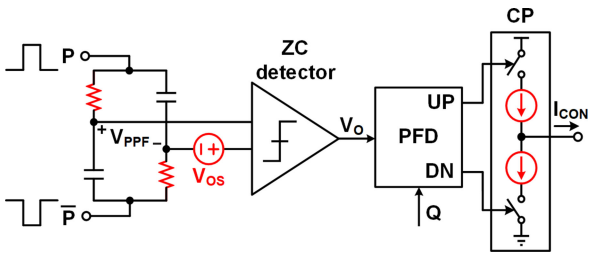

Fig. 2. Main spread sources in the PPF-based temperature sensor.

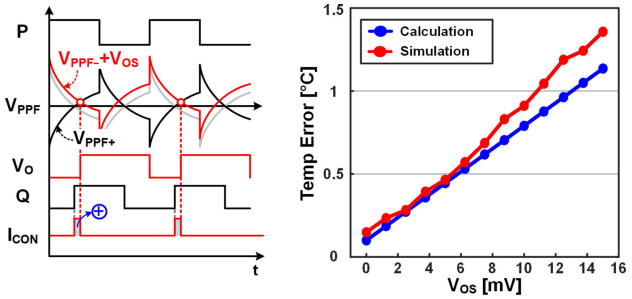

Fig. 3. Single ZC detection scheme. (a) Timing diagram. (b) Calculated and simulated temperature error (one-point trimmed) versus V_{OS}.

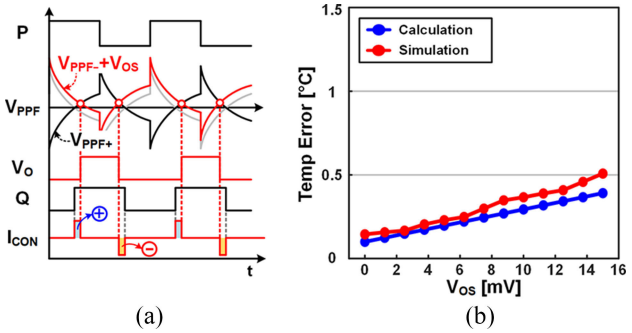

Fig. 4. Dual ZC detection scheme. (a) Timing diagram. (b) Calculated and simulated temperature error (one-point trimmed) versus V_{OS}.

in Fig. 3(a), V_{OS} either delays or advances the detected ZCs depending on its polarity. Single ZC detection, as in [4], will then cause a constant phase error, since the detected ZC will occur when $V_{PPF} = V_{OS}$. If $V_{OS}/V_{DD} = k$, the error in the rising edge Δt_{rise} can be expressed as

$$\Delta t_{rise} = RC \cdot \ln(1+k). \quad (1)$$

By using the TC of the silicided poly resistor, the resulting temperature error can be derived from this timing error. Fig. 3(b) shows the calculated and simulated temperature error versus V_{OS} for an ideal FLL with single ZC detection after a one-point trim. The temperature error is still quite sensitive to V_{OS} (~ 0.1 °C/mV). However, this can be reduced by noting that while V_{OS} delays the ZC of the rising edge of V_{PPF}, it simultaneously advances the ZC point of the falling edge, and vice-versa. This leads to the *dual* ZC detection scheme shown in Fig. 4(a). Since the error in the falling edge $\Delta t_{fall} = RC \cdot \ln(1-k)$, the average error Δt_{total} in this case can be expressed as

$$\Delta t_{total} = \Delta t_{rise} + \Delta t_{fall} = RC \cdot \ln(1-k^2), \quad (2)$$

which is much smaller than Δt_{rise}, since $k < 1$. There is some residual error, since V_{OS} introduces slightly different errors in the rising and falling edges. Fig. 4(b) shows the calculated and simulated temperature errors versus V_{OS} for an ideal FLL with a dual ZC detection

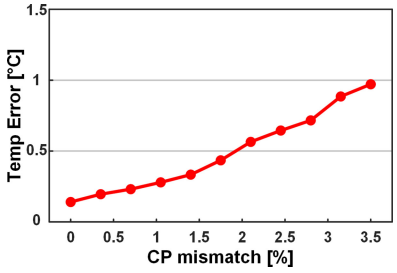

Fig. 5. Simulated temperature error (one-point trimmed) versus CP mismatch.

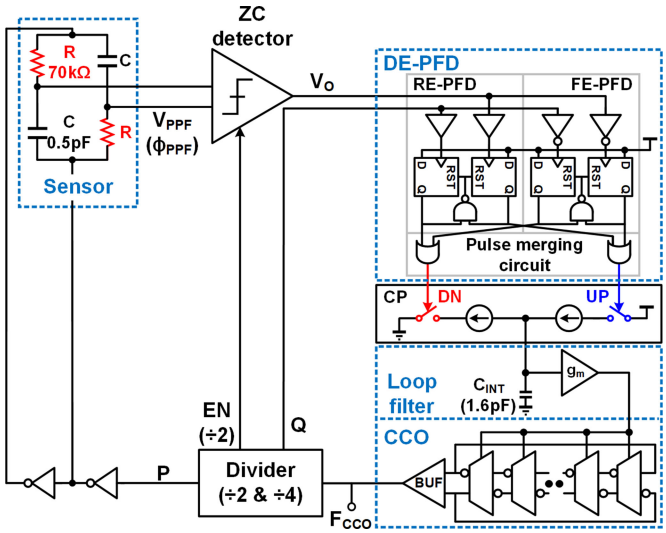

Fig. 6. Proposed PPF-based temperature sensor with dual ZC detection scheme.

scheme after a one-point trimmed. Compared to Fig. 3(b), the resulting temperature error is much smaller: less than ±0.5 °C for V_{OS} = 15 mV.

However, CP mismatch will still cause an error current to flow into C_{INT}, causing the FLL to output the wrong frequency. This leads to a constant phase error between V_O and Q, and consequently to a temperature error. Fig. 5 shows simulation results with CP mismatch only. They show that it needs to be <1.6% to ensure <±0.3 °C error.

C. Circuit Implementation

Fig. 6 shows the block diagram of the proposed PPF-based temperature sensor with dual ZC detection scheme. The PPF consists of two silicided p-poly resistors (R = 70 kΩ) and two MIM capacitors (C = 0.5 pF). When the PPF sensor is driven by F_{CCO}/4, the locked F_{CCO} varies from 15.3 MHz to 23.8 MHz as the temperature changes from −50 °C to 105 °C. From post-layout simulations, the parasitic capacitance at each PPF output node is <10 fF. This translates into a small (and systematic) temperature-sensing error of about 0.5 mK.

The dual ZC detection scheme employs a dual-edge triggered-PFD (DE-PFD), comprising a rising-edge triggered-PFD (RE-PFD), a falling-edge triggered-PFD (FE-PFD), and a pulse merging circuit. Both the RE-PFD and FE-PFD are standard edge-triggered PFDs. Their output signals are combined in a pulse merging circuit, implemented with OR gates. Compared to a single ZC detection scheme, the output rate of a dual ZC detection scheme is 2× higher. As a result, even without the extra startup circuitry of [4], the average lock-time after a power-on reset is halved: from ~9.8 μs (56 cycles) to ~4.8 μs (26 cycles).

The CCO is a 9-stage ring oscillator, with a gain of 1 MHz/μA. Its delay cells consist of two inverters, which employ cross-coupled transmission gates to attenuate common-mode signals, and thus enable pseudo-differential operation. A single-ended output buffer

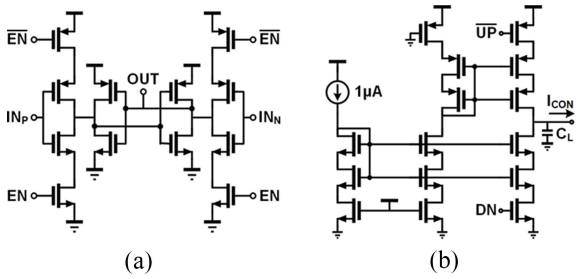

Fig. 7. Schematic of (a) ZC detector and (b) CP.

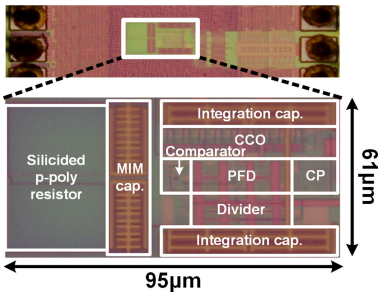

Fig. 8. Chip micrograph.

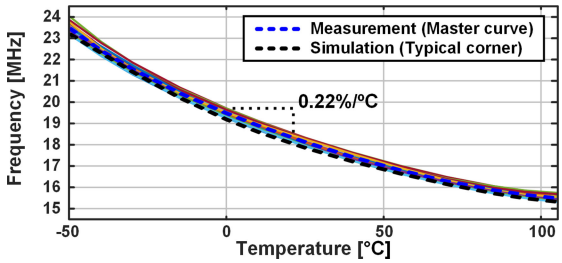

Fig. 9. Measured and simulated output frequency versus temperature.

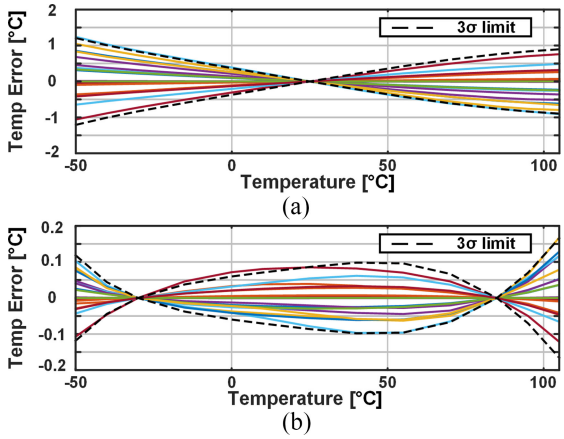

Fig. 10. Measured temperature error after (a) one-point trim and (b) two-point trim.

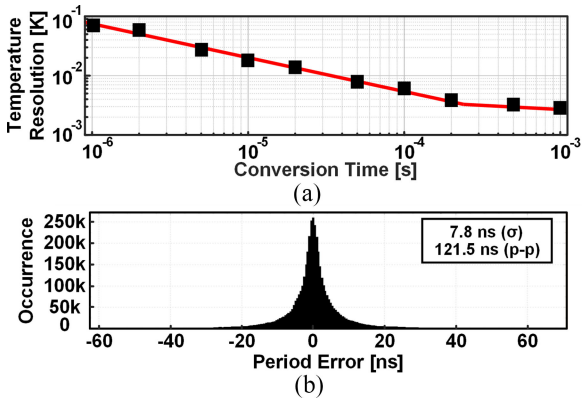

Fig. 11. (a) Temperature resolution versus conversion time. (b) Measured accumulated jitter in 1-ms time window.

employs a level shifter for rail-to-rail operation and an inverter-based latch for 50% duty cycle. The loop filter uses a large g_m (100 μS) and small C_{INT} (1.6 pF) to achieve a loop bandwidth of 160 kHz, which is wide enough to effectively reduce the phase noise of the CCO [5].

Fig. 7(a) shows the ZC detector, which consists of a preamplifier and a cross-coupled latch. To save power, it is only turned on around the expected ZCs by an enable signal (EN), derived from F_{CCO} (divided by 2 and 90° shifted). From Monte Carlo simulations, $V_{\mathrm{OS}} \sim \pm$12.5 mV, which translates into a one-point trimmed temperature inaccuracy of $\pm$0.42 °C (3σ) with a dual ZC detection scheme. The detector's delay has a negligible effect on temperature inaccuracy. From Monte Carlo simulations, the delay variation of the rising and falling edges are 6.5 ns and 5.7 ns, respectively. These translate into inaccuracies of 26 mK and 25 mK, respectively. As shown in Fig. 7(b), the CP current sources are cascoded, which ensures a current mismatch of less than the target $\pm$1.6% over PVT. In this letter, an external resistor sets the CP bias current. However, the specifications of an on-chip bias circuit are quite relaxed, since a current variation of 4.5% only translates into a temperature error of $\sim$20 mK.

III. Measurement Results

The prototype sensor is fabricated in the TSMC 65-nm CMOS process and occupies only 5800 μm^2 (Fig. 8). For flexibility, its digital backend (mainly a 16-bit counter) and bias current generation are implemented off-chip. In the chosen process, they would occupy an estimated area of 900 μm^2. Compared to [4], the resistance of silicided p-poly resistor in the PPF is 2$\times$ larger, which reduces its power consumption to 32.5 μW from a 1-V supply. Since the resistor only contributes about 15% of the total input-referred noise, this has negligible impact on the sensor's resolution. Compared to [4], the use of a cascoded CP and the omission of a startup path results in less supply sensitivity. At room temperature, the sensor achieves a supply sensitivity of 0.22 °C/V from 0.85 V to 1.3 V, which is 2.3$\times$ better than [4]. Twenty samples in a ceramic dual in-line package were measured in a temperature-controlled oven from $-$50 °C to 105 °C. To minimize the effects of oven drift, the prototypes were placed in good thermal contact with an aluminum block containing a reference sensor (platinum Pt-100 resistor sensor).

A. Temperature Inaccuracy and Resolution

The FLL output frequency varies from 15.3 MHz to 23.8 MHz (0.22 %/°C), while its period changes from 42 ns to 65.4 ns (Fig. 9). As in [4] and [6], after a first-order fit to remove process spread, the nonlinear temperature dependence in the FLL's output period can be removed by a fixed fifth-order polynomial. This nonlinearity is mainly determined by the silicided poly resistor, allowing the coefficients of this polynomial to be obtained directly from TT-corner simulations. The sensor then achieves an untrimmed inaccuracy of $\pm$5.2 °C (3σ), which improves to $\pm$1.2 °C (3σ) after a room temperature trim [Fig. 10(a)]. It can be further improved to $\pm$0.16 °C (3σ) by a two-point trim [Fig. 10(b)], which is similar to [4], but is over a wider temperature range.

The sensor's temperature-sensing resolution is determined by measuring the accumulated jitter of the FLL's output period. In Fig. 11(a), the resolution is plotted versus the conversion time (T_{CONV}). Up to $T_{\mathrm{CONV}} \sim$ 0.2 ms, the accumulated jitter exhibits a $1/\sqrt{T_{\mathrm{CONV}}}$ behavior due to thermal noise. For longer measurement times, the accumulated jitter is limited by 1/f noise. As shown in Fig. 11(b), the accumulated jitter is 7.8 ns in a 1-ms period, which corresponds

TABLE I
PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART WORKS

Publication		This work	JSSC18 Choi [4]	JSSC18 Mordakhay [8]	ISSCC18 Lu [9]	SSC-L18 Xin [10]	ASSCC18 Angevare [7]
Sensor Type (Configuration)		**Resistor (PPF)**	Resistor (PPF)	Resistor (Single)	PNP+MOS	Resistor (WhB)	Resistor (WB)
Readout Type		**FLL**	FLL	ADC	ADC	ADC	ADC
Technology [nm]		**65**	65	65	22	65	180
Area [μm^2]		**5800 (6700*)**	7000 (7700*)	10000	4300	110000	6800
Power [μW]		**32.5**	68	12.8	50	0.049	1600
Supply voltage [V]		**0.85 – 1.3**	0.85 – 1.05	1.1 – 1.4	0.97 – 1.3	0.65	1.8
Supply sensitivity [°C/V]		**0.22**	0.5	3	1.76	-	-
Temperature range [°C]		**-50 to 105**	-40 to 85	-40 to 110	-30 to 120	0 to 100	-35 to 125
Inaccuracy [°C] (3σ)	1-point	**±1.2**	±2.47	±2.85	±1.07	-1.1 / +1.5**	-
	2-point	**±0.16**	±0.12	±1.05	-	-	±0.35
Conversion time [ms]		**1**	1	0.08	0.032	0.01	0.003
Energy/Conversion [nJ]		**32.5**	68	1.024	1.6	0.00049	4.8
Resolution [mK]		**2.8**	2.5	150	580	610	120
Resolution FoM [pJ·K^2]		**0.26**	0.43	20	540	1.82	69.1

Resolution FoM = Energy/Conversion × (Resolution)^2
*: Estimated area including on-chip bias and 16-bit counter in the chosen process
**: min. / max.

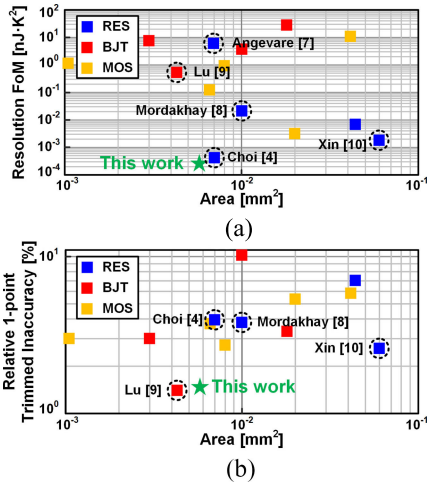

Fig. 12. Performance comparison (a) resolution FoM versus area and (b) one-point trimmed inaccuracy versus area.

to a resolution of 2.8 mK, and a competitive resolution FoM of 0.26 pJ·K^2.

B. Comparison With Previous Works

Table I shows a performance summary of the proposed PPF-based FLL temperature sensor and a comparison with other state-of-the-art works intended for thermal monitoring. The proposed temperature sensor achieves the highest accuracy and energy-efficiency, while occupying the smallest area. In particular, it is 17% smaller than our previous design [4], while its one-point trimmed inaccuracy is 2× better. The latter is mainly due to the reduction of ZC detector offset and CP mismatch in the FLL. The inaccuracy of the proposed sensor is even comparable to that of a recent BJT-based sensor [9], but with significantly better energy efficiency. Fig. 12 shows a more comprehensive comparison with the previous works [11].

C. Discussion on Process Corner Variations

Since the temperature sensor is corrected by a fixed polynomial, the accuracy will be reduced by the effect of process spread on its nonlinear temperature dependence. Table II shows the simulated one-point trimmed 3σ inaccuracy in the FF and SS corners with different polynomials. The fixed polynomial fit is determined in the TT corner, while the best polynomial fit is determined from simulations in the corresponding corners. Although the one-point trimmed 3σ inaccuracy increases to ±1.63 °C (FF) and ±1.96 °C (SS), mainly

TABLE II
SIMULATED 1-POINT TRIMMED 3σ INACCURACY COMPARISON

Process Corner	1-point trimmed 3σ inaccuracy		**Difference in 3σ error**
	w/ fixed polynomial fit	w/ best polynomial fit	
FF	±1.63 °C	±1.56 °C	**±0.07 °C**
SS	±1.96 °C	±1.78 °C	**±0.18 °C**

due to the TC spread of the silicided poly resistor, the error contributed by the use of a fixed polynomial fit is quite negligible: just ±0.07 °C and ±0.18 °C, respectively. It shows that the residual nonlinearity error of the sensor is very systematic and a fixed polynomial fit is valid over the process corners.

IV. CONCLUSION

This letter presents a temperature sensor with compact size (5800 μm^2) in 65-nm CMOS. The sensor employs a PPF for temperature sensing and an FLL with a dual ZC detection scheme. The PPF consists of MIM capacitors and silicided poly resistors, resulting in a small area with high TC and large-signal swing. The FLL incorporates a DE-PFD and cascode CP to improve its one-point trimmed inaccuracy to ±1.2 °C (3σ) from −50 °C to 105 °C. The design consumes 32.5 μW from a 1-V supply and achieves a resolution of 2.8 mK, which corresponds to a resolution FoM of 0.26 pJ·K^2. Due to its combination of compact area, moderate temperature inaccuracy, and competitive resolution FoM, the proposed PPF-based sensor is well suited for use in thermal monitoring applications in sub-100-nm CMOS.

REFERENCES

[1] U. Sönmez, F. Sebastiano, and K. A. A. Makinwa, "Compact thermal-diffusivity-based temperature sensors in 40-nm CMOS for SoC thermal monitoring," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 834–843, Mar. 2017.

[2] T. Oshita, J. Shor, D. E. Duarte, A. Kornfeld, and D. Zilberman, "Compact BJT-based thermal sensor for processor applications in a 14 nm tri-gate CMOS process," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 799–807, Mar. 2015.

[3] Y. Kim *et al.*, "A 0.02mm^2 embedded temperature sensor with ±2°C inaccuracy for self-refresh control in 25nm mobile DRAM," in *Proc. ESSCIRC*, Sep. 2015, pp. 267–270.

[4] W. Choi *et al.*, "A compact resistor-based CMOS temperature sensor with an inaccuracy of 0.12 °C (3σ) and a resolution FoM of 0.43 pJ·K^2 in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3356–3367, Dec. 2018.

[5] P. Park, D. Ruffieux, and K. A. A. Makinwa, "A thermistor-based temperature sensor for a real-time clock with ±2 ppm frequency stability," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1571–1580, Jul. 2015.

[6] S. Pan and K. A. A. Makinwa, "A 0.25 mm^2-resistor-based temperature sensor with an inaccuracy of 0.12 °C (3σ) from −55 °C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3347–3354, Dec. 2018.

[7] J. Angevare and K. A. A. Makinwa, "A 6800-μm^2 resistor-based temperature sensor in 180-nm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2018, pp. 43–46.

[8] A. Mordakhay and J. Shor, "Miniaturized, 0.01 mm^2, resistor-based thermal sensor with an energy consumption of 0.9 nJ and a conversion time of 80 μs for processor applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 10, pp. 2958–2969, Oct. 2018.

[9] C.-Y. Lu, S. Ravikumar, A. D. Sali, M. Eberlein, and H.-J. Lee, "An 8b subthreshold hybrid thermal sensor with ±1.07°C inaccuracy and single-element remote-sensing technique in 22nm FinFET," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 318–319.

[10] H. Xin, M. Andraud, P. Bltus, E. Cantatore, and P. Harpe, "A 174 pW–488.3 nW 1 S/s–100 kS/s all-dynamic resistive temperature sensor with speed/resolution/resistance adaptability," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 3, pp. 70–73, Mar. 2018.

[11] K. A. A. Makinwa. *Smart Temperature Sensor Survey*. Accessed: Aug. 11, 2019. [Online]. Available: http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls