A 0.53pJK27000µm2resistor-based temperature sensor with an inaccuracy of ±0.35°C (3σ) in 65nm CMOS

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19.3 A 0.53pJ·K² 7000µm² Resistor-Based Temperature Sensor with an Inaccuracy of ±0.35°C (3σ) in 65nm CMOS

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In microprocessors and DRAMs, on-chip temperature sensors are essential components, ensuring reliability by monitoring thermal gradients and hot spots. Such sensors must be as small as possible, since multiple sensors are required for dense thermal monitoring. However, conventional BJT-based temperature sensors are not compatible with the sub-1V supply of advanced processes. Subthreshold MOSFETs can operate from lower supplies, but at high temperatures their performance is limited by leakage [1,2]. Thermal diffusivity (TD) sensors achieve sub-1V operation and small area with moderate accuracy, but require milliwatts of power [3]. Recently, resistor-based sensors based on RC Wien-Bridge (WB) filters have realized high resolution and energy efficiency [4,5]. Fundamentally, they are robust to process and supply-voltage scaling. However, their readout circuitry has been based on continuous-time (CT) ΔΣ ADCs or frequency-locked loops (FLLs), which require precision analog circuits and occupy considerable area (>0.7mm²).

This paper presents a highly digital resistor-based temperature sensor in 65nm CMOS, which achieves a 3σ inaccuracy of ±0.35°C from -40 to 85°C and 2.8mK resolution at a 1kS/s sampling rate. The sensor can operate from 0.85V supplies, while consuming only 68µW. This corresponds to a resolution FOM of 0.53pJ·K², which is more than 15× less than a previous WB-based FLL sensor [5]. Furthermore, the sensor occupies only 7000µm², which is 13× less than [5] and comparable to state-of-the-art BJT-, MOS-, and TD-based sensors [1-3]. These advances are achieved by the use of an RC polyphase filter (PPF) as a sensing element, which is then read out by a highly digital frequency-locked loop (FLL).

The PPF consists of two silicided N-poly resistors (R=35kΩ) and two MIM capacitors (C=0.5pF). Silicided poly resistors were chosen because of their large temperature coefficient, low voltage dependency, and low 1/*f* noise [4]. Compared to a WB, a PPF requires less passive components. Furthermore, when driven by anti-phase clocks (P, $\overline{P}$), its output voltage V_{PPF} has a 5× larger swing than that of a similarly driven WB, which proportionally reduces the error contribution of the succeeding readout circuitry [6].

As shown in Fig. 19.3.1, the phase shift of an RC filter can be read out by embedding it in an FLL [4,5]. The loop settles when the input of the integrator is zero, which corresponds to a fixed phase-shift in the RC filter and hence to a fixed VCO frequency. In this work, the analog-intensive phase-demodulation scheme of [4,5] is replaced by a simple comparator that digitizes the zero-crossing of V_{PPF}, whose timing is also a function of the filter phase-shift. A phase/frequency detector (PFD) then compares the phase of the comparator output V_O with that of a quadrature feedback signal (Q) and then drives an oscillator, via a digital PI controller, such that its output frequency (F_{PPF}) corresponds to a 90° phase-shift. As a result, F_{PPF} will be proportional to $1/(R_{PPF}C)$.

Figure 19.3.2 shows the block diagram and operation principle of the proposed PPF-based FLL. By comparing the comparator output V_O with the rising edge of the Q signal, the PFD provides an up/down signal to increase/decrease the loop filter output current, which drives a current-controlled oscillator (CCO). The gain of the loop filter locks the CCO frequency F_{PPF} to the point when the phase error (φ_{DIFF}) is zero. At steady state, the current from the integral path I_{INT} is stabilized (Fig. 19.3.2, bottom). Since the VCO phase noise is shaped with the loop gain of the FLL, an analog front-end often limits the phase noise performance. In the analog-intensive approach [5], the current buffer (CB) continuously provides the output phase-demodulated current into the integration capacitor, so a considerable amount of power is required to mitigate the noise. However, since the FLL comparison instants can be predicted within a half duty cycle, the proposed front-end noise can be mitigated by increasing the power of the comparator only at the comparison moment. In the loop filter, a proportional path is added to reduce the lock-time of the loop from power-on-reset condition (<100 cycles), which is important for dense thermal monitoring applications. It also works as an added g_m, designed with a push-type charge pump (CP), and increases the loop bandwidth to 20kHz, thus reducing VCO phase noise more effectively. The proportional path is implemented with current sources that are directly driven by the PFD and the current in the proportional path I_{PROP} is defined through the voltage charged on C_{INT} (4pF) of the integral path.

Figure 19.3.3 shows the circuit-level implementation of the proposed readout circuit. To facilitate scaling in advanced processes, an inverter-based comparator is used. Two inverters serve as a preamplifier, which then drives a cross-coupled latch. Since the output of the PPF is only sampled on the rising edge of Q, the comparator can be disabled half the time to reduce the power consumption. Its power consumption is only 11µW and an input-referred noise of 18.4µV is estimated. The proportional path (CP_{PROP}) is implemented with PMOS current sources to be operated in a push-type, which also avoids a possible source of mismatch. The CP of the integral path (CP_{INT}) generates the bias voltage V_B, which is converted to I_{PROP} and I_{INT} (5 and 10µA at steady state) through PMOS transistors (M_1-M_3). I_{PROP} and I_{INT} are summed at the supply node of the CCO. Depending on the PFD state, i.e. up, reset, and down, the I_{PROP} is weighted by 2, 1 and 0 respectively, which is implemented by two switches controlled by the PFD outputs: $\overline{UP}$ and DN. The CCO is implemented using a 9-stage current-starved ring oscillator, whose gain is 1MHz/µA. Its delay cell consists of two inverters coupled with each other using transmission gates, attenuating common-mode signals by ensuring pseudo-differential operation. The CCO achieves the target output frequency range of 38 to 48MHz. The output buffer includes a level-shifter for rail-to-rail operation and an inverter-based latch for 50% duty cycle.

The prototype temperature sensor was fabricated in TSMC 65nm CMOS. The sensor occupies an area of 7000µm² (Fig. 19.3.7). It consumes 68µA from a 1V supply. The FLL output frequency changes from 38 to 48MHz over the temperature range from -40 to 85°C (Fig. 19.3.4, left). It exhibits an average temperature coefficient of 0.19%/°C. The temperature error is measured for 16 samples in ceramic DIL packages. As shown in Fig. 19.3.4 (right), after one- and two-point trimming with the removal of the systematic non-linearity following a 1st-order fit, a 3σ inaccuracy of ±3.65°C and ±0.35°C is achieved from -40 to 85°C, respectively. At room temperature, the sensor supply sensitivity of 0.5°C/V is measured from 0.85 to 1.05V. The measured phase noise at 100kHz offset is -124dBc/Hz, and the RMS jitter integrated from 1Hz to 100kHz is 12ps (Fig. 19.3.5). The accumulated jitter increases up to 10^4 cycles, showing √N behavior due to the thermal noise. Also, an accumulated jitter of 5.2ns (rms) is achieved in a 1ms time window, corresponding to 2.8mK temperature resolution. As a result, the sensor can track millisecond thermal transients with high energy efficiency (FOM of 0.53pJ·K²).

Figure 19.3.6 shows the performance summary and comparison with state-of-the-art. The proposed sensor is 13× smaller than a conventional FLL readout [5] and 100× smaller than a ΔΣ ADC readout [4]. Due to the supply voltage scaling and improved jitter performance, the resolution FOM is also highly improved by 15× compared to [5]. Even compared to a compact MOS-based sensor [2], this work is 6× more energy-efficient with similar size. It can be seen that, compared to BJT- and TD-based designs [1,3], this sensor consumes significantly less energy. These results demonstrate that the proposed PPF-based FLL can be used to realize reliable on-chip temperature sensors for dense thermal monitoring, in nanometer CMOS processes.

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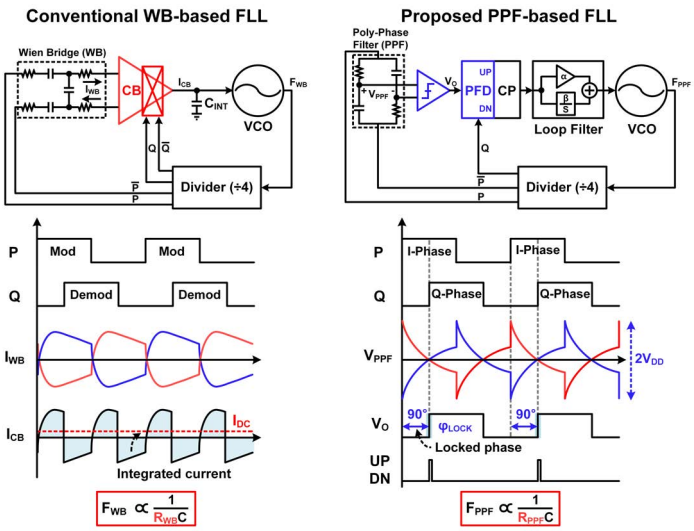

Figure 19.3.1: Architecture of the WB-based FLL and the proposed PPF-based FLL.

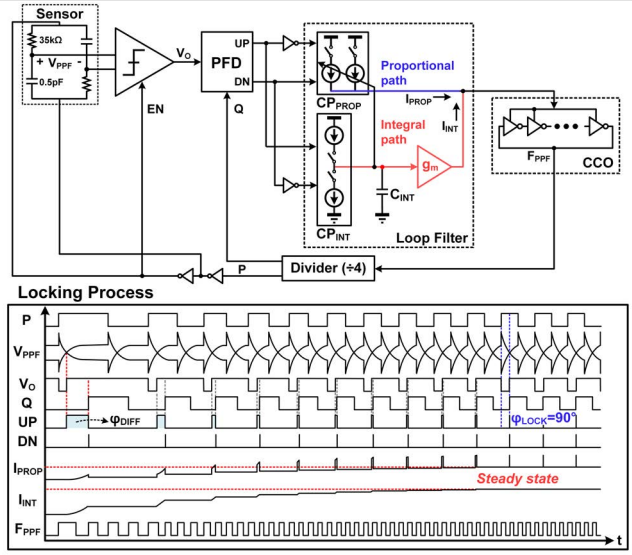

Figure 19.3.2: Block diagram and operation principle of the PPF-based FLL.

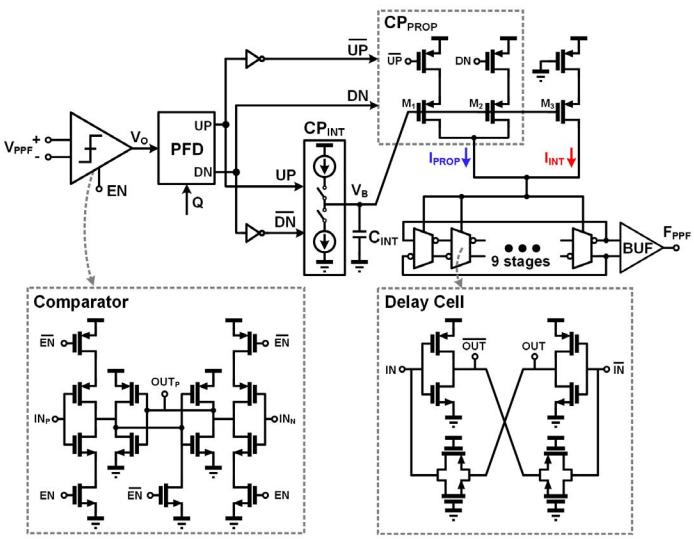

Figure 19.3.3: Circuit implementation of the readout circuit.

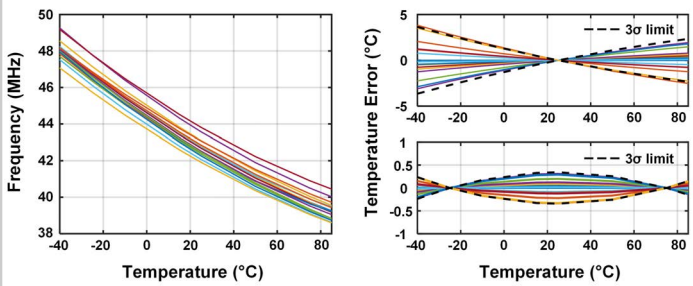

Figure 19.3.4: Measured sensor output frequency (left) and Temperature error after 1-point (top right) and 2-point trimming (bottom right).

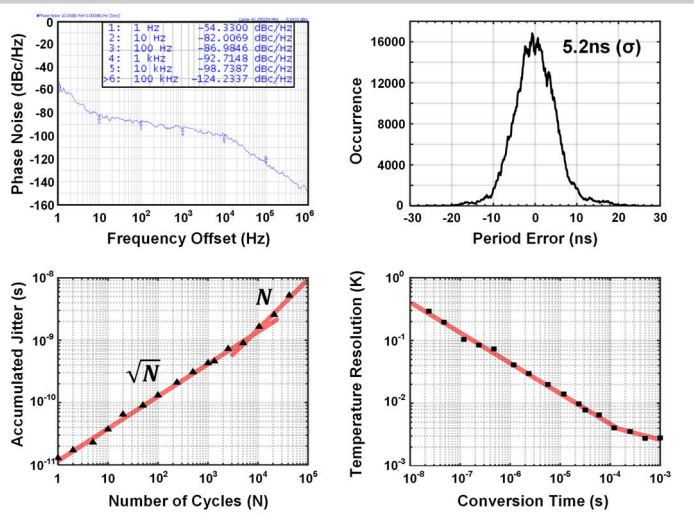

Figure 19.3.5: Measurement Results: Phase noise, Accumulated jitter on a 1ms time window, Accumulated jitter vs. number of cycles, and Temperature resolution vs. conversion time.

Publication	This Work	JSSC15 Park [5]	ISSCC17 Pan [4]	ISSCC17 Yang [2]	JSSC15 Oshita [1]	ISSCC16 Sönmez [3]
Sensor Type (Configuration)	**Resistor (PPF)**	Resistor (WB)	Resistor (WB)	MOS	BJT	TD
Readout Type	**FLL**	FLL	ΔΣ	OSC	ΔΣ	ΔΣ
Technology	**65nm**	180nm	180nm	180nm	14nm	40nm
Area [μm²]	**7000**	90000	720000	8865	8700	1650
Power [μW]	**68**	31	160	0.075	1100	2500
Supply voltage [V]	**0.85-1.05**	3.3	1.6-2	0.8-1.8	1.35	0.9-1.2
Supply sensitivity [°C/V]	**0.5**	0.4	0.17	0.13	-	2.8
Temperature range [°C]	**-40 to 85**	-40 to 85	-40 to 85	-20 to 100	0 to 100	-40 to 125
Inaccuracy [°C]	**±0.35**** (3σ)	±0.12*** (p-p)	±0.2* (3σ)	-0.22/0.19** (3σ)	±0.7** (3σ)	±0.75* (3σ)
Conversion time [ms]	**1**	32	5	8	0.02	1
Energy/Conversion [nJ]	**68**	992	800	0.6	22	2500
Resolution [°C]	**0.0028**	0.0028	0.00041	0.073	0.5	0.36
Resolution FOM [pJ·K²]	**0.53**	8	0.13	3.2	5500	324000

* 1-point trimming, ** 2-point trimming, *** 3-point trimming

Resolution FOM = Energy/conversion × (Resolution)²

Figure 19.3.6: Performance summary and comparison with the state of the art.

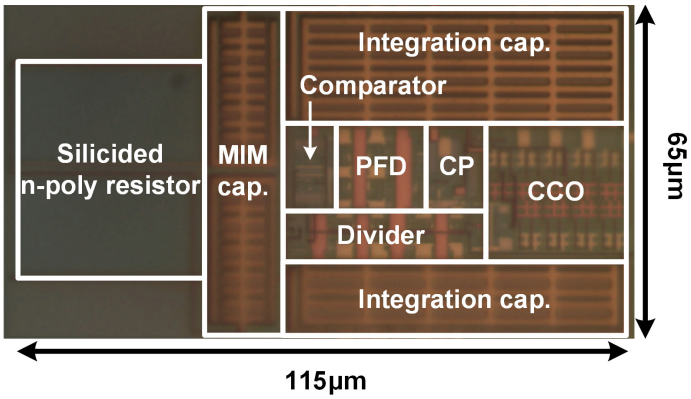

Figure 19.3.7: Die micrograph.

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