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14.5 A 280μW Dynamic-Zoom ADC with 120dB DR and 118dB SNDR in 1kHz BW

Shoubhik Karmakar[1], Burak Gönen[1], Fabio Sebastiano[1], Robert Van Veldhoven[2], Kofi A. A. Makinwa[1]

[1]Delft University of Technology, Delft, The Netherlands
[2]NXP Semiconductors, Eindhoven, The Netherlands

Micro-power ADCs with high linearity and dynamic range (DR) are required in several applications, such as smart sensors, biomedical imaging, and portable instrumentation. Since the signals of interest are then often small (tens of μV) and slow (<1kHz BW), such ADCs should also exhibit low offset and flicker noise. Noise-shaping SAR [1] and incremental ADCs [2] have been proposed for such applications, but their DR is limited to about 100dB. Although the ΔΣ modulator (ΔΣM) proposed in [3] achieves 136dB DR, it is at the expense of high power consumption (12.7mW). The incremental zoom ADC proposed in [4] combines a coarse SAR ADC and a fine ΔΣ ADC to efficiently achieve 119.8dB DR, but is limited to DC signals. The dynamic zoom ADC in [5] solves this problem, but requires external filtering to cope with out-of-band interference. This paper describes an interferer-robust dynamic zoom ADC that consumes 280μW while achieving 120.3dB DR and 118.1dB SNDR in 1kHz BW, resulting in a Schreier FoM of 185.8dB. It also achieves a maximum offset of 30μV and a 1/f corner of 7Hz. These advances are achieved by the combination of dynamic error-correction techniques, an asynchronous SAR ADC and a fully differential inverter-based ΔΣ ADC.

As shown in Fig. 14.5.1, the proposed ADC consists of a coarse 5b asynchronous SAR ADC and a fine 2nd-order 1b ΔΣM. In contrast to previous zoom ADCs [4,5], the coarse and fine conversions employ the same sampling frequency (f_s = 2MHz). During ϕ_1, the SAR ADC ($V_{LSB,SAR} = V_{REF}/31$) outputs a conversion result K, which is then used to update the ΔΣM references during the next half clock cycle (ϕ_2). The fine and coarse converters use separate DACs, and so there will be some mismatch between their LSBs. Furthermore, coarse conversion errors may occur. To ensure that the input swing of the modulator remains within its stable range under all of these conditions, over-ranging is applied. This is accomplished by setting the positive and negative references to $V_{REF+} = (K+2)\cdot V_{LSB,SAR}$ and $V_{REF-} = (K-1)\cdot V_{LSB,SAR}$, respectively. The 5b digital output of the zoom ADC (Dout) can then be obtained by combining the 5b output of the SAR with the 1b output of the ΔΣM.

Using a high-speed coarse ADC in a zoom ADC confers significant advantages. In this work, compared to [5], the use of an asynchronous SAR ADC ensures that the ΔΣM references are updated 10× faster – after half a clock cycle instead of after 5 clock cycles. This significantly reduces the input swing of the ΔΣM, thus requiring 2× less over-ranging, and making better use of its dynamic range. This, in turn, means that the target resolution could be obtained with a 2nd-order ΔΣM, rather than the 3rd-order ΔΣM used in [5]. Another advantage of the faster update rate is that it improves the robustness of the zoom ADC to out-of-band interference. Compared to [5], which could only handle full-scale signals up to 1.5× its BW before its SNDR degraded, the proposed design can handle full-scale signals up to 48× its BW. In many cases, e.g. sensor readout, this level of robustness obviates the need for external filtering.

The asynchronous SAR ADC consists of a 5b binary-weighted capacitive DAC, asynchronous SAR logic, and a comparator as shown in Fig. 14.5.2. Since the unit capacitor is small (C_0 = 5fF), a preamplifier is used before the comparator to mitigate kick-back. The input is tracked until the rising edge of CLK, when it is sampled. Each conversion cycle starts by setting the DAC inputs and then resetting the comparator with compCLK=0. After a delay (t_{settle}) to allow the DAC to settle, the comparator is clocked (compCLK=1) to make a comparison. An XOR gate monitors the comparator output and generates the outputRDY=1 signal once a decision is made. This is saved in the SAR register and a new cycle is started. After 5 asynchronous cycles, the SAR ADC returns to its input-tracking mode and the preamplifier is turned-off to save power.

A simplified schematic of the 2nd-order feed-forward 1b ΔΣM is shown in Fig. 14.5.3. It consists of two switched-capacitor integrators, a 5b unary capacitive DAC and a comparator. Correlated double sampling (CDS) is used to mitigate the effects of the 1st integrator's offset and 1/f noise. At the end of ϕ_1, the DAC capacitors $C_{DAC[1..31]}$ (437fF each, equivalent to C_S = 13.5pF) sample V_{IN} with respect to the input offset and 1/f noise of OTA1, which is configured as a unity-gain buffer. During ϕ_2, the DAC is set to m = (K+2) or m = (K-1) depending on the output bitstream (bs), so that a charge $C_S\cdot(V_{IN} - m\cdot V_{REF}/31)$ is transferred into the integration capacitor $C_{INT,1}$ (9pF). In order to minimize the coupling between the SAR ADC and the ΔΣM through the ADC input terminal, their sampling instants are kept a half clock cycle apart (Fig. 14.5.1). Also, data-weighted averaging (DWA) is applied to the DAC to improve its linearity. Each SAR conversion only takes about 10% of ϕ_1, which gives the DWA logic sufficient time before the start of ϕ_2.

As noted above, rapidly updating the references of the fine ΔΣM reduces its input swing. As a result, the loop filter can be implemented with power-efficient fully differential current-reuse OTAs (Fig. 14.5.3). For robustness to PVT, OTA1 is biased with 40μA mirrored from a constant-g_m reference. OTA2 is an 8× scaled down version of OTA1. Both OTAs use cascodes to achieve a DC gain of 60dB. While 40dB would have been sufficient to keep the quantization noise of the modulator well below the thermal noise floor, more gain improves the ability of the CDS scheme to suppress the offset and flicker noise of OTA1. Compared to the dynamically biased pseudo-differential inverter-based OTAs used in [4,5], the result is a more robust and area-efficient loop filter design.

The prototype chip (Fig. 14.5.7) is realized in a standard 0.16μm CMOS process and occupies an active area of 0.25mm^2. It draws 154.5μA (88μA analog, 42μA digital, and 24.5μA references) from a 1.8V supply. On-chip LVDS drivers were used to output the 5b output code in order to minimize on-board coupling between analog and digital. Figure 14.5.4 shows the output spectrum of the zoom ADC with a full-scale signal, and also with its inputs shorted to measure its offset and 1/f corner. The "fuzz" visible above 2kHz is due to the fact that the output spectrum is the result of adding the SAR ADC output which contains wide-band quantization noise, to the fine ΔΣM output, which is processed by the low-pass ΔΣM signal transfer function. Being a signal-processing artifact, it does not cause intermodulation issues and is suppressed by the decimation filter of the ADC. The maximum offset is 30μV (10 samples) and the 1/f corner is at 7Hz. From DC to 3kHz, the PSRR is greater than 96dB, demonstrating the benefits of using fully differential OTAs. The SNDR remains the same even with full-scale out-of-band input signals with frequencies up to 48kHz.

Figure 14.5.5 shows the peak SNR, peak SNDR and DR of the ADC, which are 119.1dB, 118.1dB, and 120.3dB, respectively, for a 152Hz input signal in a 1kHz bandwidth. The measured -125.9dB THD (6 harmonics included) and SNDR were limited by a 1st-order filter used in the measurement setup. This filter (-3dB BW of 2.3MHz) was inserted between a pair of off-chip buffers and the ADC to limit the fold-back of the wideband noise from the buffer. However, this filter also causes incomplete settling, and hence introduces some distortion.

Figure 14.5.6 summarizes the ADC performance and compares it to ADCs with similar resolution and bandwidth (>95dB SNDR, <2kHz BW). It outperforms all other designs in terms of SNDR while achieving a state-of-the-art Schreier FOM of 185.8dB, thus demonstrating that zoom ADCs can offer state-of-the-art performance and robustness in low-bandwidth high-precision applications.

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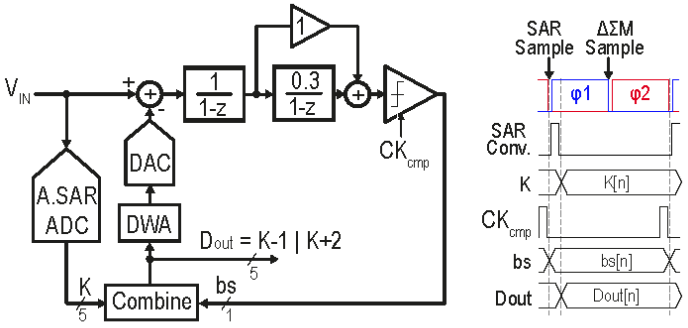

Figure 14.5.1: Block diagram and timing diagram of the proposed zoom ADC.

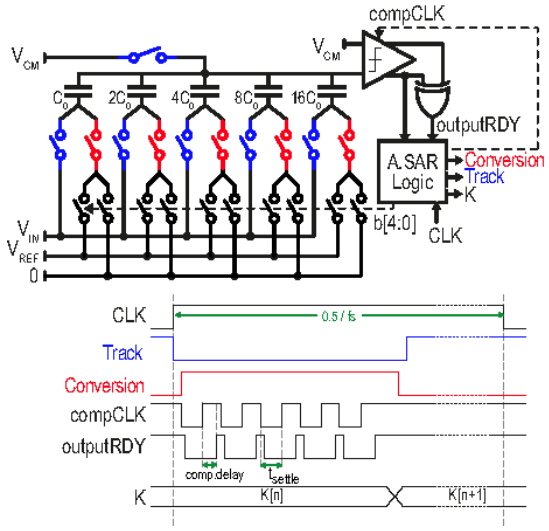

Figure 14.5.2: Simplified single ended schematic and timing diagram of the SAR ADC.

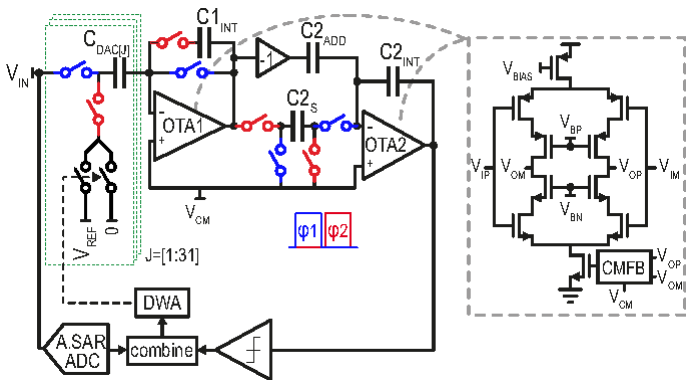

Figure 14.5.3: Simplified single-ended schematic of the proposed zoom ADC and the OTAs.

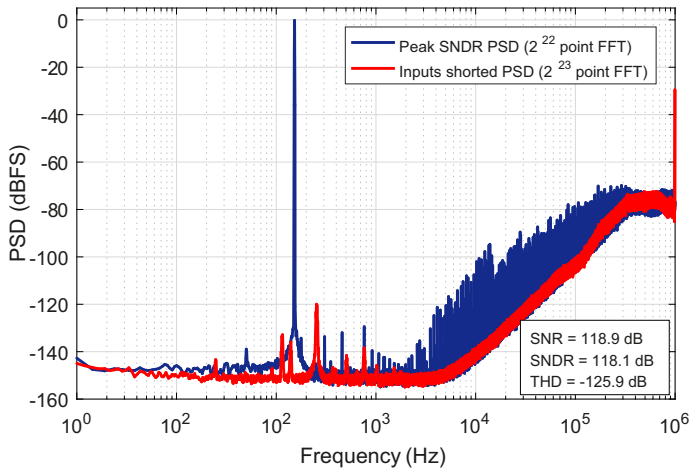

Figure 14.5.4: Measured output spectrum of the zoom-ADC at peak SNDR and with zero input (inputs shorted).

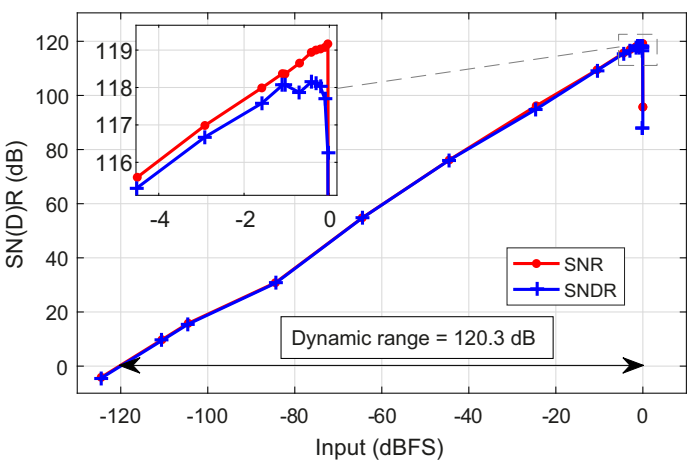

Figure 14.5.5: SNR and SNDR versus input signal amplitude (f_{in} = 152Hz, DWA on).

	This Work	[1]	[2]	[3]	[4]
Year	2018	2016	2017	2016	2013
Tech (nm)	160	55	180	350	160
Area (mm²)	0.25	0.072	0.27	11.5	0.375
Supply (V)	1.8	1.2	1.5	5.4	1.8
Power (μW)	280	15.7	33.2	12700	6.3
F_{sample}(MHz)	2	1	0.64	0.64	0.05
Bandwidth (kHz)	1	1	1.2	1	0.013
Offset (μV)	30	-		-	1
SNR_{max} (dB)	119.1	104	97.1	-	119.8
$SNDR_{max}$ (dB)	118.1	101	96.6	-	-
THD (dB)	-125.9	-	-	-116	-
DR (dB)	120.3	101.7	100.2	136.3	119.8
FoM_S** (dB)	185.8	179.7	175.8	185.3	182.7

**FoM_S = DR + 10log(BW/Power)

Figure 14.5.6: Performance summary and comparison with state of the art.

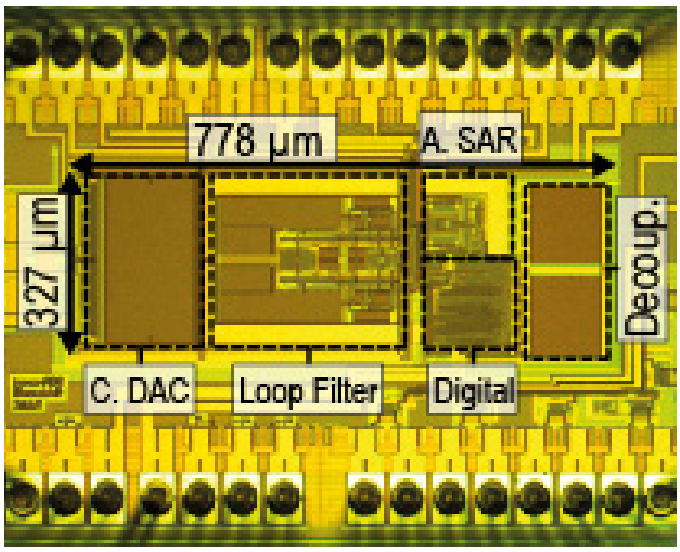

Figure 14.5.7: Chip micrograph.

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