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A 6800-μm² Resistor-Based Temperature Sensor in 180-nm CMOS

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***Abstract*—A resistor-based temperature sensor has been realized in 180 nm CMOS for SoC thermal management applications. Occupying only 6800 μm², it is the smallest resistor-based temperature sensor ever reported. This is achieved by employing a compact highly-digital VCO-based ADC. After a 2-point trim, the sensor achieves an inaccuracy of ±0.35 °C (3σ) in a temperature range from -35 °C to 125 °C. By achieving a resolution of 0.12 °C (rms) at 2.8 kSa/s, it can track the fast thermal-transients in SoCs.**

Keywords—Temperature sensor, Thermal Sensing, Wien-Bridge

I. Introduction

As the dimensions of CMOS devices continue to shrink, their energy density goes up, leading to severe self-heating issues in large Systems-on-Chips (SoCs). This can degrade performance, reduce life-time and even cause permanent damage. To prevent this, SoCs typically employ dynamic thermal management (DTM) [1, 2]. This involves using on-chip temperature sensors to monitor die temperature and then taking action to ensure that it does not rise above pre-determined limits. Possible actions range from reducing the clock frequency and/or the supply voltage to complete shutdown. To account for temperature sensor errors, however, DTM limits must include safety margins. Since such margins directly translate into unspent power, and therefore to reduced performance, the accuracy of temperature sensors for thermal management applications is paramount and should be less than ±1 °C at 70 °C [3].

In modern SoCs, local die temperatures can rise significantly in only a few milliseconds [3]. As such, local hotspots may be created, which must be monitored to avoid reliability risks. Because such hotspots are typically caused by the activity of large digital blocks, their precise location is difficult to predict at design time [3]. As a result, on-chip temperature sensors will often be located some distance away from the actual hotspot, leading to significant errors in its estimated temperature, and thus requiring even larger safety margins. To minimize such errors, large SoCs will typically contain multiple temperature sensors. These should be as small as possible to maximize area efficiency and facilitate flexible placement in digital blocks [3]. Furthermore, they should sample fast enough (> 1 kSa/s) to detect thermal transients.

Most temperature sensors proposed for thermal management applications belong to one of three categories. The most common are bandgap-based temperature sensors, which exploit the temperature dependence of parasitic bipolar transistors (BJTs) [3]. Although very accurate, their voltage headroom requirements do not scale with technology. As a scaling-friendly alternative, sensors based on gate-delay have been proposed. Although they can be quite small, they are inherently sensitive to power supply variations [5, 6] and are prone to MOSFET aging. Recently, thermal-diffusivity (TD) sensors have been proposed. These exploit the well-defined temperature-dependent propagation of heat through Silicon. Although they are naturally small, accurate and scale well with technology, they are comparatively power hungry [7-9].

As an alternative, the temperature dependence of on-chip resistors can be exploited to realize resistor-based temperature sensors [10]. Even though they are not as area efficient as transistors, the moderate accuracy and resolution requirements of DTM means that they can be quite compact. In [11], however, the sensor outputs a temperature dependent frequency, which must still be digitized by extra circuity. In this paper, a proof-of-concept resistor-based temperature sensor is proposed with a VCO-based read-out circuit that provides a direct digital output and results in an even smaller sensor.

II. Architecture

A. Wien-Bridge

In general, temperature-to-digital converters (TDCs) can be realized with either time-domain or amplitude domain techniques. Since advanced processes typically support only low supply voltages but offer very fast circuitry, TDCs in such processes can best be realized with time-domain techniques. This requires a temperature-dependent signal in the time-domain. An on-chip RC filter can generate a temperature-dependent time delay (or phase shift). This delay is mainly due to the resistors, since on-chip (MIM) capacitors are relatively stable. Such RC filters should minimize area while maximizing temperature sensitivity. 1st order low-pass (LP), Wien-Bridge (WB) [10] or Poly-Phase (PP) filters [11] can be employed. The LPF has the smallest area, but its phase shift also exhibits the lowest sensitivity to changes in resistance, and hence in temperature. This sensitivity can be doubled by using a WB or

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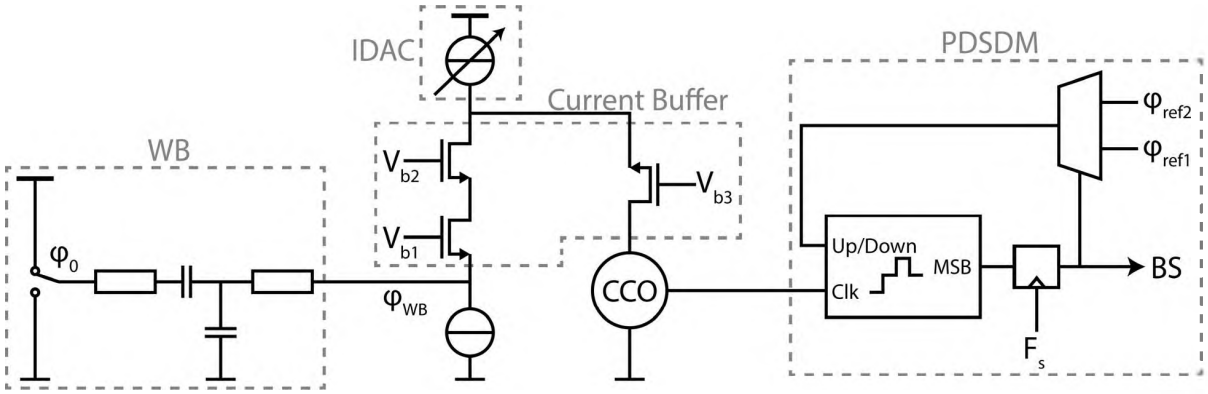

Fig. 1. Complete system schematic.

a PPF, but at the expense of more resistors and capacitors [10, 11]. However, when driven by rail-to-rail square-waves, e.g. generated by standard logic, the output voltage of a PPF exceeds these rails and thus requires the use of thick-oxide devices. The WB does not suffer from this problem, and so was chosen for use in this work. To save area, a single-ended configuration was used (Fig. 1).

The design of the WB involves a number of trade-offs. A lower center frequency (f_{WB}) results in larger phase delay, which in turn minimizes the errors caused by other sources of delay, and thus increases accuracy. However, it requires larger components. In this design, R = 28 kΩ (silicided poly) and C = 1.8 pF (MIM) were chosen, resulting in f_{WB} = 3 MHz. The resulting WB then occupies about 60% of the sensor's total area. This should scale well, since process scaling is usually accompanied by an increase in capacitance density.

B. Phase-Domain Sigma-Delta Modulator

A phase-domain sigma-delta Modulator (PDSDM) is used to readout the phase shift of the WB [8]. It uses a chopper as a phase detector, and the feedback loop of the PDSDM forces the integrator input to be 0 on average (Fig. 1). This occurs when the WB output phase (φ_{in} in Fig. 8) is 90° phase shifted with respect to the phase of the chopping waveform (φ_{in}+90°).

In [10] and [11], the analog readout circuitry was realized with the help of large integration capacitors. In this work, a highly digital VCO-based PDSDM is used [7]. By converting the signal of interest into the frequency-domain (by means of a VCO), a digital up/down counter can be used as a time-domain integrator, thus obviating the need for integration capacitors. This has three advantages: it is more area efficient, it scales well with technology, and, once designed, it can be readily synthesized.

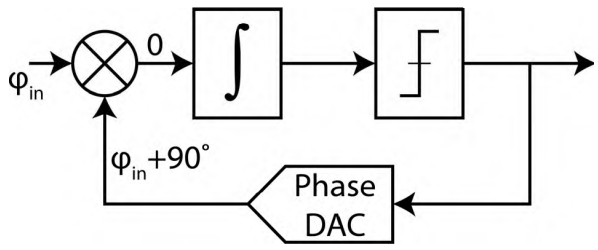

Fig. 2. Block diagram of the Phase-Domain Sigma-Delta Modulator.

Conceptually, a counter can be seen as an integrator of digital pulses. So instead of integrating current, a counter integrates frequency. The output current of the WB is processed by a current buffer that feeds a current-controlled oscillator (CCO) used to transform the WB signal into the frequency domain (Fig. 1). The CCO output is fed into the up/down counter. Toggling the counter's up/down signal inverts its integration polarity, effectively chopping the input signal and realizing the phase detector function. The comparator can also be efficiently implemented by sampling the counter's most-significant bit (MSB).

C. Counter

In this design the quantization noise associated with the use of a counter as a discrete-time integrator [12] is the dominant noise source. It has a white spectrum and can be minimized by maximizing the ratio between the CCO's oscillation frequency and the chopping frequency (up/down frequency), and by maximizing the CCO's output swing so as to make optimal use of the counter's dynamic range. However, a higher CCO output frequency requires more counter bits to prevent overflow. As a compromise, a 7-bit counter with a maximum clock frequency of 800 MHz was designed.

To reduce the counter's area and power consumption, it is split into a 2-bit fine and 5-bit coarse counter (Fig. 3). The fine counter uses gray-coding to reduce circuit complexity and employs clock-gating to reduce the frequency in the coarse counter by a factor 4, and reduce its power consumption. To

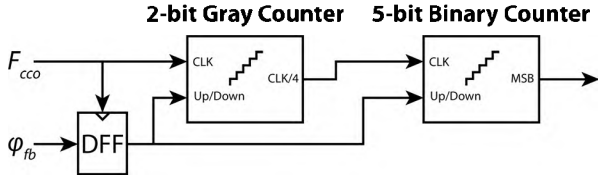

Fig. 3. Block diagram of the counter.

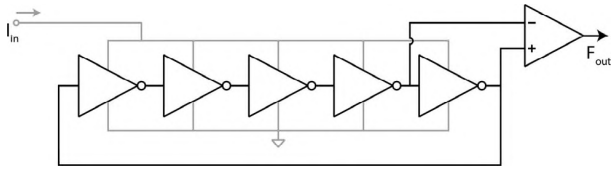

Fig. 4. Schematic of the current-controlled oscillator and levelshifter.

prevent meta-stability issues, the up/down signal is re-clocked by the counter clocking signal. The complete digital circuit, including the 2-bit gray and 5-bit binary counter, was designed to operate from -55 to 125 °C.

D. Current Controlled Oscillator

The combination of the WB and the CCO were designed to generate a frequency swing of about 600 MHz peak-to-peak, leaving some margin for process spread. An additional (6-bit) current DAC allows for a one-time trim of the mean CCO frequency, ensuring that it is close to the middle of the desired frequency range, i.e., 400 MHz.

The CCO consists of a 5-stage ring-oscillator (Fig. 4). Since its output amplitude varies significantly over PVT, a level-shifter is used to generate a rail-to-rail output signal. However, this must be quite fast to avoid introducing extra delay. In [9], the level shifter consisted of a CM sensing circuit and a differential pair. In this design, both inputs are simply connected to consecutive stages of the ring-oscillator.

For accuracy, the output of the WB should be connected to a low impedance node to avoid altering f_{WB} and causing extra phase spread. Because the CCO has a significant input impedance (~20 kΩ), a folded-cascode current buffer (Fig. 3) is used to create a better virtual ground (~600 Ω). The folded cascode requires a bias current of ~100 µA in order to reduce the phase-shift contribution. Due to the finite output impedance of the various current sources, the gain of the current buffer is less than unity. However, this is not a problem, since the PDSDM measures phase information, and is insensitive to amplitude variation.

III. Measurement Results

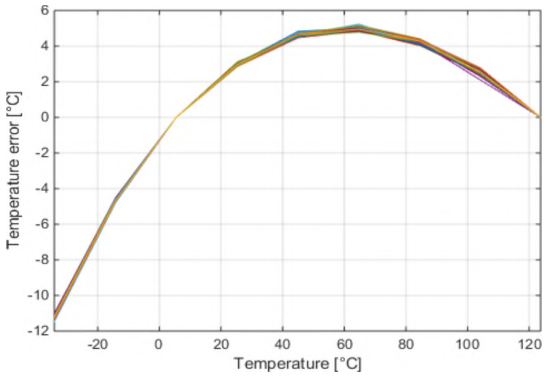

Fig. 6. Measured temperature error, before systematic non-linearity removal.

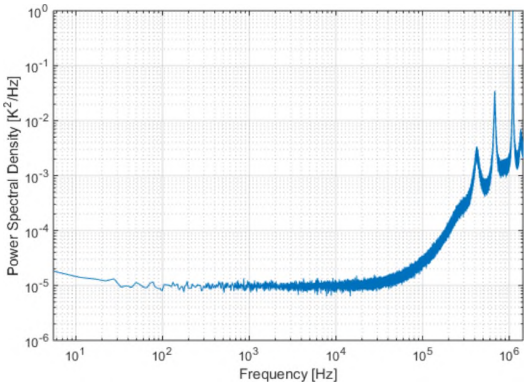

Fig. 5. PSD of 2^{19} bitstream samples, averaged over 100 cycles.

The sensor has been realized in a 180-nm CMOS process and occupies 6800 µm². Each chip consists of 20 temperature sensors and shared bias and reference phase generators. The latter supplies a selected sensor with a zero-phase WB drive signal and two reference phases for the PDSDM feedback. Each sensor dissipates 1.6 mW, 60% of which is consumed by the counter.

The PDSDM is operated at 2.9 MHz and each conversion consist of 1024 clock cycles resulting in a conversion rate of 2.8 kSa/s. After decimation by a sinc¹ filter, the sensor's output is processed by a 1st order polynomial whose coefficients are derived by a two-point calibration (at 5 °C and 125 °C). The resulting systematic non-linearity (Fig. 6) is then removed by a fixed 3rd order polynomial. For flexibility, both the decimation filter and the polynomial correction were implemented off-chip. As shown in Fig. 7, the sensor achieves an inaccuracy of ±0.35 °C in a temperature range from -35 °C to 125 °C. The resulting relative accuracy is the best in class and is only surpassed by [10], which requires a much larger. Fig. 5 shows the PSD of the bitstream, which indicates that the sensor is white noise limited up to 10 kHz. Fig. 8 shows a chip photograph of the sensor. In Table I the sensor's performance is compared to other state-of-the-art temperature sensors intended for DTM applications.

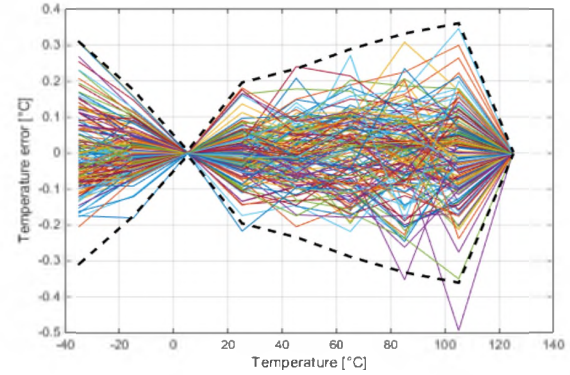

Fig. 7. Measured temperature error for 8 measured chips (160 sensors) after a two-point trim. Black dashed lines indicate the 3σ error.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART.

Publication	*This Work*	*U. Sonmez* [9]	*S. Pan* [10]	*W. Choi* [11]	*Y-C Hsu* [13]	*M. Eberlein* [14]
Year	2018	2016	2017	2018	2017	2017
Type	Resistor	TD	Resistor	Resistor	PNP	NPN
Technology	180nm	40nm	180nm	65nm	28nm	28nm
Area (μm²)	6800	1650	720000	7000	9460	3800
Inaccuracy (3σ, °C)	-	1.4	-	-	0.87	3.6
Inaccuracy, 1-pt trim (3σ, °C)	-	0.75	0.3	-	-	-
Inaccuracy, 2-pt trim (3σ, °C)	0.35	-	0.075	0.35	-	-
Relative inaccuracy (3σ, m°C/°C)	2.19	8.48 / 4.55	2.4 / 0.6	2.8	6.96	24
Temperature Range (°C)	-35 to 125	-40 to 125	-40 to 85	-40 to 85	0 to 125	-20 to 130
Resolution (°C)	0.12	0.36	0.00017	0.0028	0.15	0.5
Speed (kSa/s)	3	1	0.1	1	0.15	0.5
Supply Voltage (V)	1.8	1	1.8	0.85-1.05	1.8	1.1
Power (mW)	1.6	2.5	0.18	0.068	0.0188	0.0176

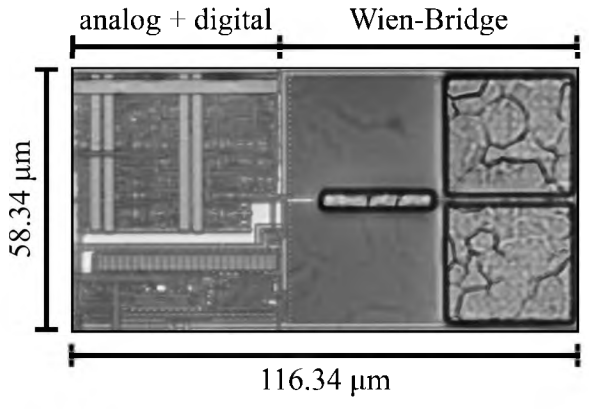

Fig. 8. Chip photograph.

IV. CONCLUSION

A compact resistor-based temperature sensor has been proposed. Compared to other resistor-based temperature sensors aimed at thermal management, this proof of concept design achieves the lowest area and best relative accuracy, despite being realized in a mature 180nm process. The reason for its low area is the use of a highly digital VCO-based ADC. Since this design scales well with technology, its performance is expected to improve when ported to more advanced processes.

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