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A Compact Resistor-Based CMOS Temperature Sensor With an Inaccuracy of 0.12 °C (3σ) and a Resolution FoM of 0.43 pJ · K^2 in 65-nm CMOS

Woojun Choi, *Student Member, IEEE,* Yongtae Lee, *Student Member, IEEE,* Seonhong Kim, Sanghoon Lee, Jieun Jang, Junhyun Chun, Kofi A. A. Makinwa, *Fellow, IEEE,* and Youngcheol Chae, *Member, IEEE*

***Abstract*— This paper presents a compact resistor-based CMOS temperature sensor intended for dense thermal monitoring. It is based on an *RC* poly-phase filter (PPF), whose temperature-dependent phase shift is read out by a frequency-locked loop (FLL). The PPF's phase shift is determined by a zero-crossing (ZC) detector, allowing the rest of the FLL to be realized in an area-efficient manner. Implemented in a 65-nm CMOS technology, the sensor occupies only 7000 μm^2. It can operate from supply voltages as low as 0.85 V and consumes 68 μW. A sensor based on a PPF made from silicided p-poly resistors and metal–insulator–metal (MIM) capacitors achieves an inaccuracy of ±0.12 °C (3σ) from −40 °C to 85 °C and a resolution of 2.5 mK (rms) in a 1-ms conversion time. This corresponds to a resolution figure-of-merit (FoM) of 0.43 pJ·K^2.**

***Index Terms*— Area-efficient, CMOS temperature sensor, energy-efficient, frequency-locked loop (FLL), poly-phase filter (PPF), resistor-based sensor, trimming, zero-crossing (ZC) detection.**

I. Introduction

TODAY'S microprocessors and DRAMs contain billions of transistors operating at gigahertz clock speed. Since the self-heating of such large chips can severely degrade their performance, thermal management is a key design consideration [1]–[3]. On-chip temperature sensors provide local temperature information about thermal gradients and hot spots, and thus prevent overheating and enhance reliability. Since the exact location of hotspots is difficult to predict in the design phase, the sensors should be as densely distributed as possible. As a result, they must be small (<0.01 mm^2), low power (<100 μW), and energy-efficient (<1 pJ·K^2). They should also be moderately accurate (3σ inaccuracy < ±1 °C) to avoid the need for large guard-bands to account for sensing errors and guarantee reliability. Furthermore, since they must track fast on-chip temperature gradients, their conversion time should be about 1 ms or less.

Conventional bipolar junction transistor (BJT)-based temperature sensors are widely used for on-chip temperature sensors due to their excellent accuracy [3]–[7]. However, they are based on parasitic p-n-p or n-p-n transistors, which are increasingly difficult to realize in scaled technologies. Moreover, their base–emitter voltages (∼0.7 V at room temperature) do not scale with technology, making them incompatible with the sub-1-V supply voltages common in modern CMOS processes. Although this can be circumvented by using a voltage doubler [4], the resulting accuracy (±2.8 °C) is rather poor. An alternative is to exploit the exponential behavior of MOSFETs in the subthreshold region [1], [8], [9]. Such sensors can operate from sub-1-V supplies, but at high temperatures, their accuracy is limited by leakage currents [1]. Thermal diffusivity (TD) sensors can scale well with technology and power supply, and can achieve moderate accuracy [2], [10]. However, they typically draw several milliwatts, which is a serious drawback in thermal management applications.

Recently, temperature sensors based on on-chip resistors have been proposed [11]–[20]. Being passive components, resistors can be implemented in any process and operated at any supply voltage. In standard CMOS processes, several types of resistors are available: N-well, metal, diffusion, and poly-silicon resistors. Of these, poly-silicon resistors have a low-voltage dependence, low $1/f$ noise, and a reasonably linear temperature dependence. They can also be combined with a silicide layer, which further increases their temperature coefficient (TC). Temperature sensors based on the temperature-dependent phase shift of *RC* Wien-bridge (WB) filters [12]–[14] or the temperature-dependent output current of Wheatstone-bridges (WhB) [15]–[17] have been realized. They can achieve high resolution in an energy-efficient manner by utilizing delta–sigma ($\Delta\Sigma$) modulator-based readout circuits but occupy considerable area (0.72 mm^2 in [14] and 0.25 mm^2 in [16]). In contrast to WB sensors, WhB sensors do not require an external frequency reference [15], [16], and

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can be read out by area-efficient SAR ADCs [17]. However, the reported area, 0.044 mm^2 in [17], is still too large for on-chip thermal management applications.

This paper presents a compact energy-efficient resistor-based CMOS temperature sensor, which is based on the combination of an *RC* poly-phase filter (PPF) and a frequency-locked loop (FLL) [18]. Compared to WB filters, PPFs provide higher frequency-to-phase gain and larger voltage swing, allowing the synchronous phase detectors of previous work to be replaced by a much simpler zero-crossing (ZC) detector. This then forms the heart of an area-efficient FLL. A prototype sensor, implemented in 65-nm standard CMOS process, occupies only 7000 μm^2. It operates at supply voltages from 0.85 V and consumes 68 μW. After a two-point trim, the silicided p-poly sensor achieves an inaccuracy of $\pm$0.12 °C (3σ) from −40 °C to 85 °C and 2.5-mK$_{\rm rms}$ resolution in a 1-ms conversion time, which corresponds to a competitive resolution figure-of-merit (FoM) of 0.43 pJ · K^2.

This paper is organized as follows. Section II reviews conventional resistor-based temperature sensors, and Section III explains the proposed resistor-based temperature sensor. Section IV describes the implementation details, and Section V shows measurement results. Finally, the conclusion is presented in Section VI.

II. Conventional Resistor-Based Temperature Sensors

A resistor-based sensor can be implemented by either sensing the temperature-dependent phase shift of *RC* filters [12]–[14] or the ratio of two resistances with different TCs [11], [15]–[17]. This section describes two representative types of resistor-based sensors: WB sensors and WhB sensors.

A. Wien-Bridge Sensor

WB sensors, which are based on the 2nd-order *RC* bandpass filters (BPF), have been proposed for temperature sensing because their temperature-to-phase characteristic has a higher TC and better linearity than a simple 1st-order low-pass filter (LPF) [12]–[14]. The temperature dependence of a WB will be mainly determined by its resistors, because on-chip capacitors are comparatively insensitive to temperature. As shown in Fig. 1(a), for a sinusoidal input voltage $V_{\rm IN}$, the output current $I_{\rm WB}$ is given by

$$\frac{I_{\rm WB}(j\omega)}{V_{\rm IN}(j\omega)} = \frac{Cj\omega}{1 - R^2C^2\omega^2 + 3RCj\omega} \tag{1}$$

and the phase shift of the WB $\phi_{\rm WB}(\omega)$ is

$$\phi_{\rm WB}(\omega) = \tan^{-1}\frac{1 - R^2C^2\omega^2}{3RC\omega} \tag{2}$$

which is 0 at the filter's center frequency $f_0 = 1/(2\pi RC)$.

As an example, consider a WB realized from silicided n-poly resistors and metal–insulator–metal (MIM) capacitors in the TSMC 65-nm CMOS process. When driven at a fixed f_0, $\phi_{\rm WB}$ will then vary from 8° to −4° over the industrial temperature range (−40 °C–85 °C). On the other hand, when $\phi_{\rm WB}$ is regulated to 0, the center frequency f_0 varies from

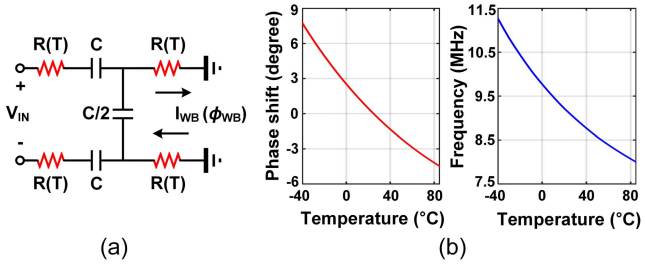

Fig. 1. (a) Schematic of the WB and (b) its phase shift and frequency shift over the industrial temperature range.

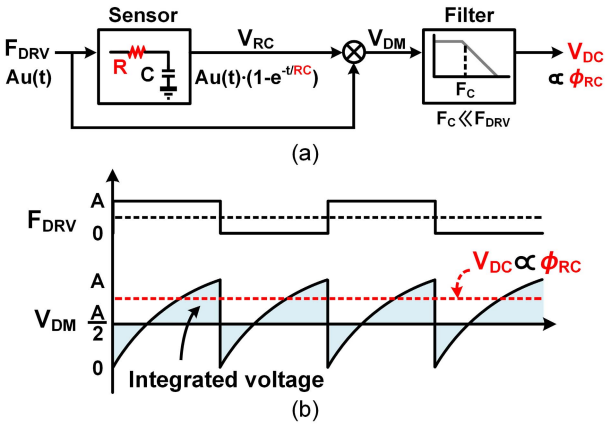

Fig. 2. (a) Synchronous phase detector with an *RC* filter and (b) its timing diagram.

11.25 to 8 MHz over the same temperature range, as shown in Fig. 1(b).

To accurately determine the filter's phase shift, synchronous phase detectors are often used [13], [14]. As shown in Fig. 2, such a detector consists of a chopper demodulator followed by an LPF. For a filter driven by a periodic input, typically a square-wave, the dc component of the detector's output voltage $V_{\rm DC}$ will be proportional to the filter's *RC* time constant, which, in turn, is proportional to its phase shift. In this arrangement, the noise bandwidth is defined by the LPF, whose cutoff frequency F_C must be low enough to achieve the necessary resolution and suppress the even-order harmonics generated by the chopper demodulator. Therefore, large filter capacitors are often required, resulting in a large area (0.09 mm^2 in [13] and 0.72 mm^2 in [14]).

B. Wheatstone-Bridge Sensor

As shown in Fig. 3(a), a WhB sensor consists of two different types of resistors (R_1 and R_2), which have similar resistances at room temperature but different TCs [15], [16]. When connected to a virtual ground, e.g., the input of an active integrator, the WhB will output a temperature-dependent current $I_{\rm WhB}$. By combining resistors with opposite TCs (α_1 and α_2) [16], the TC of the output current ($=\alpha_1 - \alpha_2$) can be larger than that of a single resistor, as shown in Fig. 3(a).

An energy-efficient way to read out $I_{\rm WhB}$ is by directly applying it to the input of a continuous-time $\Delta\Sigma$ modulator (CT$\Delta\Sigma$M), as shown in Fig. 3(b). As temperature changes,

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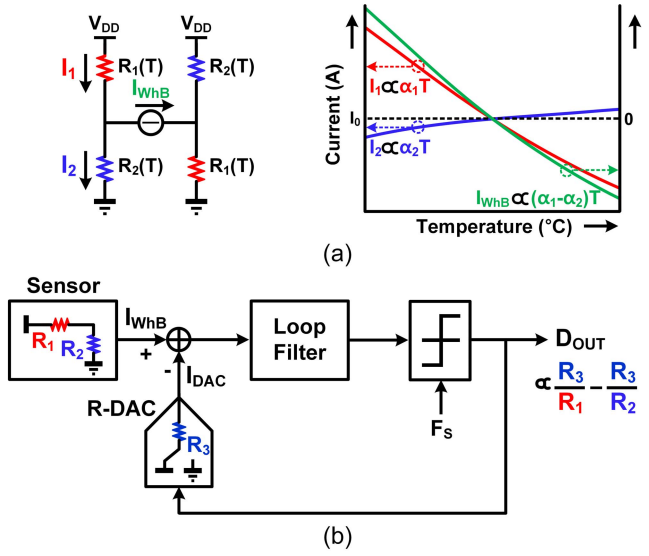

Fig. 3. (a) Schematic of the WhB and its current characteristics over temperature and (b) its CTΔΣM-based readout scheme.

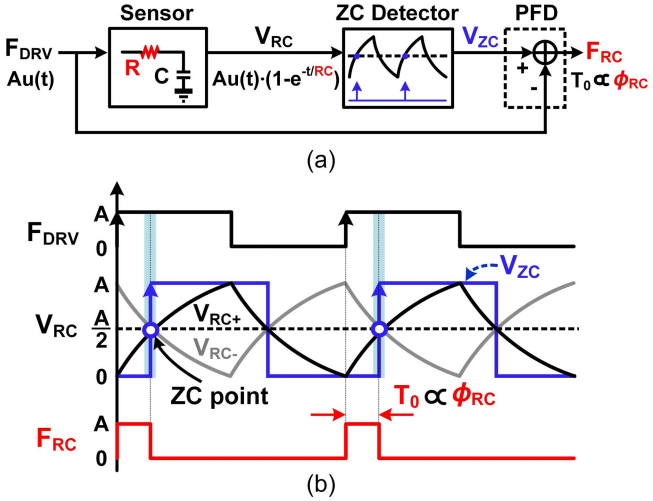

Fig. 4. (a) ZC detection scheme with an *RC* filter and (b) its timing diagram.

I_{WhB} is continuously balanced by the current I_{DAC} from a resistive DAC. The resulting digital output of the modulator, $D_{\mathrm{OUT}} = I_{\mathrm{WhB}}/I_{\mathrm{DAC}}$, mainly depends on the TCs of the WhB resistors. The enhanced TC of the sensor and the CTΔΣM readout lead to both high resolution and high energy-efficiency (32 fJ · K^2 in [16]).

However, this comes at the expense of area because the capacitors of the 1st integrator need to be large enough to filter the quantization noise of the DAC, resulting in a relatively large area of 0.43 mm^2 in [15] and 0.25 mm^2 in [16]. Moreover, unlike a WB sensor, a WhB sensor uses, at least, two types of resistors. As a result, its accuracy is more vulnerable to process spread, especially when implemented in a small area. These considerations make WhB-based sensors less attractive for use in dense thermal monitoring applications.

III. Proposed Resistor-Based Temperature Sensor

A. Proposed Zero-Crossing Detection Scheme

Fig. 4 illustrates the proposed ZC detection scheme, which consists of a ZC detector and a digital phase/frequency detector (PFD). When an *RC* filter is driven by a fixed frequency F_{DRV}, the shape of its output waveform (V_{RC}) will depend on the filter's time-constant. In practice, a differential topology will be used, as shown in Fig. 4(b). When V_{RC+} and V_{RC-} reach the threshold voltage $A/2$, the ZC point of their differential voltage will be sensed by a ZC detector, resulting in the output signal V_{ZC}. A digital PFD then compares the rising edges of F_{DRV} and V_{ZC} and provides a digital pulse F_{RC} with a duty cycle T_0. A key observation is that T_0 is proportional to the phase shift ϕ_{RC}, which contains the desired temperature information. Compared to a synchronous phase detector, a ZC detector does not need a narrow-band LPF, which often requires large capacitors, resulting in a more compact implementation. Even so, the filter's absence results in less resolution because the front-end's wide-band noise is not filtered.

TABLE I
Characteristics of Poly Resistors in Two CMOS Processes

Process	Resistor type	Temperature coefficient	Non-linearity	Sheet resistance
0.18 μm	Silicided Poly	Large ~0.3 %/°C	Small	Highly Small 1 □†
	Poly	Medium / Small <0.15 %/°C	Large	Large >35 □
65 nm	Silicided Poly	Large ~0.25 %/°C	Large	Small 2 □
	Poly	Small <0.05 %/°C	Large	Large >15 □

† The sheet resistance of the silicided poly resistor in 0.18 μm CMOS : 1 unit resistance = □

B. Poly Resistors in CMOS Process

In [12]–[14] and [16], poly resistors in a 0.18-μm CMOS process were used as sensing elements because of their high TC and high stability over a wide temperature range. To investigate the impact of process scaling, the characteristics of poly resistors are compared in two different process nodes (TSMC 65-nm and 0.18-μm CMOS), as shown in Table I. In both nodes, the use of a silicide layer increases their TCs (5× in 65-nm CMOS and 2× in 0.18-μm CMOS). In 65-nm CMOS, however, the sheet resistance of the silicided poly resistor increases by 2×, leading to proportionally smaller resistors. Although the silicided poly resistors in 65-nm CMOS have a more non-linear temperature dependence as in [21], this can be corrected in the sensor's digital back end [12]. These considerations led to the choice of silicided poly resistors as being the most suitable temperature-sensing resistors available in the target 65-nm CMOS process.

C. PPF-Based Temperature Sensor

To better utilize the properties of the sensing resistors, an *RC* PPF is proposed as a temperature sensor. Fig. 5(a) shows the schematic of a PPF sensor, which, like a 1st-order *RC* LPF, consists of a pair of resistors and capacitors. Both ends of the *RC* PPF are driven by anti-phase clocks ($\pm V_{\mathrm{IN}}/2$).

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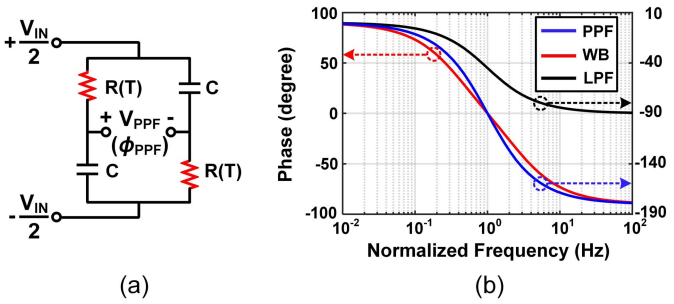

Fig. 5. (a) Schematic of PPF sensor. (b) Phase response of various RC filters.

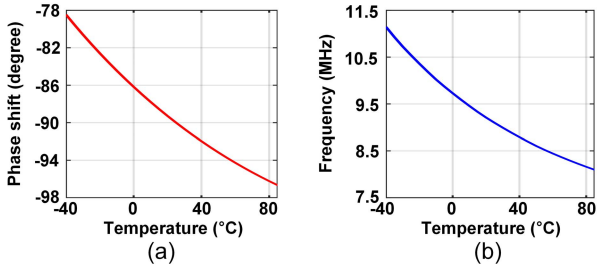

Fig. 6. Temperature properties of the PPF sensor. (a) Phase shift. (b) Frequency shift.

The output voltage V_{PPF} to the differential input voltage V_{IN} is then given by

$$\frac{V_{\mathrm{PPF}}(j\omega)}{V_{\mathrm{IN}}(j\omega)} = \frac{1 - RCj\omega}{1 + RCj\omega} \tag{3}$$

and the phase shift of the PPF $\phi_{\mathrm{PPF}}(\omega)$ is

$$\phi_{\mathrm{PPF}}(\omega) = 2 \cdot \tan^{-1}(-RC\omega). \tag{4}$$

Fig. 5(b) shows the phase response of three RC filters with normalized characteristic frequencies with $f_0 = 1/(2\pi RC)$. As can be seen, the positive zero in (3) results in a 2nd-order phase response. Therefore, compared to the 1st-order LPF, the frequency-to-phase gain of the PPF is doubled at f_0: $d\phi_{\mathrm{PPF}}/d\omega = -RC$, which is also 1.5× larger than that of the WB filter: $d\phi_{\mathrm{WB}}/d\omega = -2/(3RC)$. As shown in Fig. 6, when driven at a fixed f_0, the PPF's phase shift is 18° over the industrial temperature range, 1.5× larger than the WB filter's (12°). On the other hand, when the phase shift is adjusted to 0, the frequency shift for both the WB filter and the PPF is the same. Moreover, since the number of PPF elements ($2R$ and $2C$) is less than that of the WB sensor ($4R$ and $3C$), the PPF can be implemented in a more area-efficient way.

Fig. 7 illustrates the operation of the PPF sensor with its output voltage waveform. It is driven by anti-phase clocks of f_0 with a voltage swing of V_A. During the charging phase ϕ_1, the capacitor is charged to an intermediate voltage V_C, and the ZC point occurs after one quarter of the driving period ($T/4$). During the discharging phase ϕ_2, the output voltage V_{PPF} is initially boosted to $V_C + V_A$ due to the capacitive coupling and then starts to discharge via $R(T)$. After the discharging phase, a negative boosting also happens at the start of the next phase ϕ_1. Therefore, the signal swing of the PPF sensor can be much larger compared to other RC-based sensors [22].

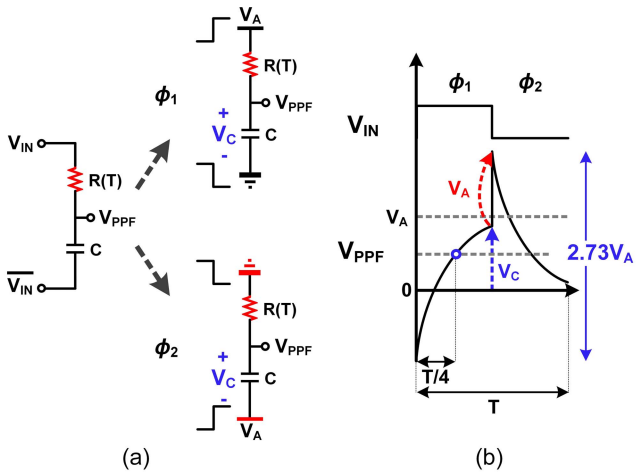

Fig. 7. (a) Operation of the PPF sensor and (b) its output voltage waveform.

Given a square-wave input with duty cycle t_{ON} and period T, the periodic steady-state response V_{PSS} is given by

$$V_{\mathrm{PSS}}(t) = V_A \left\{ 1 - 2e^{-\frac{t}{RC}} \left(\frac{e^{\frac{T}{2RC}}}{1 + e^{\frac{T}{2RC}}} \right) \right\} \quad (0 < t < t_{\mathrm{ON}})$$
$$= 2V_A \cdot e^{-\frac{t}{RC}} \left(\frac{e^{\frac{T}{RC}}}{1 + e^{\frac{T}{2RC}}} \right) \quad (t_{\mathrm{ON}} < t < T). \tag{5}$$

Assuming a 50% duty cycle ($t_{\mathrm{ON}} = T/2$) and a ZC point at $T/4$ ($V_{\mathrm{PSS}}(T/4) = V_A/2$), T can then be expressed as $4RC \cdot \ln(2+\sqrt{3})$. As shown in Fig. 7(b), the output signal swing of the PPF sensor is then $(1 + \sqrt{3})\ V_A \approx 2.73\ V_A$ (single-ended), which is 7× larger than that of the WB sensor. Therefore, the error contribution of the following readout circuitry can be highly reduced.

D. Proposed PPF-Based FLL

Based on the fact that the PPF's phase shift is −90° at f_0, it can be read out by embedding it in an FLL and forcing the phase difference between its ZC output and the quadrature-phase signal of f_0 to be 0. Fig. 8 shows the block and timing diagrams of the proposed PPF-based FLL. The output frequency F_{PPF} of a current-controlled oscillator (CCO) is divided by 4 to provide an in-phase feedback signal (P) for the PPF ($R = 35$ kΩ and $C = 0.5$ pF) and a quadrature-phase signal (Q) for the PFD. The ZC of the sensor output (V_{PPF}) is converted into V_O via the ZC detector, which is implemented by a comparator. As shown in Fig. 8(b), if the phase error ϕ_{DIFF} between V_O and Q occurs, a digital tri-state PFD provides up or down signal into a charge pump (CP), whose output current flows into an integration capacitor (C_{INT}) of the loop filter and controls its output current I_{INT} by a g_m stage. I_{INT} is then adjusted to drive ϕ_{DIFF} to 0. At steady state, F_{PPF} is locked to four times the PPF's center frequency, where the PPF's phase shift ϕ_{LOCK} is 90°.

Since the PPF's phase shift is always less than 180°, the ZC point also occurs within a half duty-cycle. Therefore, the ZC detector can be duty-cycled around the ZC point to reduce its power consumption. The division ratio of the divider can be

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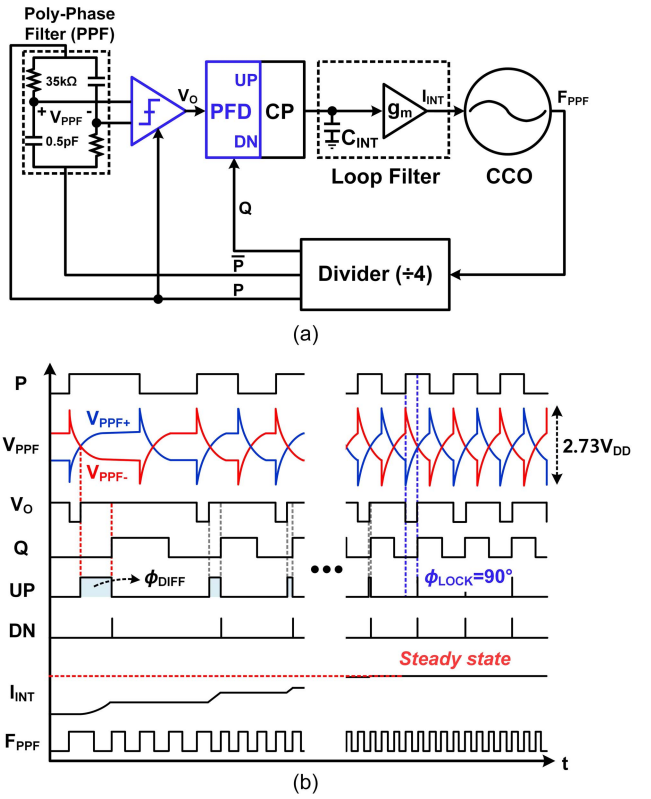

Fig. 8. (a) Proposed PPF-based FLL and (b) its operating timing diagram.

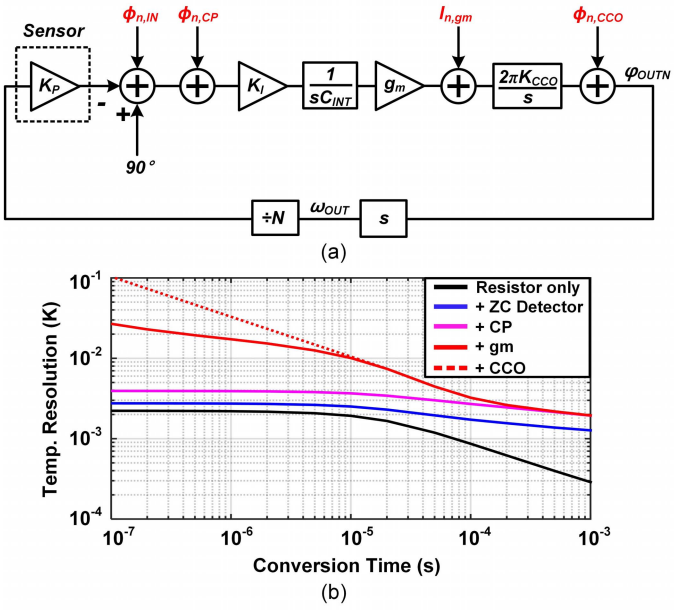

Fig. 9. (a) Small-signal model of the PPF-based FLL and (b) estimated temperature resolution with the model.

designed to be an integer value larger than 4, but this increases the total output noise due to the reduction of the feedback gain [24]. Therefore, we used a divide-by-4 in this paper.

E. Noise Analysis

In order to estimate the temperature resolution of the PPF-based FLL readout, a linearized small-signal model of the FLL is shown in Fig. 9(a), where K_P is the frequency-to-phase gain of the sensor, K_I is the PFD/CP gain, and K_{CCO} is the CCO tuning gain. The front-end noise from the PPF sensor and the ZC detector is defined as the phase noise $\phi_{n,\mathrm{IN}}$, which results from the output-referred voltage noise ($V_{n,R}$) of the sensing resistor and the input-referred voltage noise ($V_{n,\mathrm{ZC}}$) of the ZC detector. The total voltage noise ($V_{n,\mathrm{IN}}$) of the front end is given by

$$V_{n,\mathrm{IN}}^2 = V_{n,R}^2 + V_{n,\mathrm{ZC}}^2. \tag{6}$$

Then, the front-end phase noise can be expressed in terms of this voltage noise and derived from the timing jitter t_d at the sensor output and the sensor's driving frequency f_0 [23]. The jitter is determined by the voltage noise $V_{n,\mathrm{IN}}$ and the slope of the sensor output voltage at the ZC point (i.e., $t = T/4$) and can be calculated by using the derivative dV/dt from (5). Therefore, the front-end phase noise can be calculated as

$$\phi_{n,\mathrm{IN}}^2 = (2\pi f_0 t_d)^2 = \left(2\pi f_0 \frac{dt}{dV} V_{n,\mathrm{IN}}\right)^2 = \frac{V_{n,\mathrm{IN}}^2}{A^2} \tag{7}$$

where A is the peak-to-peak voltage swing of f_0.

At steady state, the output of the PFD will be a short pulse with a duration t_{PFD} that is much smaller than the driving period t_{DRV} [24]. The current noise of the CP ($I_{n,\mathrm{CP}}$) can then be modeled as phase noise as shown in the following:

$$\phi_{n,\mathrm{CP}}^2 = \frac{I_{n,\mathrm{CP}}^2}{I_{\mathrm{CP}}^2} \frac{t_{\mathrm{PFD}}}{t_{\mathrm{DRV}}} \tag{8}$$

where I_{CP} is the output current of the CP.

For simplicity, the phase noise of the front end and the CP is combined into $\phi^2{}_n = \phi^2{}_{n,\mathrm{IN}} + \phi^2{}_{n,\mathrm{CP}}$ at the sensor output. The noise transfer function (NTF) from ϕ_n to F_{OUT} can be calculated as

$$\begin{aligned} H_{\mathrm{IN}}(s) &= \frac{F_{\mathrm{OUT}}(s)}{\phi_n(s)} = \frac{1}{2\pi} \frac{K_I \frac{g_m}{sC_{\mathrm{INT}}} 2\pi K_{\mathrm{CCO}}}{1 + \frac{K_P}{N} K_I \frac{g_m}{sC_{\mathrm{INT}}} 2\pi K_{\mathrm{CCO}}} \\ &= \frac{N}{2\pi K_P} \frac{G(s)}{1+G(s)} \approx \frac{N}{2\pi K_P} \end{aligned} \tag{9}$$

where $G(s)$ is the open-loop transfer function of the FLL. (Thus, $G(s) \gg 1$ near dc.) While ϕ_n is low-pass filtered by its NTF, it can be seen that g_m current noise $I_{n,\mathrm{gm}}$ and the CCO phase noise $\phi_{n,\mathrm{CCO}}$ are high-pass filtered by each NTF (H_{gm} and H_{CCO}). From (6)–(9), the power spectral density (PSD) of the FLL's output frequency noise $S_{\mathrm{FOUT}}(f)$ can be expressed as

$$\begin{aligned} S_{\mathrm{FOUT}}(f) = S_n(f) \cdot |H_{\mathrm{IN}}(f)|^2 + S_{\mathrm{gm}}(f) \cdot |H_{\mathrm{gm}}(f)|^2 \\ + S_{\mathrm{CCO}}(f) \cdot |H_{\mathrm{CCO}}(f)|^2 \end{aligned} \tag{10}$$

where $S_n(f)$, $S_{\mathrm{gm}}(f)$, and $S_{\mathrm{CCO}}(f)$ are the PSDs of the phase noise at the sensor output, the g_m current noise, and the CCO phase noise, respectively. Since an off-chip counter digitizes the FLL's output frequency F_{OUT} by counting the number of the edges of F_{OUT}, it works as a sinc filter with a time length t_{conv}. This means filtering out F_{OUT} with a noise bandwidth of $(2t_{\mathrm{conv}})^{-1}$ [13]. As a result, the RMS frequency noise can be easily calculated by integrating $S_{\mathrm{FOUT}}(f)$ up to the bandwidth.

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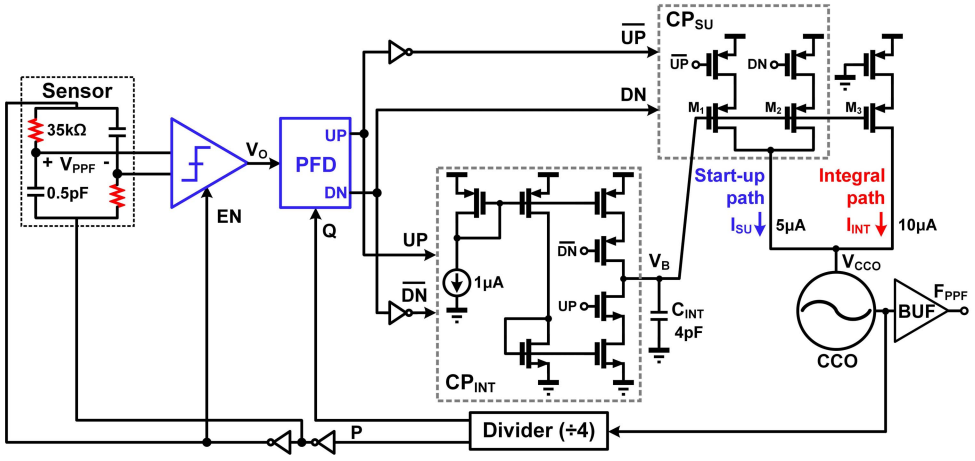

Fig. 10. Block diagram of the PPF-based FLL.

To estimate the achievable temperature resolution of this sensor, a noiseless readout circuit is assumed with the noise bandwidth smaller than the loop bandwidth. Then, the temperature resolution is limited by the sensing resistor's thermal noise. Given that the output-referred voltage noise of the sensor is $V^2_{n,R,\text{out}} = 4\ kTR$, its PSD is folded due to the sampling effect of the PFD [24] as follows:

$$S_{n,R}(f) = \frac{V^2_{n,R}}{A^2} = \frac{2V^2_{n,R,\text{out}}}{A^2} = \frac{8\ kTR}{A^2}. \tag{11}$$

Combining this with (10) and (11), the RMS frequency noise is given by

$$\begin{aligned}\Delta F_{\text{OUT}} &= \sqrt{S_{n,R}(f)\cdot|H_{\text{IN}}(f)|^2}\cdot\sqrt{\frac{1}{2t_{\text{conv}}}} \\ &= \frac{N}{\pi\,\text{AC}}\sqrt{\frac{kT}{t_{\text{conv}}R}}.\end{aligned} \tag{12}$$

The temperature resolution is then calculated by dividing ΔF_{OUT} into its temperature sensitivity. Given that the TC of the resistor is α and the resistance at room temperature is R_0, the resolution ΔT at room temperature is calculated as follows:

$$\begin{aligned}\Delta T &= \Delta F_{\text{OUT}}\cdot\frac{dT}{dF_{\text{OUT}}} = \frac{N}{\pi\,\text{AC}}\sqrt{\frac{kT}{t_{\text{conv}}R_0}}\cdot\frac{2\pi R_0 C}{N\alpha} \\ &= \frac{2}{\alpha A}\sqrt{\frac{kTR_0}{t_{\text{conv}}}}.\end{aligned} \tag{13}$$

In the actual design, the PPF sensor is implemented with $R_0 = 35$ kΩ and $A = 1$ V. As shown in Fig. 9(b), a PPF sensor based on silicided p-poly resistors has a fundamental temperature resolution of 288 μK_{rms} at $t_{\text{conv}} = 1$ ms. In practice, the temperature resolution is degraded by the noise added by the following blocks: the ZC detector, the CP, the g_m stage, and the CCO. Since their NTFs are formed by the FLL, the noise of g_m stage and the CCO and the front-end noise are high-pass and low-pass filtered, respectively. Now, consider an estimated loop bandwidth of 20 kHz, which is equivalent to a conversion time of 25 μs. Then, at $t_{\text{conv}} > 25$ μs, the resolution is limited by $1/f$ noise of the ZC detector and the CP. In the opposite case, the thermal noise of CCO and $1/f$ noise of g_m stage are dominant sources of the total noise. Consequently, the resolution is estimated to be 1.95 mK_{rms} at $t_{\text{conv}} = 1$ ms.

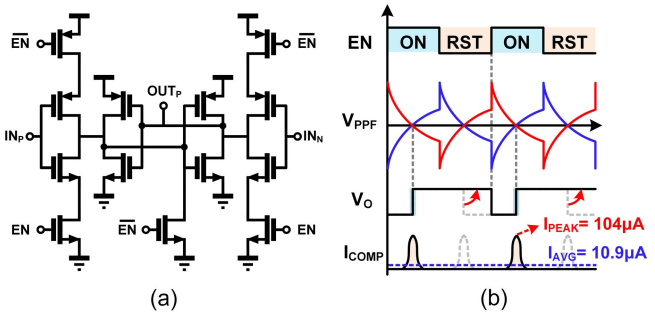

Fig. 11. (a) Schematic of the ZC detector and (b) its operating principle.

IV. Implementation

Fig. 10 shows the full block diagram of the proposed PPF-based FLL readout. The loop filter of the readout circuits consists of a push–pull CP (CP_{INT}), a push-type CP (CP_{SU}), an integration capacitor C_{INT}, and a g_m. In Sections IV-A–IV-C, each block will be described in detail.

A. ZC Detector

Fig. 11 shows the schematic of the ZC detector. It is implemented as a two-stage inverter-based comparator to facilitate scaling in advanced processes [25]. Two inverters serve as a preamplifier, which then drives a cross-coupled latch. As shown in Fig. 11(b), the output voltage V_{PPF} of the PPF sensor is only sampled on the rising edge of quadrature-phase signal Q in Fig. 8(b). Then, to reduce the power consumption, the ZC detector can be disabled and reset by turning off the first stage. Therefore, its averaged current can be reduced from 20.5 to 10.9 μA. Moreover, the periodic switching of both the enable and reset switches can reduce the $1/f$ noise of the input transistors [26]. From simulations, the input-referred noise is reduced from 38.26 to 8.76 μV_{rms}.

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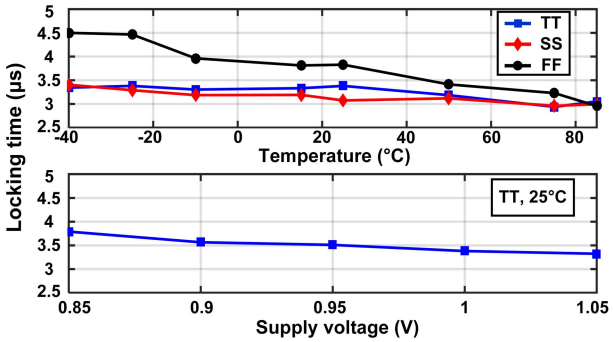

Fig. 12. Simulated locking time across the PVT variations.

For the silicided p-poly sensor with a 1-ms conversion time, it improves temperature resolution from 6.48 to 1.95 mK_{rms}, thus leading to the high resolution. From Monte Carlo simulations, the variation of the offset voltage is ±12.5 mV, which translates into a temperature inaccuracy of ∼0.06 °C (3σ) after digital calibration, as will be described in Section V-B. Since the PPF's output peak voltage is about 1.87× the supply voltage, it can exceed the maximum gate voltage allowable at the detector's input transistors. So, the supply voltage of this paper is limited to 1.05 V in the chosen process. To accommodate higher supplies, the input transistors should be realized with thick-oxide devices.

B. Loop Filter

The schematic of the loop filter combined with the CCO is shown in Fig. 10. The loop filter is composed of a startup path and an integral path. To start the current-starved oscillator, a pull-up circuit is implemented in a push-type CP (CP_{SU}), which avoids mismatch by using only PMOS current sources [27]. Moreover, the startup path (I_{SU}) reduces the locking time of the loop from power-ON–reset condition, which is important for dense thermal monitoring. Consequently, the locking time (cycle) is decreased by 2× from ∼6.8 (70 cycles) to ∼3.4 μs (35 cycles). As shown in Fig. 12, the locking time (cycle) varies between ∼3 (20 cycles at 75 °C of SS corner) and ∼4.5 μs (90 cycles at −40 °C of FF corner) across the process, voltage and temperature (PVT) variations.

The CP of the integral path, CP_{INT}, controls the bias voltage V_B across C_{INT} to generate I_{SU} and I_{INT} (5 and 10 μA at steady state) via PMOS transistors (M_1–M_3). Then, both currents are summed at the CCO's supply node (V_{CCO}). Depending on the PFD state, i.e., up, reset, and down, I_{SU} is weighted by 2, 1, and 0, respectively. This is performed by two switches that are controlled by the PFD outputs ($\overline{UP}$ and DN). Since I_{SU} is generated from CP_{INT}, it works as an added g_m (120 μS) and increases the loop bandwidth to about 20 kHz, reducing the CCO phase noise effectively. From Monte Carlo simulations, matching error between two current sources of CP_{INT} is ±3.5%, which translates into a temperature inaccuracy of ∼0.04 °C (3σ) after digital calibration, as will be described in Section V-B.

C. CCO

As shown in Fig. 13, the CCO is designed as a nine-stage current-starved ring oscillator, whose tuning gain

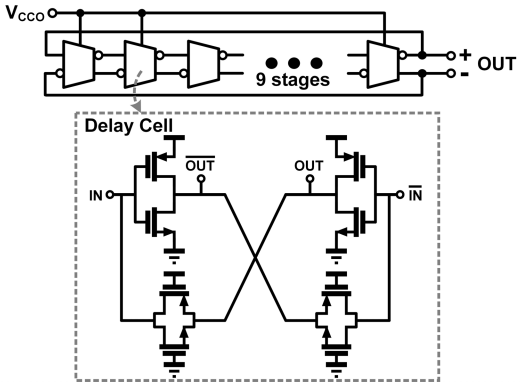

Fig. 13. Schematic of the CCO and its delay cell.

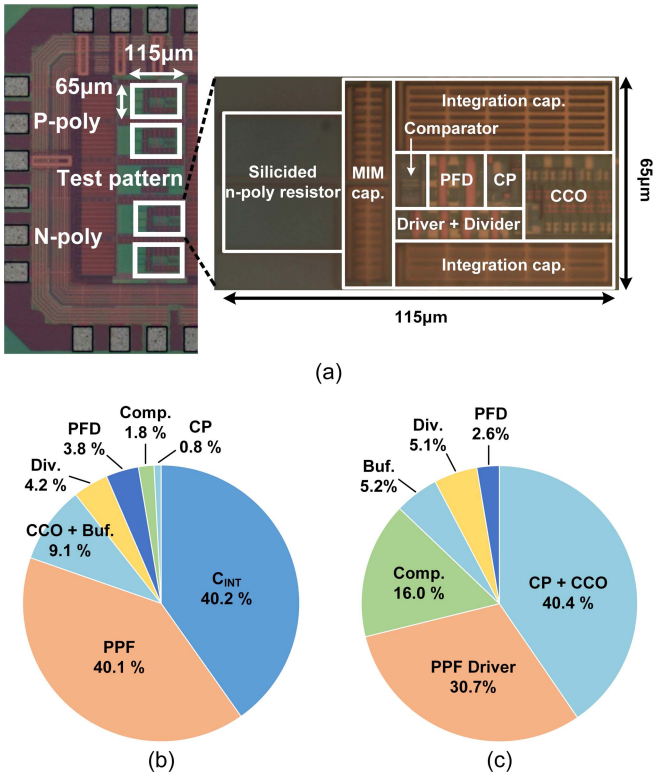

Fig. 14. (a) Micrograph of the temperature sensor. (b) Area breakdown. (c) Power breakdown.

K_{CCO} is 1 MHz/μA. It achieves the target output frequency range from 38 to 52 MHz for both silicided n-poly and p-poly sensors. Its delay cell consists of two inverters cross-coupled with each other in a feed-forward manner using transmission gates, which attenuates the common-mode signals by ensuring pseudo-differential operation [28]. As shown in Fig. 10, following the CCO output, the output buffer achieves rail-to-rail operation and 50% duty cycle via a level-shifter and an inverter-based latch, respectively.

V. Measurement Results

The sensor is fabricated in 65-nm standard CMOS technology, and the chip micrograph is shown in Fig. 14(a). For flexibility, a counter, a digital back end, and current bias circuits were implemented off-chip. Each sample contains

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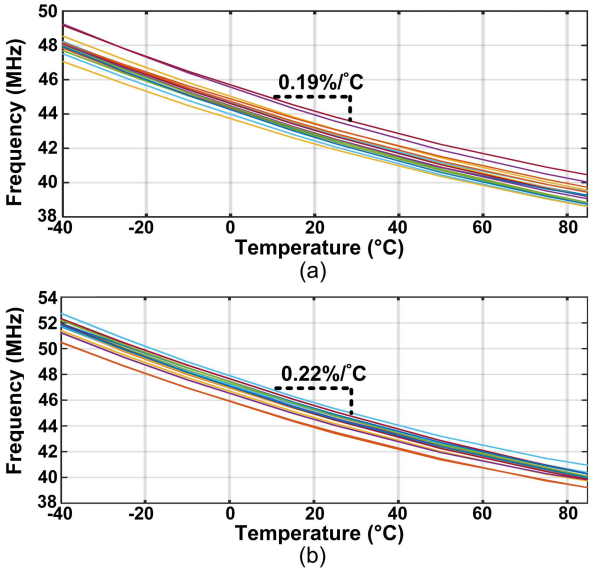

Fig. 15. Measured output frequency of (a) s-n-poly sensor and (b) s-p-poly sensor over temperature.

two different sensors: one with silicided p-poly (s-p-poly) resistors and the other with silicided n-poly (s-n-poly) resistors, shown in [18]. We use an off-chip bias current and the current is copied to each sensor. The current is set at room temperature, and the sensor's temperature inaccuracies are measured by using the fixed bias current. When an on-chip bias current is used, changes in bias current might affect the mismatch between the CP's up and down current, which causes temperature inaccuracy. Assuming the use of a simple bootstrapped current source [30] with a 4% spread, this results in a temperature inaccuracy of 10 mK after a two-point trim. Therefore, its impact is negligible. For both sensors, 16 samples in ceramic dual in-line packages are characterized from −40 °C to 85 °C in a temperature-controlled oven, in which the actual temperature of the sensor is established by a platinum Pt-100 resistor sensor. Each sensor occupies only the active area of 7000 μm^2, 40% of which is occupied by the PPF sensor, as shown in Fig. 14(b). It draws 68 μA from a 1-V supply, and its power breakdown is also described in Fig. 14(c). The CCO with the loop filter and the PPF driver dissipate about 71% of the power consumption. At room temperature, a supply sensitivity of 0.5 °C/V is measured for supply voltages from 0.85 to 1.05 V.

A. Noise and Temperature Resolution

Fig. 15 shows the measured sensors' output frequencies: 48–38 MHz for s-n-poly sensors (0.19%/°C) and 52–40 MHz for s-p-poly sensors (0.22%/°C), respectively. Since the TC of s-p-poly sensor is about 15% higher than that of s-n-poly sensor, it can be seen that the resolution of s-p-poly sensor is better than that of s-n-poly sensor. Fig. 16 shows the measured phase noise of FLL's output (s-n-poly sensor) with the estimated noise contributions of the front end, CP, g_m, and CCO. With the loop bandwidth of 20 kHz, it can be seen that the CCO and

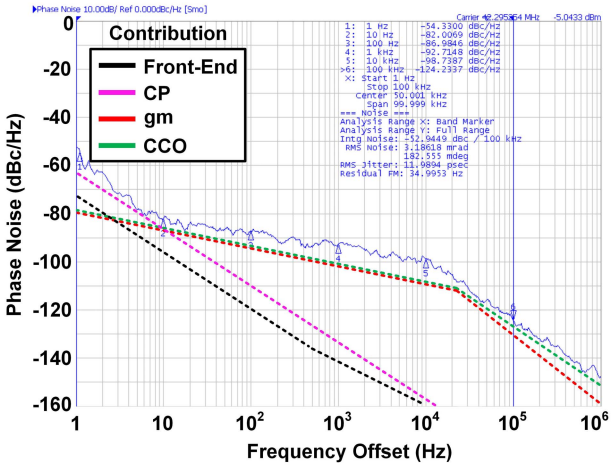

Fig. 16. Measured phase noise of the FLL's output.

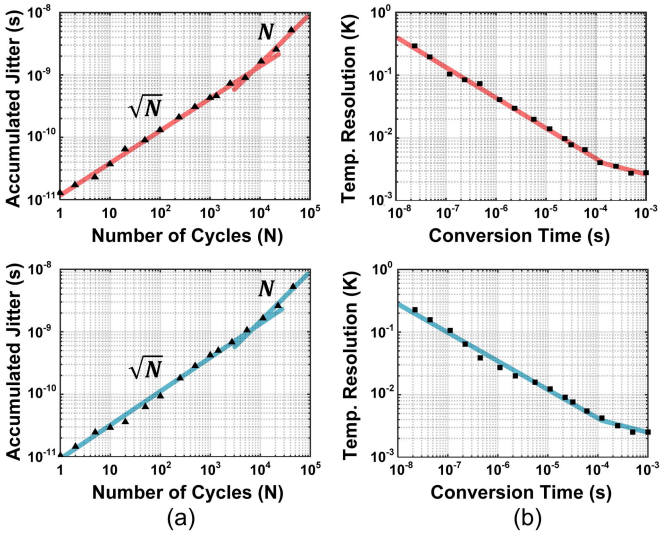

Fig. 17. (a) Measured accumulated jitter versus the number of cycles and (b) measured temperature resolution versus conversion time for s-n-poly sensor (top) and s-p-poly sensor (bottom).

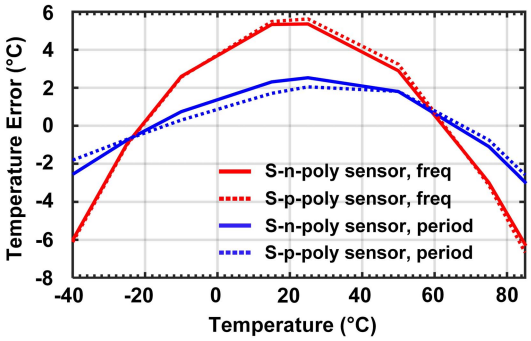

Fig. 18. Measured systematic temperature non-linearity.

g_m noise are high-pass filtered, and the front end and the CP noise are low-pass filtered. The measured phase noise is −124 dBc/Hz at 100 kHz offset, and the RMS jitter integrated from 1 Hz to 100 kHz is 12 ps. As shown in Fig. 17, the accumulated jitter for both sensors is plotted versus the

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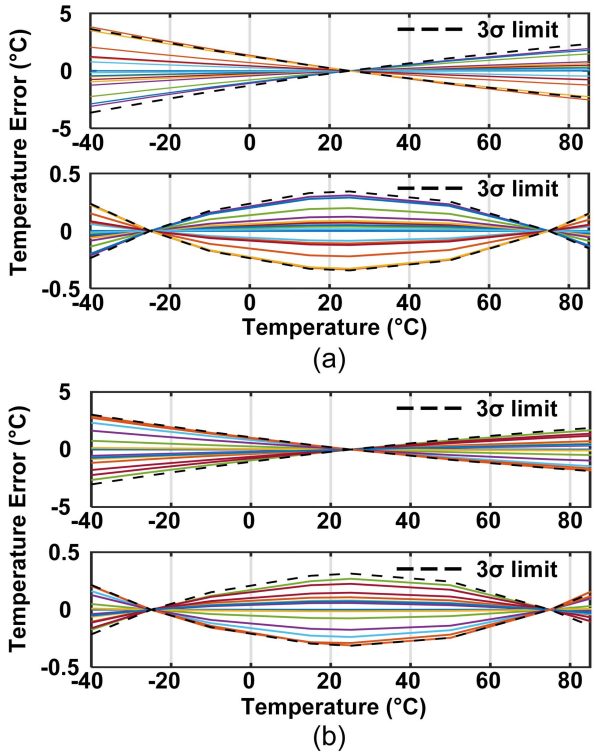

Fig. 19. Temperature error of (a) s-n-poly sensor and (b) s-p-poly sensor after one-point trim (top) and two-point trim (bottom) with the removal of the systematic non-linearity following a 1st-order frequency-fit.

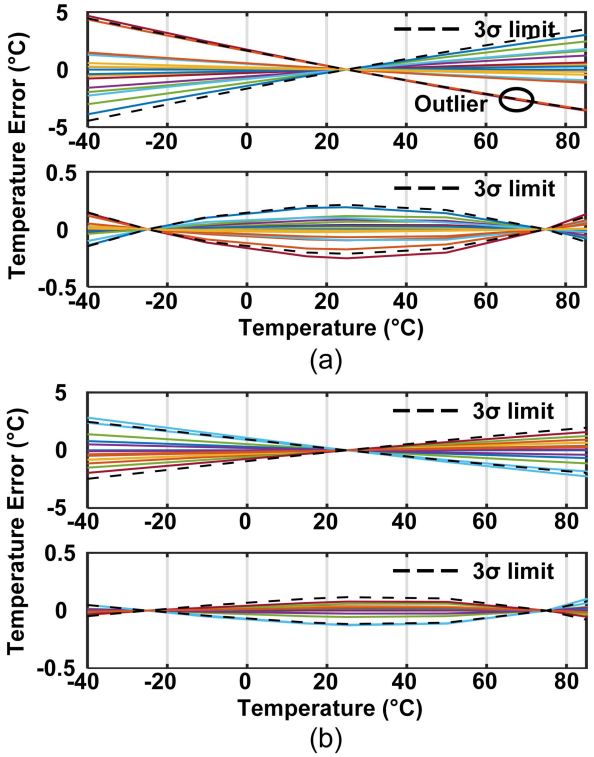

Fig. 20. Temperature error of (a) s-n-poly sensor and (b) s-p-poly sensor after one-point trim (top) and two-point trim (bottom) with the removal of the systematic non-linearity following a 1st-order period-fit.

number of cycles, and it can be measured in a fixed time window corresponding to a conversion time. The accumulated jitter increases up to 10^4 cycles with $\sqrt{N}$ behavior due to thermal noise, while showing N behavior by the $1/f$ noise after the cycles. The temperature resolution is determined by the accumulated jitter and the TC of the output period within the operating temperature range, as shown in Fig. 17(b). For a 1-ms conversion time, the accumulated jitters of 5.2 ns (rms) for s-n-poly sensor and 5.23 ns (rms) for s-p-poly sensor are measured, which correspond to the temperature resolutions of 2.8 and 2.5 mK_{rms}, respectively. Therefore, the sensor can track millisecond thermal transient with a few millikelvin temperature resolutions.

There are several ways to digitize an oscillator's output [1], [8], [9], [13], [20]. Considering an on-chip counter driven by a lower reference frequency, the sensor's output frequency can be digitized by using one or more clock cycles to determine the gating time of the counter. For instance, given a 1-ms gating time of the counter, the quantization noise can be translated to a temperature noise of about 3 mK (rms), in which case, the temperature resolution of the sensor may be limited by quantization noise. However, the quantization noise can also be reduced by using the CCO's multi-phase information as in [13].

B. Systematic Non-Linearity Correction and Calibration

The PPF sensor's output frequency is directly affected by the sensing resistor and the MIM capacitor. Since the MIM capacitor's TC is very low (~15 ppm/°C), the resistor's TC mainly determines the sensor's temperature dependence. As described in Section III-B, however, the resistors have a non-linear temperature dependence, which leads to increased inaccuracy and needs to be removed. After a 1st-order linear fit of the sensor's output frequency, only the systematic non-linearity remains, as shown in Fig. 18. Then, it is fit with a fixed polynomial (fifth-order) function [14]. Thus, the non-linearity function is corrected from the measured output in the digital back end, and the linearly calibrated output can be finally obtained.

As shown in Fig. 19, after one- and two-point trim with the removal of the systematic non-linearity, the s-n-poly sensor achieves a 3σ inaccuracy of ±3.65 °C and ±0.35 °C, while the s-p-poly sensor achieves a 3σ inaccuracy of ±3 °C and ±0.31 °C. It should be noted that the output frequency of the FLL is proportional to $1/RC$ and thus the systematic non-linearity of the resistor also appears inversely at the output. This makes the non-linearity of the output much larger than that of the resistor and interferes with a precise 1st-order linear fit. As a result, the sensor's spread with larger non-linearity further increases the inaccuracy. However, since the output period of the FLL is directly proportional to RC, the remaining non-linearity after a 1st-order period-fit is less than that after a 1st-order frequency-fit for both sensors, as shown in Fig. 18. As shown in Fig. 20, the resulting inaccuracy after one- and two-point trim following the proposed period-fit has decreased to ±2.47 °C (3σ) and ±0.12 °C (3σ) for s-p-poly sensor. The spread sources of s-p-poly sensor's inaccuracy consist of 50% for the offset voltage of the ZC

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TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER STATE-OF-THE-ART WORKS

	This work	JSSC15 Park [13]	ISSCC18 Pan [16]	VLSI14 Horng [20]	ISSCC17 Yang [9]	JSSC15 Oshita [3]	ISSCC16 Sonmez [2]
Sensor Type (Configuration)	**Resistor (PPF)**	Resistor (WB)	Resistor (WhB)	Resistor (Single)	MOS	BJT	TD
Readout Type	**FLL**	FLL	ΔΣ	OSC	OSC	ΔΣ	ΔΣ
Technology	**65nm**	180nm	180nm	16nm	180nm	14nm	40nm
Area (μm^2)	**7000** (†7700)	90000	250000	15000	8865	8700	1650
Power (μW)	**68**	31	94	70	0.075	1100	2500
Supply voltage (V)	**0.85–1.05**	3.3	1.6–2	0.7	0.8–1.8	1.35	0.9–1.2
Supply sensitivity (°C/V)	**0.5**	0.4	0.02	-	0.13	-	2.8
Temperature range (°C)	**-40 to 85**	-40 to 85	-55 to 125	-10 to 90	-20 to 100	0 to 100	-40 to 125
Inaccuracy (°C)	**±0.12**** **(3σ)**	±0.12*** (p-p)	±0.12** (3σ)	±1** (3σ)	-0.22/0.19** (3σ)	±0.7** (3σ)	±0.75* (3σ)
Conversion time (ms)	**1**	32	5	1.6	8	0.02	1
Energy/Conversion (nJ)	**68**	992	470	112	0.6	22	2500
Resolution (°C)	**0.0025**	0.0028	0.00026	1	0.073	0.5	0.36
Resolution FoM (pJ·K^2)	**0.43**	8	0.032	112000	3.2	5500	324000

† Estimated area including on-chip bias and 16-bit counter in the chosen process
* 1-point trimming, ** 2-point trimming, *** 3-point trimming
Resolution FoM = Energy/conversion × (Resolution)^2

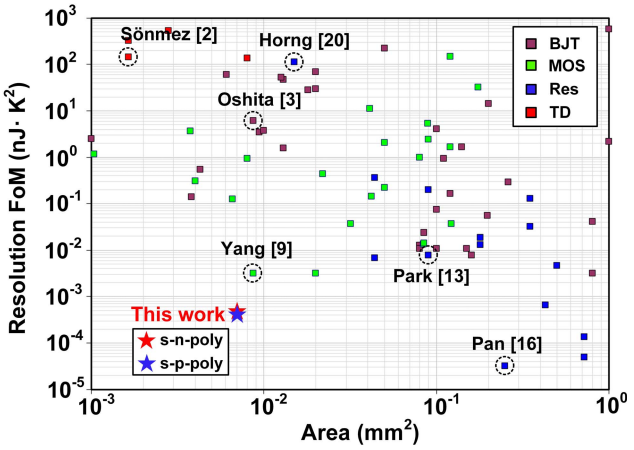

Fig. 21. Resolution FoM versus area for CMOS smart temperature sensors.

detector, 33.3% for the CP mismatch, 12.5% for the resistor mismatch, and 4.2% for other blocks. For the s-n-poly sensor, the 3σ inaccuracy after a one-point trim has increased to ±4.5 °C due to an outlier, while decreasing to ±0.21 °C after a two-point trim [Fig. 20(b)]. This confirms that the period-fit can be effective for both sensors.

C. Comparison to Previous Work

The performance of the sensor based on the s-p-poly resistors is summarized in Table II and compared to other compact energy-efficient CMOS temperature sensors. After a two-point trim, the sensor achieves an inaccuracy of ±0.12 °C (3σ), which is comparable to that of state-of-the-art sensors. It achieves a competitive energy-efficiency of 0.43 pJ·K^2, only occupying the area of 7000 μm^2. Even if the estimated area of the on-chip bias and counter in the chosen process is considered, the total area would be 7700 μm^2. As shown in Fig. 21, this work is 13× smaller than a WB-based FLL sensor [13] and significantly smaller than a WhB-based sensor with CTDSM [16]. Due to the supply-voltage scaling and improved jitter performance, the resolution FoM of this work is also highly improved by 18× compared to [13]. The size of this work is very close to that of a compact MOS-based sensor [9], while achieving 7× improvement on energy-efficiency. Compared to the state-of-the-art TD- and BJT-based sensors [2], [3], this sensor consumes significantly less energy.

VI. CONCLUSION

A resistor-based CMOS temperature sensor for on-chip thermal monitoring has been implemented in a standard 65-nm CMOS technology. It is based on a PPF implemented with silicided poly resistors and stable MIM capacitors, which provides small area, high TC, and large-signal swing. The PPF's temperature-dependent phase shift is effectively measured with a ZC detector, which allows implementing an area- and energy-efficient FLL. The prototype sensor occupies only 7000 μm^2, the smallest among all the resistor-based temperature sensors, and also operates at supply voltages from 0.85 V. The sensor has been characterized with two different resistors (s-p-poly/s-n-poly). The sensor based on the s-p-poly resistors achieves a resolution of 2.5 mK$_{\text{rms}}$ in a 1-ms conversion time, corresponding to a competitive resolution FoM of 0.43 pJ·K^2. After a two-point calibration, the sensor achieves an inaccuracy of ±0.12 °C (3σ) from −40 °C to 85 °C, which is also comparable to the state-of-the arts. These results demonstrate that the proposed resistor-based sensor is suitable for realizing a reliable temperature sensor for dense thermal monitoring in nanometer CMOS.

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