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Chapter 6
A Hybrid ADC for High Resolution: The Zoom ADC

Burak Gönen, Fabio Sebastiano, Robert van Veldhoven, and Kofi A. A. Makinwa

6.1 Introduction

Digital audio systems require high-resolution and high-linearity ADCs to digitize analog signals with high dynamic range. In today's system on chips (SoCs), such ADCs are typically integrated with digital signal processing blocks, thus forcing both to be realized in nanometer CMOS technology. Due to the relatively high silicon cost of such technologies, ADC area then becomes an important component of product cost. Moreover, the trend toward more mobile and wearable applications poses stringent constraints on the available power/energy. Thus, ADCs for digital audio systems should be both area and energy efficient.

Sigma-delta modulators (SDMs) are often employed in audio applications because they can achieve excellent linearity, even without calibration. However, compared to Nyquist-rate ADCs, which are typically less linear or require extensive calibration, SDMs are somewhat less energy efficient [13, 14]. To improve energy efficiency, recent ADCs have combined elements of Nyquist-rate and SDM architectures [1–6]. Such hybrid ADCs try to address the inability of both Nyquist-rate and SDM architectures to simultaneously achieve wide dynamic range, high resolution, and high accuracy, in an efficient manner. To do this, they typically split their input range into coarse and fine segments, each of which can be converted by different sub-ADCs that are optimized to handle the dynamic range of the different segments. The challenge then lies in combining the results of these conversions efficiently and accurately.

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In this paper, we describe a dynamic zoom ADC [10, 11], i.e., a hybrid ADC that consists of a compact and efficient coarse SAR ADC and an accurate and high-resolution fine discrete-time SDM (DT-SDM). The hybrid ADC achieves 109-dB dynamic range (DR), 106-dB signal-to-noise ratio (SNR), and 103-dB signal-to-noise-and-distortion ratio (SNDR) in a 20-kHz bandwidth, while dissipating 1.12 mW and occupying only 0.16 mm^2 in a 0.16-μm CMOS process.

The paper is organized as follows: first, the energy and area efficiency of high-resolution high-linearity ADCs is discussed (Sects. 6.2 and 6.3). This is followed by an overview of hybrid ADC architectures (Sect. 6.4). The zoom ADC and its system-level design are then introduced (Sect. 6.5), followed by its circuit design (Sect. 6.6). Finally, experimental results are presented (Sect. 6.7), followed by conclusions.

6.2 Energy Efficiency of High-Resolution DT-SDMs

The energy efficiency of an ADC is measured in terms of its energy per conversion E_{conv}, i.e., the energy spent by the ADC to produce an output sample. Figure 6.1 shows E_{conv} for ADCs published in recent years [14]. For low-resolution ADCs with N output bits, the energy per conversion is often limited by the energy required to compute the N output bits, thus E_{conv} scales with the number of conversion steps, i.e., $E_{conv} \propto 2^N$. For high-resolution ADCs, i.e., ADCs with >75-dB DR, the energy per conversion is limited by the need to achieve sufficiently low thermal noise, which requires a quadratic increase of energy for each additional quantization step ($E_{conv} \propto 2^{2N}$) [13]. Consequently, ADC power consumption will scale with DR. This consideration leads to the definition of the Schreier figure of merit (FoM_S) [12]:

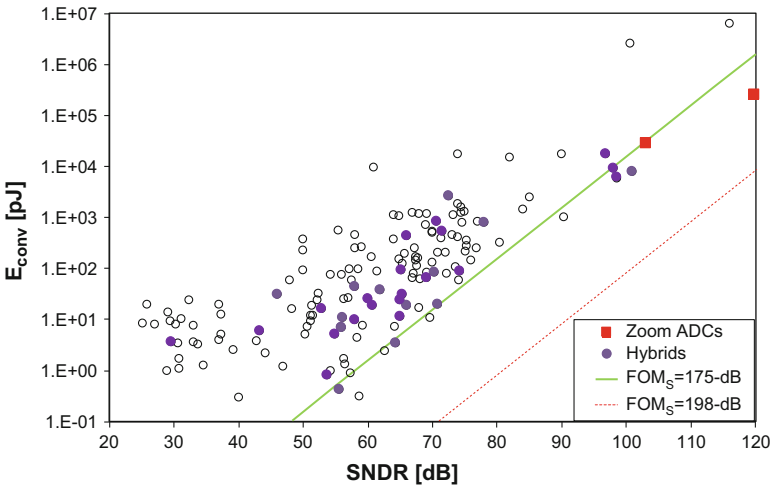


Fig. 6.1 SNDR vs energy per conversion of ADCs (2012–2017) [14]

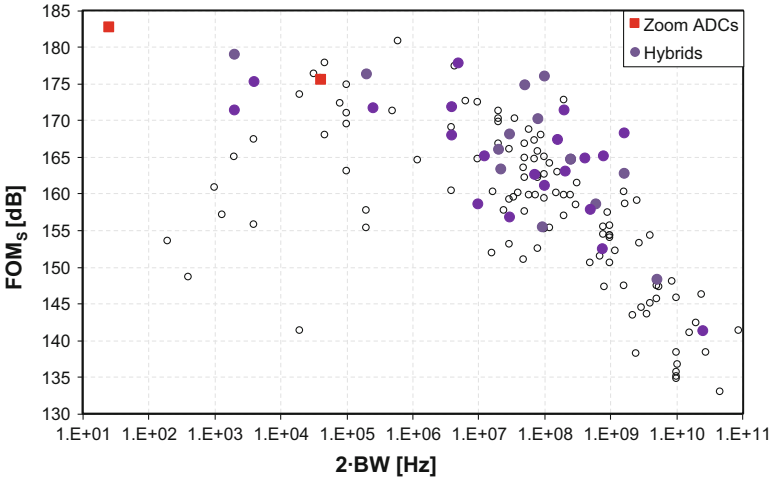


Fig. 6.2 Signal bandwidth vs $\mathrm{FoM_s}$ of ADCs (2012–2017) [14]

$$\mathrm{FoM_s} = DR + 10 \cdot \log_{10} \frac{f_{bw}}{P} \ [dB] \tag{6.1}$$

where DR is the dynamic range in dB, f_{bw} is the ADC bandwidth, and P is the ADC power consumption. Sometimes $\mathrm{SNDR_{max}}$ is used instead of DR, e.g., as in [14], because the former is usually worse than the latter. Energy efficiency is also difficult to combine with high speed, as shown in Fig. 6.2, which reports $\mathrm{FoM_S}$ vs input bandwidth for ADCs published in recent years [14]. $\mathrm{FoM_S}$ is higher for low and moderate bandwidths (0–10 MHz). It can be shown that a 198-dB $\mathrm{FoM_S}$ is theoretically achievable [15], which means that there is still an approximately 20-dB gap between this limit and the current state of the art (Fig. 6.1).

The reason for this gap lies in the implicit assumption behind the definition of $\mathrm{FoM_S}$, i.e., that most of an ADC's power consumption is used in its input stage to reduce thermal noise. In practice, however, this is not the case. First, other ADC subblocks consume a non-negligible amount of power. In a DT-SDM, for example, such subblocks will include the integrators that follow the input stage, the quantizer, the biasing circuits, and the digital back end. Second, even the power consumption of the input stage is often not limited by thermal noise but by other requirements such as linearity, slew rate, and settling time.

Bearing this in mind, it is then clear that to maximize $\mathrm{FOM_S}$, a number of different design strategies can be adopted. First, the power consumption of all ADC subblocks, especially that of the critical input stage, should be reduced. Several recent works have targeted improvements in the efficiency of the amplifiers used in the SDM loop filters. Various inverter-based amplifiers have been proposed [1, 10, 16–22] which double efficiency by summing the transconductances of NMOS and PMOS transistors biased by the same current. A further improvement is achieved in

[19] by stacking multiple inverters and adopting a high-supply-voltage technology. As a second design strategy, the chosen ADC architecture must maximally relax all requirements on the input stage apart from those related to thermal noise. For example, the use of multi-bit quantization reduces the signal swing processed by the loop filter and thus relaxes the input stage's slewing and settling time. However, to avoid excess loop delay, this often involves the use of quantizers based on power-hungry flash ADCs. Furthermore, fast and power-hungry digital logic is needed to implement the dynamic element matching techniques needed to guarantee linearity. Thus, efficient multi-bit quantization schemes are required.

6.3 Area Efficiency of High-Resolution ADCs

A similar approach can be used to analyze ADCs from an area efficiency perspective. Most of their silicon area should then be used to ensure low enough thermal noise. However, since the matching of integrated components scales with the square root of their area, i.e., two times more accuracy requires four times larger area, the accuracy requirements on active and passive components also impose a lower limit on the silicon area [20]. This implies that in a DT-SDM the total area should ideally be dominated by thermal-noise-critical and matching-critical components, such as sampling capacitors, the first integrator, and the DAC.[1] It should also be noted that over-sampling effectively reduces the in-band thermal noise in an ADC, hence relaxing the area requirement of the noise-critical capacitors for the same DR. Although good for area efficiency, over-sampling comes at the expense of increased power consumption in the quantizer and in the digital back end.

However, components not limiting noise or accuracy will also occupy a non-negligible chip area. For example, SDMs with multi-bit quantizers usually suffer an area penalty due to the quantizer's exponentially increasing area [20]. Furthermore, not all passives are sized for thermal noise or accuracy requirements. For example, the size of the integration capacitors in the switched-capacitor (SC) integrators of a DT-SDM is determined by the choice of loop-filter coefficients and the desired integrator output swing.

Figure 6.3 shows an area vs DR comparison of state-of-the-art audio ADCs [11]. It shows that higher DR indeed corresponds to higher chip area. It should be noted that both device matching and capacitor density (capacitance per unit area, in $F/\mu m^2$) and, hence, the resulting chip area are strongly technology dependent. Technology scaling also helps to reduce the power consumption of the digital logic and the quantizer, thus facilitating, for example, the use of multi-bit SDMs. System-level design should then include a careful choice of the technology in order to exploit the possible presence of high-density passives.

[1] While it is trivial that lower thermal noise requires larger capacitors in DT circuits, this is also true for continuous-time circuits: lower thermal noise implies lower resistances and, consequently, larger capacitors for the same total bandwidth.

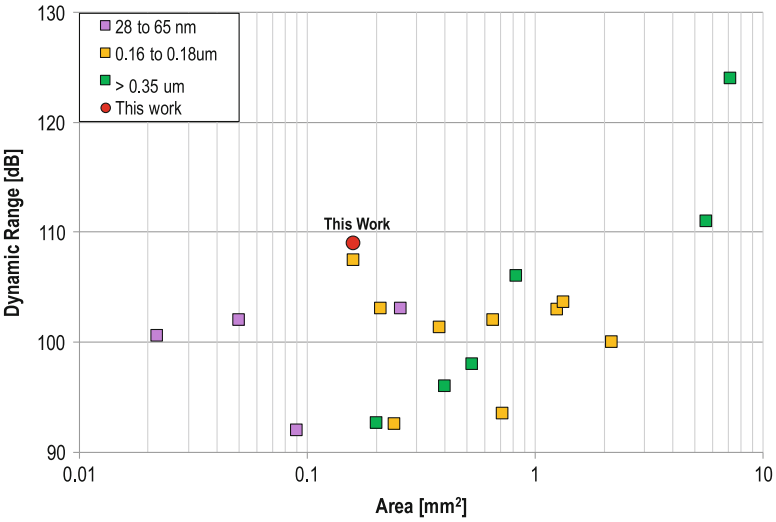


Fig. 6.3 Chip area vs DR for state-of-the-art audio ADCs [11]

To improve the area efficiency of DT-SDMs for a given technology, the following design flow should be followed. First, the over-sampling ratio (OSR) should be increased until the power consumed by the digital back end and the quantizer becomes significant. Second, the architecture should be chosen to reduce the area of system blocks that do not directly determine resolution and accuracy, such as the integration capacitors not in the first integrator, the quantizer, and the digital logic.

6.4 Hybrid ADCs

As mentioned before, most ADC architectures are not energy efficient when high resolution and high linearity are both required. Even conventional SAR ADCs, known for their excellent energy efficiency, suffer under high-resolution requirements due to the increased power consumption of the comparator. Furthermore, some ADC architectures, such as VCO-based converters, exhibit excessive nonlinearity for large input signals, thus limiting their DR [8]. Thus, it is often beneficial to divide the input dynamic range into "manageable" subranges, i.e., coarse and fine ranges, to decouple the problems associated with large signals, low noise, and high accuracy levels. In this way, the challenges of each design space, i.e., "subrange", can be addressed with an appropriately tailored ADC architecture. ADCs based on this approach are called *hybrid ADCs*. It is beneficial to have a close look into a subset of the hybrid ADCs, subranging ADCs, to understand their architectural motivation. Subranging ADCs were originally used to improve the efficiency of flash ADCs for high resolution by dividing the input range into multiple

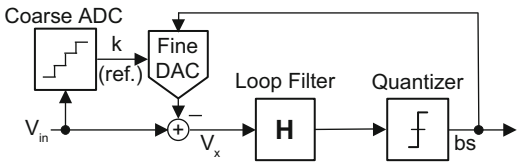


Fig. 6.4 Block diagram of a dynamic zoom ADC

subranges, most commonly into two coarse and fine ranges. However, they suffered from interstage matching, i.e., the coarse converter and the fine converter should have a perfectly matched range. This results in tough requirements on the thermal noise and accuracy of the coarse converter, which, in turn, lead to degraded energy efficiency. For this reason, back-end correction techniques such as redundancy (over-ranging) and/or calibration are often employed to relax the coarse converter's accuracy requirements [15], leading to very efficient designs.

By dividing the full input range into two or more subranges, hybrid two-step architectures in the form of SAR + SAR pipeline [9], SAR + single slope [7], SAR + SDM [1–4, 8], and flash + SDM [5, 6] achieve state-of-the-art energy efficiency, as shown in Figs. 6.1 and 6.2. In addition, their linearity is often improved thanks to the reduction of the signal swing at the input of the linearity-critical fine converter. It is observed that the architectures of the coarse and fine converters are tailored to the desired performance. For low-to-moderate input bandwidths, i.e., not close to the speed limits of the technology used, the coarse converter is often a SAR ADC [1–3, 7–9] due to their compactness and superior energy efficiency. When the speed of the coarse conversion is important, a flash ADC is preferred [5, 6]. In very efficient high-resolution (DR > 75 dB) hybrids, the fine converter is either a SDM [1, 2, 5], an over-sampling SAR [4], or a single-slope ADC [7], to achieve high resolution with maximum efficiency.

The zoom ADC architecture has been proposed for high-resolution and high-linearity applications, in which it simultaneously achieves excellent energy efficiency and small die area [1]. The system block diagram of a zoom ADC is shown in Fig. 6.4. It consists of a coarse ADC and a fine SDM. The coarse ADC's output (k) corresponds to an analog range $k{\cdot}V_{\mathrm{LSB},C} < V_{\mathrm{in}} < (k+1){\cdot}V_{\mathrm{LSB},C}$ where $V_{\mathrm{LSB},C}$ is its quantization step or least significant bit (LSB). The digital value k is then used to adjust, i.e., "zoom in," the references of the SDM's DAC such that $V_{\mathrm{REF}-} = k{\cdot}V_{\mathrm{LSB},C}$ and $V_{\mathrm{REF}+} = (k+1){\cdot}V_{\mathrm{LSB},C}$. These reference voltages straddle the input signal V_{in}, thus ensuring that it lies in the input range of the fine $\Delta\Sigma$M. In contrast to other Nyquist-rate ADC + SDM hybrids, there is no computation of an analog residue signal resulting from the coarse conversion. Instead, only the digital result of the coarse conversion is used to "zoom in" on the signal level. By using a wider fine input range (i.e., over-ranging), the coarse converter's linearity and accuracy can be considerably relaxed. The overall linearity is determined by the fine SDM, in particular by its DAC, whose linearity is then improved by using dynamic element matching techniques.

Like a multi-bit SDM, zooming reduces the signal swing at the input of the SDM, thus relaxing the slewing requirements of the first SDM stage. Its performance will

also be similar to that of a multi-bit SDM with the same OSR, despite the fact that there its multi-bit quantizer is *outside* the SDM loop. Consequently, higher quantizer delays can be tolerated, which means that the coarse converter can be implemented as a compact and efficient SAR ADC.

6.5 Incremental Zoom ADC

The first zoom ADCs were implemented as incremental converters, in which the coarse and fine conversions were performed sequentially [1, 2, 23]. The time-domain operation of an incremental zoom ADC is shown in Fig. 6.5. The conversion starts with a SAR phase to quickly determine the correct zoom range, followed by a fine 1-bit SDM phase that uses the nearest two reference levels to accurately determine the final digital value. This approach works well for quasi-static signals, such as those encountered in sensor readout [2, 23], or instrumentation applications [1], but it does not work for dynamic signals.

The time-domain operation of an incremental zoom ADC with a dynamic (time-varying) signal is shown in Fig. 6.6. After the SAR period, the ADC will assume that the chosen reference values are valid throughout the whole fine conversion. However, this is not true for dynamic signals, leading to modulator overload. Thus, the maximum input signal frequency will be limited to when assuming a 1-LSB_C (coarse LSB) of fine input range, i.e., no over-ranging:

$$f_{\text{in,max}} < \frac{f_s}{2\pi \cdot \text{OSR} \cdot 2^N} \tag{6.2}$$

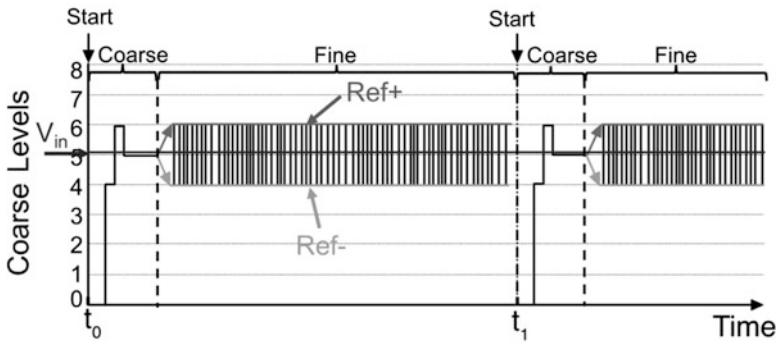


Fig. 6.5 Time-domain operation of an incremental zoom ADC with a static input. Showing the SAR ADC's comparator output during the coarse period, and the SDM's bitstream during the fine period

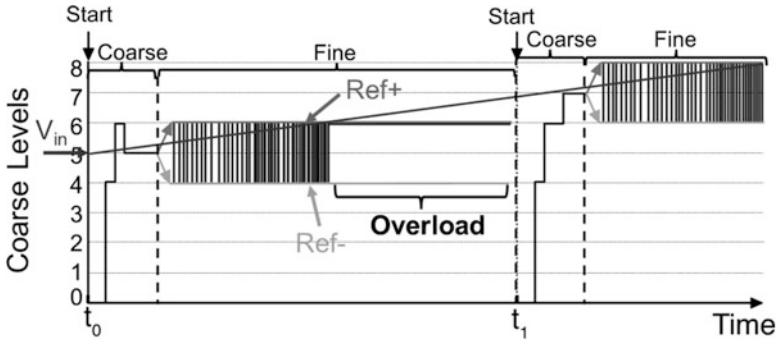


Fig. 6.6 Time-domain operation of an incremental zoom ADC with a dynamic input. Showing the SAR ADC's comparator output during the coarse period, and the SDM's bitstream during the fine period

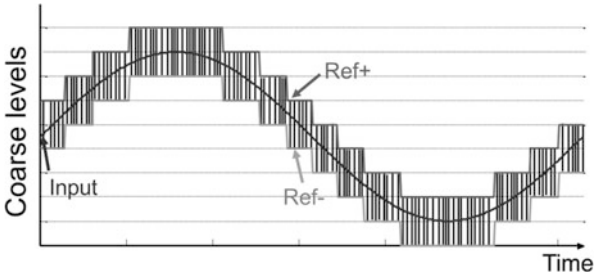


Fig. 6.7 Time-domain operation of a dynamic zoom ADC

where f_S is the sampling frequency, OSR is the over-sampling ratio of the zoom ADC, and N is the coarse ADC's number of bits. Thus, this architecture is only well suited to the conversion of quasi-static signals.

6.5.1 Dynamic Zoom ADC

In order to achieve greater input bandwidth, a *dynamic* zoom ADC is proposed in which the coarse and fine conversions are performed concurrently, i.e., in parallel [10, 11]. The time-domain operation of a dynamic zoom ADC with a sinusoidal input is shown in Fig. 6.7. The SDM references Ref + and Ref- then track the input signal fast enough to ensure that they always straddle it. The maximum input bandwidth for a dynamic zoom ADC is then

$$f_{\text{in,max}} < \frac{f_{\text{coarse}}}{2\pi \cdot 2^N} \tag{6.3}$$

where f_{coarse} is the coarse ADC sampling frequency, which is an integer fraction of f_S, i.e., f_S/N for an N-bit SAR ADC or f_S for a flash ADC. Compared to its

incremental counterpart, the maximum input frequency of the dynamic zoom ADC is not a function of the SDM's OSR, thus allowing the use of a large OSR with the associated benefits in terms of resolution and area occupation.

6.5.2 A Dynamic Zoom ADC for Digital Audio

A prototype dynamic zoom ADC for digital audio has been designed as a proof of concept. The targeted specifications are 106-dB SNR and SNDR higher than 100 dB in the 20-kHz audio bandwidth with 1.25 V_{rms} input range. The chosen process technology is 0.16-μm CMOS. The system-level design starts with architectural choices. For a dynamic zoom ADC, these include the choice of the following parameters: F_s (OSR), coarse ADC resolution, coarse ADC redundancy (over-ranging), SDM loop-filter structure and order, and SDM quantizer resolution.

6.5.3 The SDM: OSR, Loop Filter, and the Quantizer

The efficiency of a SDM is, to first order, independent of its OSR. Increasing OSR is desirable to reduce the signal-to-quantization-noise ratio (SQNR) and the chip area and increase $f_{in,max}$ in (6.3). However, the power consumption of the digital sections (DEM, SAR controller, clocking) increases proportionally with the SDM sampling frequency f_s and, consequently, proportionally with OSR. For the chosen 0.16-μm CMOS technology, system simulations revealed that 11.2896 MHz (audio standard), corresponding to OSR = 282, is a good compromise between chip area, $f_{in,max}$, and digital power consumption.

For high energy efficiency, a thermal-noise limited SNR is desired, i.e., the quantization noise should be much less than the thermal noise. To achieve the targeted thermal-noise limited 110-dB SNR, SQNR = 130 dB is chosen. The zoom ADC's total SQNR is determined by the coarse resolution and the SDM's SQNR. The last depends on its loop-filter order, the quantizer resolution, and the OSR. Zooming relaxes the SQNR requirement of the SDM by reducing its input range. Thus, more than 1-bit quantization in the loop is not necessary.

To determine the loop-filter order of the SDM, Fig. 6.8 shows the $SQNR_{max}$ (for an ideal loop filter) as a function of the OSR for a zoom ADC with a 1-bit SDM quantizer and a coarse SAR ADC with 3–5 bits, for different loop-filter orders [12]. It is observed that for each increased bit in the coarse ADC, $SQNR_{max}$ increases by 6.02 dB similar to multi-bit SDMs. For the chosen OSR = 282, a second-order loop filter would be sufficient. However, for a robust design, a third-order SDM is chosen. Thanks to the noise scaling of the third stage, the power consumption of the third stage is expected to account for only 15% of the whole loop filter (simulated). For the implementation, a switched-capacitor (SC) loop filter is chosen for its robustness to clock jitter. The SC loop filter is chosen as a cascade of integrators with feed-forward (CIFF) for its superior linearity.

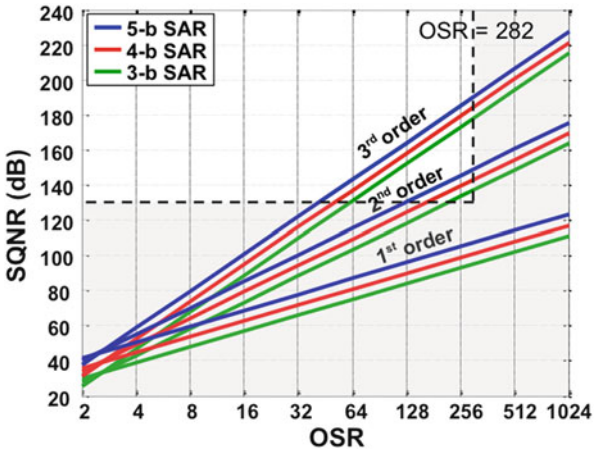


Fig. 6.8 OSR vs maximum SQNR of a zoom dynamic for different loop-filter orders and SAR resolutions

6.5.4 The SAR ADC and Over-ranging

As mentioned before, the fine DAC in Fig. 6.4 uses the digital result (k) of the SAR ADC to dynamically adjust its references. If according to the coarse converter the input signal satisfies $k{\cdot}V_{\mathrm{LSB},C} < V_{\mathrm{in}} < (k+1){\cdot}V_{\mathrm{LSB},C}$ where $V_{\mathrm{LSB},C}$ is the coarse converter quantization step or least significant bit (LSB), the references of the fine DAC are set to $V_{\mathrm{REF}-} = k{\cdot}V_{\mathrm{LSB},C}$ and $V_{\mathrm{REF}+} = (k+1){\cdot}V_{\mathrm{LSB},C}$. However, using the zoomed-in references has several problems. Foremost, SDMs are not stable over the full range of their DACs. So, if V_{in} is close $V_{\mathrm{REF}+}$ or $V_{\mathrm{REF}-}$, the SDM could be overloaded. Furthermore, any error in the coarse ADC due to mismatch or the coarse converter's thermal noise can lead to an error in k causing V_{in} to fall outside the SDM's input range. In that case, the SDM overloads and fine conversion becomes totally invalid, similar to the interstage mismatch problem of subranging converters [15]. To address this issue, the input range of the SDM can be widened by using *over-ranging*, so that the SDM DAC references are chosen as $V_{\mathrm{REF}+} = (k+1+M/2){\cdot}\mathrm{LSB}_C$ and $V_{\mathrm{REF}-} = (k\text{-}M/2){\cdot}LSB_{\mathrm{C}}$ where M is the over-ranging factor. Since the SDM DAC range is widened both at the low and at the high side, the DAC references symmetrically straddle the signal, i.e., V_{in} is approximately in the center of the SDM input range. Thus, even in the presence of a coarse conversion error smaller than ±M/2, the SDM can operate without overloading. This allows for larger errors in the coarse ADC converter.

Figure 6.9 shows simulated maximum acceptable SAR ADC INL vs M for zoom ADCs with 4–6-bit SAR ADCs and third-order SDM with 1-bit quantization. For each data point, a 100-point Monte Carlo simulation has been run, and the maximum INL which causes less than 10-dB SQNR deviation is reported. The offset of the SAR ADC is not included for the sake of simplicity. The maximum tolerable INL ($\pm\mathrm{LSB}_{\mathrm{C}}$) is found independent of the coarse resolution; however, the relative matching of the unit elements increases quadratically for each coarse bit, i.e., from

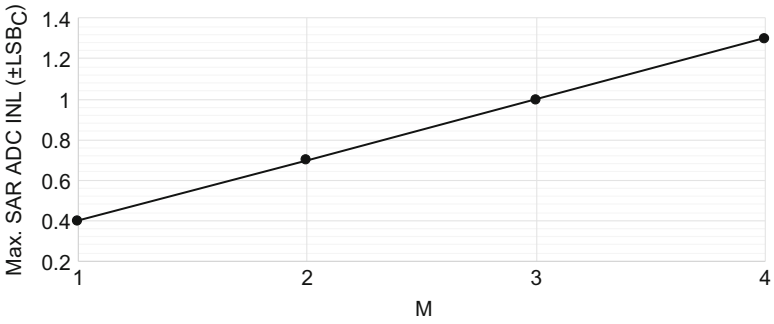


Fig. 6.9 Maximum simulated tolerable SAR ADC INL (LSB_C) vs M for zoom ADCs with a third-order SDM

5 bits to 6 bits, due to the smaller size of LSB_C. As it is seen from Fig. 6.9, the maximum acceptable INL error increases proportionally with M, thus dramatically relaxing the SAR ADC's accuracy requirements. Even missing codes are tolerated for $M \geq 3$.

Over-ranging comes at the cost of a lower SQNR, since doubling M results in a 1-bit less coarse resolution, i.e., 6-dB less SQNR, but it greatly simplifies the design of the SAR ADC and, consequently, its power consumption and area occupation. Thus, it makes an energy-efficient two-step conversion possible while keeping the SDM input range small ($= [M + 1]\cdot LSB_c$), avoiding strict matching requirements between two converters, and overloading in the SDM. Over-ranging also helps in increasing the maximum input signal bandwidth by modifying (6.3) into

$$f_{\text{in,max}} < \frac{(M+1)\cdot f_{\text{coarse}}}{2\pi \cdot 2^N} \tag{6.4}$$

Figure 6.10 shows M vs $f_{\text{in,max}}$ for SAR ADCs with 4–6 bits and with $f_s = 11.29$ MHz. To allow for the 20-kHz signal bandwidth, viable options are both a 4-bit SAR ADC with $M = 2$ and a 5-bit SAR ADC with $M = 4$. However, the latter provides a better coarse resolution, i.e., a more precise reference range estimation, with negligible additional power and area. So, in this work a 5-bit SAR ADC with 4-LSB_c over-ranging is used.

6.5.5 The Overall System

A system-level block diagram of the proposed dynamic zoom ADC is shown in Fig. 6.11. The CIFF loop filter is optimized for area as explained in the following. In a CIFF SDM, the first integrator's gain coefficient a_1 (Fig. 6.11) is usually smaller than one to utilize a large stable input range [12]. However, in our case, a larger a_1 is possible since zooming causes a first-integrator input much smaller than the zoom

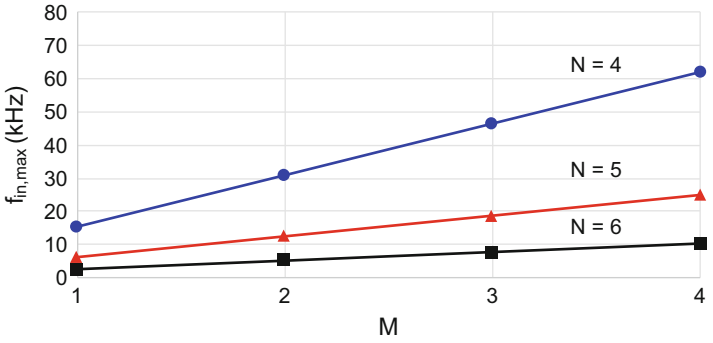


Fig. 6.10 $f_{in,max}$ vs M for 4–6-bit SAR ADCs clocked at 11.29 MHz f_S

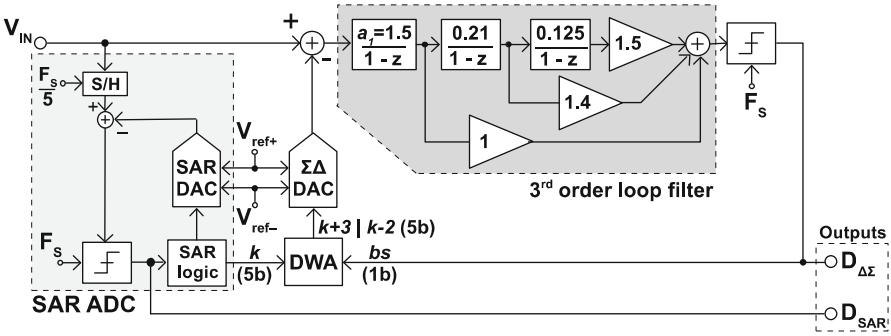


Fig. 6.11 System-level block diagram

ADC total full-scale input. A larger a_1 can be exploited to save a considerable silicon area, as explained in the following. Coefficient a_1 in the proposed implementation can be expressed as:

$$a_1 = \frac{C_S}{C_{\text{int 1}}} \tag{6.5}$$

where C_{int1} is the first integration capacitor and C_S is the sampling capacitor. The integrator is assumed to be non-inverting for the sake of simplicity. C_S is determined by the kT/C noise requirement, and it is fixed for a given OSR, thus resulting in C_{int1} being proportional to a_1. Since the area of a DT-SDM is dominated by the first-stage capacitors, $a_1 > 1$ allows for a large area saving. As a drawback, this increases the output swing of the first integrator, which however is quite small in a zoom ADC, and increasing it does not constitute an issue. Hence, $a_1 = 1.5$ is chosen (Fig. 6.11) corresponding to a first-integrator output swing of 27% of the full-scale output range. Such output swing is within the linear range of the inverter-based class-AB OTA used to implement the first integrator (see Sect. 6.5.5).

6.6 Circuit Design

A simplified circuit schematic of the proposed dynamic zoom ADC is depicted in Fig. 6.12. The 5-pF sampling capacitor is sized for kT/C noise and implemented by a parallel array of 31 capacitors that is also used as the fine DAC. The size of each integration capacitor $C_{\text{int},p-n}$ is 3.3 pF each. In the tracking phase Φ_1, all capacitors $C_{\text{s}[1..31]}$ are connected to the input. At the end of the tracking period, switch S_{13}, driven by an earlier phase clock Φ_{1e}, opens to sample the input on all capacitors while cancelling the input common-mode voltage. Input common-mode rejection is thus limited by the relative matching of the two sampling capacitor arrays, which was considered sufficient for the targeted application. In the integration phase Φ_2, m DAC elements ($m = k - 2$ or $m = k + 3$) are connected to $V_{\text{ref},p}$ in the positive DAC (to $V_{ref,n}$ in the negative DAC), while the others are connected to $V_{\text{ref},n}$ ($V_{\text{ref},p}$). Thus, a charge-domain zooming is effectively performed via charge redistribution. Accuracy of the zooming is improved by scrambling the units used in each period by using a data-weighted averaging (DWA) DEM algorithm. Switches $S_{S[1..31]}$ are bootstrapped to improve their linearity.

Simple energy-efficient CMOS inverters are used to implement the integrators. A dynamic biasing scheme similar to the one in [1] is employed to bias the inverter in a PVT robust manner. However, the OTA in [1] uses the large cascode transistors as switches. Since the gate capacitances of the cascodes are loading, the biasing circuit in each clock period and the biasing circuit power consumption would be too high for the high sampling frequency used in this dynamic zoom ADC. Thus, a new dynamic biasing scheme shown in Fig. 6.13a is proposed in the following: during the sampling phase Φ_1, the input transistors M_1 and M_2 are diode connected

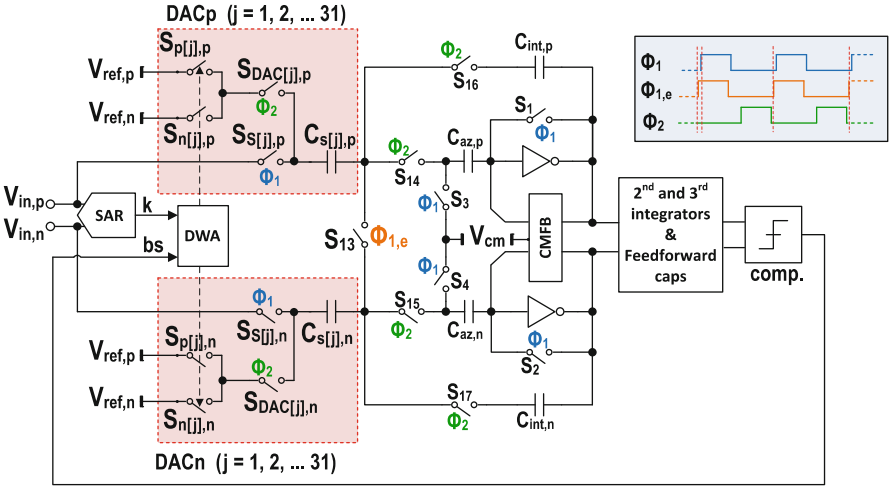


Fig. 6.12 A simplified circuit schematic of the proposed dynamic zoom ADC

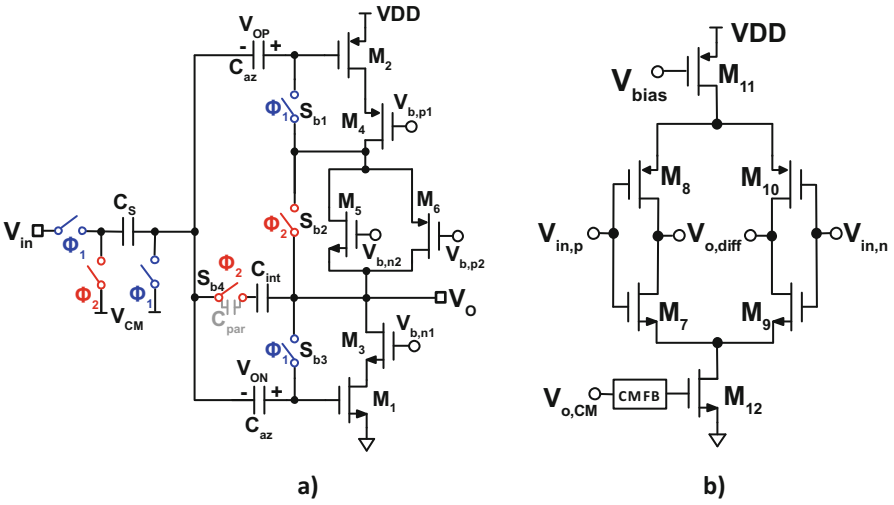


Fig. 6.13 (**a**) Proposed dynamic-biased inverter-based OTA. (**b**) Current-reuse OTA

by switches $S_{b1,3}$ and biased at 125 μA by a floating current source comprising M_5 and M_6. The bias voltages V_{OP} and V_{ON} are sampled together with of the offset and the $1/f$ noise of the OTA on the auto-zeroing capacitors C_{az} (2 pF each) effectively implementing auto-zeroing. In the integration phase Φ_2, the diode connections are broken, and the floating current source is simply bypassed by S_{b2}. A low-power biasing circuit can then be implemented, since it does not see any dynamic loading. Thanks to the cancellation of the input CM signal during sampling, the output CM drift of the OTA can be avoided by a simple SC common-mode feedback (CMFB) circuit [16]. Since the parasitic capacitance across S_{b4} (C_{par}) is discharged at every Φ_2, it might degrade the DC gain of the integrator. In the physical implementation, S_{b4}'s source and drain are shielded from each other by a grounded metal shield placed on top of the gate, so that C_{par} is reduced to less than 1fF, which is more than enough for a 65-dB DC OTA gain.

The second and third integrators are implemented by using fully differential current-reuse inverter-based OTAs biased at 50 μA each (Fig. 6.13b), and their capacitors were also scaled per their input-referred noise contribution scaling. The 1-bit quantizer is designed as a regenerative latch preceded by a static preamplifier and consumes 3.5 μA.

The implemented SAR ADC consists of a conventional synchronous logic, a charge redistribution capacitive DAC, and a comparator, as depicted in Fig. 6.14. The 11-fF unit capacitors are sized to ensure that coarse conversion errors are less than 1 LSB_C. The SAR ADC operates with the same sampling frequency of the SDM ($f_s = 11.29$ MHz), and it takes five cycles to make a conversion. The same comparator as in SDM is used.

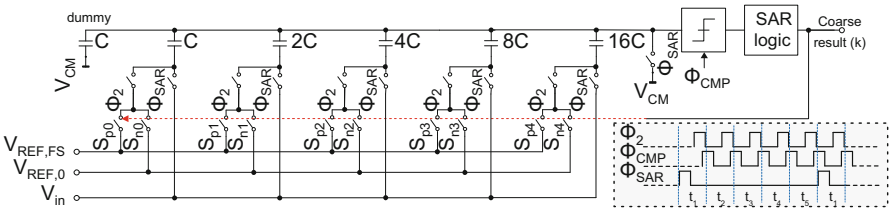
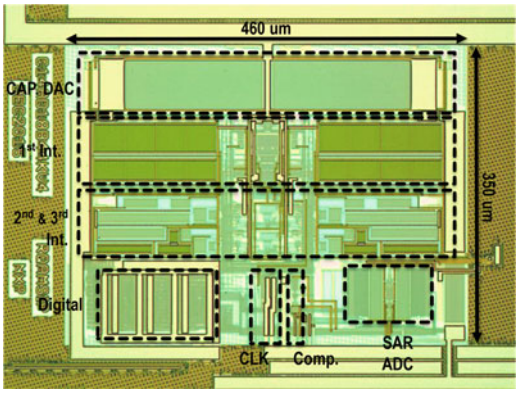


Fig. 6.14 The SAR ADC

Fig. 6.15 Chip micrograph



6.7 Measurement Results

The prototype dynamic zoom ADC has been fabricated in a 0.16-μm CMOS technology [11]. It occupies an area of 0.16 mm^2 as shown in the chip micrograph (Fig. 6.15). Its total power consumption is 1.12 mW with the digital circuitry consuming 29% of the power (including DWA, SAR logic, and the nonoverlapping clock generator and excluding the digital decimator). The analog power consumption is dominated by the first integrator (56%, simulated). In contrast, the SAR ADC's analog section draws only 7 μW (measured).

The digital outputs of the ADC were the SAR ADC's comparator output, the SDM bit stream, and a clock synchronized to the data. Since the outputs were single-ended and full-CMOS level (0 V–1.8 V), their interference with the external voltage reference on the test PCB limited the measured SNDR to 98.3 dB in 20-kHz BW in the first experimental characterization [10]. After lowering the supply of the digital output drivers from 1.8 V to 0.9 V, the interference is reduced (Figs. 6.16 and 6.17) so that the maximum measured SNDR is 103 dB.

The ADC's peak SNR and DR were 106 dB and 109 dB, respectively, with DWA active (Fig. 6.17). Peak SNDR is limited to 72 dB with DWA off due to the fine DAC mismatch. Thanks to the input common-mode cancellation scheme, the CMRR is greater than 62 dB from DC up to 1 MHz for full-scale common-mode inputs. The ADC's 1/*f* corner measured to be below 20 Hz, proving the effectiveness of the auto-zeroing employed in the first OTA.

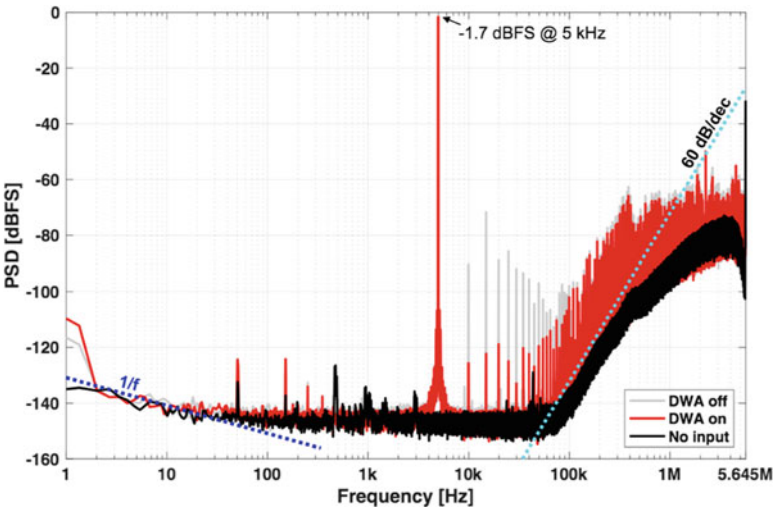


Fig. 6.16 Measured output spectra for DWA off, DWA on, and no input. Inputs are connected to V_{CM} for no input case, with DWA on

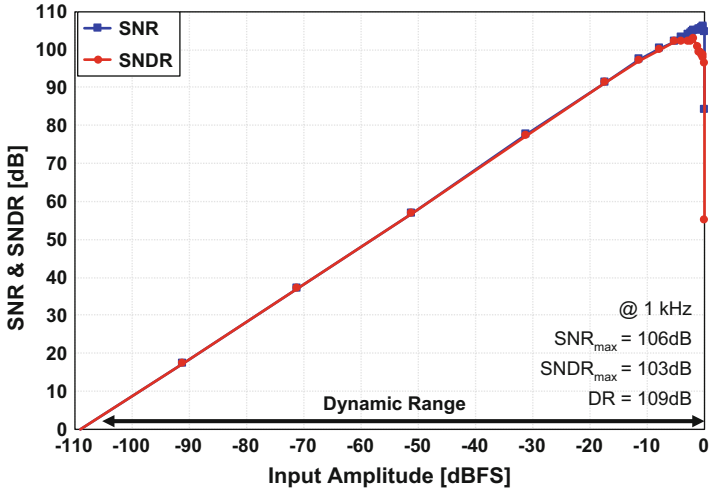


Fig. 6.17 Measured SNR/SNDR vs input amplitude (DWA on)

In order to test the overloading of the SDM with full-scale out-of-band signals, a full-scale sine wave is applied to the ADC's input, and its frequency is swept from 10 Hz to 100 kHz. In-band noise is measured for each point to predict the achievable DR as shown in Fig. 6.18. The degradation of the DR is observed with full-scale signals above 27 kHz, as predicted in system-level simulations. A first-order RC low-pass filter (LPF) with 30-kHz corner frequency is inserted before the

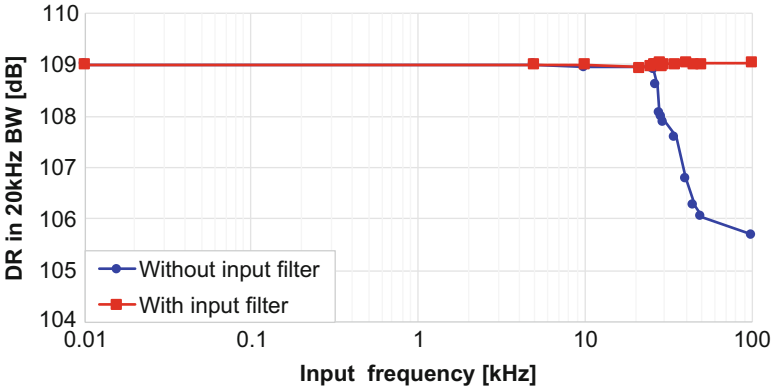


Fig. 6.18 DR in 20-kHz BW in the presence of in- and out-of-band full-scale inputs with and without an LPF at the input with 30-kHz corner frequency (DWA on)

Table 6.1 Performance summary and comparison with state-of-the-art audio ADCs

	Unit	This work	[24]	[25]	[26]	[27]	[18]
Year	–	2016	2016	2016	2016	2011	2016
Loop-filter type	–	DT	CT	CT	CT	CT+DT	DT
Technology	nm	160	160	130	65	40	130
Die area	mm^2	0.16	0.21	1.33	0.256	0.05	0.31
Power consumption	mW	1.12	0.39	0.28	0.8	0.5	0.3
Sampling frequency	MHz	11.29	3	6.144	6.4	6.5	6.1
Signal bandwidth	kHz	20	20	24	25	24	20
Peak SNR	dB	106	93.4	99.3	100.1	–	93.6
Peak SNDR	dB	103	91.3	98.5	95.2	90	97.7
DR	dB	109	103.1	103.6	103	102	100.5
FOMs[a]	dB	181.5	180.2	182.9	177.9	179	178.7

[a]FOMs = DR+10 log(signal bandwidth/Power)

ADC input, which ensures that the DR is constant up to at least 100 kHz (the max. measurement frequency is limited by the low-noise audio signal generator).

A performance comparison with the ADCs with similar resolution (>100-dB DR) and bandwidth is presented in Table 6.1. Although the proposed zoom ADC is a discrete-time design, it shows state-of-the-art 181.5-dB FoM_S. It is also considerably more area efficient than the previous designs implemented in similar technology nodes. As discussed before, the ADC's area is dominated by the capacitors defined by the kT/C noise required to obtain the 109-dB DR, so the area is used efficiently.

6.8 Conclusions

The dynamic zoom ADC is presented as a hybrid ADC suitable for high-resolution and high-linearity digital audio applications. The proposed zoom ADC employs a 5-bit SAR ADC working in parallel to assist a third-order SDM. This improved the overall energy efficiency by reducing the signal swing of the SDM and relaxed its nonthermal-noise-related power consumption. A 0.16-mm^2 prototype chip is implemented in 0.16-μm CMOS technology, achieving 109-dB DR, 106-dB peak SNR, and 103-dB peak SNDR while having an excellent FoM_S of 181.5 dB.

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