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3.1 A Quiet Digitally Assisted Auto-Zero-Stabilized Voltage Buffer with 0.6pA Input Current and 0.6µV Offset

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The readout of high impedance sensors and sampled voltage references [1] requires amplifiers with both low offset and low input current. Chopper amplifiers can achieve low offset, but the switching of their input chopper gives rise to significant input current (40 to 110pA) [2-4]. Auto-zero (AZ) amplifiers require less input switching, but exhibit more voltage noise. However, ping-pong amplifiers continuously swap two auto-zeroed input stages, leading to more switching [5,7]. In this work, an AZ stabilized topology is proposed, in which a single amplifier is always present in the signal path. Only one input switch is required, resulting in an input current of 0.6pA (max), a 66× improvement on the state-of-the art [4]. Furthermore, a digitally assisted offset-reduction scheme reduces its low-frequency (LF) noise to the theoretical √5× limit. It also achieves a state-of-the-art maximum offset of 0.6µV.

The AZ stabilized amplifier is shown in Fig. 3.1.1. It consists of a 3-stage unity-gain buffer (BUF), whose offset (V_{os1}) and 1/*f* noise are cancelled by an AZ stabilization loop, which consists of an integrator (INT) and two OTAs: AZ1 and AZ3. During phase ϕ_2, AZ1 is auto-zeroed. Its input is shorted and the resulting output current is integrated on capacitors $C_{int21\text{-}int22}$ (10 pF each). AZ2 then converts the result into a current that cancels V_{os1}. The corresponding correction voltage V_{EF} is stored on the input capacitors $C_{21\text{-}22}$ (5pF each) of AZ2. During phase ϕ_1, AZ1 senses the buffer's offset, which, due to feedback, appears between its inputs. The output current of AZ1 is then integrated on capacitors $C_{int31\text{-}int32}$ (10pF each), thus generating, via AZ3, an appropriate cancellation current. The corresponding correction voltage V_{GH} is stored on the input capacitors $C_{31\text{-}32}$ (5pF each) of AZ3. To achieve µV-level offset, each stabilization loop should have >120dB gain. This is achieved by a single gain-boosted integrator amplifier (INT), which is multiplexed between the two loops.

The main drawback of auto-zeroing is increased LF noise due to the fold-back of wideband thermal noise. In the chosen topology, the LF voltage-noise spectral density is theoretically limited to $\sqrt{5}\cdot e_n$, where e_n is the thermal noise density of AZ1 and BUF (Fig. 3.1.2). This can be understood as follows. During one AZ cycle, AZ1 first auto-zeros itself before auto-zeroing BUF, thus contributing $\sqrt{2}\cdot e_n$ to the total LF noise. Adding the contribution of BUF, this leads to a total of $\sqrt{3}\cdot e_n$. However, after AZ1 auto-zeros itself, its sampled noise is stored by $C_{21\text{-}22}$ and so reaches the output in both AZ phases. This means that its contribution to the total LF noise is correlated, leading to a minimum LF noise density of $\sqrt{5}\cdot e_n$.

To reduce noise folding, the ratio between the AZ loop bandwidth (BW_{AZ}) and the auto-zeroing frequency f_{AZ} should be minimized. Reducing the former is preferable, since increasing f_{AZ} increases the rate of switching spikes, and hence, input current. This requires either large integration capacitors or a large ratio between the transconductances of AZ1 & BUF and AZ2 & AZ3, respectively. Simulations show that a ratio of about 500× is required to reach the √5× limit (Fig. 3.1.2). However, this limits the offset correction range of each loop to ~500µV. In order to handle the expected mV-range, a digitally-assisted coarse/fine AZ scheme is proposed.

The digitally-assisted local (through AZ2) and overall AZ loops (through AZ3) are shown in Fig. 3.1.3. A coarse (5-bit + Polarity-bit) current DAC (IDAC) is used in parallel with each fine analog loop. The IDAC state is controlled by a SAR, which is driven by a comparator that samples the integrator output. At startup, the coarse loop minimizes the integrator swing; BW_{AZ} is temporarily increased for fast settling after each bit trial. The SAR bits are then fixed, BW_{AZ} is decreased (via the end of conversion (EOC) bit) and the analog loop turned on to cancel the remaining offset and drift. With an IDAC LSB corresponding to 100µV of offset, this greatly relaxes the job of the analog loop.

Output spikes can occur at the transitions between the two operating phases of the AZ scheme. These are mainly due to the charge injection of the input switches of AZ1 ($SW_{4\text{-}6}$) and the finite time needed for the integrator's output to settle to the different voltages (V_{EF}, V_{GH}) required to cancel the offsets of AZ1 and BUF, respectively. The digitally-assisted AZ loop greatly relaxes the swing and settling time of the integrator, minimizing its contribution to the output spikes. To minimize spikes due to on-chip crosstalk, the AZ clock is applied to the chip as a differential current via low-impedance inputs. The transitions of the resulting differential voltage are then re-synchronized by on-chip current-steering SR-latches.

Most of the buffer's input current is due to the charge injection and clock feedthrough of SW_6. Being a transmission gate, this depends on the mismatch between its PMOS and NMOS switches, which, in turn, depends on the input voltage, and so cannot be completely cancelled. Capacitors $C_{11\text{-}12}$ (1 pF) minimize the common-mode transient (due to leakage) at the input of AZ1 during phase ϕ_2, since this also causes output spikes. However, due to the buffer's residual offset V_{os_res}, these capacitors are also a source of input current. During ϕ_1, C_{11} samples $V_{in} + V_{os\_res}$, while C_{12} samples Vin. The associated charge is then shared during ϕ_2, which means that C_{11} must be charged from $V_{in} + V_{os\_res}/2$ back to V_{in} during the next ϕ_1 phase. This results in an average input current $I_{in} = C_{11}V_{os\_res}f_{AZ}/2$. For V_{os_res} = 0.6µV, I_{in} = 5fA, which is quite negligible.

The buffer's extremely low input current is evaluated by reading out the voltage across an on-chip hold capacitor C_H (36pF). This can be set to an external voltage via a low-leakage sampling switch $SW_{1,2}$. To minimize the leakage of the sampling switch, extra hold capacitors C_T (3 pF) and, via SW_3, C_B (36 pF) ensure that the channel and body-diodes of SW_2 are operated at zero reverse bias. The same technique is applied to AZ1's input switches $SW_{4\text{-}6}$, as their leakage will otherwise discharge $C_{11\text{-}12}$ and cause CM transients. The S&H switches $SW_{1\text{-}3}$ are simultaneously closed to sample the external voltage and opened to start the hold phase. The voltage drift across C_H is then an accurate measure of the buffer's input current, avoiding the need for low-leakage bootstrapped ESD diodes.

The digitally-assisted AZ stabilized voltage buffer was realized in a 0.18µm CMOS process (Fig. 3.1.7). It has an active area of 0.55mm², 0.12mm² of which is taken by the S&H circuit and draws 210µA from a 1.8V supply. With a 1V input and f_{AZ} = 15kHz, measurements show that its input current is below 0.6pA (15 samples), and that its offset does not exceed 0.6µV (Fig. 3.1.4). In Fig. 3.1.5, the buffer's voltage noise spectral density is shown. Over BW_{AZ} a LF noise density of 29nV/√Hz is achieved, which equals the √5× noise limit. No tones at f_{AZ} can be seen, demonstrating the effectiveness of the spike reduction techniques. The voltage drift across C_H is also shown (typical sample, 1V input). With AZ off, there is negligible leakage, illustrating the effectiveness of the low-leakage techniques. With AZ on, the variation in input current over the buffer's input range (0.1 to 1.3 V) indicates that it is indeed mainly due to the charge injection of SW_6. In Fig. 3.1.6 the performance of the auto-zeroed voltage buffer is summarized and compared with the state-of-the-art. It achieves 66× less input current (0.6pA), as well as state-of-the-art offset (0.6µV) and competitive LF voltage noise (29nV/√Hz).

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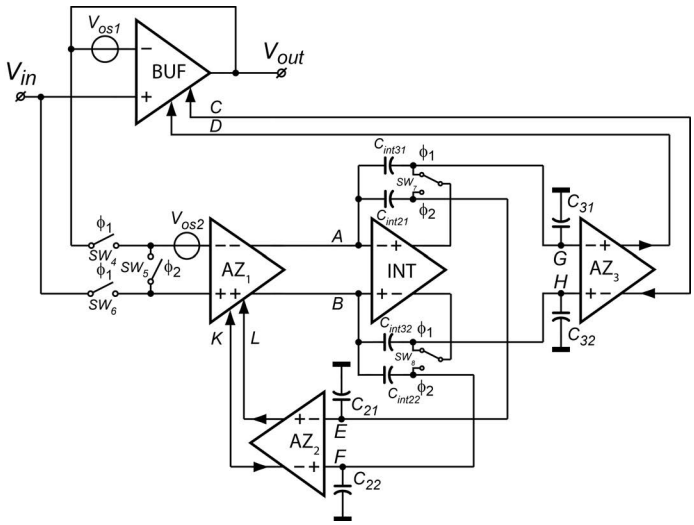

Figure 3.1.1: Block diagram of an auto-zero stabilized voltage buffer.

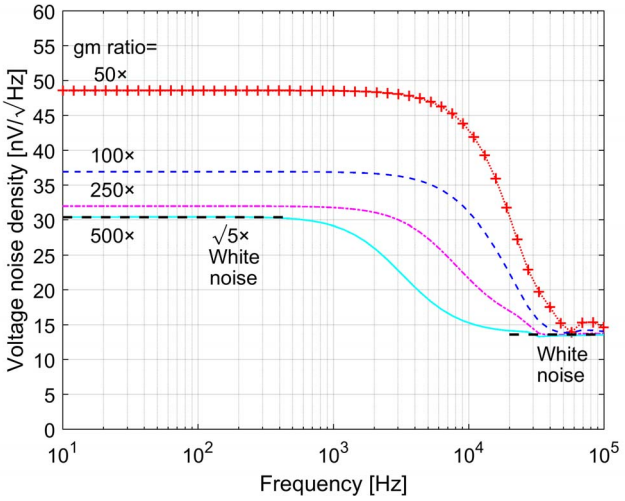

Figure 3.1.2: Simulated voltage noise density for different transconductance (g_m) ratios of AZ1 & BUF and AZ2 & AZ3, respectively (50×, 100×, 250× and 500×).

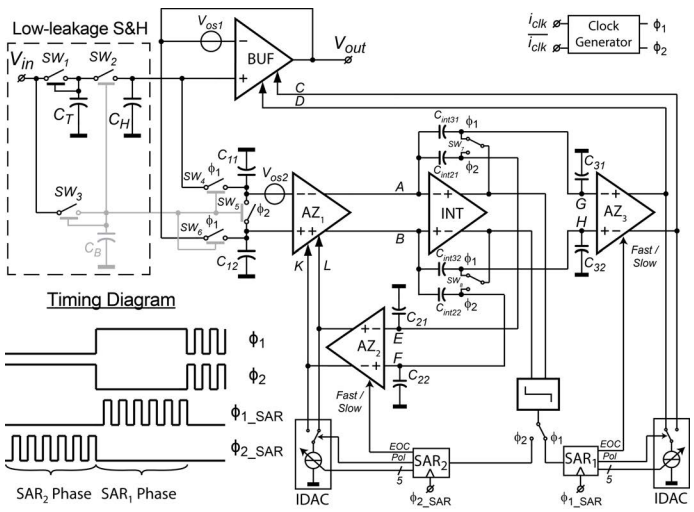

Figure 3.1.3: Block and timing diagram of the digitally-assisted auto-zero stabilized voltage buffer.

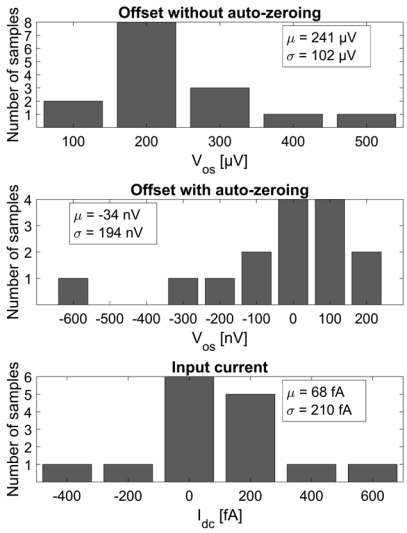

Figure 3.1.4: Histograms (15 samples) of the measured offset (without and with AZ) and input current (f_{AZ} = 15 kHz, V_{in} = 1V).

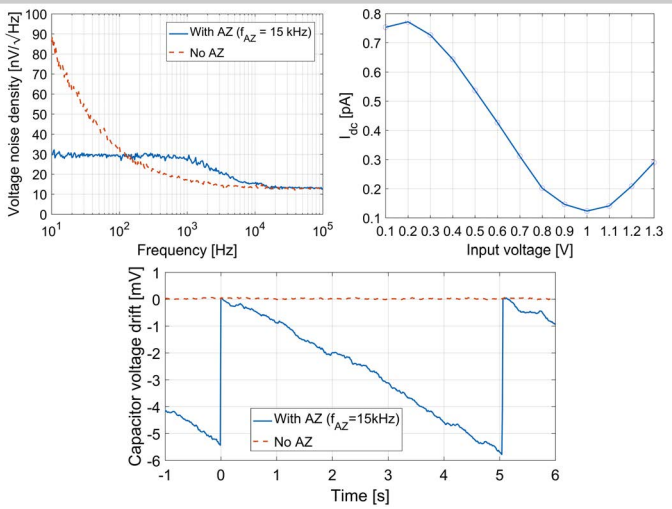

Figure 3.1.5: Measured voltage noise density: with and without AZ (Top left). The input current (I_{dc}) vs the input voltage for a typical sample (Top right). The capacitor voltage drift of a typical sample with and without AZ (Bottom).

	This work	[2]	[3]	[4]	[5]	[6]	[7]
Dynamic technique(s)	**Auto-zeroing**	Chopping	Chopping	Chopping and Auto-zeroing	Chopping and Auto-zeroing	Auto-zeroing	Chopping and Auto-zeroing
Input current (Max)	**0.6 pA**	110 pA	72 pA	40 pA	-	50 pA	-
Offset (Max)	**0.6 µV**	1 µV	0.78 µV	3 µV	2.8 µV	5 µV	4 µV
Voltage noise (nV/√Hz)	**29**	10.5	5.9	20	38 (AZ) 27 (CH&AZ)	75	140 (AZ) 28 (CH&AZ)
NEF	**7.4**	4.8	8.7*	21.8*	43.5*	-	-
GBW (MHz)	**1.45**	1.8	4	2.5	0.8	1	-
PSRR (dB)	**125**	120	142	-	138	130	128
Frequency (kHz)	**15**	30	200	15 / 7.5	28 / 14	4	11 / 7.33
Supply current	**210 µA**	143 µA	1.47 mA	800 µA	1.7 mA	750 µA	480 µA
Supply voltage	**1.8 V**	5 V	2.5 - 5.5 V	5 V	2.7 - 5.5 V	2.7 V	3.3 - 5.5 V
Die area (mm^2)	**1.4**	1.8	1.26	0.67	2.5	-	1.48

* Estimated value [2]

Figure 3.1.6: Performance summary and comparison with previous works.

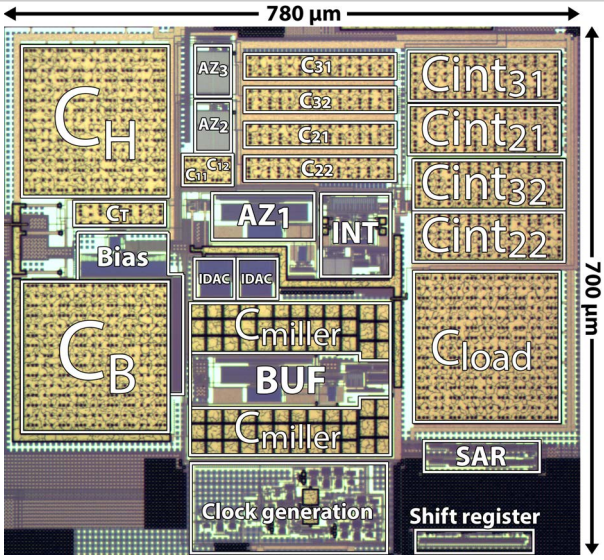

Figure 3.1.7: Die micrograph.

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