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DOI
10.1109/ISSCC.2018.8310315

Publication date
2018

Document Version
Final published version

Published in
2018 IEEE International Solid-State Circuits Conference, ISSCC 2018

19.4 A ±4A High-Side Current Sensor with 25V Input CM Range and 0.9% Gain Error from -40°C to 85°C Using an Analog Temperature Compensation Technique

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This paper presents a fully integrated ±4A current sensor that supports a 25V input common-mode voltage range (CMVR) while operating from a single 1.5V supply. It consists of an on-chip metal shunt, a beyond-the-rails ADC [1] and a temperature-dependent voltage reference. The beyond-the-rails ADC facilitates high-side current sensing without the need for external resistive dividers or level shifters, thus reducing power consumption and system complexity. To compensate for the shunt's temperature dependence, the ADC employs a proportional-to-absolute-temperature (PTAT) reference voltage. Compared to digital temperature compensation schemes [2,3], this analog scheme eliminates the need for a temperature sensor, a band-gap voltage reference and calibration logic. As a result, the current sensor draws only 10.9μA and is 10× more energy efficient than [2]. Over a ±4A range, and after a one-point trim, the sensor exhibits a 0.9% (max) gain error from -40°C to 85°C and a 0.05% gain error at room temperature. The former is comparable with that of other fully-integrated current sensors [2-4], while the latter represents the state-of-the-art.

Figure 19.4.1 shows a simplified block diagram of the current sensor. The load current is measured by digitizing the voltage drop V_S across a metal shunt resistor R_S inserted between the battery and the load. To safely handle ±4A currents, the 10mΩ shunt consists of four metal layers (M2-M5) and occupies 450μm×880μm (Fig. 19.4.1). Being made of aluminum, its resistance has a large temperature dependence: $R_S = R_0\times(1+\alpha_{shunt}\times(T-T_0))$, $T_0 = 25°C$, where $\alpha_{shunt} \approx 0.34\%/°C$, which means that Joule heating or ambient temperature variations will cause significant gain error.

In previous work, the shunt's temperature dependence has been calibrated in the digital domain, by sensing the shunt temperature *T* and then using this information to correct the ADC's output with the help of a calibration polynomial [2,3]. Noting that the metal shunt's temperature dependence is almost perfectly PTAT ($R_S \approx k_R\cdot T_A$, T_A is absolute temperature) over the industrial temperature range, we propose an analog compensation scheme in which the ADC is driven by a PTAT voltage reference $V_{Ref} = k_V\cdot T_A$ (Fig. 19.4.1). Consequently, the shunt's 1st-order temperature dependency is corrected in a ratiometric manner without calibration. Although this approach does not correct for the non-linear components of the shunt's temperature dependence, simulations show that the resulting gain error will be less than ±1% from -40°C to 85°C. Furthermore, the spread of the nominal values of the shunt resistance R_0 (±10%) and the magnitude of V_{Ref} can both be corrected by a single trim at room temperature.

The schematic of the V_{Ref} generator is shown in Fig. 19.4.1. It consists of a bias circuit and a bipolar core, both based on pairs of NPN transistors with an emitter-area ratio *p = 7*. In the bias circuit, one pair is biased by two identical current sources, thus generating a base-emitter voltage difference $\Delta V_{BE} = (k/q)\times\ln(p)\times T_A$. This is then forced across a poly-resistor R_b, resulting in a PTAT current $\Delta V_{BE}/R_b$. Leveraging the vertical NPNs available in the chosen process means that this can be done without the extra low-offset amplifier required by PNP-based bias circuits, e.g. as used in [2]. The PTAT biasing current is then mirrored (1:4) to the bipolar core and used to bias the second pair of NPNs, thus generating the accurate ΔV_{BE} that is used as V_{Ref}. The two current sources in the bipolar core are chopped to suppress their *1/f* noise. To avoid intermodulation issues, the chopping frequency is the same as the ADC's sampling frequency. The NPN transistors are located underneath the shunt to ensure good thermal coupling between the metal shunt and the voltage reference. This is further improved by using thermal vias to connect the shunt to a sheet of M1 around the NPNs [2]. Compared to the analog compensation scheme described in [5], which uses a bandgap voltage reference followed by a reference buffer with a temperature-dependent gain, the proposed solution is much simpler and more power efficient.

Figure 19.4.2 shows the schematic of the beyond-the-rails ADC [1]. It is based on a 2nd-order feedforward SC ΔΣ ADC built around two current-reuse OTAs. During $\phi1$, the input signal, V_S, and the OTA offset are sampled on the 2.5pF input capacitors, C_{S1}. During $\phi2$, the HV chopper CH_{HV} reverses the polarity of V_S and thus transfers a charge packet proportional to $2\cdot C_{S1}\cdot V_S$ to the integration capacitors, C_{INT}. In a similar manner, the PTAT voltage reference ΔV_{BE} is sampled onto feedback capacitors C_{S2} (2.5pF) via an LV chopper CH_{LV} with the polarity determined by the modulator's bitstream. This cross-coupled sampling scheme ensures that the only components exposed to the input CM voltage are the input capacitors and the HV chopper. Together with switches S_{1-2}, it also realizes a correlated-double-sampling (CDS) scheme that suppresses the offset and 1/*f* noise of the 1st OTA. The switch timing is designed to ensure that the residual offset is mainly due to the charge-injection mismatch of switches S_{1-2}, and so can be further reduced by low-frequency chopping (CHL). In [1], this was implemented by an additional capacitively-coupled HV input chopper, which then had to be periodically toggled to keep its coupling capacitors charged. In this design, the same functionality is achieved by swapping the clock signals $\phi1$, $\phi2$ applied to the input chopper CH_{HV} (Fig. 19.4.2), thus allowing CHL to be completely disabled if necessary. For good matching, both C_{S1} and C_{S2} are implemented as fringe capacitors with a 70V breakdown voltage.

The schematic of CH_{HV} is shown in Fig. 19.4.2. Its clock signals ϕ_1, ϕ_2 are capacitively-coupled to the gates of four sampling switches M_{1-4} via two HV capacitors $C_{1,2}$. A minimum selector $M_{S1,2}$ connected between the input terminals V_{ip} and V_{in} selects the lowest input voltage. Its output is tied to the reference of the clock level shifter comprising coupling capacitors $C_{1,2}$ and a latch $M_{5,6}$. As a result, the coupled clocks are always superimposed on V_{min} (the lower of V_{ip} and V_{in}), which minimizes the leakage of M_{1-4} in the presence of bidirectional input voltages [1].

The current sensor was implemented in a 0.18μm HV BCD CMOS technology and occupies 1.4mm² (Fig. 19.4.7). It draws 10.9μA from a 1.5V supply at room temperature. The reference generator, the ADC and the digital clock generator consume 4μA, 5.2μA and 1.7μA respectively. Figure 19.4.3 shows the output spectrum of the ADC for different input currents. At a sampling frequency of 250kHz, the ADC achieves a resolution of $1.5\mu V_{rms}$ in a conversion time of 2ms, which translates into a current-sensing resolution of $150\mu A_{rms}$.

10 sensors were characterized in a current range of ±4A from -40°C to 85°C (Fig. 19.4.4). After trimming its digital output (at +3A and ~25°C), the sensor gain error is only 0.05% at room temperature, increasing to 0.9% over the full temperature range. Over a 25V input CMVR, the ADC maximum offset is 6.4μV (640 μA), dropping below 400nV (40μA) when CHL is enabled (Fig. 19.4.5). This varies by less than 700nV over the full CMVR, corresponding to a CMRR of 151dB, which is improved to 158dB after CHL. The sensor input CMVR is limited by the ESD diodes at the input terminals to -0.7V to 25V.

The performance of the sensor is summarized in Fig. 19.4.6. Its energy efficiency, like that of a temperature sensor, can be expressed in terms of a resolution FOM [6]. Compared to other fully integrated current sensors in the table, this design achieves 10× better energy efficiency, the best accuracy at room temperature, and comparable accuracy over the industrial temperature range.

Acknowledgement:
The authors would like to thank Zuyao Chang for chip bonding and Saleh Heidary Shalmany for layout review.

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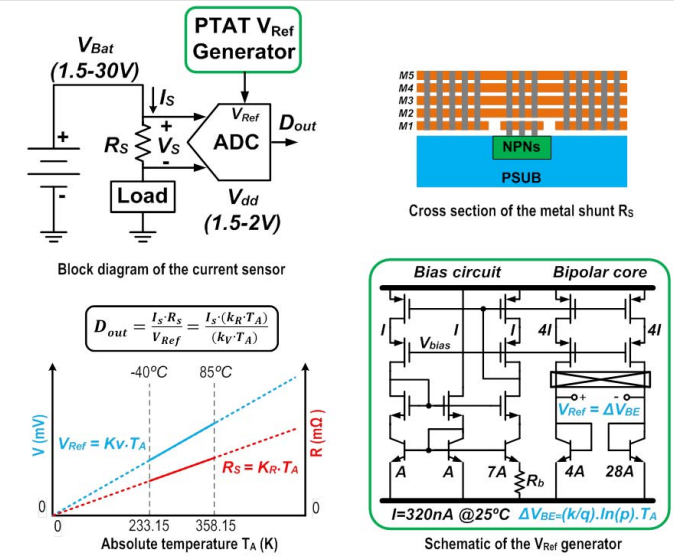

Figure 19.4.1: Block diagram of the current sensor.

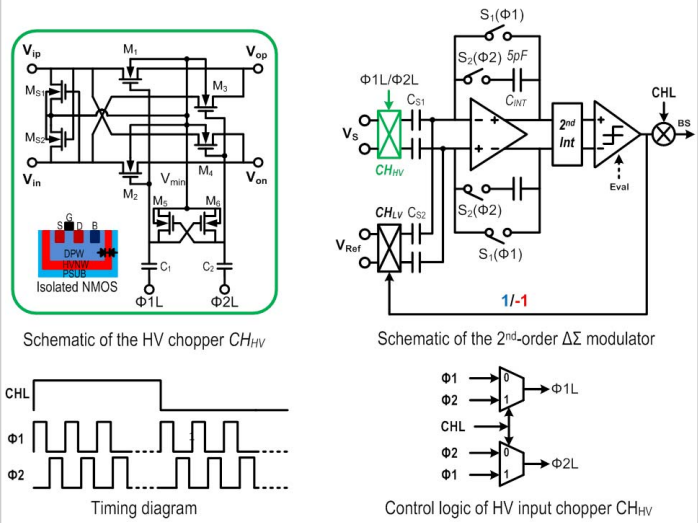

Figure 19.4.2: Block diagram of the beyond-the-rails ADC.

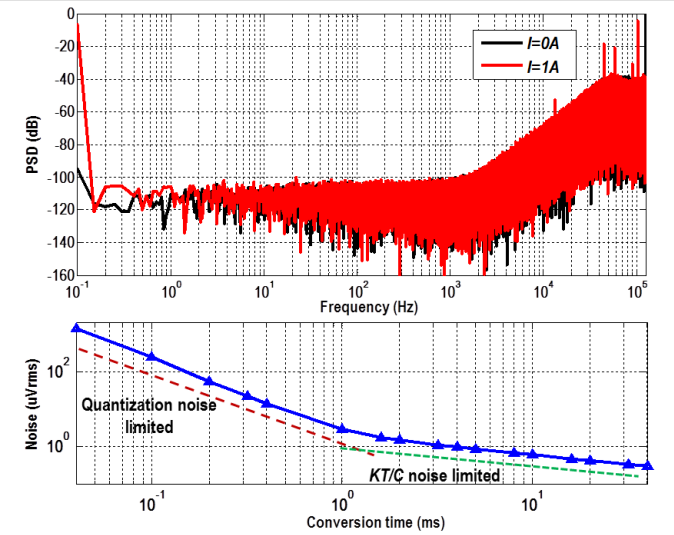

Figure 19.4.3: Measured output spectrum of the beyond-the-rails ADC (CHL is off).

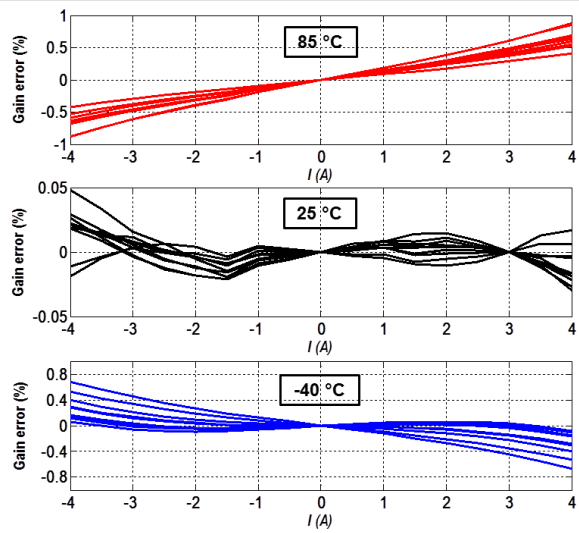

Figure 19.4.4: Measured current-sensing gain error at different ambient temperatures (10 samples).

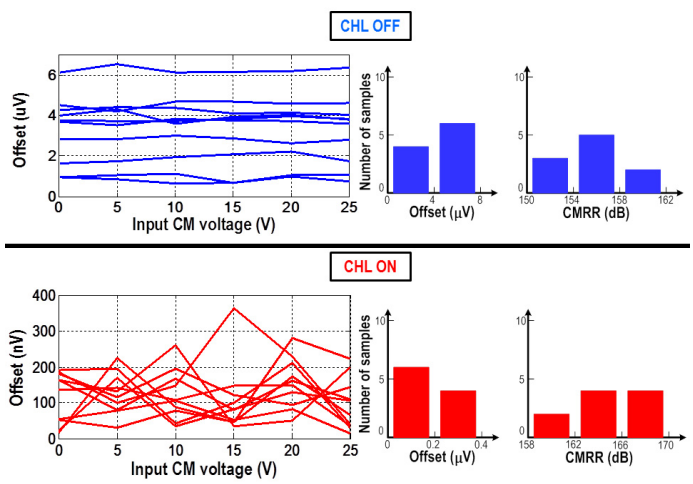

Figure 19.4.5: Measured CMRR and offset (10 samples) over input CMVR with CHL off (top) and on (bottom).

	This work	JSSC 17 [2]	LT2947 [3]	INA260 [4]
I-range	**±4A**	±5A	±30A	±10A
Temperature range	**-40-85°C**	-55-85°C	-40-85°C	-40-125°C
Shunt	**10mΩ**	10mΩ	300μΩ	2mΩ***
Input CM range	**0-25V**	0-0.75V	0-15V	0-36V
Gain error (25°C)	**0.05%**	0.1%	0.75%	0.15%
Gain error (-40-85°C)	**0.9%**	0.3%	1%	0.5%
Offset	**40μA**	4μA	9mA	5mA
Resolution	**150μA**	200μA	3mA	1.25mA
ENOB	**13bit**	13bit	11.5bit	11bit
Conversion time	**2ms**	10ms	100ms	8.2ms
Supply voltage	**1.5-2V**	1.3-1.7V	4.5-15V	2.7-5.5V
Supply current	**10.9μA**	13μA	9mA**	310μA
Polynomial Calibration	**No**	Yes	Yes	No
FOM*	**0.74fJ·A²**	**7.8fJ·A²**	--	--

* FOM = (Energy / Conversion) × Resolution²

** Includes the power of current-sense ADC, voltage-sense ADC, temp. sensor and digital circuitry

*** Uses a custom low-TC shunt

Figure 19.4.6: Performance summary and comparison table.

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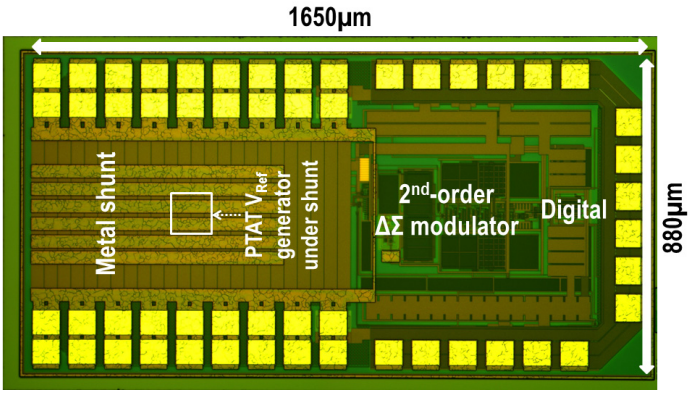

Figure 19.4.7: Die micrograph.

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