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A -121.5 -dB THD Class-D Audio Amplifier With 49-dB LC Filter Nonlinearity Suppression

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Abstract—Class-D audio amplifiers produce electromagnetic interference (EMI), which often needs to be suppressed by an external LC filter. However, due to component nonlinearity, this filter can itself cause significant distortion. This article presents a class-D amplifier that suppresses LC filter nonlinearity by 49 dB and is robust to $\pm 30\%$ variations in its cutoff frequency. This is achieved by a dual-loop architecture, in which an inner loop provides stability, while an outer loop provides the high gain needed to suppress the LC filter and output-stage nonlinearity. A prototype, implemented in a 180-nm BCD process, achieves -121.5 -dB total harmonic distortion (THD) and -107.1 -dB THD+N, which is maintained to within 3 dB even as the LC filter cutoff frequency is varied from 62 to 106 kHz. It can deliver a maximum of 21 W into a 4- Ω load with 87% efficiency and 12 W into an 8- Ω load with 91% efficiency, measured at 10% THD.

Index Terms—Audio power amplifier, class-D amplifier, feed-back after LC filter, nonlinearity compensation, total harmonic distortion (THD).

I. INTRODUCTION

CLASS-D amplifiers are widely used in audio applications due to their superior power efficiency. However, the switching activity of their output stages produces electromagnetic interference (EMI). This necessitates the use of an LC filter [1]–[5] in some applications (e.g., automotive) to comply with the associated EMI standards (e.g., CISPR-25 [6]). This EMI challenge has led recent designs to employ pulsewidth modulation (PWM) schemes with a switching frequency (f_{PWM}) above the AM band [1]–[3]. This choice also enables high loop gain (> 70 dB in [2] and [3]), pushing the total harmonic distortion (THD) +N below -100 dB.

Fig. 1 shows a conventional PWM-based class-D amplifier. A closed-loop architecture is commonly used to suppress the distortion and supply sensitivity of the output stage, and an LC filter is placed at the output to suppress EMI emission. Due to the nonlinearity of practical inductors and capacitors, however,

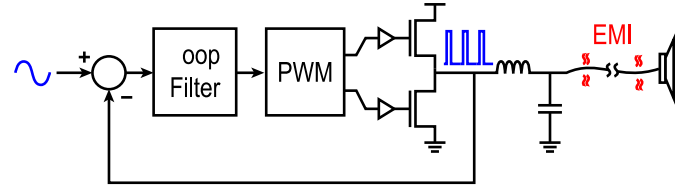





Fig. 1. Conventional Class-D amplifier with output LC filter.

TABLE I
SELECTED INDUCTORS FOR CLASS-D AMPLIFIER APPLICATIONS

			
Dimension (mm)	28 x 20 x 16	8 x 8 x 7	4 x 4 x 2
I_{SAT}	100 A	19 A	3.7 A
THD*	-102 dB	-102 dB	-60 dB
Cost	\$\$\$	\$\$	\$

Source: Bourns, Würth, Murata

*Measured right before clipping across a 4- Ω load.

the LC filter may cause significant distortion. According to Berkhout [7], the distortion is dominated by the inductor's current dependence and can be estimated by the following equation:

$$\text{THD}_L \approx \frac{f_{\text{IN}}}{f_{LC} Q} \cdot \frac{P_{\text{OUT}}}{6 R_L I_{\text{SAT}}^2} \quad (1)$$

where $f_{LC} = (2\pi(LC))^{-1/2}$ is the LC filter's cutoff frequency and I_{SAT} is the inductor's saturation current.

According to (1), THD can be improved by using inductors with a high saturation current or increasing f_{LC} . This is corroborated by Table I, which shows the measured THD of the class-D amplifier described in [3] when its LC filter is realized with three different inductors. However, inductors with a high saturation current tend to be bulky and expensive. In [3], a 580-kHz f_{LC} is enabled by the combination of a multi-level output stage and a 4.2-MHz f_{PWM} . However, its THD still depends on inductor choice. From (1), $I_{\text{SAT}} > 12$ A would be required for THD < -100 dB, while the maximum load current is only 3.6 A. Hence, the use of inductors with

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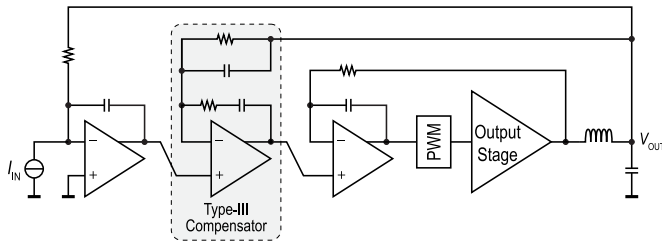


Fig. 2. Triple-loop architecture of [12].

a large footprint and high cost is still necessary to guarantee high linearity.

Feedback-after- LC architectures have been proposed to reduce the impact of LC filter nonlinearity [4], [8]–[12]. In such architectures, LC filter nonlinearity is suppressed by the amplifier's overall loop gain. However, implementing this is challenging because the LC filter introduces two additional complex poles into the amplifier's feedback path. Furthermore, practical inductors and capacitors have manufacturing tolerances, as well as bias (current and voltage) dependencies, leading to variations in f_{LC} . In [8]–[10], self-oscillating architectures that take advantage of the LC filter's poles have been employed. However, their PWM frequency is signal- and f_{LC} -dependent, leading to an unpredictable EMI spectrum, which restricts their use in EMI-sensitive applications.

In fixed-frequency PWM designs, zeros can be added to the loop filter to compensate for the LC filter's phase shift. However, with a single feedback path, the loop bandwidth (f_U) will be a function of f_{LC} . This limits the allowable f_{LC} tolerance because f_U should not exceed f_{PWM}/π in class-D amplifiers with fixed-frequency PWM [11], [13]. In [11], the effect of capacitance variation is eliminated by using a current-mode inner loop, but f_U still depends on the inductance, and the maximum modulation index is limited to 0.85. To mitigate this, a triple-feedback architecture (see Fig. 2) is proposed in [12], where the first feedback path around the output stage and before the LC filter desensitizes the loop bandwidth from f_{LC} variations. The second feedback path after the LC filter is then stabilized with the help of a Type-III compensator. Finally, an outer first-order feedback path increases the suppression of LC filter nonlinearity. However, due to its limited loop filter order and a low f_{PWM} of 100 kHz, this design only achieves a modest (10 dB) suppression of LC filter nonlinearity at 20 kHz.

In [4], a digital feedback architecture is proposed in which a fifth-order digital loop filter provides 50 dB of the loop gain around the LC filter at 20 kHz. To maintain stability, the LC filter's poles are nominally canceled by an LC^{-1} filter implemented in the digital domain. This architecture requires a high-performance and low-latency ADC in the feedback path, significantly increasing its complexity. Furthermore, the mismatch between the external LC filter and the digital LC^{-1} filter compromises stability, which is exacerbated by its low loop bandwidth (100 kHz). As a result, the coefficients of the digital LC^{-1} filter have to be adjusted for a given LC filter, resulting in significantly increased application cost.

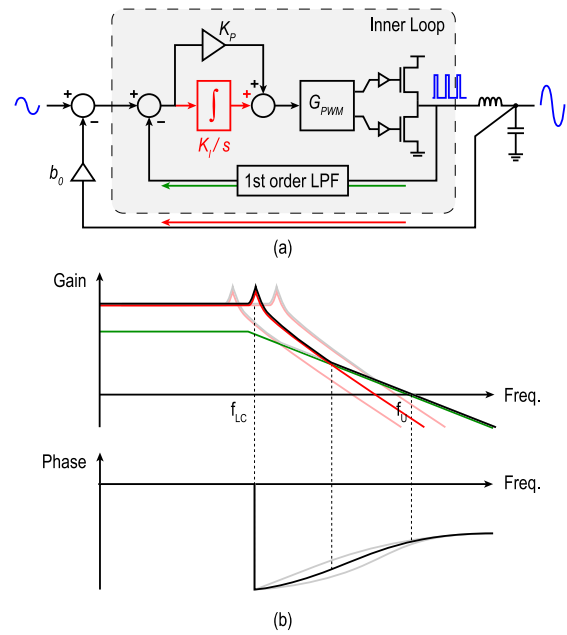


Fig. 3. (a) Proposed feedback-after- LC architecture stabilized by the inner loop and (b) loop gain around the output stage under LC filter variations.

In this article, which is an extension of [14], a dual-loop architecture is proposed that aims to suppress LC filter nonlinearity by at least 40 dB, based on the data in Table I, and is robust to $\pm 30\%$ variation in LC filter cutoff frequency to accommodate the manufacturing tolerances and bias dependencies of typical components. In contrast to [12], a single inner loop desensitizes the loop bandwidth from f_{LC} variations and ensures stability. An outer loop then employs a resonator with optimized in-band poles to maximize the suppression of LC filter nonlinearity. This is enhanced by the use of a high (1.2 MHz) loop bandwidth, which is enabled by a high (4.2 MHz) PWM frequency.

This article is organized as follows. Section II introduces the proposed architecture and explains the design considerations for the loop filter parameters. Section III describes circuit implementation details. Measurement results are presented in Section IV. Section V concludes this article.

II. PROPOSED ARCHITECTURE

A. Inner Loop

Fig. 3(a) illustrates the proposed architecture. It consists of an inner loop, which incorporates a first-order RC low-pass filter (LPF), which bypasses the main feedback loop (with a gain of b_0) at high frequencies. The inner loop has three main functions: 1) it compensates for LC filter phase shift and, therefore, stabilizes the overall amplifier; 2) it ensures that the loop bandwidth around the output stage is insensitive to LC filter variation [see Fig. 3(b)] and satisfies the PWM stability criteria ($f_U < f_{PWM}/\pi$) since the loop gain around f_U is dominated by the first-order path; and 3) it provides the loop gain needed to suppress output-stage nonlinearity.

To evaluate the dampening effect of the inner loop on the LC filter's complex poles, its closed-loop gain $H_{CL,inner}$ will

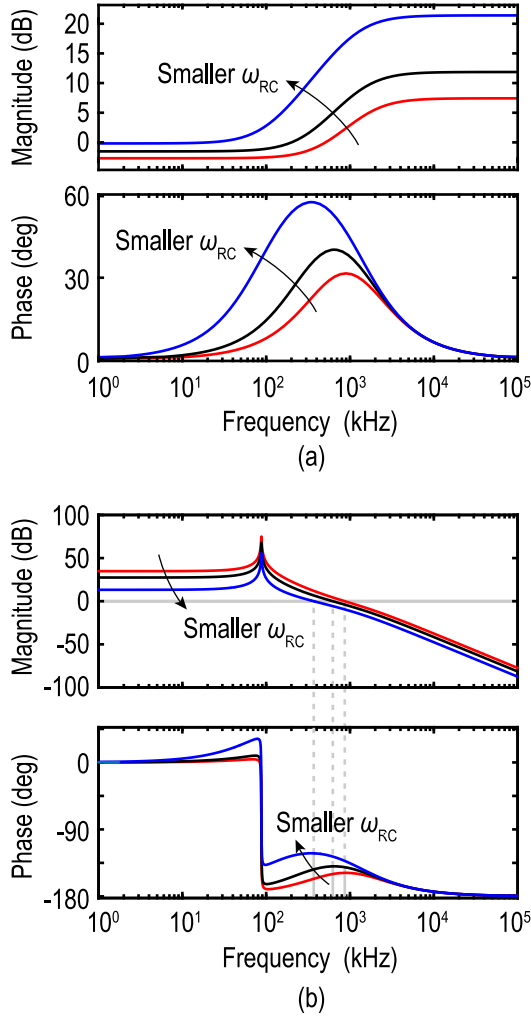


Fig. 4. (a) Inner loop's closed-loop response $H_{CL,inner}$ and (b) loop gain around the *LC* filter H_{outer} for the system of Fig. 3(a).

be analyzed. For simplicity, the integral path K_I/s (drawn in red) is initially ignored. Then, $H_{CL,inner}$ can be expressed as

$$H_{CL,inner}(s) = K_P G_{PWM} \cdot \frac{s + \omega_{RC}}{s + (1 + K_P G_{PWM})\omega_{RC}} \quad (2)$$

where K_P denotes the proportional gain in the forward path, G_{PWM} is the equivalent gain of the output stage (the ratio between its supply voltage and the amplitude of the triangular wave used for PWM generation) [13], and ω_{RC} is the cutoff frequency of the first-order LPF. From Fig. 3, the loop bandwidth f_U is given by

$$\omega_U = 2\pi f_U \approx K_P G_{PWM} \omega_{RC} \quad (3)$$

where f_U is slightly lower than f_{PWM}/π . Hence, (2) can be simplified to

$$H_{CL,inner}(s) = \frac{\omega_U}{\omega_{RC}} \cdot \frac{s + \omega_{RC}}{s + (\omega_{RC} + \omega_U)}. \quad (4)$$

Equation (4) shows that the inner loop acts as a lead compensator with a low-frequency zero at ω_{RC} . Fig. 4(a) shows its Bode plot, which illustrates how its phase lead can

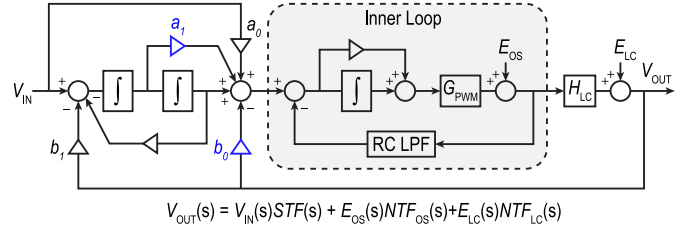


Fig. 5. Complete block diagram of the proposed class-D amplifier.

be used to compensate for the phase lag introduced by the *LC* filter.

The loop gain around the *LC* filter is given by

$$H_{outer}(s) = b_0 H_{CL,inner}(s) H_{LC}(s) \quad (5)$$

where $H_{LC}(s)$ is the *LC* filter's frequency response. Fig. 4(b) shows the Bode plot of $H_{outer}(s)$. There is a tradeoff between the phase margin and the in-band magnitude of $H_{outer}(s)$. This is because a smaller ω_{RC} implies a higher $|H_{CL,inner}|$, especially at frequencies above ω_{RC} , so b_0 must be reduced to achieve the extra phase lead.

Apart from stabilizing the outer loop, the gain of the inner loop also helps to suppress output stage nonlinearity. This can be improved by adding an integral path in parallel with K_P , forming a PI compensator in the forward path. Then, (2) should be modified as follows:

$$H_{CL,inner}(s) = \frac{G_{PWM} H_{PI}(s)}{1 + G_{PWM} H_{PI}(s) \cdot \frac{1}{1 + \frac{s}{\omega_{RC}}}} \quad (6)$$

where $H_{PI}(s) = (K_P s + K_I)/s$ is the PI compensator's transfer function.

By choosing the PI compensator's zero to coincide with ω_{RC} , i.e., $K_I/K_P = \omega_{RC}$, the loop gain around the output stage reduces to that of an integrator, and (6) simplifies to

$$H_{CL,inner} = \frac{G_{PWM}(sK_P + K_I)}{s + G_{PWM}K_I}. \quad (7)$$

Due to the pole-zero cancellation, the inner loop remains first order, and the closed-loop response is still that of a lead compensator. The accuracy of the pole-zero cancellation can be ensured by defining K_I/K_P and ω_{RC} with the same type of *RC* components on-chip. The loop bandwidth is given by

$$\omega_U = 2\pi f_U = G_{PWM} K_I \quad (8)$$

where K_I is defined by on-chip *RC* components, which can be set with sufficient accuracy by a one-time trim [3], [15]. Consequently, the loop bandwidth becomes insensitive to *LC* filter variations.

However, as shown in Fig. 4(b), the loop gain around the *LC* filter is still relatively low in the audio band. Also, the loop gain around the output stage does not suppress its nonlinearity sufficiently. These problems are addressed by the addition of an outer loop.

B. Outer Loop

The outer loop employs two additional stages to increase the suppression of the *LC* filter and output stage nonlinearity,

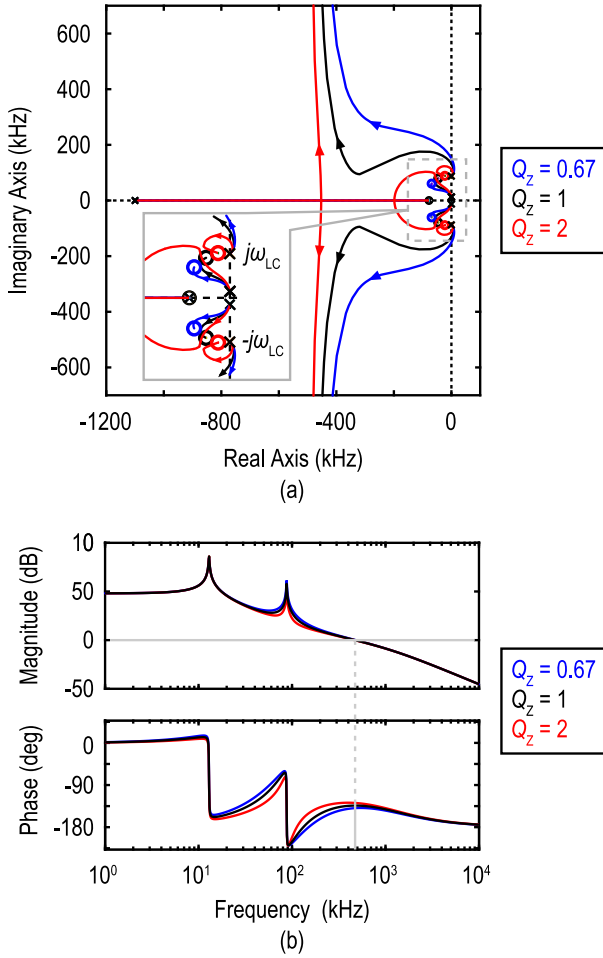


Fig. 6. (a) Root loci and (b) loop gain around the LC filter for different Q 's of the outer loop zeros.

as shown in Fig. 5. These stages form a resonator that is designed to maximize the in-band loop gain. A feedforward path (a_1) is used to reduce the output swing of the first integrator [16]. A direct input feedforward path (a_0) is used to reduce the output swing of the second integrator [17]. The inclusion of these paths relaxes the amplifiers' specifications and facilitates smooth overdrive recovery (see Section III-B).

Besides adding two poles to boost the audio-band gain, the outer loop introduces two zeros due to the presence of the feedforward (a_1) and feedback (b_0) paths highlighted in Fig. 5. In contrast to the zero provided by the inner loop, these two zeros can be arranged as a complex conjugate pair, which pulls the LC filter poles further into the left half-plane (LHP) without compromising loop gain [18], as shown in Fig. 6. However, Q of these zeros cannot be made too high. In this case, shown by the red traces in Fig. 6, the LC filter poles no longer move into the LHP but stay close to the imaginary axis, implying excessive ringing in the transient response. In this work, to balance performance and robustness, Q of these zeros is set to unity. The zero locations of the inner loop and outer loop are co-optimized in the overall system.

C. Nonlinearity Suppression

In Fig. 5, the LC filter and the output stage nonlinearity are modeled as additive errors. The LC filter nonlinearity is

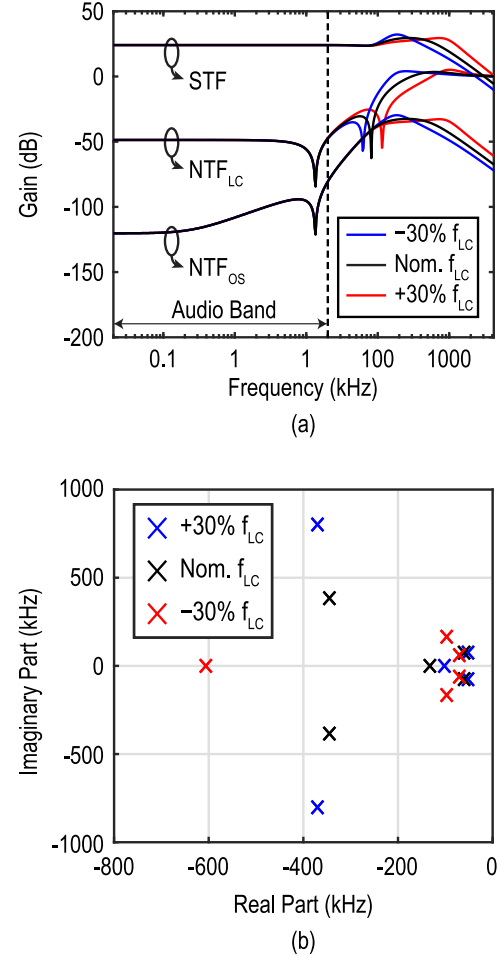


Fig. 7. (a) STFs and NTFs and (b) locations of closed-loop poles under f_{LC} variations.

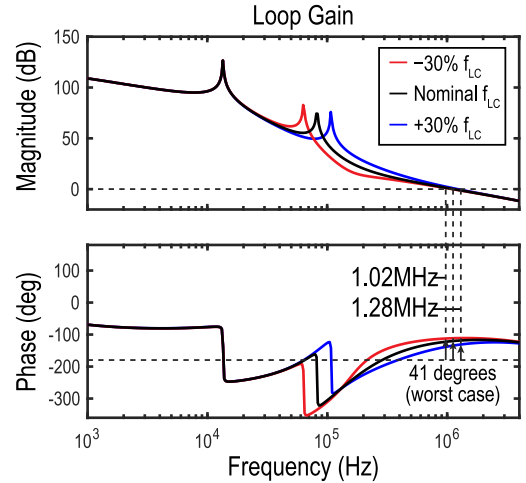


Fig. 8. Loop gain around the output stage under $\pm 30\%$ f_{LC} variations.

suppressed by the gain of the resonator and the closed-loop gain of the inner loop. This results in the following noise transfer function (NTF):

$$NTF_{LC}(s) = \frac{V_{OUT}(s)}{E_{LC}(s)} = \frac{1}{1 + H_{CL,inner}(s)H_{RES}(s)H_{LC}(s)} \quad (9)$$

where $H_{RES}(s)$ is the open-loop gain of the resonator.

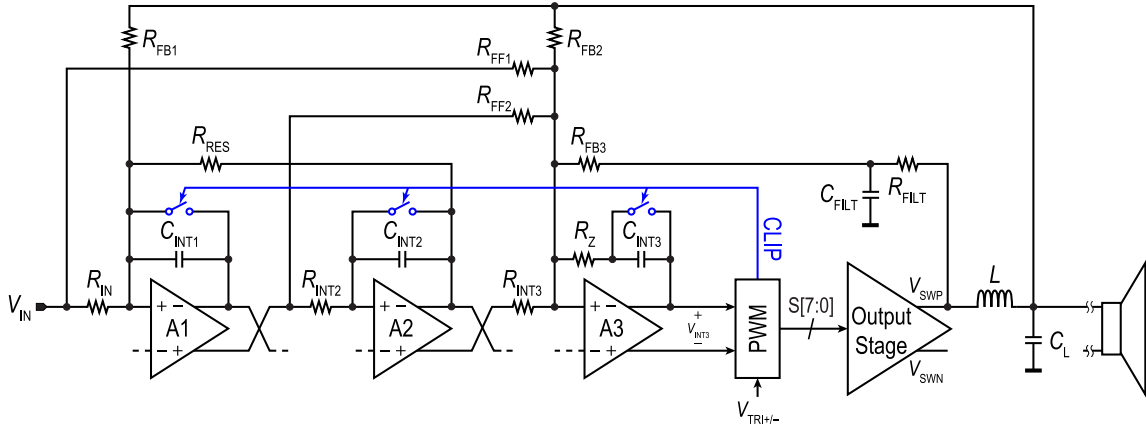


Fig. 9. Circuit implementation of the loop filter.

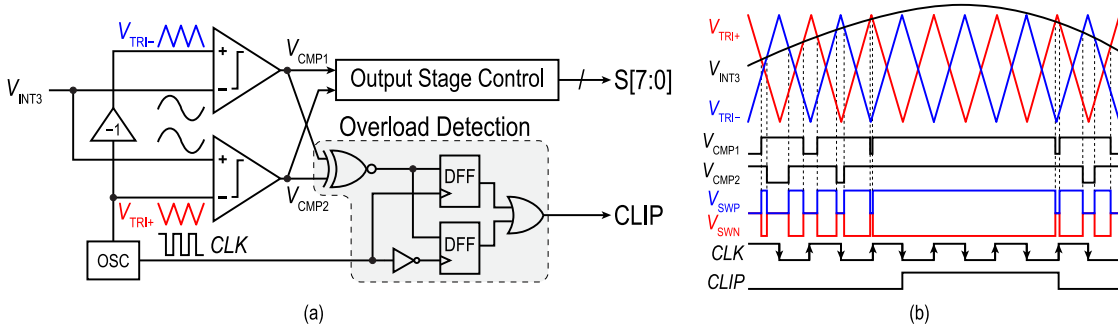


Fig. 10. (a) Block diagram of the PWM generation with overload detection and (b) its corresponding waveform.

The output stage nonlinearity is suppressed by both the inner loop and the outer loop, resulting in the following NTF:

$$\begin{aligned} \text{NTF}_{\text{OS}}(s) &= \frac{V_{\text{OUT}}(s)}{E_{\text{OS}}(s)} \\ &= \frac{H_{LC}(s)}{1 + \frac{G_{\text{PWM}}K_L}{s} + H_{LC}(s)H_{\text{RES}}(s)H_{\text{PI}}(s)}. \end{aligned} \quad (10)$$

Fig. 7(a) plots $\text{NTF}_{LC}(s)$ and $\text{NTF}_{\text{OS}}(s)$. As shown, LC filter nonlinearity is suppressed by more than 47-dB in-band, and the output stage nonlinearity is suppressed by more than 80 dB. This is advantageous since $|E_{\text{OS}}(s)|$ is higher (about -40 dB according to simulations).

D. f_{LC} Tolerance

The proposed architecture should be robust to $\pm 30\%$ variations in f_{LC} . As shown in Fig. 7(a), such variations do not affect the in-band magnitude of the NTFs. Furthermore, they do not affect amplifier stability since all the poles remain well within the LHP [see Fig. 7(b)].

The loop gain around the output stage is plotted in Fig. 8. With $\pm 30\%$ variations in f_{LC} , the loop bandwidth varies by only $\pm 12\%$ and remains below f_{PWM}/π . The lower phase margin when f_{LC} increases is not a problem since the resulting STF peaking is far beyond the audio band, as shown in Fig. 7(a).

III. CIRCUIT IMPLEMENTATION

A. Loop Filter

Fig. 9 shows a simplified schematic of the loop filter. The implementation is fully differential, and active RC integrators are used for high linearity. Note that, in the feedback-after- LC architecture, high-frequency content at the amplifier's output is heavily attenuated by the LC filter, significantly relaxing the speed and linearity requirements on the outer loop filter. The first-order LPF in the inner loop is implemented by R_{FILT} , C_{FILT} , and R_{FB3} .

To realize the target RC time constants after a one-time foreground calibration, the loop filter's capacitors are implemented as 2-bit switchable banks. As a result, the tolerable f_{LC} range can be centered around the nominal f_{LC} of 85 kHz despite process variations. In contrast to the coefficient calibration of the digital filter in [4], this calibration does not have to be tailored to a particular LC filter as long as f_{LC} is within the tolerable range.

B. Overload Detection and Recovery

When the amplifier is overdriven, the integrators in the fifth-order loop will saturate, and their outputs will clip. As a result, an audible settling transient, dictated by the loop dynamics, will occur when the overdrive is removed.

To avoid such transients, an overdrive detection block is implemented in the PWM generator, as shown in Fig. 10(a). Due to the feedforward architecture, the integrators in the loop

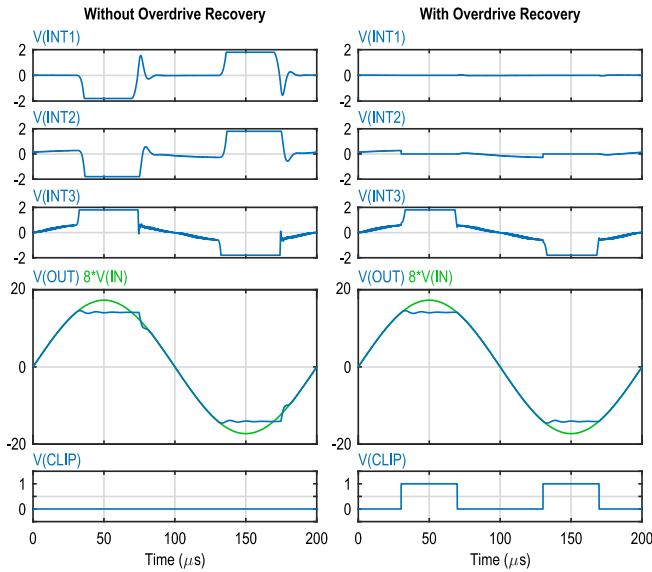


Fig. 11. Simulated waveform of the proposed class-D amplifier with and without overdrive recovery.

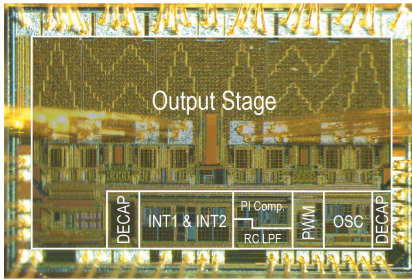


Fig. 12. Die micrograph.

filter only process small error signals during normal operation. Once overdrive is detected, however, the integrator outputs are reset to zero. After the overdrive is removed, they can then return quickly to the small error signals that occur during normal operation, as shown in Fig. 11, resulting in smooth overdrive recovery.

This class-D amplifier employs a three-level PWM scheme that maintains a constant output common-mode voltage [3]. The waveforms in the pulsewidth modulator and the overdrive detection circuit are shown in Fig. 10(b). During the normal operation, the PWM input V_{INT3} lies between the peaks of the triangular wave, and the two comparator outputs have opposite polarity at the peaks of either triangular wave. Therefore, overdrive can be detected by first xnor-ing the comparator output and then sampling the result at the peaks of both triangle waves, giving the CLIP signal.

IV. MEASUREMENT RESULTS

A prototype chip is fabricated in a 180-nm BCD process and occupies an active area of 5 mm^2 (see Fig. 12). The output stage employs a 14.4-V supply. The loop filter and PWM operate with a 1.8-V supply.

A. Audio Performance

The audio performance is measured with an APx555 analyzer. Fig. 13 shows the measurement setup. To estimate the

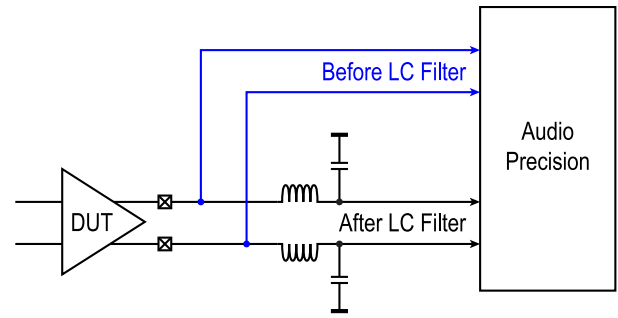


Fig. 13. Measurement setup for estimating LC filter nonlinearity.

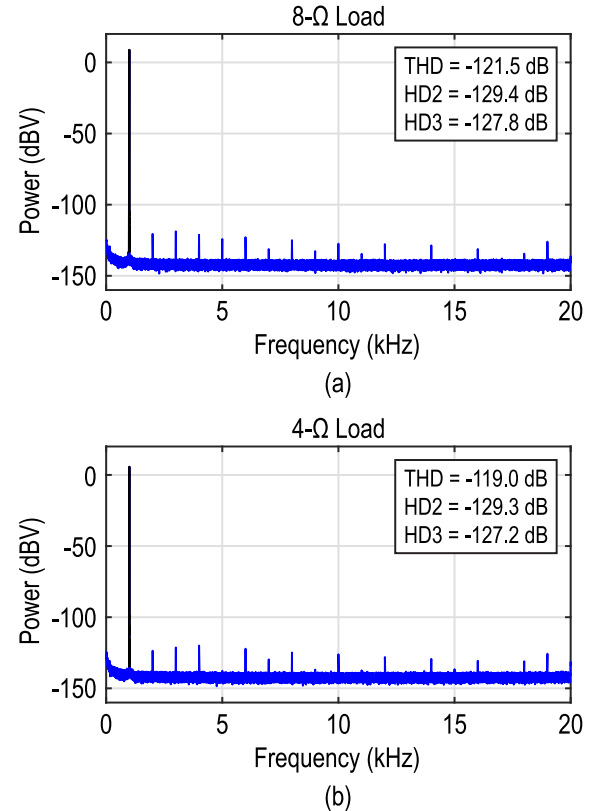


Fig. 14. Output spectra for (a) 8- and (b) 4-Ω loads.

magnitude of LC filter nonlinearity, the THD+N at the LC filter input is measured as well. This waveform includes the pre-distortion applied by the feedback loop to linearize the LC filter output.

Fig. 14 shows the output spectrum after the LC filter at an output power of 1 W with a 1-kHz sine wave input. The amplifier achieves a THD of -121.5 and -119.0 dB, when driving an 8-Ω load and a 4-Ω load, respectively.

The solid lines in Fig. 15 show the measured THD+N with a 4-Ω load as the input amplitude is swept. The measurement is repeated for the three inductors listed in Table II, which has different current dependencies, and for input frequencies of both 1 and 6 kHz. The difference in THD+N due to the inductors (measured right before clipping) is only 1.1 dB for the 1-kHz input and 3 dB for the 6-kHz input.

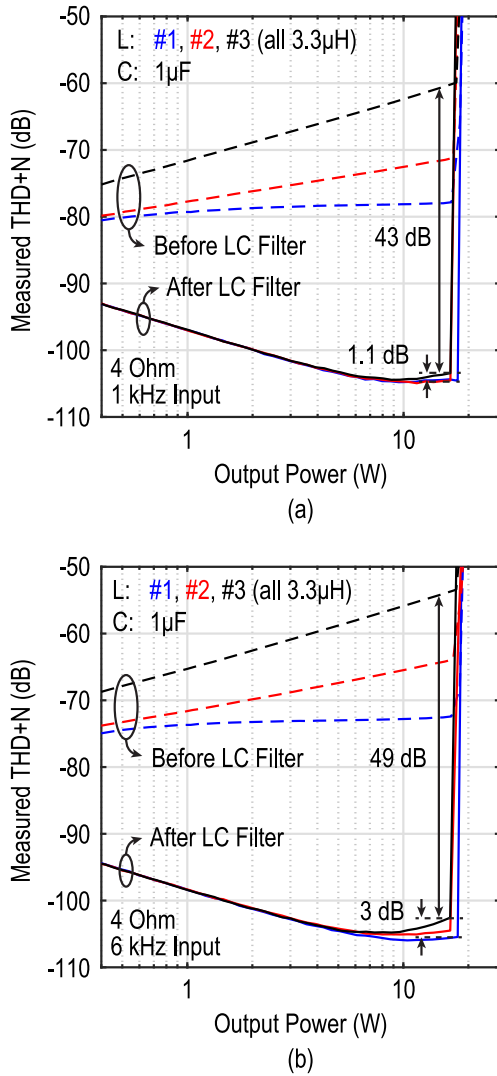


Fig. 15. THD+N for (a) 1-kHz input and (b) 6-kHz input.

TABLE II
INDUCTORS USED IN THE MEASUREMENT FOR FIG. 15




			
Vendor	Würth	Würth	Murata
Part No.	7443340330	74437346033	FDSD0420-H-3R3M=P3
Dimensions (mm)	8.4x7.9x7.2	7.3x6.6x2.8	4.2x4.2x2

Fig. 16 shows the measured overdrive recovery behavior. The smooth recovery confirms the effectiveness of the overdrive recovery scheme.

B. Suppression of *LC* Filter Nonlinearity

As shown in the dashed lines in Fig. 15, the nonlinearity of all three *LC* filters is above -80 dB, with the worst being close to -55 dB for a 6-kHz input. The class-D amplifier suppresses the *LC* filter nonlinearity by up to 49 dB. As expected, the

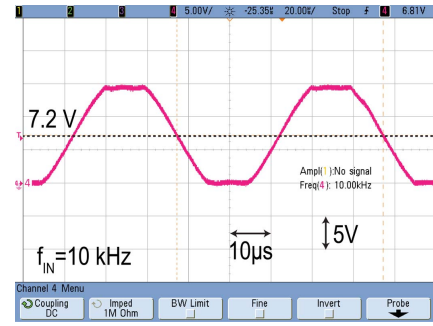


Fig. 16. Measured overdrive recovery transient.

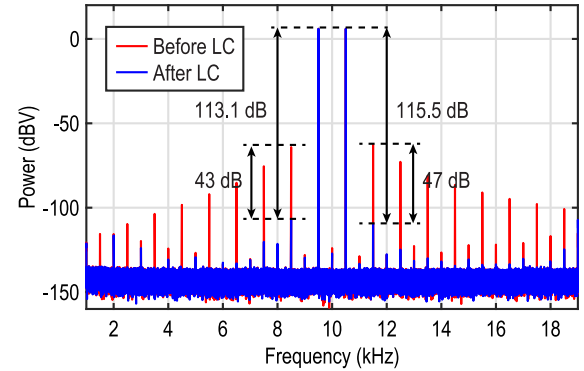


Fig. 17. Output spectra from a two-tone test.

smallest inductor has the largest nonlinearity, but, due to the feedback-after-*LC* architecture, it only degrades the overall THD+N by some 3 dB.

Fig. 17 shows the spectra of the signals before and after the *LC* filter obtained from a two-tone test. The signal before the *LC* filter contains significant intermodulation products that spread across the entire audio band. In a conventional class-D amplifier, with feedback *before* the *LC* filter, a similar spectrum would have appeared across the load. In contrast, for the proposed architecture, the intermodulation products at the *LC* filter output are significantly suppressed, and the residual IM3 is -113.1 dBc.

C. Variations on Loading and f_{LC}

Besides load resistance, practical speakers also present an inductive impedance to the class-D amplifier. To verify the robustness to load impedance variations, the THD+N measurement is performed for load inductances varying from 0 to 330 μ H. As shown in Fig. 18, the high linearity performance is maintained. Fig. 19 shows the robustness of the class-D amplifier to f_{LC} variation from 62 to 106 kHz, obtained by intentionally varying the *LC* filter's capacitance. Across six samples, the variation in THD+N is less than 3 dB.

D. Efficiency and Idle Power

Fig. 20 shows the power efficiency of the prototype as a function of output power. It achieves 91% efficiency for an 8- Ω load and 87% efficiency for a 4- Ω load. It can deliver

TABLE III
PERFORMANCE SUMMARY AND COMPARISON

	This Work		TAS6424 [1]	Karmakar JSSC'20 [2]	Zhang JSSC'21 [3]	Schinkel JSSC'17 [4]	Adduci J. AES'12 [12]
Supply Voltage (V)	14.4		14.4	14.4	14.4	14.4/25	25
R_L (Ω)	8	4	4	4	8	4	4
Efficiency	91%	87%	86%	91%	91%	87%	>90%
THD (dB)	-121.5	-119.0	-	-108.9	-	-	-
THD+N at 1kHz (dB)	-107.1	-105.9	-76.5	-102.2	-107.8	-102.6	-87.9
THD+N at 1kHz (%)	0.0004	0.0005	~0.015	0.0008	0.0004	0.0007	0.004
LC error suppression (dB)	49	0	0	0	0	50*	10
f_{LC} tolerance (kHz)	62 ~ 106	N/A	N/A	N/A	N/A	-	-
SNR (dB-A)	110.0	-	109	109.7	-	-	110
DR (dB-A)	110.8	-	-	-	111.2	115	108
PSRR (dB) (Frequency Range [Hz])	70 ~ 58 (20 ~ 20k)	75 ~ 57 (20 ~ 20k)	70 ~ 62 (20 ~ 20k)	-	88 ~ 60 (100 ~ 20k)	-	-

*Estimated from loop gain

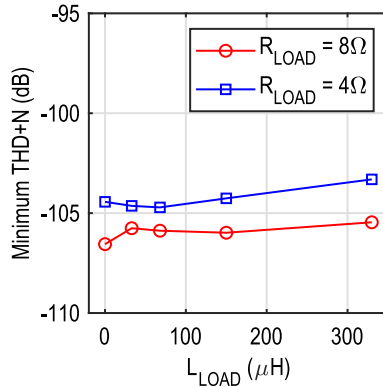


Fig. 18. Peak THD+N versus series load inductance.

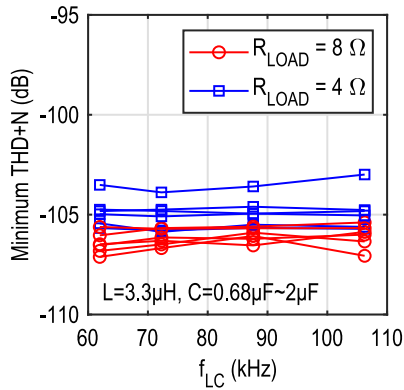


Fig. 19. Peak THD+N versus f_{LC} .

a maximum of 21 W, measured at 10% THD, and consumes 120 mW of idle power.

E. Comparison With Prior Art

Table III summarizes the prototype's performance and compares this work with other state-of-the-art class-D amplifiers. It achieves the best THD, as well as the best THD+N for a 4- Ω load. Last but not least, it suppresses LC filter nonlinearity by 49 dB while being the only work that is robust to a wide variation in f_{LC} .

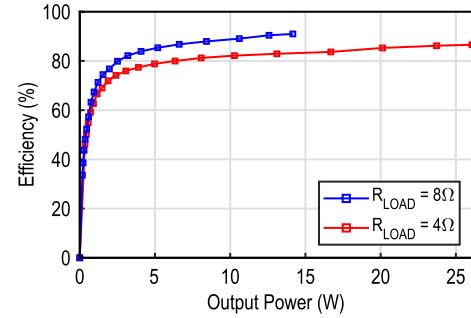


Fig. 20. Power efficiency versus output power ($L_{LOAD} = 0$).

V. CONCLUSION

A dual-loop analog-input class-D amplifier with feedback after the LC filter is presented. An inner loop dampens the LC poles, improves f_{LC} tolerance, and suppresses output-stage nonlinearity, while an outer loop further suppresses both LC filter and output-stage nonlinearity. A prototype implemented in a 180-nm BCD process achieves -121.5-dB THD and 49-dB suppression of LC filter nonlinearity. It is also robust to $\pm 30\%$ f_{LC} variation, thereby enabling the use of small and low-cost LC components in high-linearity class-D amplifiers.

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