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A 200dB FOM 4-5GHz Cryogenic Oscillator with an Automatic Common-Mode Resonance Calibration for Quantum Computing Applications

Low-power, low phase noise (PN) cryogenic frequency generation is required for the control electronics of quantum computers. To avoid limiting the performance of quantum bits, the frequency noise of a PLL should be <1.9kHz$_{rms}$ [1]. However, it is challenging for RF oscillators, as the heart of frequency synthesizers to satisfy such a requirement at cryogenic temperatures (CT), since 1) white noise in nanoscale CMOS devices is limited by temperature-independent shot noise; 2) the transistor 1/f noise is much higher, resulting in the oscillator PN being dominated by the 30dB/dec region [1].

Adjusting the oscillator common-mode (CM) resonance at twice the oscillation frequency (F_O) is a powerful technique to minimize both white and 1/f noise upconversion in RF oscillators [2-3]. This condition has been previously satisfied even with a single tank by accurately modeling of CM inductance (L_{CM}) and *manually* controlling the ratio of single-ended to differential-mode (DM) capacitance ($X=C_C/C_D$) [2-3]. However, in the presence of PVT variations, the parasitic capacitance of the oscillator's core devices and of the switches in the capacitor banks change dramatically, shifting the expected frequency of the CM resonance. Consequently, the oscillator PN degrades significantly if the same control bits for the DM and CM capacitor banks (b_{CD}, b_{CC}) are used over PVT variations. This penalty is even more severe at CT, since the parasitic single-ended capacitances change significantly due to carrier freeze-out in the substrate. In this paper, we propose a digital calibration loop to automatically adjust the configuration of the DM and CM capacitor banks to ensure that the oscillator always operates near its optimum performance, suppressing the oscillator PN at 100kHz offset frequency (Δf) by >10dB over the temperature range from 4K to 300K.

Fig.1 shows the block diagram of the proposed calibration loop and the oscillator schematic. Due to the auxiliary CM resonance at $2F_O$, the oscillator FOM, the tank's CM impedance and thus the amplitude of the 2nd harmonic component of the oscillation waveform (A_{H2}) are simultaneously maximized for the same X value. Hence, the calibration goal is to find the optimum b_{CD} and b_{CC} codes in which A_{H2}

is maximized. At the beginning of the calibration, the CM capacitor bank is kept off, while b_{CD} is set to reach the desired frequency, resulting in the lowest possible X. The 2nd harmonic of the oscillation voltage is extracted at the common node of differential capacitors C_{PD}. A peak detector with a gain of K_{PD} then produces a DC voltage (V_{PD}) proportional to A_{H2}. V_{PD} is compared with the output of an 8-bit DAC (V_{DAC}), and the result is fed to a finite-state machine (FSM). For now, suppose that V_{DAC} is set exactly to the maximum V_{PD} ($=K_{PD}\cdot A_{H2,max}$). Initially, X is set at its minimum, and the tank configuration is not optimum; thus $V_{PD}<V_{DAC}$ and comparator output (D_{CP}) is one. Consequently, the FSM increases X via reducing b_{CD} by 1-LSB and increasing b_{CC} by 2-LSBs. In this way, the tank's total capacitance (C_C+C_D) and thus F_O remain almost constant during the calibration. This procedure continues until $V_{PD}\geq V_{DAC}$ and D_{CP} becomes zero, indicating that the current b_{CD} and b_{CC} states are near to the optimum.

The maximum V_{PD}, and hence the required V_{DAC} depend on PVT, tank's CM quality factor (Q_{CM}), and F_O. Therefore, a second loop is added to adjust V_{DAC}, accordingly. Initially, V_{DAC} is intentionally set to a voltage level that is safely higher than the maximum possible V_{PD}. Hence, D_{CP} is always 1, resulting in X being swept from its minimum to maximum. The FSM then lowers down V_{DAC} by 1-LSB and resets X to its minimum possible value again. This process is repeated until D_{CP} becomes zero for the first time. At this point, the DAC and b_{CD} and b_{CC} states are frozen. The calibration circuit is then shut down to save power. In this design, the resistive DAC, comparator, and FSM emulate the behavior of an ADC while minimizing area and complexity. The flow chart of the proposed calibration loop and its related waveforms are shown in Fig.2.

To satisfy the CM resonance condition, C_C/C_D should be adjusted to (1+k)/(3-5k), where k is the coupling factor between the tank inductors [1]. Prior works employed coils with an even number of turns (either as the tank main inductance [2] or a transformer's secondary windings [3,4]) to achieve k>0, allowing a large C_C. However, to attain a low PN at a low supply voltage, the tank's DM impedance should be reduced, thus advocating for the use of a single-turn inductor. Since in that case, k becomes negative, C_C, which includes parasitics, reduces to impractically small values. To minimize the unwanted magnetic

coupling, we use two individual coils placed orthogonally (see Fig.3). Furthermore, the center tap of the inductor is now much closer to the source of the core devices, thus alleviating parasitic L_{CM} by securing the shortest return path for the CM current. For the same inductance, the area of the proposed inductor is also ~30% lower compared to that of the conventional spiral one, but with a slightly lower DM and CM quality factor due to the partial magnetic-flux cancellation inside each half inductor.

In the peak-detection block in Fig.3, a buffer isolates the oscillator from the detector switching activities. Its output is then connected to the detector core, consisting of an NMOS transistor (M_2) and a capacitor (C_1). The voltage drop on the buffer load resistance (R_1) is designed to be about the threshold voltage of M_2. Hence, M_2 acts as a switch and only turns on in the negative half cycle of the buffer's output (V_{BUF}). During this phase, M_2 ON resistance and C_1 form a low-pass filter to extract the average value of V_{BUF} negative cycle, leading to a peak detection gain of ~$1/\pi$. Since the fundamental tone of V_{BUF} is at $2F_O$ (~10GHz), M_2 and C_1 are sized to achieve a few hundreds of MHz corner frequency to provide enough attenuation for V_{BUF} high-frequency components and to guarantee the loop settling within ~20nsec, as shown in Fig.3. Another amplifier further boosts the desired signal to relax the requirements on the DAC resolution and the comparator noise. K_{PD} of the entire peak detection block is ~6. The simulated noise of the calibration loop referred to the input of the peak detector is ~90μV_{rms}, ensuring that the calibrated PN is within 1dB of the optimum, as evident from Fig.1 left.

Fabricated in 40nm CMOS, the 0.15mm^2 oscillator consumes 4.3mW and 5.2mW at 300K and 4K, respectively (excluding 0.4mW of the calibration loop). The oscillator PN is measured over all possible b_{CC} and b_{CD} states while disabling the calibration to find the best and worst PN profiles for different frequencies. The calibration loop is then activated to investigate the effectiveness of the proposed technique. Fig.4 and 5 show the measured oscillator PN across its tuning range (TR) at 300K and 4K, respectively. The calibration loop successfully finds the optimum b_{CC} and b_{CD} codes, suppressing the oscillator PN at Δf=100kHz by 10dB at 300K and 12dB at 4K. It also reduces the 1/f noise corner from 1MHz(10.5MHz) to 130kHz(1.3MHz) at 300K(4K).

Compared to prior art (Fig.6), the FOM achieved at room temperature is limited by the low supply voltage and by the lower tank's quality factor, due to the use of a smaller single-turn inductor and a larger capacitor bank (see Fig.7). However, our work is the only one offering automatic CM resonance calibration, while requiring a negligible area overhead ($0.01mm^2$). Thanks to the calibration loop and the optimization of the inductor layout, this work achieves a frequency noise of 1.6kHz and an FOM of 200dB at 4K. It also shows 4× lower 1/f corner, and 6dB higher FOM, compared to the cryogenic oscillator in [1]. The proposed technique will potentially enable the realization of cryogenic low-power low-jitter frequency synthesizers required for the control of quantum computers.

References

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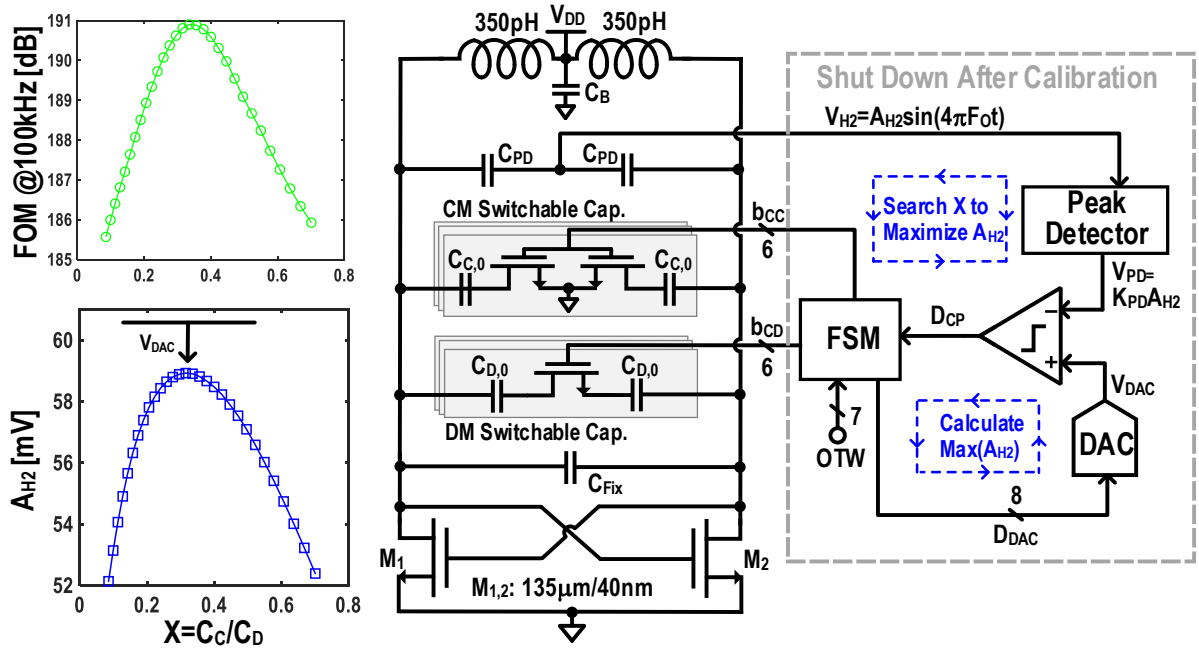

Fig. 1: Simulated A_{H2} and FOM versus X for a class-D/F_2 oscillator (left); the block diagram of the proposed calibration (right).

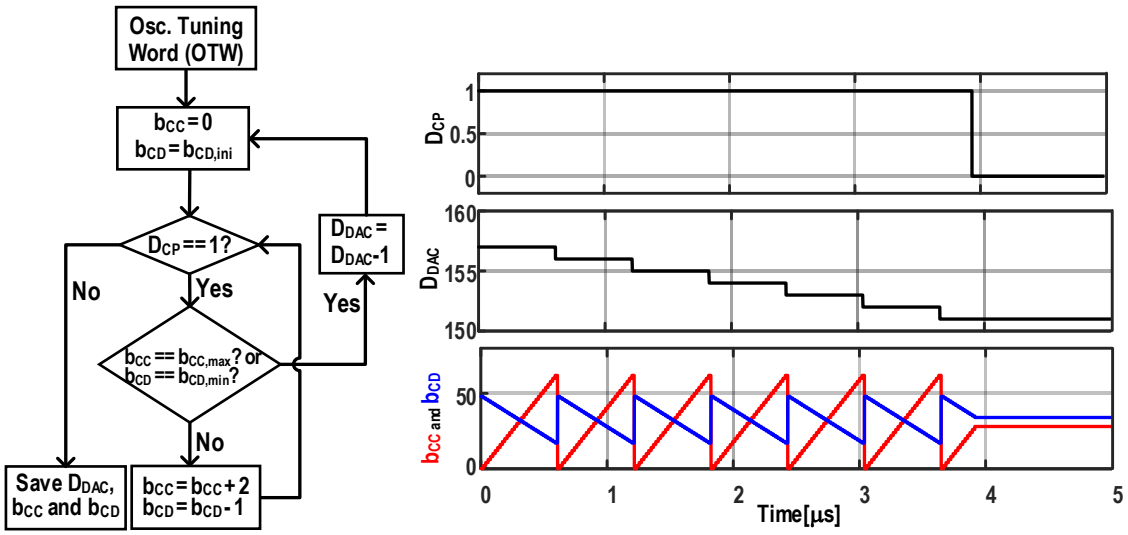

Fig. 2: Calibration flowchart (left); the comparator output, DAC code, and the control bits of CM and DM capacitor bank during calibration (right).

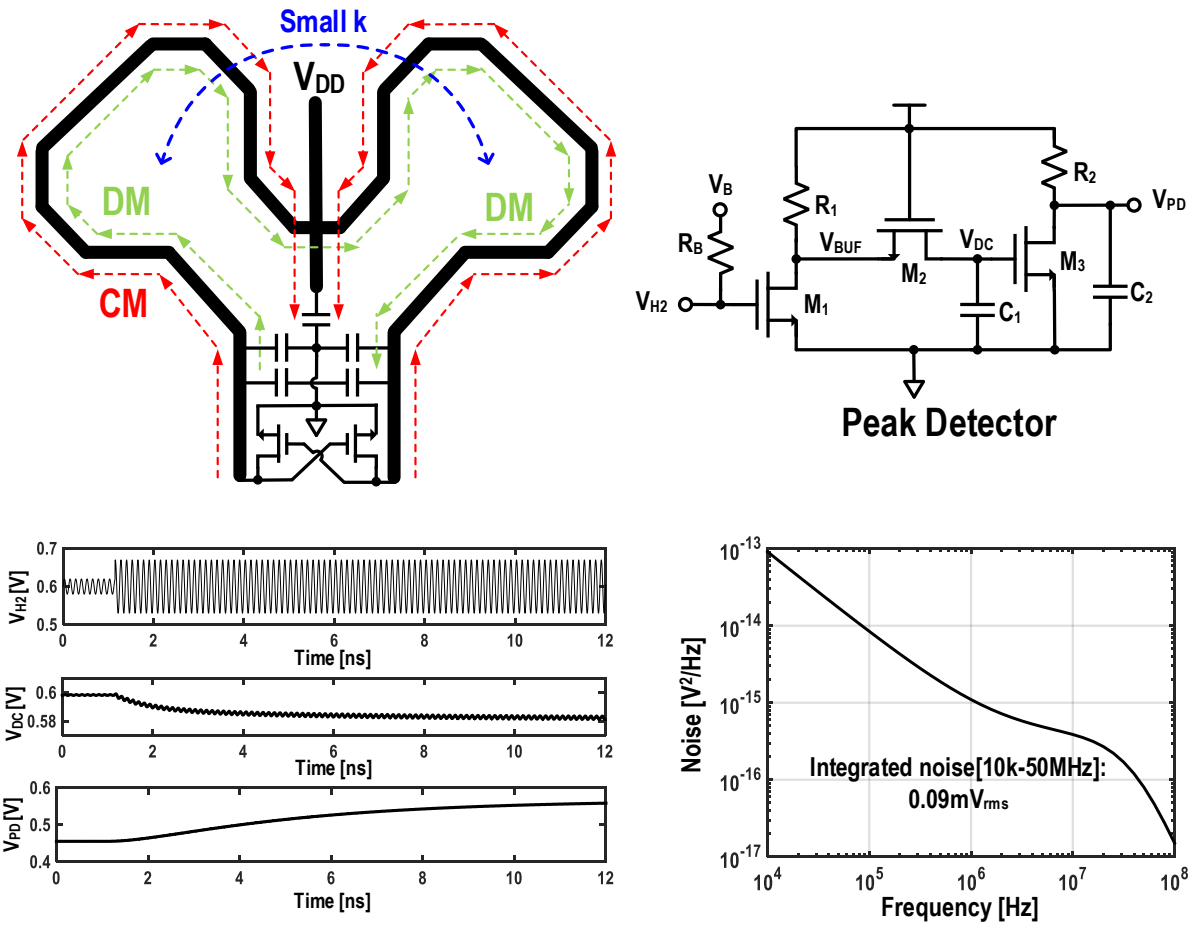

Fig. 3: Oscillator floor plan with the proposed inductor (top left); the peak detector schematic (top right), and its simulated settling behavior (bottom left); the simulated input referred noise of the calibration loop (bottom right).

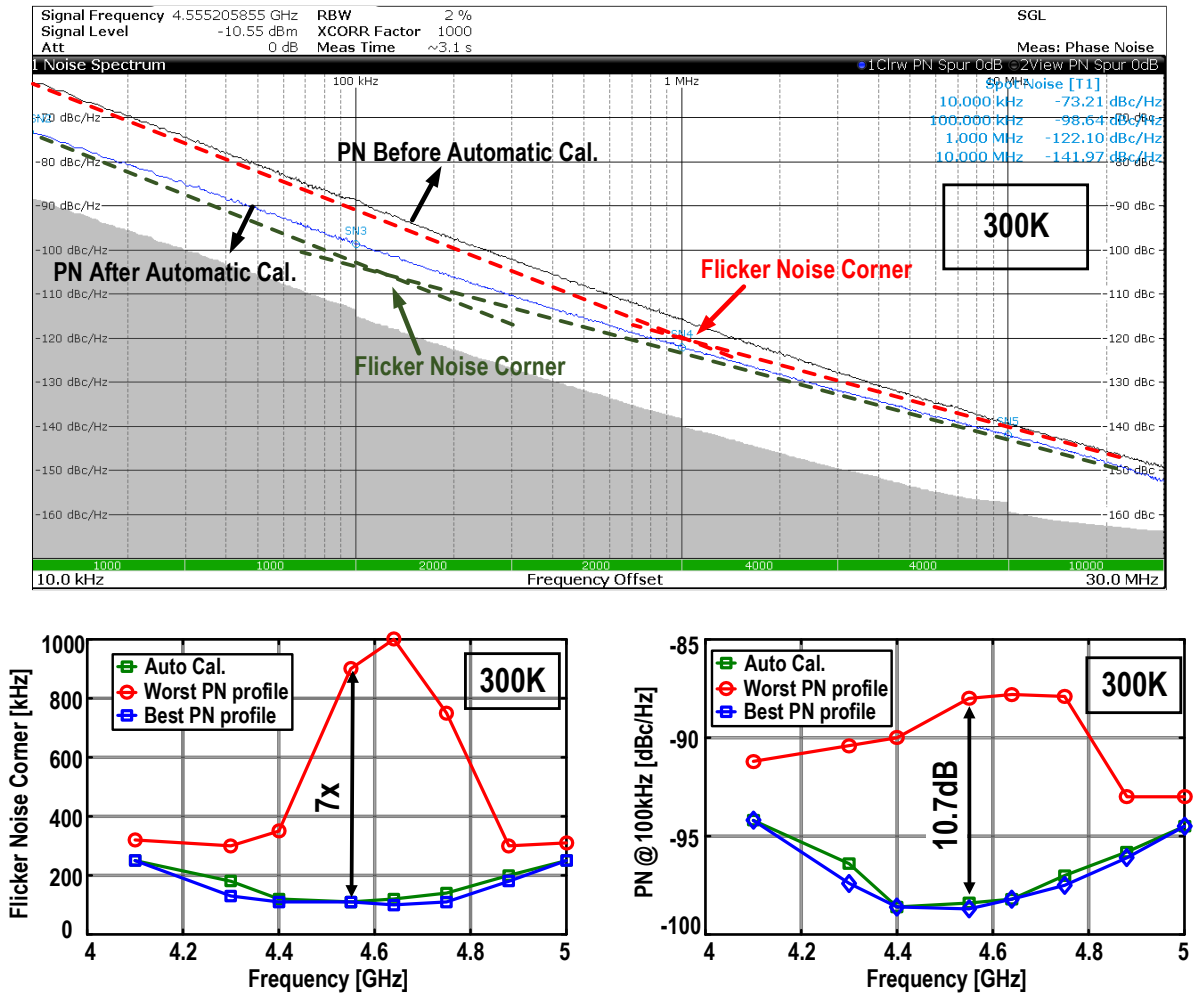

Fig. 4: Oscillator measured PN before and after calibration at 4.56GHz (top); Oscillator's performance over its tuning range for the worst, best, and calibrated phase noise profiles (bottom) at 300K.

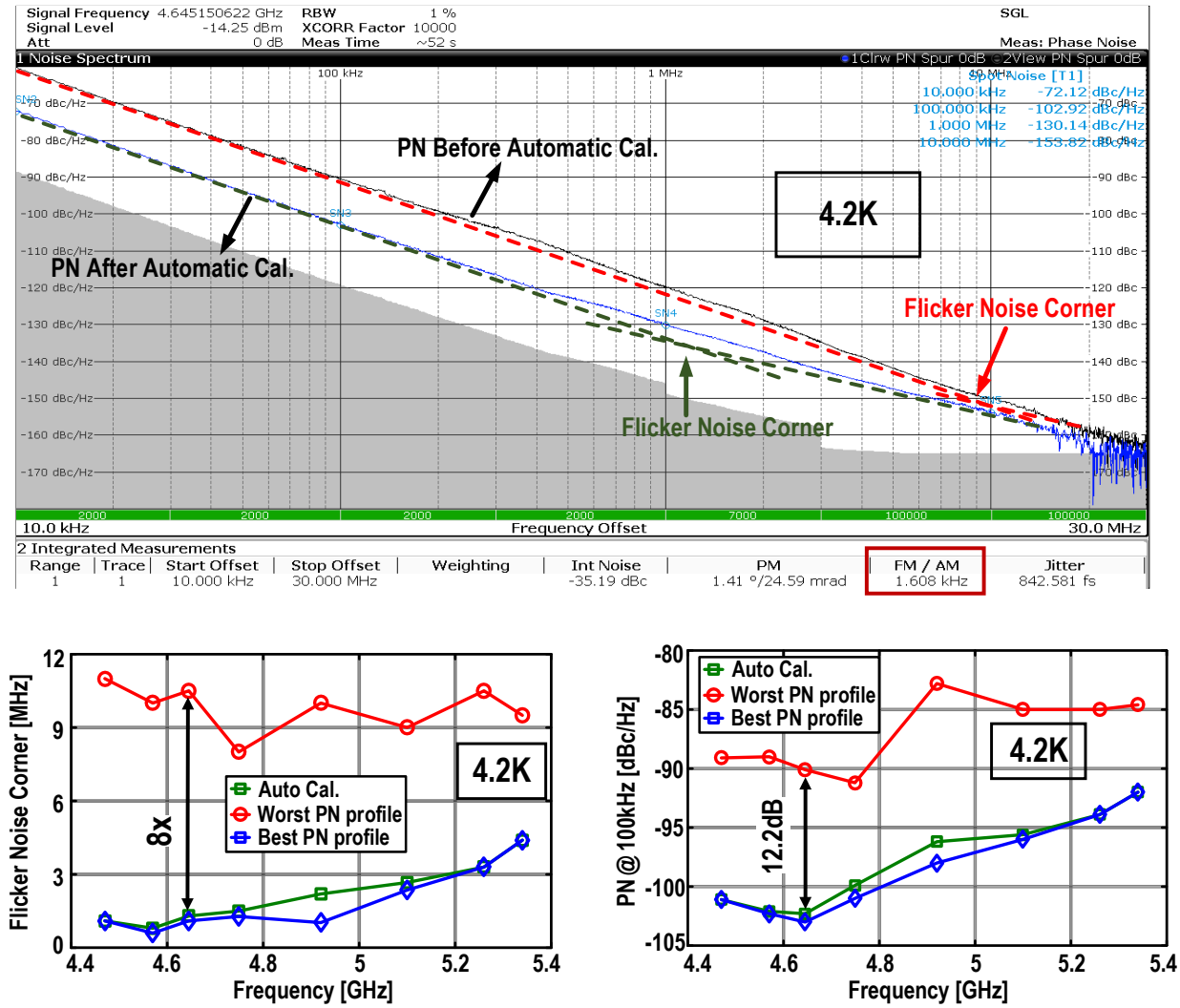

Fig. 5: Oscillator measured PN before and after calibration at 4.65GHz (top); Oscillator's performance over its tuning range for the worst, best, and calibrated phase noise profiles (bottom) at 4.2K.

	This Work		ISSCC'2017 [1]	ISSCC'2015 [2]	ISSCC'2015 [3]	ISSCC'2018 [4]	JSSC'2015 [5]
Osc. Topology	NMOS CM Resonance Class-D/F_2		NMOS CM Resonance Class-$F_{2,3}$	NMOS Implicit CM Resonance	NMOS CM Resonance Class-$F_{2,3}$	CMOS CM Resonance Inverse Class-F	NMOS $2f_{LO}$ Tail Tuning
Temperature [K]	300	4.2	4.2	300	300	300	300
Frequency [GHz]	4.6	4.65	6.3	3.3	7	4.51	8.4
Supply Voltage [V]	0.5	0.6	1	0.9	1	0.6	1.5
Tuning Range	4.1-5 (19.8%)	4.4-5.3 (18.6%)	5.8-7.3 (25%)	2.85-3.37 (27.2%)	5.4-7 (25%)	3.49-4.51 (25.5%)	7.4-8.4 (12.7%)
Power [mW]	4.3	5.3	12	6.8	10	1.14	20
PN [dBc/Hz] @100kHz/1MHz/10MHz	-99.3/ -123.1/ -143.1	-102.9/ -130.2/ -153.8	-94/ -120/ -149	-106*/ -129.5*/ -150.2*	-102.1/ -124.5/ -144.5	-98.5/ -123.7*/ -143.7	-88*/ -118*/ -146.8
FOM [dBc/Hz] @100kHz/1MHz/10MHz	186.2/ 190/ 190	189/ 196.3/ 200	179.2/ 185/ 194	188/ 191.5/ 192.2	188.9/ 191.4/ 191.4	191/ 196.2/ 196.2	173.5/ 183.5/ 192.3
Flicker Corner [kHz]	130	1300	5700	200	130	300	600
Technology	40nm		40nm	28nm	40nm	65nm	55nm
Osc. Area [mm^2]	0.14		0.13	0.19	0.13	0.14	0.17
Cal. Area [mm^2]	0.01		NA	NA	NA	NA	NA
Inductor	One Turn		1:2 XFMR	Two Turns	1:2 XFMR	2:4 XFMR	One turn+tail Ind.
Common-mode Resonance Cal.	Auto		Manual	Manual	Manual	Manual	NA

*Estimated from the measured phase noise plot of the oscillator

Fig. 6: Table of comparison with prior art employing the common-mode resonance technique.

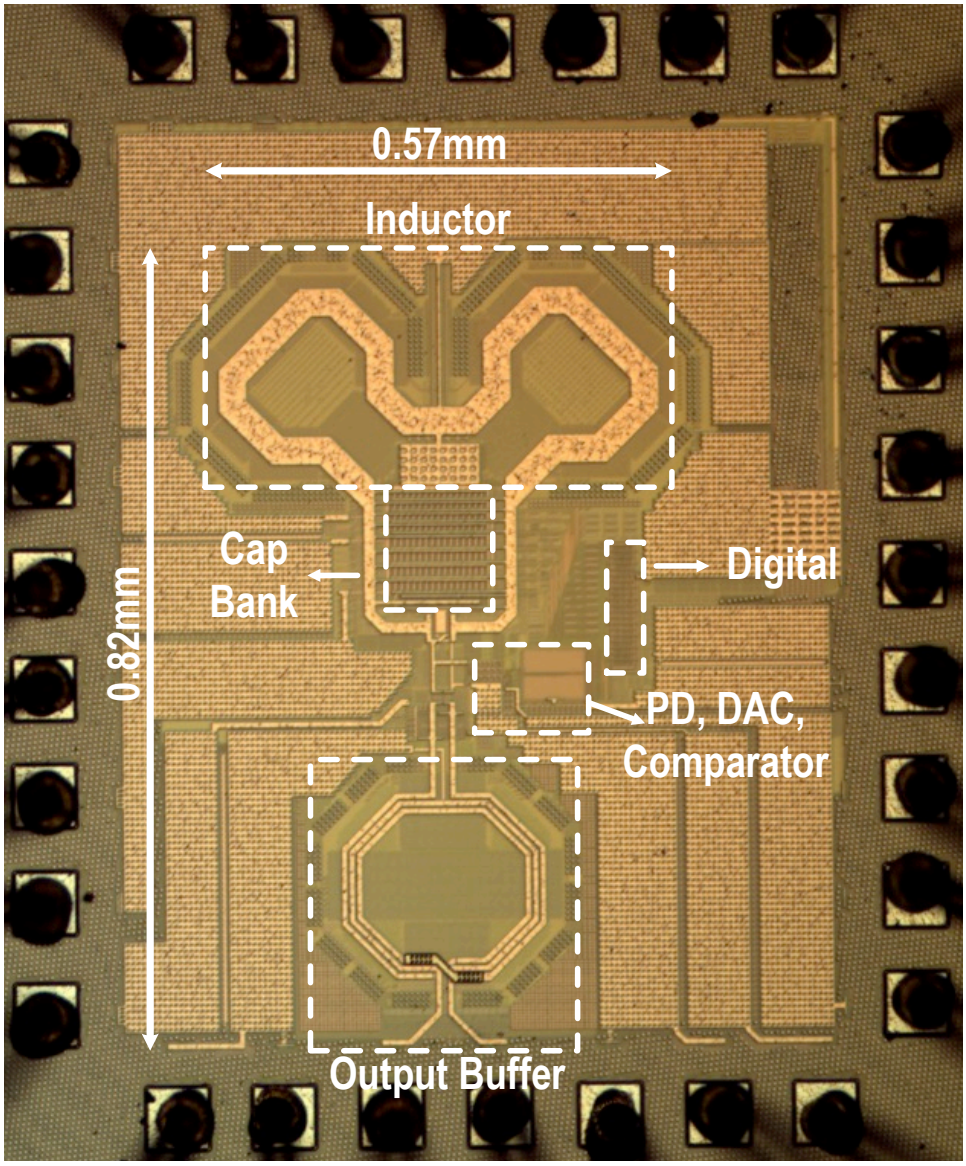

Fig. 7: Die micrograph.

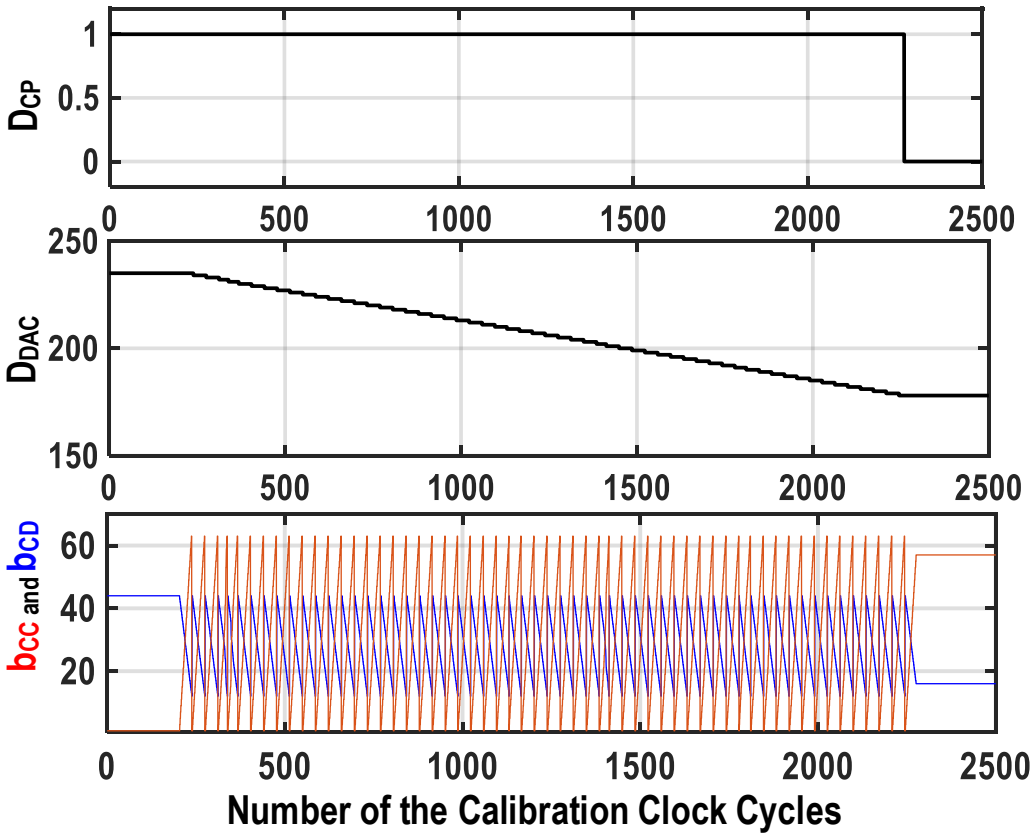

Fig. S.1: Measured settling of the calibration loop. For this measurement, instead of the regular 50MHz clock frequency, a very low-speed clock (0.5kHz) is used for the calibration loop to allow monitoring of the comparator output, DAC code, and b_{CC} and b_{CD} states during the calibration via an SPI link. The calibration loop successfully settles from an initial setting (1, 44) to the optimized b_{CC} and b_{CD} states (57, 16).

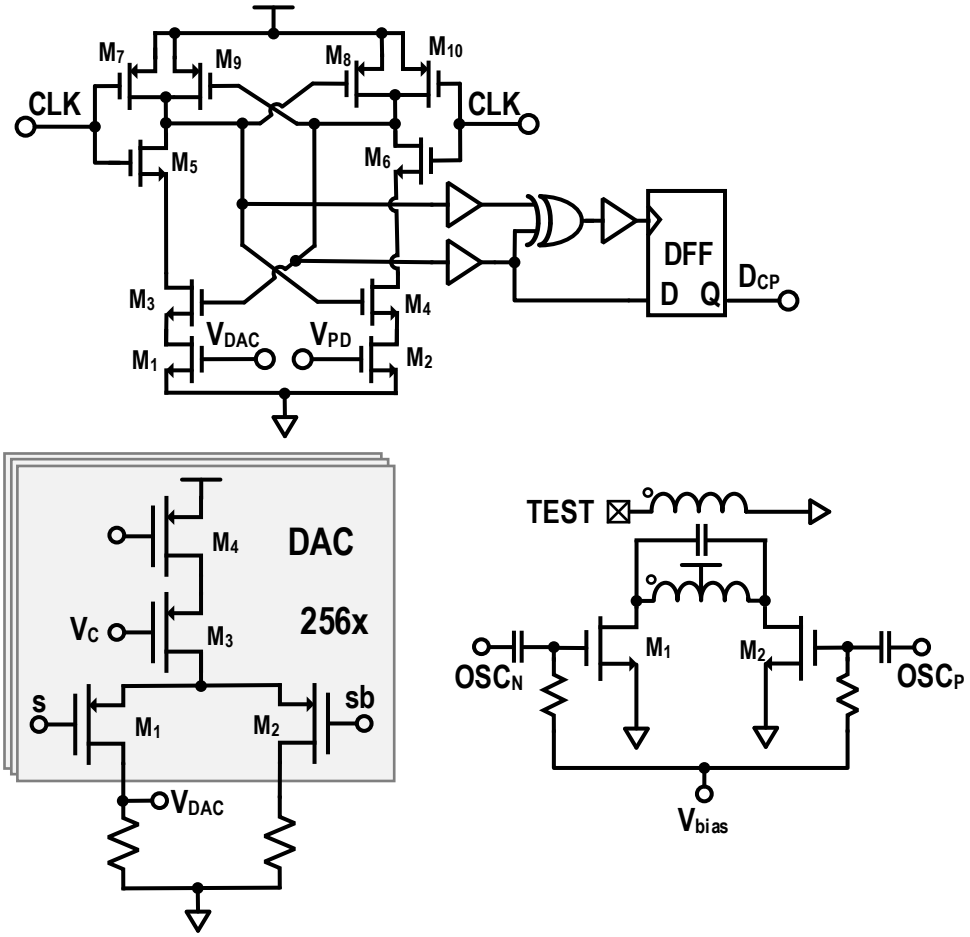

Fig. S.2: Schematics of the comparator, the current steering cell of the 8-b DAC, and the output buffer.

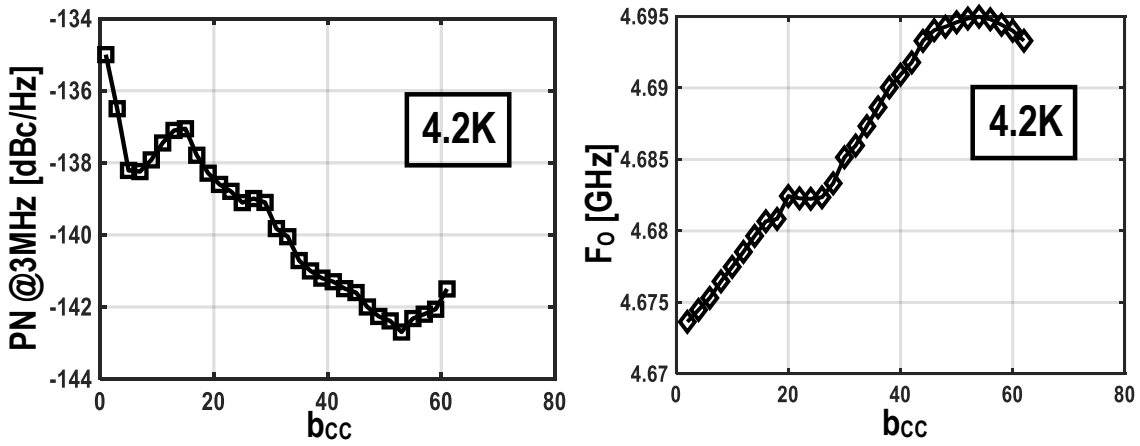

Fig. S.3: Measured PN and oscillation frequency (F_O) versus b_{CC} while sweeping $X=C_C/C_D$ at 4.2K. At each sweep step, b_{CC} is increased by 2-LSBs and b_{CD} is reduced by 1-LSB. In this way, F_O remains almost constant during the calibration. When this technique is employed in a PLL, F_O is first roughly adjusted by the coarse frequency selector, this calibration is then run to find the optimum X, and finally PLL locks to the desired frequency by using tracking bank.