Integrated Transceiver Circuits for Catheter-Based Ultrasound Probes and Wearable Ultrasound Patches

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Integrated Transceiver Circuits for Catheter-Based Ultrasound Probes and Wearable Ultrasound Patches

Mingliang Tan

Integrated Transceiver Circuits for Catheter-Based Ultrasound Probes and Wearable Ultrasound Patches

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chair of the Board for Doctorates

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Ultrasound imaging for medical diagnostic was first introduced in 1947 by Austrian neurologist Karl Theo Dussik [1]. After decades of developments, ultrasound imaging is a well-established imaging modality in clinical practice [2]. The diagnosis of cardiovascular diseases (CVDs) also benefits from the developments of medical ultrasound. CVDs are a general designation of a group of disorders related to the heart and blood vessels, such as coronary heart disease and congenital heart disease. According to the World Health Organization (WHO), approximately 17.9 million people died from CVDs in 2016, which is around 1/3 of all global deaths [3]. To reduce the death rate, early diagnosis and treatment are crucial. Surgical treatment and early diagnosis both rely on a good understanding of the pathophysiology of CVDs by visualizing the heart and its vasculature. Compared to imaging modalities like nuclear scintigraphy, magnetic resonance imaging (MRI), computed tomography (CT), ultrasound imaging is safe and cost-effective and can provide real-time images to guide percutaneous interventional procedures with a reduced procedure time [4].

Conventionally, ultrasound imaging is performed using a handheld probe connected to a cart-based imaging system. For instance, a transthoracic echocardiography (TTE) probe is placed on the chest of the patient to visualize the heart [5]. However, due to the limited penetration depth and interference of the ribs and lungs, the image quality provided by TTE is in some cases not sufficient to obtain clear cardiac structures. To enable minimally-invasive procedures which require long, thin, and flexible tubes or catheters threaded into the heart,

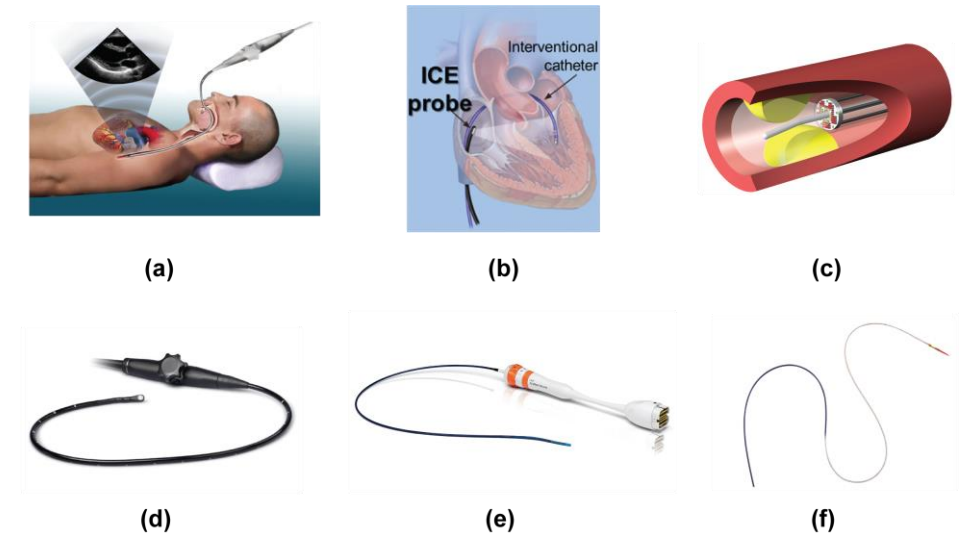

Figure 1.1 Conceptual diagram of (a) transesophageal echocardiography (figure reproduced from piedmontcardiovascular.com); (b) intra-cardiac echocardiography (ICE); (c) intravascular ultrasound (IVUS); (d) TEE probe (Oldelft Ultrasound, the Netherlands); (e) ICE catheter (Siemens ACUSON AcuNav ICE catheter); (f) IVUS catheter (Philips Eagle Eye)

ultrasound images obtained closer to the heart or even from inside the heart are essential for the doctors to have a clearer picture on the heart condition during the procedures. As such, an ultrasound probe that is mounted on the tip of the catheter, *a.k.a.* catheter-based probe, is necessary, which, however, brings technical challenges in terms of electronics, catheter assemble, etc.

In addition to its application in the diagnosis of CVDs, ultrasound imaging has also great potential in applications that need continuous monitoring, such as bladder-volume monitoring [6], overnight monitoring of sleep apnea events [7], treatment of chronic wounds [8]. For such monitoring applications, conventional handheld probes that are connected to a bulky and expensive cart-based imaging system controlled by a well-trained sonographer are not suitable. In recent years, portable probes connecting with mobile devices have been introduced as an alternative [9, 10]. However, due to their limited battery capacity, such devices can only serve for diagnosis during several hours. Moreover, they still require manual operation. To monitor body parameters continuously without aid from caretakers, wearable ultrasound patches (WUPs) are a promising solution. Compared to wearable body patches based on electrocardiography (ECG) or photoplethysmography (PPG) [11], which measure surface parameters on the skin, WUPs allow for monitoring of health parameters inside the

human body. To build a patch that can be worn on the body for days, efforts in miniaturizing conventional handheld probes are needed.

The focus of this thesis is to utilize integrated circuit (IC) technology in combination with advanced ultrasound transducers to address the shared challenge of catheter-based ultrasound probes and WUP devices, which is the need to interface with an array of transducer elements using compact low-power electronics integrated in the device. To do so, various circuit and system design techniques will be proposed.

1.1.1 Catheter-Based Ultrasound

In contrast with a TTE probe which is placed on the patient's chest, in a transesophageal echocardiography (TEE) probe, shown in Figure 1.1a, a long gastroscopic tube is used to guide the ultrasound transducer into the esophagus through the throat of the patient. Since the human heart is physically close to the wall of the esophagus, this approach reduces the attenuation, so that a better cardiac image can be obtained. However, to operate the TEE probe, sedation or general anesthesia is required and the image quality of the far-field part in the anterior heart is limited [12-13].

To have an even closer "look" at the heart, a minimally-invasive imaging modality called intra-cardiac echocardiography (ICE) has been developed [14-16]. As shown in Figure 1.1b, the ultrasound transducer array is mounted at the tip of a long, thin, and flexible catheter that is threaded into the heart through the blood vessels. Compared to TEE, ICE only requires conscious sedation and local anesthesia, leading to a shorter procedure time [17]. Since an ICE probe is located inside the heart and works at a higher frequency than TTE (~7 MHz), the image quality is similar or better than that of TEE [18]. However, the small catheter size (8-10 Fr) brings challenges in ultrasound transducer fabrication and catheter assembly.

To obtain images inside the arteries of the heart, another minimally-invasive imaging modality has been proposed, called intravascular ultrasound (IVUS) [19, 20]. IVUS, shown in Figure 1.1c is also based on a flexible catheter but with a smaller diameter and higher operation frequency, hence offering higher imaging resolution. Conventional side-looking (SL) IVUS catheters contain a single-element transducer at the tip of the catheter that is mechanically rotated to obtain cross-sectional images of the artery [20]. To avoid mechanical rotation, which may lead to imaging artifacts, a circular transducer array placed around the catheter tip has been proposed such that the acoustic beam can be steered electronically [21]. However, SL-IVUS probes are not suitable for imaging of vessels that are filled with atherosclerotic lesions, so-called chronic total occlusions (CTO) [22]. For imaging of CTOs, forward-looking (FL) IVUS probes have been developed to obtain images in front of the probe tip. In [23-25], the use of a single-element transducer that is mechanically rotated around the catheter axis to obtain 2-D images has been proposed. To mitigate the sensitivity

to motion artifacts, 2-D transducer arrays have been applied to obtain 3-D volumetric images without mechanical rotation, leading to 3-D FL-IVUS probes [26-27].

The small diameter of the catheters used for ICE and IVUS brings several challenges. First, connecting a 1-D or 2-D transducer array with an imaging system through the long and thin catheter shaft is challenging and labor-intensive. As in many cases the number transducer elements exceeds the number of cables that can be accommodated, efforts are required in reducing the cable-count using application-specific integrated circuits (ASICs) close to the transducer array at the catheter tip [14, 28-30]. Moreover, these ASICs also serve to mitigate the loading effect of the cables, which, when directly connected to small transducer elements, would lead to a significant reduction in signal-to-noise ratio [31]. Since these ASICs need to operate with the stringent size constraints and temperature limitations of a catheter, low-power and compact integrated circuits are required. In this thesis, various techniques at the system and circuit level will be proposed to address these challenges. Their effectiveness has been demonstrated by several prototypes, which will be discussed in the following chapters.

1.1.2 Wearable Ultrasound

Wearable body patches allow for continuous monitoring of body vital parameters and thus have been used by hospitals and caretakers. However, conventional body patches focus on surface body parameters, for instance, IMEC's ECG body patch monitors the heart rate by measuring the electric signals on the skin [11]. Since ultrasound can penetrate the human body harmlessly, a wearable ultrasound patch (WUP) can be used to monitor health-related parameters deep inside the body, opening up various interesting applications: monitoring of the bladder volume [6], measurement of blood pressure [32], therapy of chronic wounds [8] and measurement of the blood flow [33].

Since the WUPs are intended to operate for several days on the surface of the human body, they should be:

- Comfortable: The wearing comfort of a patient is a very subjective item, which can be affected by many factors, for instance, the physical feel of the wearable device and concerns about being embarrassed [34]. WUPs should be small, light, and flexible.

- Conformal: The patch should be made conformal to provide angular coverage over the contact area such that proper acoustic contact can be maintained in the presence of natural movement of the body.

- Energy-efficient: Attached to the surface of the human body, a WUP gets its power from a battery. Due to the limited size and weight of the WUP, the capacity of the

battery would also be very limited. To facilitate continuous monitoring, the electronics in the WUP should be extremely energy efficient.

- Wireless: To enable continuous monitoring, without being restricted the daily movements of the patients, WUPs should be wirelessly controlled and read out.

Efforts towards WUPs have been mainly focused on the design of conformal ultrasound transducer arrays, implemented by either flexible and stretchable materials or conventional rigid transducers mounted on top of a flexible substrate. In [35], a flexible transducer array based on polyvinylidene fluoride (PVDF) is implemented for non-destructive evaluation (NDE) applications. However, PVDF transducers tend to have a relatively low transmit efficiency, limiting their usage in pulse-echo-based imaging. Further developments have been made in flexible piezoelectric micromachined ultrasound transducers (PMUTs) [36] and flexible capacitive micromachined ultrasound transducers (CMUTs) [37]. Both designs are integrated on top of a flexible polydimethylsiloxane (PDMS) substrate for insulation and acoustic impedance matching. In [32], a conformal transducer array based on rigid 1-3 composite piezoelectric materials with soft structural components is proposed for continuous monitoring of blood pressure. Another approach proposed in [38] employs a diced rigid PZT array on top of a Flex PCB to make the device conformal.

Although the abovementioned designs have shown promising results towards future WUP devices, the front-end electronics are still based on bulky and power-hungry off-the-shelf ICs. For instance, in [39], a Verasonics imaging system is applied to connect with a flexible transducer array via cables. The challenges in designing flexible front-end energy- and area-efficient electronics have not been addressed. In this thesis, we present a WUP prototype which integrates transceiver ASICs and a transducer array on a flexible substrate. The proposed low-power ASIC architecture allows for a battery-powered prototype whose effectiveness has been demonstrated electrically and acoustically.

1.2 ASICs for Catheter-based Ultrasound Probes

In a conventional ICE or IVUS probe, the transducer is mounted at the tip of the catheter and connected to an imaging system through a bundle of micro-coaxial cables with a length of ~2 meters [26, 40, 41]. The high-voltage (HV) excitation signals (tens of Volts) provided by the imaging system and the low-voltage (LV) echo signals (several micro-Volts) received by the transducer are both transferred through these long coaxial cables, leading to signal attenuation and distortion. Application-specific integrated circuits (ASICs) integrated closely to the transducer array have been used to reduce these loading effects [28, 42].

Apart from reducing the loading effect of the micro-coaxial cables, ASICs have also been used to reduce the number of cables. For 3-D ICE or 3-D IVUS, a 2-D transducer array with tens or hundreds of elements is needed [26, 40, 41]. Connecting each of them with a micro-

coaxial cable is challenging, labor-intensive, and would lead to a cable bundle that is hard to accommodate in a catheter shaft. The cable-count reduction is done in the ASIC by means of multiplexing [43-46], sub-array beamforming [29, 47], column-row-parallel addressing [48-49], or row-by-row connections [50-51].

There are several challenges in the design and integration of ASICs at the tip of an ultrasound catheter. First, the connections between the ASIC and a 2-D transducer array with a large number of elements are still complex. To address this interconnection challenge, different ASIC-transducer integration schemes have been proposed in recent years. The first approach is to place the ASIC and transducer on the same printed circuit board (PCB) on which transducer elements are connected to the ASIC via PCB traces [52-53]. However, the parasitic capacitance introduced by these connections will introduce SNR degradation and crosstalk. To mitigate these problems, an interposer layer has been employed for the interconnection in [14, 48, 54]. The transducer elements are vertically routed to the ASIC inputs with short interconnects, which reduces the parasitic capacitance significantly. However, this approach requires fine-pitch PCB or interposer technology to create small enough vias for vertical routing. Another approach is to directly integrate the transducer array on top of a pitch-matched ASIC through flip-chip bonding [55-56], a custom metallic interconnect layer [57], or monolithic integration [9, 42].

A second challenge is that the small dimensions of IVUS and ICE catheters impose constraints on the available area for the ASIC. For instance, a typical diameter of an IVUS catheter is less than 2 mm [19, 21], implying that the ASIC dimensions are limited to even less than that. Squeezing the front-end electronics in such a small area is very challenging.

Third, to transfer the echo signals to the imaging system in a robust manner through micro-coaxial cables with large parasitic capacitance, analog cable drivers can be used to match the cable's characteristic impedance for sufficient bandwidth and low signal distortion. However, analog signals are usually sensitive to crosstalk and environmental interference. To avoid that, on-chip ADCs have been implemented to locally digitize the received signals and then transfer a robust digital bit stream to the system side through the micro-coaxial cables [58-59]. However, it is challenging to design the ADC and the datalink that transfers the bit stream within the stringent power and area budget of a catheter-based probe.

The abovementioned challenges in implementing catheter-based probes call for innovations in:

- Compact ASIC-transducer integration schemes to minimize parasitic.
- Compact, low-power HV pulsers and LNAs with TGC functionality to meet the stringent area- and power-consumption budget.
- Power and area-efficient in-probe ADCs and datalink designs to enable robust bit stream transmission through micro-coaxial cables.

In this thesis, two ASIC prototypes will be presented that address these objectives and have been implemented and integrated with transducer arrays for ICE (chapter 2 and 3) probes and FL-IVUS (chapter 4).

1.3 ASICs for Wearable Ultrasound Patches

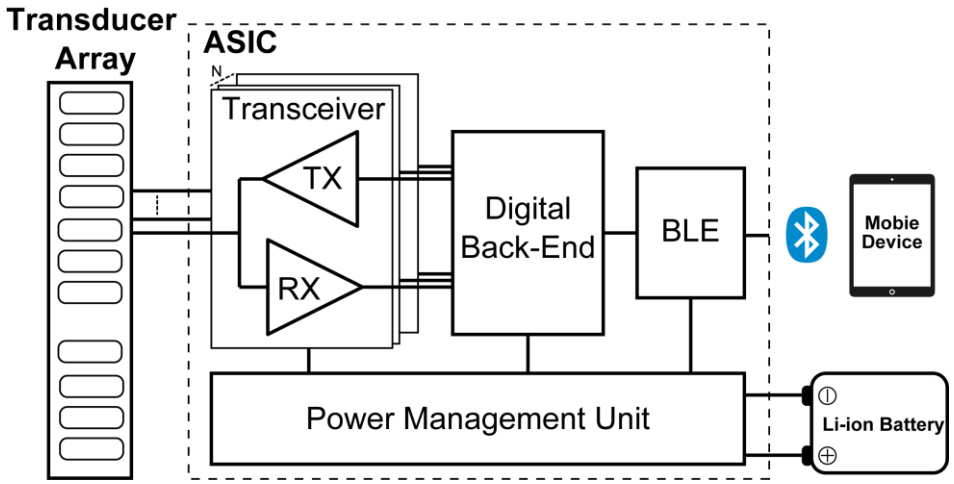

Figure 1.2 Block diagram of an ASIC for a wearable ultrasound body patch

To date, most research on WUPs has focused on the design of flexible or stretchable transducer arrays, which have been characterized using an external imaging system rather than employing electronics integrated in the patch [32, 36, 39, 60-61]. Other WUPs employ discrete commercial ICs integrated with the transducer array on top of a flexible substrate [6, 33, 38, 62-64]. However, due to the limited size and battery capacity of a WUP, it is not realistic to apply conventional off-the-shelf electronics with significant area- and power-consumption overhead. As such, an ASIC optimized in area and power is desirable. Ideally, the ASIC should be designed as a system-on-chip (SoC) in which various building blocks are included. Figure 1.2 shows a block diagram of such an ASIC. It includes an ultrasound transceiver interfacing with the transducer array, a digital back-end processing the echo signal, a power management unit (PMU) providing the ASIC power, and a Bluetooth low-energy (BLE) module communicating with mobile devices. The ASIC, which is directly powered by a battery, is integrated with the transducer array on top of a flexible substrate, e.g., a flexible PCB.

The design of ASICs for WUPs is still a largely unexplored research area. Compared to the ASICs for catheter-based probes, the ASICs for WUPs share similar challenges in terms of ASIC-transducer integration, i.e. limitations in dimensions and power consumption, and the

need for on-chip digitization, calling for innovations in system and circuit implementations. This is addressed in chapter 5 of this thesis, which describes an ASIC with 64 reconfigurable transceiver channels, designed as part of a technology platform for ultrasound patches. The ASIC is able to interface with different types of transducer array, such as a low-frequency (2.5 MHz) CMUT array for a bladder monitoring patch and a higher frequency (8 MHz) CMUT array for a blood-pressure sensing patch.

1.4 Thesis Organization

The organization of this thesis is as follows.

Chapter 2 presents a 64-channel transmit beamformer with programmable bipolar pulsers for catheter-based ultrasound probes. The transmit beamformer is programmed and configured through a single clock and data line to steer and focus an ultrasound beam at an angle and depth that is defined in the imaging system. The compact HV pulser design includes an RZ switch that has been constructed such that it can also serve as T/R switch. A new floating-gate driver that uses only a single HV transistor provides level-shifting functionality to turn on and off the MOS transistors in the switch. Thus, the number of HV transistors and passive components required is reduced. Electrical and acoustical experimental results obtained in combination with a 64 element CMUT array successfully demonstrate the functionality of the HV pulser and TX beamformer.

Chapter 3 extends the transmit beamformer discussed in the previous chapter with receive functionality to realize a transceiver ASIC designed for ICE. This includes LNAs to amplify the echo signals and TGC to reduce their dynamic range. The chapter gives an overview of existing TGC circuits with a discussion of their advantages and limitations. Then system architecture and circuit techniques are presented to implement an LNA with built-in TGC functionality, as a more compact and power-efficient alternative to conventional solutions with a separate LNA and TGC amplifier. The operation principle of the proposed TGC scheme is described with an analytical analysis of the capacitive feedback network. Electrical measurements demonstrate continuous gain control to within ±1 dB. Imaging results obtained using a prototype employing a 64-element CMUT array demonstrate the effectiveness of the proposed techniques, showing that the proposed topology is a promising solution for ultrasound ASICs.

In chapter 4, a front-end ASIC targeted for a forward-looking IVUS imaging probe is presented. The ASIC interfaces with 16 TX elements and 64 RX elements using only four 1.5-m micro-coaxial cables. A PZT-on-ASIC integration scheme has been applied in this prototype with the ASIC being fabricated in a donut shape, allowing the catheter's guidewire to pass through a hole in the middle of the chip. To minimize the number of cables, a multi-functional mixed-voltage command scheme is applied that merges power supply, clock and data on a single cable. Moreover, load-modulation-based data transmission is proposed as an

efficient way to return digitized echo signals to an imaging system, and HV multiplexing to perform synthetic-aperture imaging. The effectiveness of these techniques has been successfully demonstrated in a 3D ultrasound imaging experiment.

Chapter 5 presents a reconfigurable front-end ASIC for wearable ultrasound patches. The ASIC includes 64 transceivers channels that can be reconfigured to interface with different transducer elements with different center frequencies (2 MHz to 8 MHz) and capacitance (20 pF to 120 pF) by dynamically parallelizing transceiver channels. A reconfigurable sampling network is employed such that one ADC can digitize multiple RX channels for a low-frequency transducer and a single RX channel for a high-frequency transducer. Electrical measurements demonstrate the functionality of the ASIC. A wearable prototype of a bladder-monitoring patch, with ASIC, transducer array, and peripheral building blocks integrated on top of a flexible PCB, has been successfully evaluated acoustically using a bladder phantom.

Chapter 6 concludes the thesis by highlighting the main contributions and the main findings. Suggestions for future improvement and research are also presented.

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CHAPTER 2

TRANSMIT BEAMFORMER WITH ±30V BIPOLAR HIGH-VOLTAGE PULSERS

This chapter is based on the publication: M. Tan, E. Kang, J. S. An, Z. Y. Chang, P. Vince, T. Mateo, N. Senegond, and M. A. P. Pertijs "A 64-channel transmit beamformer with ±30-V bipolar high-voltage pulsers for catheter-based ultrasound probes," IEEE J. Solid-State Circuits, vol. 55, no. 7, pp. 1796–1806, 2020.

2.1 Introduction

Ultrasound imaging is a safe, cost-effective, and widely-used imaging modality for the diagnosis and treatment of cardiovascular conditions. Miniaturized ultrasound devices mounted at the tip of a catheter or endoscope are becoming increasingly important as they can provide better image quality than external hand-held probes, for instance, to guide minimally-invasive cardiac interventions [1]. A prime example is intra-cardiac echocardiography (ICE) probes, which generate ultrasound images from inside the heart using a transducer array mounted at the tip of a catheter [2]. The image construction relies on the transmission of acoustic waves and post-processing of the reflected echo signals. The acoustic waves are generated by exciting the elements of the transducer array with voltage pulses. Typically, these pulses are timed such that an acoustic beam is formed that is focused and steered at a particular angle. Different pulse timing in successive pulse-echo cycles allows the beam to scan the region of interest to form an image. Since the acoustic signal will be significantly attenuated as it propagates through tissue, high-voltage (HV) pulses (with

amplitudes of tens of volts) are required to generate enough pressure so that the overall signal-to-noise ratio is sufficiently high at the largest imaging depth [3].

In most commercial ICE catheters, the elements in the transducer array are connected to transmit (TX) and receive (RX) circuitry in an imaging system through long micro-coax cables. Given the signal attenuation caused by such cables and difficulties of the cable assembly, application-specific integrated circuits (ASICs) have been integrated closely to the transducer array to reduce the number of cables and increase the signal-to-noise ratio by locally amplifying the echo signals [4]–[9].

An important challenge in the design of such in-probe ASICs is that the required HV TX circuitry cannot be implemented in standard CMOS technologies. This applies to the HV pulsers as well as to the transmit/receive (T/R) switches needed to protect the low-voltage (LV) RX circuitry during pulse transmission. Therefore, HV BCD technologies are usually adopted in which HV MOS transistors are available [4], [5], [8]. Such transistors, however, tend to occupy a large die area while the available area is limited in catheter-based devices. This calls for a compact pulser and T/R SW design.

Unipolar pulsers have been applied (which can only generate positive HV pulses), as they can be implemented using a small number of HV transistors [10], [11]. However, this comes with several disadvantages. In contrast with the bipolar pulses commonly generated by conventional imaging systems, unipolar pulses contain more low-frequency out-of-band energy, and thus lead to lower SNR for the same peak-to-peak amplitude [12]. Moreover, many image-enhancing techniques, such as pulse inversion and coded excitation, are easier to implement using bipolar pulses [13]. Therefore, it is worthwhile to design an on-chip bipolar pulser although the architecture is more complicated.

An added benefit of using bipolar pulsing is that it can reduce the dynamic power consumption of the pulser by at best a factor of 2 compared to a unipolar pulser with the same peak-to-peak output voltage, provided a return-to-zero (RZ) pulser is used[14]. This is an important advantage, since the overall power consumption of the ASIC should be minimized to avoid tissue over-heating.

In this chapter, we present a front-end ASIC for a 64-element transducer array that includes an on-chip transmit beamformer and programmable bipolar pulsers. The chapter extends on our previous work [15], [16], in which the bipolar pulser has been described. Here, we present a complete ASIC intended for a CMUT-based 2D ICE probe. With a width of less than 2 mm, the ASIC is suitable for catheter integration and directly connects to the transducer elements in a pitch-matched fashion through a PCB interposer. The ASIC only needs two low-voltage differential signaling (LVDS) clock and data lines to program the on-chip transmit beamformer. Electrical and acoustical measurement results are presented that successfully show the functionality of the bipolar pulser and the complete TX beamformer.

This chapter is organized as follows. Section 2.2 describes the system architecture. Section 2.3 discusses the design of the bipolar pulser, while Section 2.4 presents details of the circuit implementation. Sections 2.5 and 2.6 present the experimental results and conclusions.

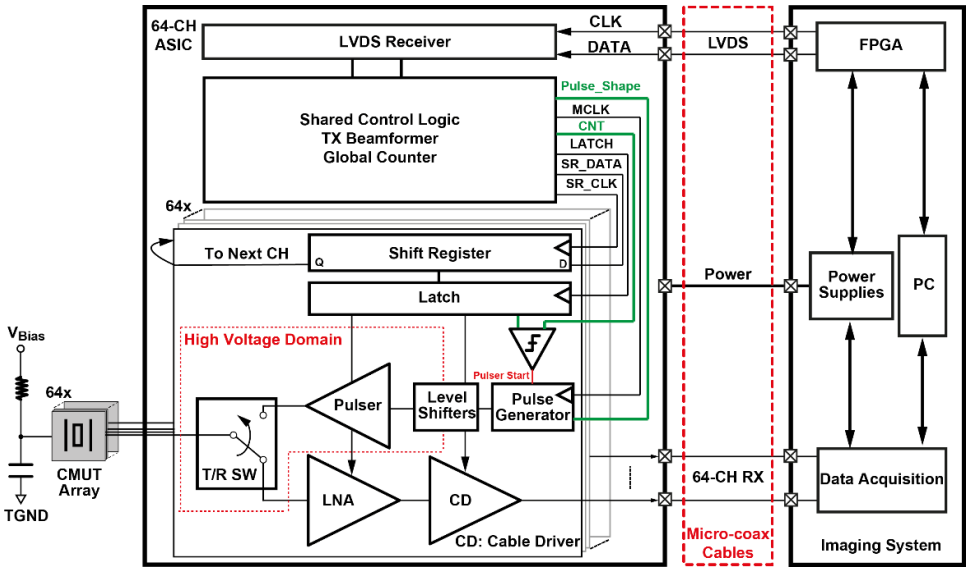


Figure 2.1. System Architecture

2.2 System Architecture

Figure 2.1 shows a block diagram of the proposed system. It consists of a 64-element CMUT transducer array, a front-end ASIC and the imaging system. The elements of the transducer array are directly connected to channels of the ASIC at the tip of the catheter, while a bundle of micro-coax cables (~ 2-m long) is used to connect the ASIC with the imaging system.

We employ a CMUT transducer array with a center frequency of 7.5 MHz, targeting ICE applications [9], [11]. All the CMUT elements are DC-biased at V_{bias} and AC-coupled to the transducer ground (TGND) through a shared RC network. To interface with the CMUT elements, each channel of the ASIC contains a T/R switch, a HV TX pulser with associated level shifters and pulse generator, a low-noise amplifier (LNA), a cable driver (CD), and a latched shift register (SR) for the configuration.

Clock and data are provided to the ASIC by an FPGA through LVDS signals, which are first converted to 1.8 V standard logic levels through an on-chip LVDS receiver. Then, shared control logic will generate a clock (SR_CLK) and data (SR_DATA) for the element-level SRs, a latch signal (LATCH) for the element-level latches, and a master clock (MCLK) and counter (CNT) for the timing control of the pulse generators. The SR of each channel

provides the configuration data for the RX amplifiers and HV pulsers, as well as a counter value, which is compared to CNT to define the start time of the pulse. The SRs are daisy-chained to allow the element-level configuration data to be loaded sequentially from the shared control logic. According to the loaded data in the SR, the pulse generator will generate low-voltage (LV) signals to control the HV pulser through the level shifters with a proper timing.

When the CMUT transducer element is excited by the HV pulses, ultrasonic waves are emitted into the medium. The resulting echo signals are amplified by the low-noise amplifiers (LNAs), which are connected to the transducer elements via the T/R switches after pulsing, and then transferred to the imaging system through micro-coax cables with the help of cable drivers (CD). The details of the LNA and CD are presented in [17]. The imaging system will record the echo signals and process them for image reconstruction.

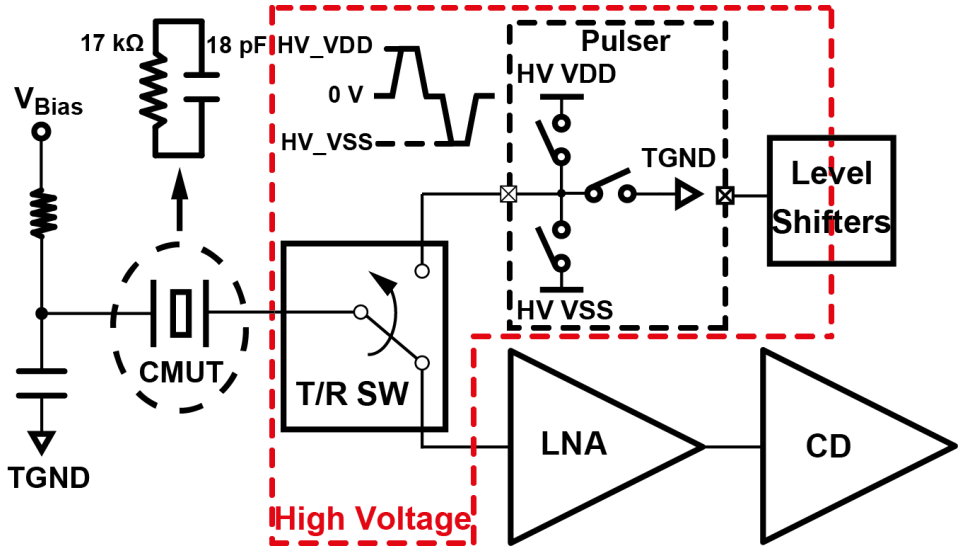


Figure 2.2. Simplified block diagram of a single transceiver channel of the ASIC.

2.3 Bipolar Pulser Design

Figure 2.2 shows the simplified block diagram of a single ultrasound transceiver channel of the ASIC. To generate RZ bipolar pulses, the pulser consists of a pull-up switch that drives the CMUT transducer to a positive HV supply (HV_VDD), a pull-down switch that drives it to a negative HV supply (HV_VSS), and a RZ switch that pulls the transducer back to ground. The impedance of the CMUT element used in this work can be modelled as 18 pF//17 kΩ.

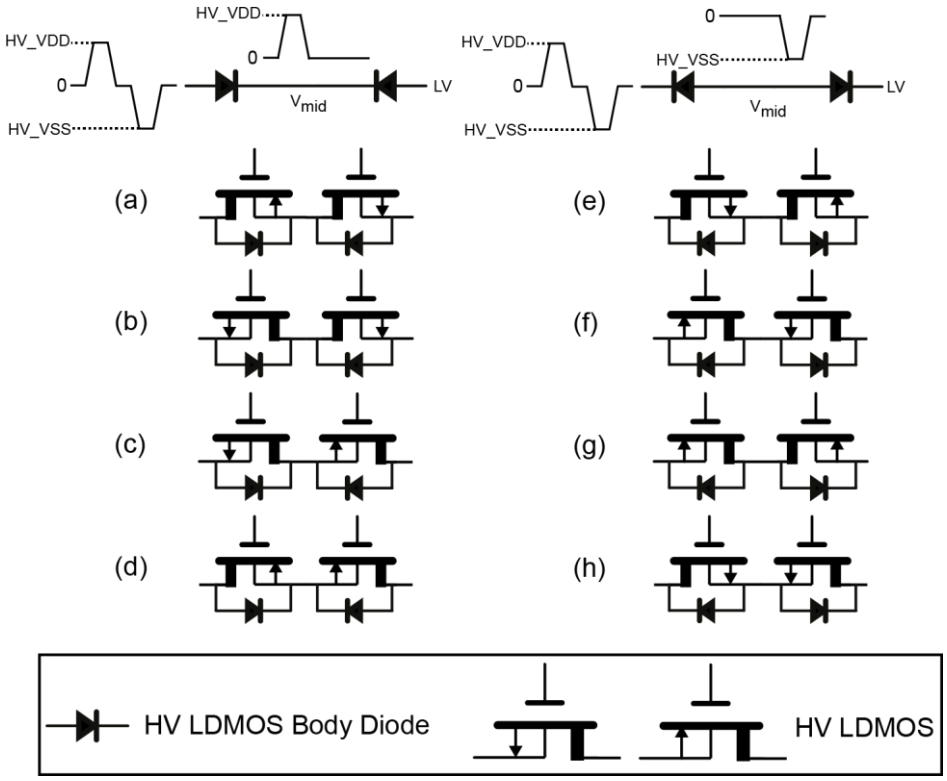


Figure 2.3. Overview of HV MOS configurations that can provide back-to-back isolation.

2.3.1 Switch Configurations with Bidirectional Isolation

The RZ switch needs to provide bidirectional HV isolation, in the sense that when it is off, it should be able to handle both positive and negative voltage drop. Similarly, the T/R switch, which connects the transducer to the LNA during echo reception, needs to provide bidirectional HV isolation during pulsing. Two technology-related limitations of the HV MOS transistors in BCD technologies, the body diode and the limited gate-oxide breakdown voltage, increase the implementation complexity of the T/R switch and the RZ switch. The presence of the body diode implies that two back-to-back connected HV transistors are needed to provide bidirectional isolation. The relatively low gate-oxide breakdown voltage requires a more complicated gate-driver design compared to HV technologies with thick gate oxide.

Figure 2.3 shows the eight possible back-to-back configurations of HV NMOS and PMOS transistors. The body-diode orientation in configurations (a)-(d) is such that the middle node

between the transistors (V_{mid}) swings up with the positive HV pulse, while in configurations (e)-(h) it swings down with the negative HV pulse. In all configurations, at least one of the sources of the transistors swings up and/or down with the HV pulse, implying that a HV gate driver is needed that keeps the gate-source voltage below the gate-oxide breakdown limit (5.5V in our technology). To prevent this HV floating-gate driver from having to operate at both positive and negative high voltages, configurations in which the source of the left-hand transistor connects to the transducer should be avoided. Driving the source of the right-hand transistor is easier if it connects to the low-voltage circuitry rather than to V_{mid}. This leaves configurations (a) and (e) as the preferred choice, both of which are applied in parallel in our implementation.

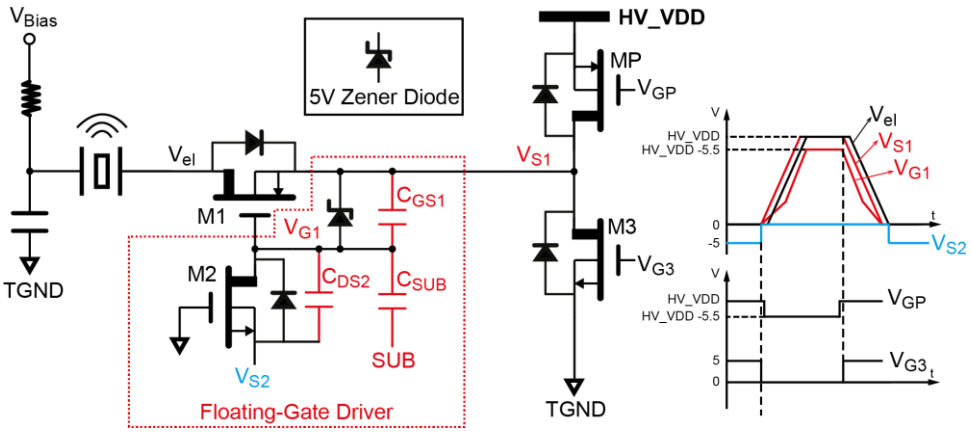


Figure 2.4. Circuit diagram of a high-side pulser employing the single-transistor HV floating-gate driver circuit.

2.3.2 Floating-Gate Driver

In previous HV switch designs [5], [8], [18], bootstrapped gate drivers have been employed. However, they cannot be applied in an RZ switch, because they only allow the switch to be turned on when it is at ground level, while the RZ switch needs to be turned on when the pulser output is at HV_VDD or HV_VSS. Therefore, we propose a compact and energy-efficient floating-gate driver that utilizes parasitic capacitance to control the gate-source voltage and requires only one additional small HV MOS transistor.

This circuit is shown in Figure 2.4, in the context of a unipolar (high-side) pulser. HV transistors MP and M1 are used to pull the transducer to HV_VDD, while M1 and M3 together form the switch configuration of Figure 2.3a to provide the return-to-zero switching. The gate of MP is driven relative to HV_VDD using a conventional level-shifter circuit. The gate of M1 is driven by our new gate-drive approach using transistor M2. Initially, to short

the transducer to ground, M3 and M1 are turned on. M1 is turned on through M2 by connecting M2's source to -5 V and its gate to ground, so that the gate of M1 is pulled to -5 V. Before the HV pulsing starts, the source of M2 is switched to ground, so that the gate of M1 is discharged to ground through the body diode of M2. After this, M2 is off and the gate of M1 floats. When MP is turned on and M3 is turned off, the voltage step on V_{S1} will also create a step on the gate of M1 because of the capacitive divider formed by C_{GS1} and C_{DS2} + C_{SUB}, where C_{SUB} is the capacitance from the gate of M1 to the substrate. By properly sizing M2 to make C_{DS2} + C_{SUB} larger than C_{GS1}, V_{GS1} will increase, turning on M1 and thus allowing the transducer to be charged to HV_VDD. A Zener diode prevents V_{GS1} from exceeding the breakdown voltage. At the beginning of the RZ phase, MP is turned off and M3 is turned on, while M1 remains on. This discharges the transducer until V_{el} reaches the threshold voltage of M1 of 0.7 V (~85 times smaller than the pulse peak-to-peak amplitude), thus realizing an almost complete RZ operation. Finally, the gate of M1 is pulled to -5 V through M1.

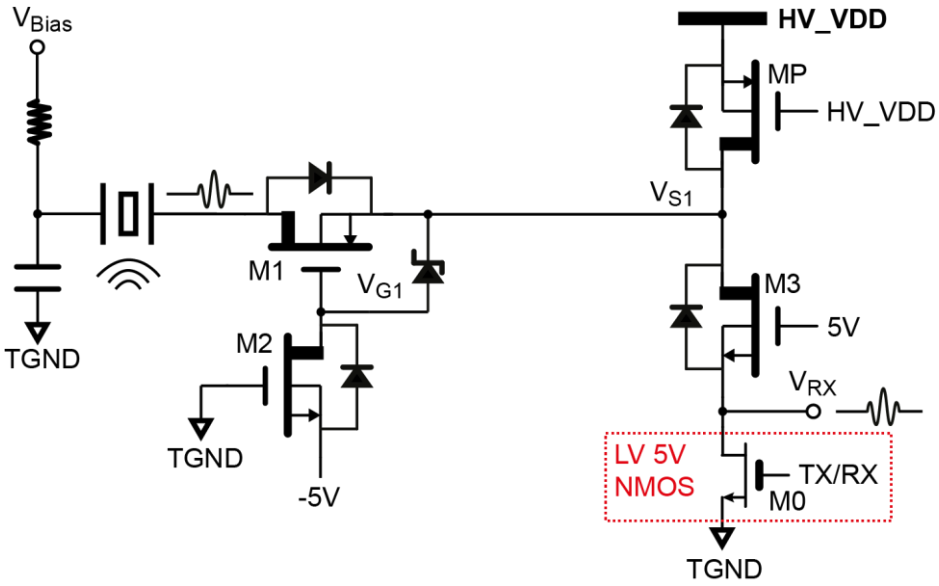


Figure 2.5. Circuit diagram of the high-side pulser with embedded T/R switch.

2.3.3 Embedded T/R Switch

The circuit of Figure 2.4 can be extended with one additional low-voltage transistor M0 to allow it to act also as a T/R switch, as shown in Figure 2.5. This transistor is placed in series with the source of M3 and is turned on during the TX phase, allowing the circuit to operate

as before and preventing any feedthrough of the HV pulse from reaching the RX circuitry. Although M0 will increase the total series resistance for the RZ phase, it can be sized to have a low on-resistance compared to that of M1 and M3 without significantly affecting the total die area since it is an LV MOS transistor. During the TX phase, when the HV pulsing finishes and VS1 and VG1 are at ground level, M1, M3 and M0 are turned on to short the transducer to TGND. During the RX phase, M0 is turned off so that the received echo signal can pass through M1 and M3 to the LV receive circuitry. Since the parasitic capacitance of the LV transistor M0 is relatively small, the transient introduced by the switching of M0 is negligible. Turning on M1 through M2 requires the source of M2 to be -5 V, which is realized using a simple low-voltage charge-pump-based level shifter (see Section 2.4.2). Thus, only 4 HV transistors are used to implement HV pull-up, return-to-zero, and T/R switch functionality.

2.3.4 Complete Bipolar Pulser

To realize a complete bipolar pulser, the high-side circuit of Figure 2.5 is combined with a complementary low-side version. Figure 2.6 shows the resulting circuit, including the various level-shifters and the associated timing diagram. During the TX phase, M2 and M5 are turned off to float the gate of M1 and M4. Pulling up the pulser output from ground to HV_VDD and pulling down the output from HV_VDD to ground (RZ phase) are done by turning on MP and M3, respectively, as discussed in Section 2.3.3. The same concept is applied in the complementary low-side pulser for the transition from ground to HV_VSS and HV_VSS to ground, by turning on MN and M6, respectively. After the TX phase, the two sets of RZ switches (M1, M3) and (M4, M6) are turned on in parallel to serve as a T/R switch, reducing the on-resistance (and the associated noise) by 2x, and saving substantial area compared to a separate T/R switch.

Depending on configuration bits stored in the element-level SR, the pulse generator can provide the following operating modes: A) bipolar RZ pulsing as shown in the timing diagram of Figure 2.6; B) bipolar non-RZ pulsing (by setting the RZ time to 0); C) unipolar pulsing (by setting the pull-up time or the pull-down time to 0). Moreover, the width of the pulses can be defined (in terms of cycles of the 200 MHz clock) to enable pulse-width programming, allowing the pulser to be used at different frequencies.

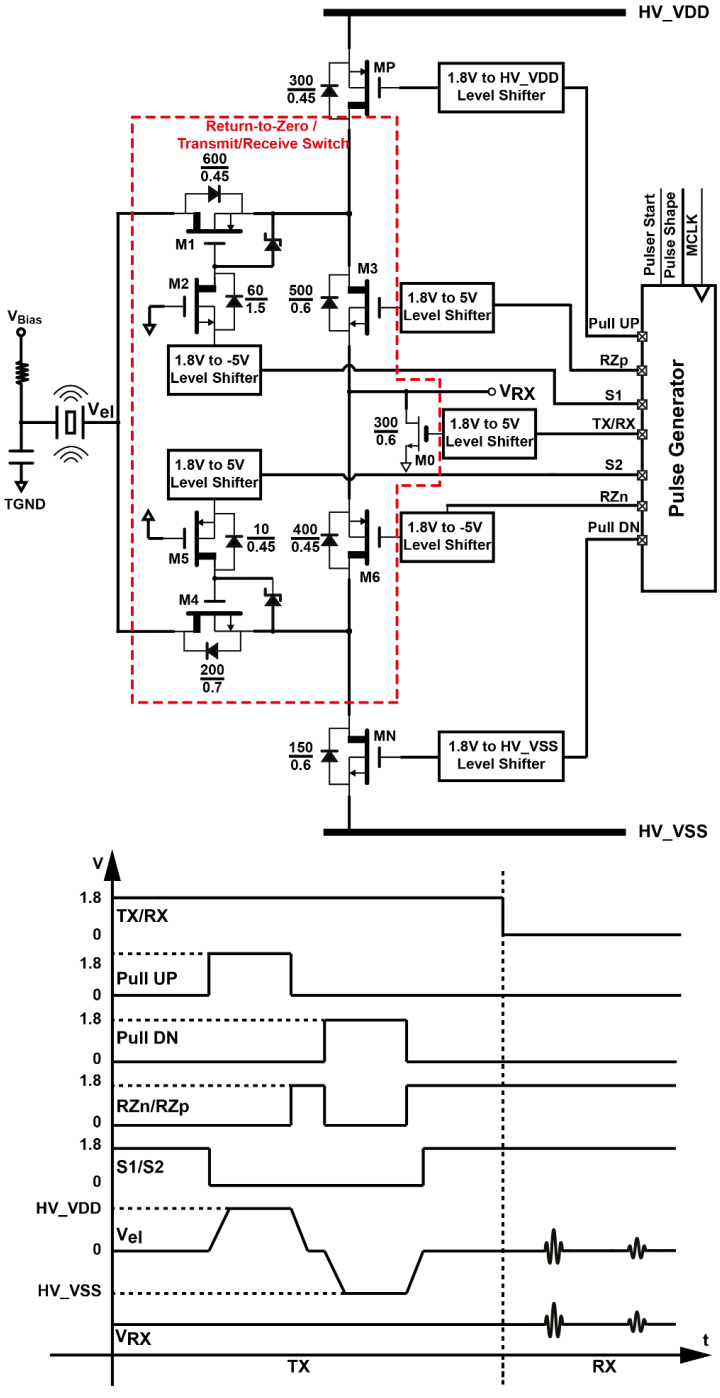


Figure 2.6. Circuit diagram of the complete pulser, with associated timing diagram.

2.4 Circuit Implementation Details

2.4.1 Supply Domains

Figure 2.7 shows the power supplies used in the proposed system. The power supply for the digital blocks (DVDD) is locally decoupled to the digital ground (DGND) on the PCB, while HV_VDD, HV_VSS and the 5 V supply for the level shifters (VDD5V) are locally decoupled to TGND. These supplies and grounds are connected to the system side through cables. To prevent transients associated with the operation of the digital circuits from affecting the analog circuitry, DGND and TGND are joint together on the system side. A limited set of decoupling capacitors, sized to be able to fit inside a catheter, are placed as close to the ASIC as possible to provide transient supply currents. Nevertheless, there is still certain inductance between these decoupling capacitors and the on-chip circuitry, which will give rise to di/dt transients on the supplies. The level shifters need to be designed to be immune to these transients.

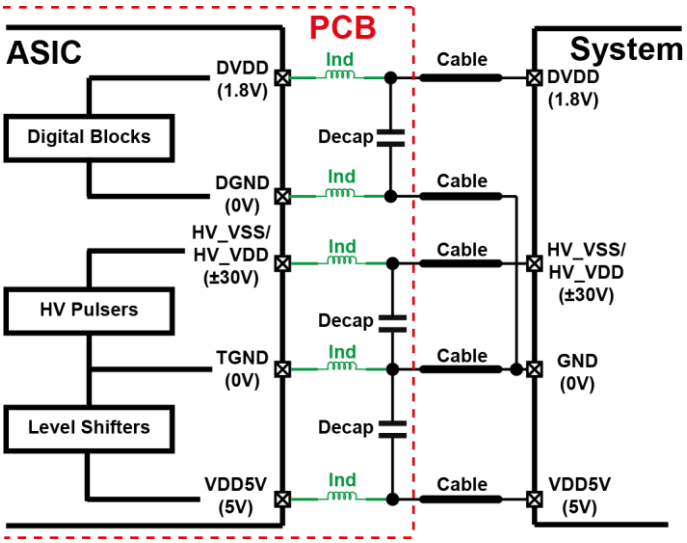


Figure 2.7. Overview of the power supplies in the proposed system.

2.4.2 Level Shifters

The level shifters shift the 1.8 V logic-level signals to 5 V signals relative to ground, HV_VDD and HV_VSS to drive the gates of the HV MOS transistors (see Figure 2.6). To reliably level-shift logic-level signals in the DGND-DVDD domain to the TGND-VDD5V domain, in the presence of potential voltage transients between DGND and TGND, we

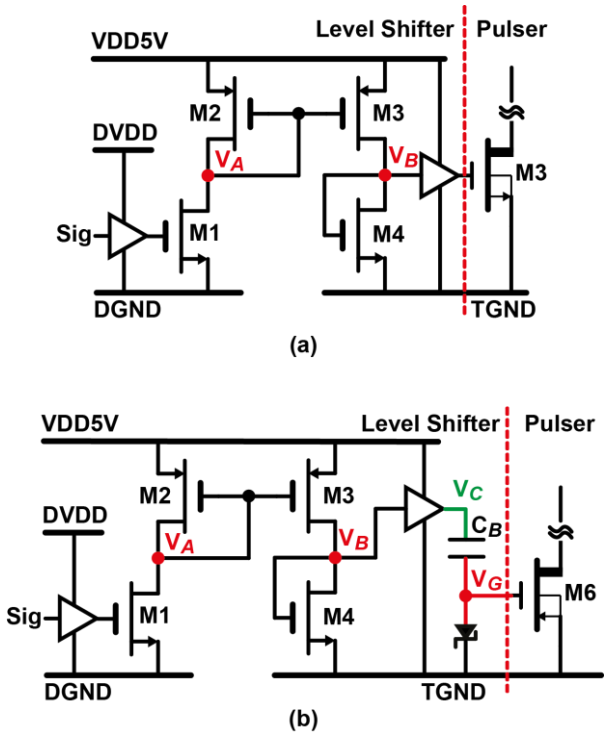


Figure 2.8. (a) 1.8 V to 5 V level shifter; (b) 1.8 V to –5 V level shifter.

propose the current-mode level-shifter architecture shown in Figure 2.8a. When the logic input is high, a current provided by M1 is copied to the 5 V domain by current mirror M2, M3, causing a high level on diode-connected transistor M4, which is buffered to a proper 5 V level to drive HV MOS MN. When the logic input is low, the absence of current in M4 leads to a low level that turns off MN.

To turn on HV PMOS M6 in Figure 2.6, a negative 5 V level is required. Instead of using an external –5 V supply, a charge-pump based architecture is used. Figure 2.8b shows the circuit diagram. During the start-up, V_G is discharged to TGND through diode leakage. Then, the bootstrap capacitor is pre-charged to VDD5V through a 1.8 V to 5 V level shifter. Therefore, V_G will be pulled down to –5 V when the levels shifter output is 0 V in the ideal case. The bootstrap capacitor C_B is sized to ~5.4 pF so that MP gets enough over-drive voltage even though some charge will be lost due to the gate capacitance at node V_G.

Because HV_VDD and HV_VSS are also suffering from di/dt noise, the 1.8 V to HV_VDD and HV_VSS level shifters also apply a current-mode architecture, as shown in Figure 2.9. The V_{GS} of MP and MN in the pulser is determined by the IR drop on resistors R1 and R2, while the current mainly depends on the over-drive voltage and the transistor size of M1 and M2. By applying the architecture shown in Figure 2.8a for the 1.8 V to 5 V level shifter, an

over-drive voltage that is insensitive to the di/dt noise of HV_VDD/HV_VSS is obtained. Thus, MP and MN of the pulser can be turned on or off safely. Monte Carlo simulations indicate that the expected channel-to-channel mismatch introduced by the level shifters is less than 1% of the cycle time of the 7-MHz pulse, which has a negligible impact on the beamforming.

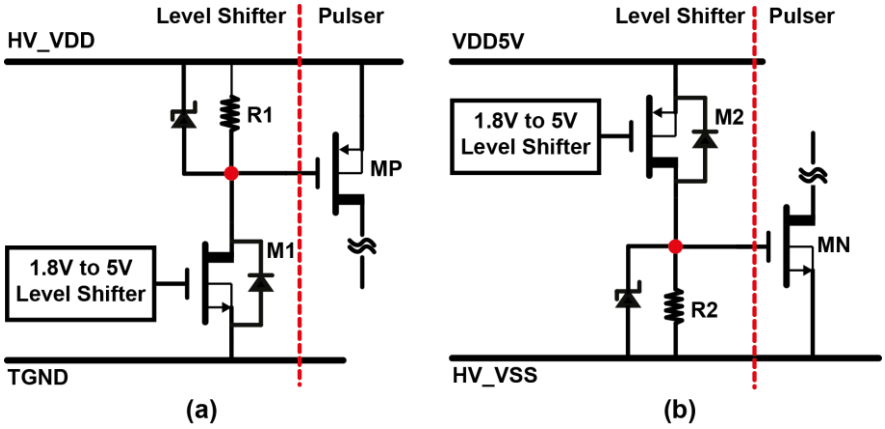


Figure 2.9. (a) 1.8 V to HV_VDD level shifter; (b) 1.8 V to HV_VSS level shifter

2.4.3 TX Beamforming Logic

For TX beamforming, the pulser in each channel should start generating a HV pulse at a well-defined time. This is done by comparing the start time pre-programmed in each channel with a global counter output (CNT in Figure 2.1), clocked at 200 MHz (MCLK). Figure 2.10 illustrates the block diagram and associated timing diagram of the TX beamformer logic. At the start of the RX period, configuration data (SR_DATA) is loaded sequentially into the daisy-chained shift registers of the shared logic and the 64 channels. The data for controlling the pulse shape and the pulse start time are loaded first and latched by LATCH_TX. These data will be used in the TX period and updated in the next RX period. During the remaining part of the RX period, the SR clock, SR data and the global clock are quiet unless RX control data (like the gain setting of the LNAs) needs to be updated. This leads to low average power consumption and minimizes the interference with the sensitive RX circuitry. At the start of the TX period, the global counter starts to run at the frequency of MCLK of 200 MHz. The counter output is distributed across the 64 channels and is compared to the start time which is pre-stored in the latch of each channel. If the counter output matches the stored start time and the channel is enabled, a pulser start signal will be generated to start the HV pulsing with a pre-defined pulse shape determined by the pulse-shape configuration data stored in the shared logic. Approximately 10 µs is needed to load all the configuration data with a

SR_CLK of 100 MHz. This leads to a maximum pulse-repetition frequency (PRF) of 100 kHz, which is sufficiently high in this application.

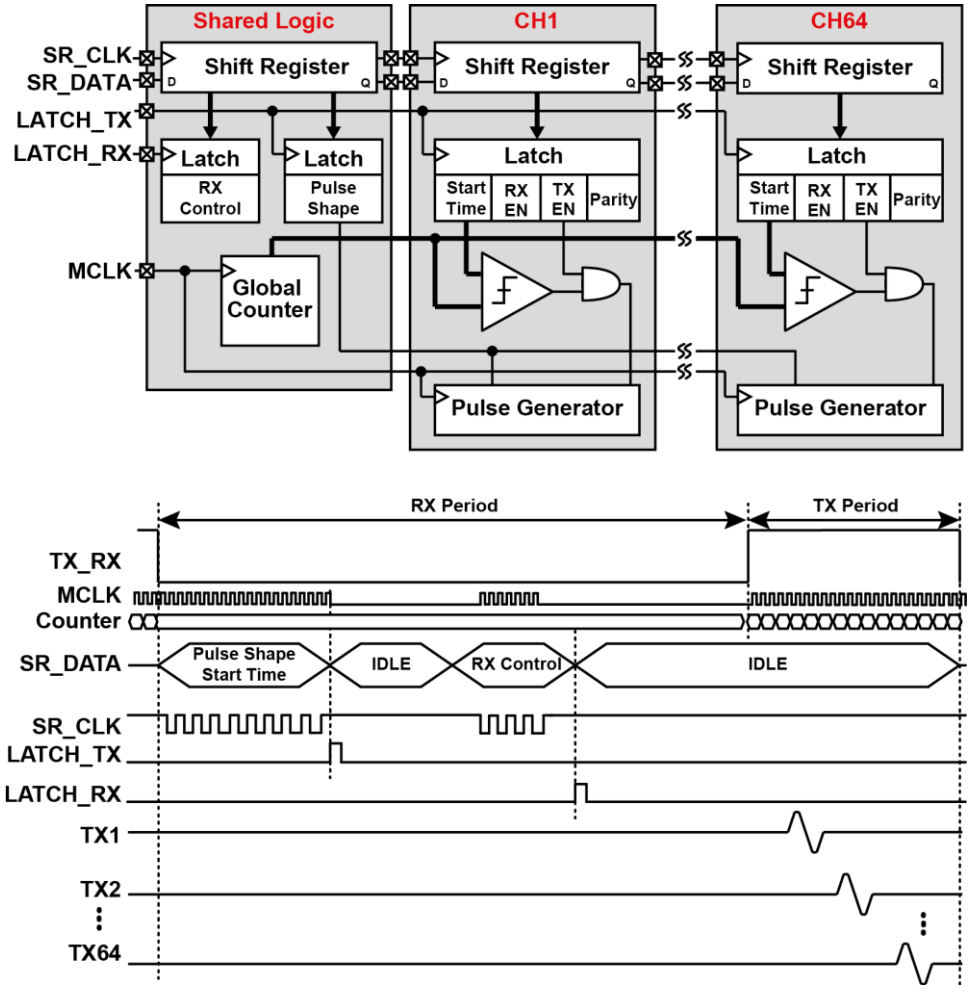


Figure 2.10. Block diagram and timing diagram of the TX beamformer logic.

2.4.4 Shared Digital Logic

Figure 2.10 shows that a total of 5 signals are needed for the TX beamformer, which are SR_CLK, SR_DATA, LATCH_TX, LATCH_RX and MCLK. To avoid an unnecessary increase in the cable-count, the SR_CLK, SR_DATA, LATCH_TX and LATCH_RX are encoded into the LVDS data line, while MCLK is derived from the LVDS clock line. Figure 2.11 illustrates the decoder and associated finite-state machine (FSM). The LVDS clock and data are first converted to single-ended signals by the LVDS receiver. The single-ended clock

output serves as MCLK and as the clock of the FSM, while the singled-ended data output controls the state transitions of the FSM.

As shown in the state diagram in Figure 2.11, the bit sequence of “010” corresponds to the latch signal for the RX shift registers (LATCH_RX), while the bit sequence of “011” generates the LATCH_TX signal for the TX shift registers. The data loading of the shift register starts with a bit sequence of “100”. After that, the bits are loaded sequentially with the DATA bit ‘0’ and ‘1’ being encoded as “00” and “01” respectively. When the data loading finishes, the FSM will return to the IDLE state in which both clock and data lines remain quiet.

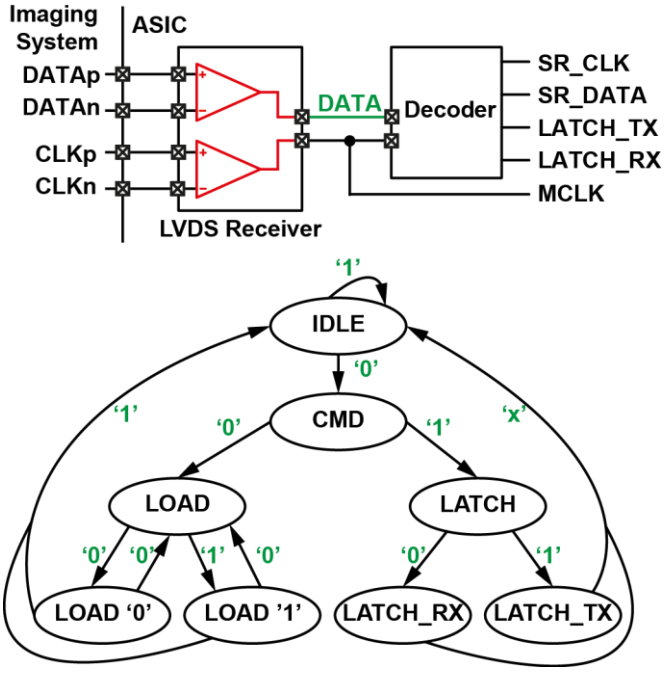


Figure 2.11. Shared control logic, with state diagram of the associated FSM.

2.5 Experimental Results

2.5.1 Experimental Prototype

The ASIC has been realized in TSMC 0.18-µm HV BCD technology with a total area of 1.8 x 16.5 mm^2, as shown in Figure 2.12. The 64 element-level circuit blocks (TX beamformer, HV pulsers, LNAs and cable drivers) are located at the center of the chip, occupying an area of 1.8 × 13.12 mm^2. They are arranged in two rows of 32 blocks with a pitch of 410 µm,

allowing direct connections to the 64-element CMUT transducer. Figure 2.12(b) shows a zoom-in view of the element-level TX circuitry, which occupies an area of 410 × 408 μm^2. The power supplies and grounds are routed horizontally across the chip in the top metal. The power consumption strongly depends on the ultrasound imaging mode and is dominated by the dynamic power consumed in driving the transducer capacitance.

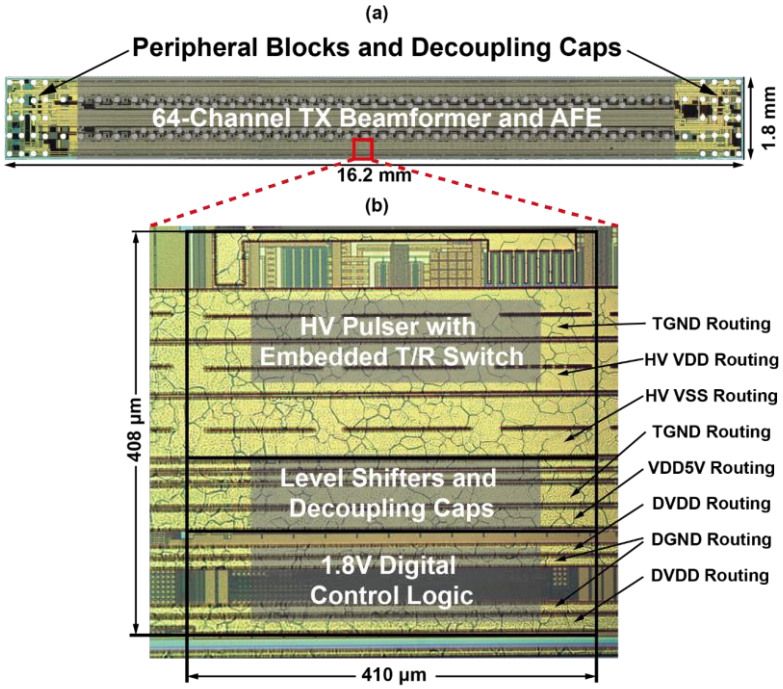


Figure 2.12. (a) Chip photograph of the 64-channel ASIC with (b) zoom-in of the element-level transmit circuits.

2.5.2 Electrical Measurement Results

To electrically characterize the prototype, an 18 pF capacitor is used as the load of the HV pulser, mimicking the transducer capacitance. To demonstrate the programmability of the proposed bipolar pulser, different configurations are applied to the pulser via the shift register. Figure 2.13 shows the measured output voltage of a single pulser channel with RZ times of 50 ns, 25 ns and 0 ns. The pulser can also be configured to generate pulses with different frequencies, allowing it to interface with different transducer elements for different applications. Figure 2.14 shows the measured output voltage for 4 MHz, 7 MHz and 9 MHz RZ and NRZ pulsing. Moreover, the proposed pulser can also be programmed to generate

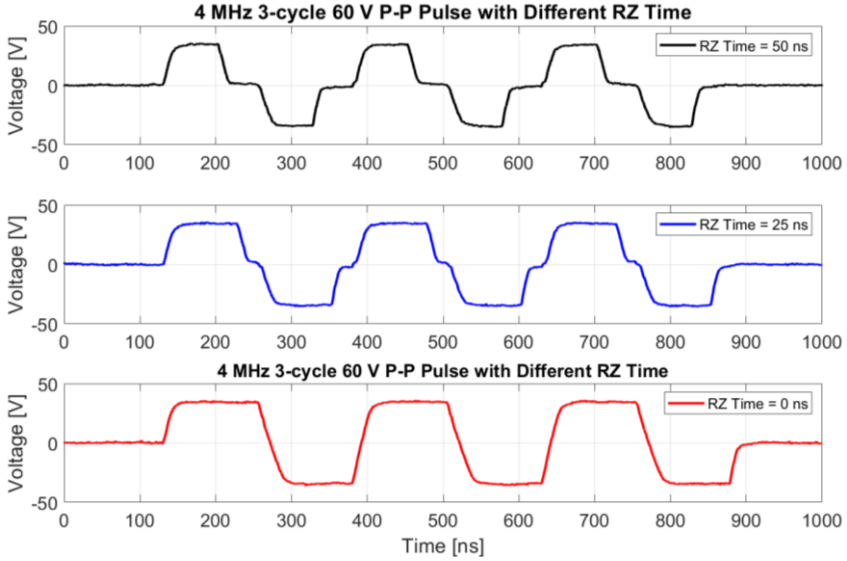


Figure 2.13. Measured output voltage for different programmed RZ times.

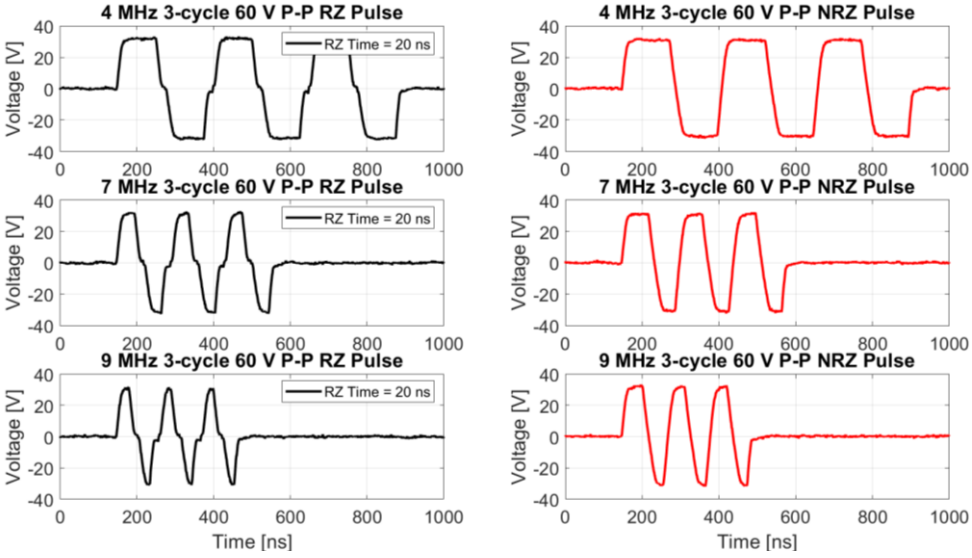
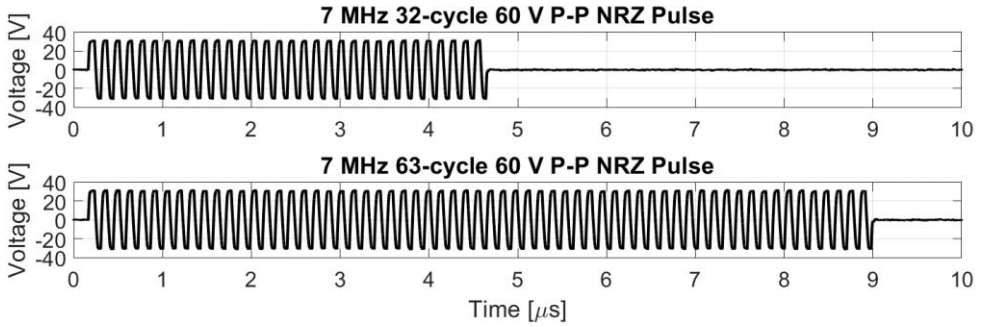
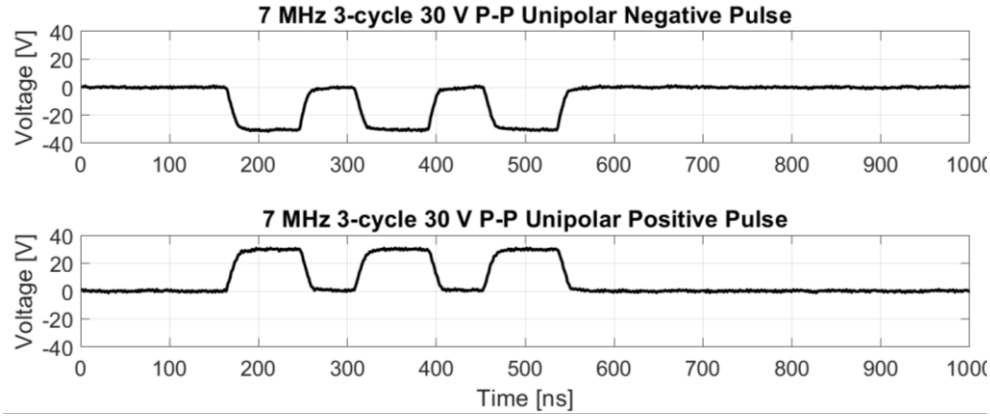


Figure 2.14. Measured output voltage for different programmed pulse frequencies.

bursts of up to 63 pulses, which is suitable for Doppler imaging, as shown in Figure 2.15a. It is also possible to trade-off power consumption with penetration depth by configuring the pulser to generate unipolar negative or positive pulses, as shown in Figure 2.15b. Note that



(a)



(b)

Figure 2.15. Measured output voltage for (a) 7-MHz 32- and 63-cycle NRZ pulses, and (b) 7-MHz 3-cycle 30-V unipolar negative and positive pulses.

there is some slew-rate mismatch between the rising and falling edges of the pulses. The associated second-order harmonic content of the pulse can be an issue in harmonic imaging, but this is not targeted in this work. If needed, slew-rate matching can be improved by optimizing the sizing of the high-voltage pull-up or pull-down transistors, or by trimming their overdrive voltages by means of adjustable level-shifters.

To electrically demonstrate the delay-control functionality of the beamformer, different start times are programmed into the shift registers of two channels in the ASIC. When the start time difference is set to a minimum value of 1 for channel 1 and channel 2, the measured delay is around 6.3 ns as shown in Figure 2.16a, which is slightly larger than the intended delay of 5 ns. When the start time difference is set to a maximum value of 4093 for channel 1 and channel 2, the measured delay is around 20.4714 µs as shown in Figure 2.16b, which is slightly larger than the intended value of 20.465 µs. The mismatch between the measured and intended delay is less than 5% of the cycle time of the 7-MHz pulses and has a negligible

impact on the beamforming. It is likely caused by the imperfect clock distribution across the ASIC and mismatch of the level shifters among different channels.

Crosstalk performance has also been evaluated by disabling one channel and pulsing on an adjacent channel. The measured output voltages and the corresponding spectra of both channels are shown in Figure 2.17. The measured crosstalk is around -66 dB at 7 MHz, which makes its impact on the beamforming negligible.

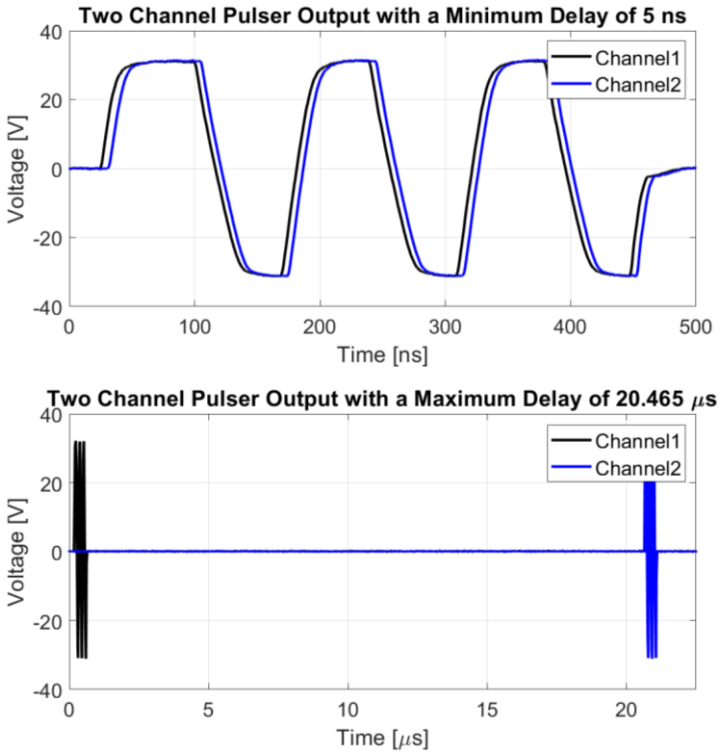


Figure 2.16. Measured minimum and maximum delay of two pulser channels.

An important performance metric of the T/R switch is its on-resistance. Since the T/R switch is placed in between the CMUT element and the TIA, its finite on-resistance adds noise to the received echo signal. This should be smaller than the noise of the CMUT element (which in our design can be modelled as 18 pF//17 kΩ at resonance) so as to not degrade the noise figure. The measured on-resistance of 180 Ω is in reasonable agreement with the simulated value of 155 Ω. At this level, T/R switch increases the noise figure by 4.7 dB, which indicates there is room of improvement by reducing the on-resistance of the switches.

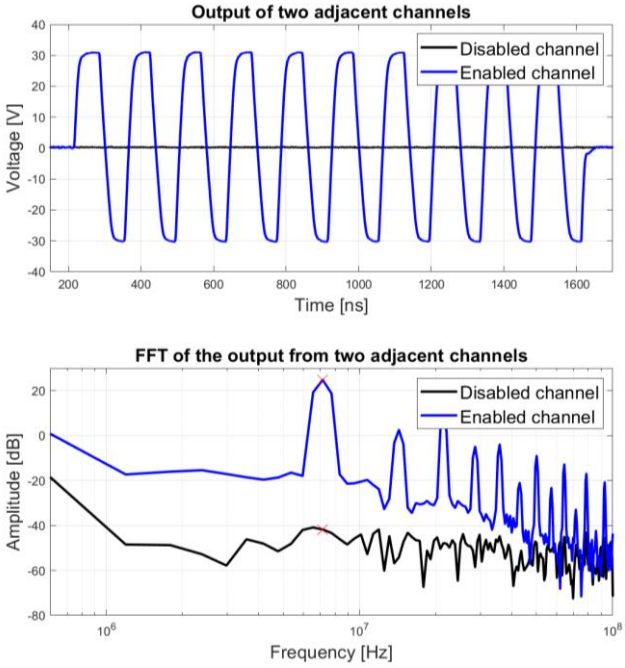


Figure 2.17. Measured crosstalk between two adjacent channel.

The ASIC's power consumption is highly dependent on the pulse repetition frequency (PRF) and the number of pulse cycles programmed. The power consumption of the TX circuitry strongly depends on the ultrasound imaging mode and is dominated by the dynamic power consumed in driving the transducer capacitance. The RX circuitry, which is described in more detail in [17], consumes on average 4.9 mW per channel. Figure 2.18 shows the power breakdown for 3-cycle pulses at a PRF of 4 kHz. The total power per channel is then around 1 mW, which is dominated by the pulser.

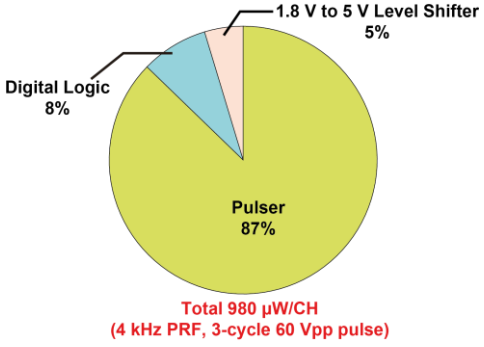


Figure 2.18. Power-consumption breakdown

2.5.3 Acoustical Measurement Results

To acoustically evaluate the transmit beamforming, the ASIC and the CMUT transducer have been flip-chip mounted on two sides of a printed circuit board (PCB), as shown in Figure 2.19. To provide a test medium that is acoustically similar to the human body, this prototype was placed at the surface of a water tank, with the CMUT side immersed. Via a connector on the PCB, the ASIC was connected to power supplies, an FPGA that provides the clock and data signals to program the ASIC, and a Verasonics imaging system that records the received echo signals.

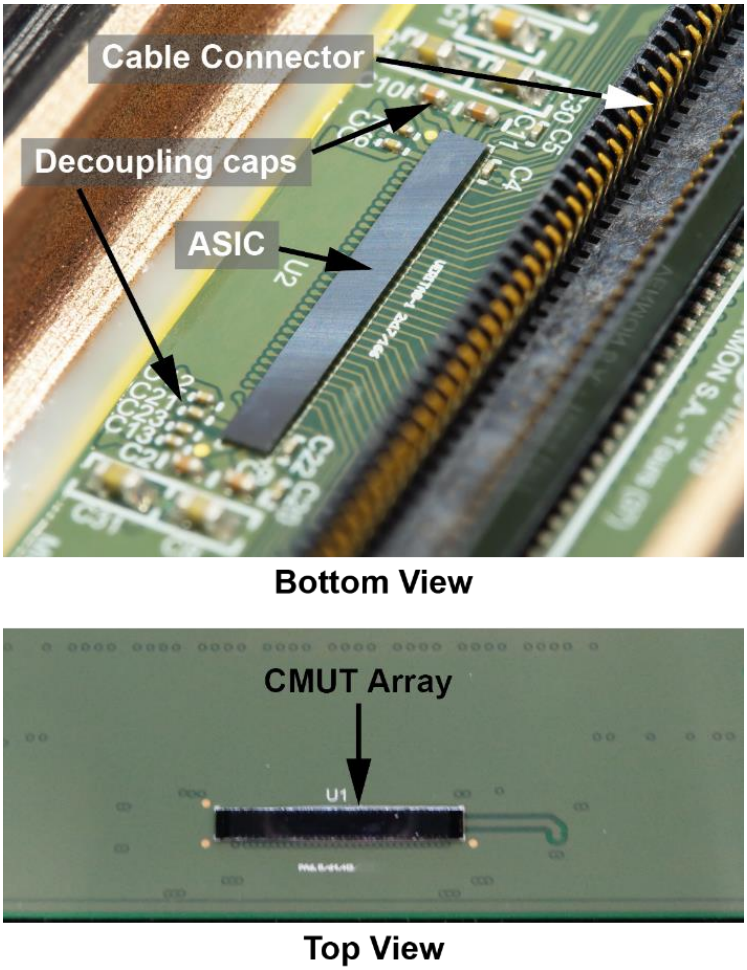


Figure 2.19. Assembled ASIC-PCB-CMUT prototype.

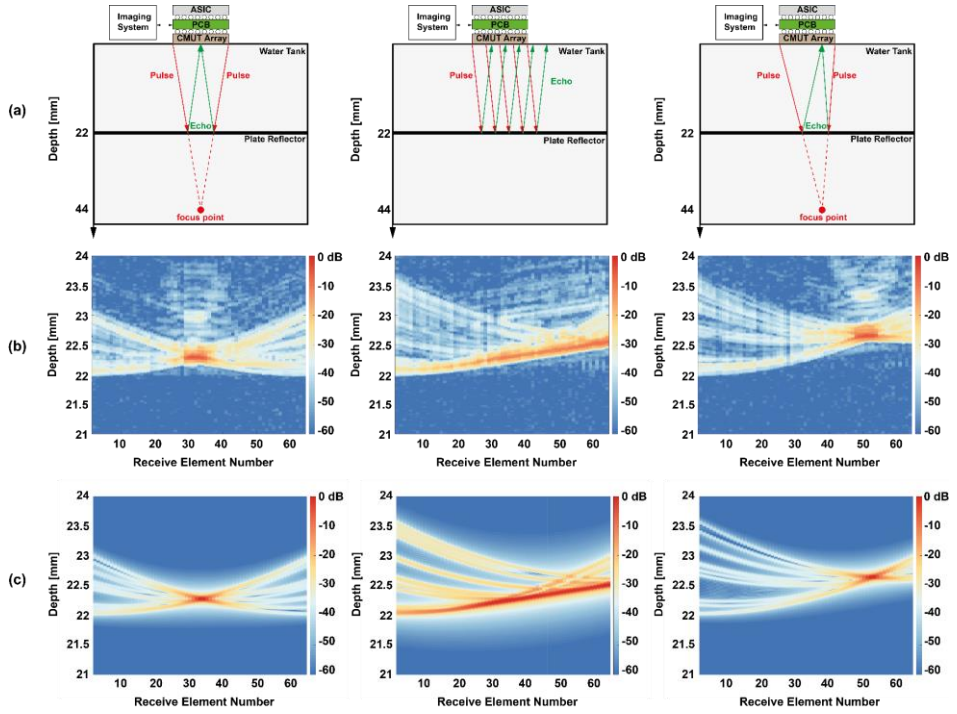


Figure 2.20. Acoustic transmit beamforming experiment with a focused beam (left), steered beam (middle) and focus and steered beam (right): (a) acoustic measurement setup with a sketch of the beam, (b) measured echo signals from a pulse-echo experiment using the ASIC, (c) simulated echo signals.

To demonstrate the beamforming capability, the ASIC was configured to drive the CMUT array so that it generates various ultrasound beams (focused, steered, both), as shown in Figure 2.20a. A plate reflector was placed at 22 mm from the transducer array, causing the transmitted acoustic waves to reflect back to the transducer array, where they are recorded through the RX channels of the ASIC. As shown in Figure 2.20b, programming the TX beamformer to focus at 44 mm (round-trip distance between the transducer and the plate reflector) causes the reflected pulse to focus at the transducer array, as expected, even when steering delays are added. Transmission of a plane wave at an angle of 5 degrees results in the reception of the expected reflected plane wave at the same angle. Figure 2.20c shows, for comparison, echo signals are simulated using DREAM Matlab toolbox [19]. It should be noted that 9 elements in the array were not working, which was also taken into account in the simulation. (These missing elements (spread across the array) are responsible for additional edge waves that can be observed both in the measurements and simulations.) The measurement results are in very good agreement with the simulations, confirming the correct operation of the beamformer.

TABLE 2-1. COMPARISON WITH THE PRIOR ART

HV 3-level Pulser			
	This Work	JSSC'19 [4]	JSSC'13 [20]
Technology	TSMC 180nm HV BCD	XFAB 180nm HV SOI	TSMC 180nm HV CMOS[a]
T/R embedded	Yes	No	No
Bipolar pulse	Yes	Yes	No
# HV MOS[b]	10	10[c]	10[c]
# HV diodes	0	2	0
Max output	60 Vpp	138 Vpp	30 Vpp
Pulse freq.	9 MHz @ 18pF	2 MHz	3.3 MHz @ 40pF
Area	0.167 mm^2	0.09 mm^2 [d]	0.33 mm^2 [d]
Floating-Gate Driver			
	This Work	ESSCIRC'18 [18]	JSSC'18 [5]
Technology	TSMC 180nm HV BCD	N/A	TSMC 180nm HV BCD
Application	RZ & T/R switch	HV switch (bipolar)	HV switch (unipolar)
# HV MOS	1	3	1
# HV diodes	0	3	0
# Passives[e]	1	6	4
Transmit Beamformer			
	This Work	TBCAS'18[11]	JSSC'19 [4]
Delay Resolution	5 ns	5 ns	25 ns
Delay Dynamic Range[f]	72 dB	66 dB	54 dB
# Channels	64	64	3072

a) Gate-oxide can handle 30 V swing. b) Including HV MOS in level shifters.
c) excluding HV transistors in T/R switch. d) Area for RX circuitry also included.
e) Capacitors, resistors and Zener diodes. f) Delay Dynamic Range = 20 · log10(max_delay / min_delay).

TABLE 2-1 compares the proposed HV pulser, floating-gate driver and transmit beamformer with the prior art. In contrast with earlier pulsers [4], [20], this chapter provides embedded T/R switch functionality without increasing the number of the HV transistors. Note that an area comparison is somewhat arbitrary, given the different pulser specifications and given that [4] uses SOI technology with smaller lateral dimensions for HV isolation than the junction-isolated technology used in this chapter. We expect our proposed pulser topology is equally applicable in such technology and would provide an area benefit when optimized for the much smaller matrix transducer elements used in [4]. Moreover, the floating-gate driver requires fewer HV components than those used in earlier HV switches [5], [18]. The transmit beamformer achieves the same delay resolution of 5 ns and the same number of elements of 64 with the highest delay dynamic range of 74 dB.

2.6 Conclusions

This chapter has described a 64-channel transmit beamformer with programmable bipolar pulsers for catheter-based ultrasound probes. The transmit beamformer is programmed and configured through a single clock and data line to steer and focus an ultrasound beam at an

angle and depth that is defined in the imaging system. The compact HV pulser design includes an RZ switch that has been constructed such that it can also serve as T/R switch. A new floating-gate driver that uses only a single HV transistor provides level-shifting functionality to turn on and off the MOS transistors in the switch. Thus, the number of HV transistors and passive components required is reduced. Electrical and acoustical experimental results obtained in combination with a 64-element CMUT array successfully demonstrate the functionality of the HV pulser and TX beamformer.

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CHAPTER 3

LOW-NOISE TRANSIMPEDANCE AMPLIFIER WITH EMBEDDED TIME-GAIN COMPENSATION

This chapter is based on the publication: E. Kang, M. Tan, J. S. An, Z. Y. Chang, P. Vince, N. Senegond, T. Mateo, C. Meynier, and M. A. P. Pertijs "A variable-gain low-noise transimpedance amplifier for miniature ultrasound probes," IEEE J. Solid-State Circuits, vol. 55, no. 12, pp. 3157–3168, Dec. 2020.

3.1 Introduction

Ultrasound imaging is a safe and cost-effective tool for the diagnosis of medical conditions and the guidance of treatment. Size reduction of imaging devices has enabled ultrasound imaging from the tip of a mm-size catheter, for instance for intracardiac echocardiography

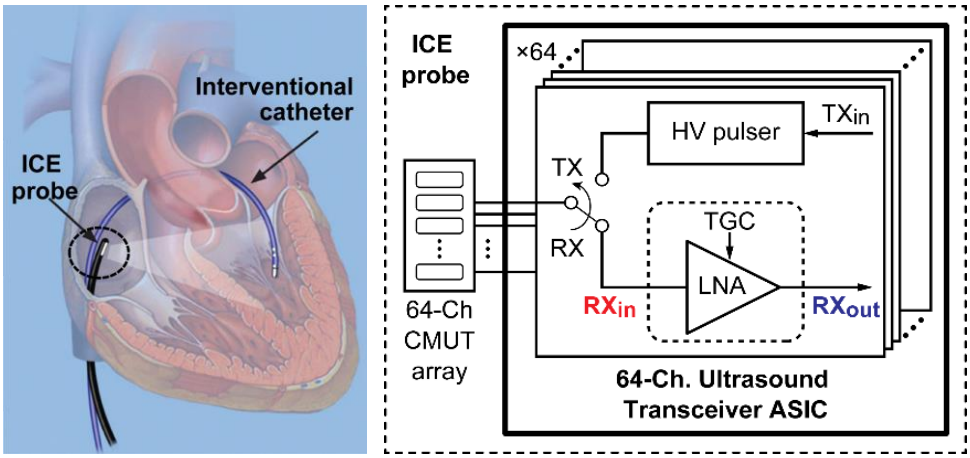


Figure 3.1 (a) Application scenario of an ICE probe; (b) block diagram of the transceiver ASIC with the proposed TIA.

(ICE), as illustrated in Figure 3.1(a) [1], [2]. Applications of ICE probes include guidance and monitoring of catheter ablation for the treatment of atrial fibrillation, guidance of closure of atrial septal defects, and guidance of transcatheter valve implantation [3], [4].

ICE probes, and other miniature ultrasound probes alike, employ an array of ultrasound transducer elements to transmit ultrasonic pulses and record the resulting echo signals, from which an image is reconstructed using beamforming techniques [5]. In many probes, each transducer element is electrically connected via a cable to the external imaging system [5]–[7]. However, this approach limits the number of transducer elements due to the limited number of cables that can be accommodated, and results in signal attenuation due to the fact that the cables load the elements. Increasingly, application-specific integrated circuits (ASICs) are integrated in the probe close to the transducer array to address these issues [8]–[13].

Figure 3.1(b) shows a block diagram of the front-end of such an in-probe ASIC. For each transducer element, it contains transmit (TX) and receive (RX) circuitry. The former tends to include a high-voltage (HV) pulser that drives the element to generate a pressure wave [8]–[11]. At the start of the RX signal path, a low-noise amplifier (LNA) amplifies the echo signal so that it can be further processed by the following circuitry, which may involve beamforming, multiplexing and digitization [12], [13].

An important function in the RX signal path is time-gain compensation (TGC), which reduces the echo-signal dynamic range (DR) by compensating for the propagation attenuation experienced by the acoustic waves as they travel through the body [14]. Due to this attenuation, echo signals from deep tissue, which need to travel longer than echoes from nearby structures and therefore arrive later, are more attenuated. This leads to an exponential

decrease in echo amplitude with time, as illustrated in Figure 3.2(a). Since propagation attenuation increases with frequency [14], this is particularly significant at the relatively high frequencies (>5 MHz) typically used in miniature probes. The attenuation may amount to 40 dB at the largest imaging depth. It can be compensated for by providing a gain that increases linearly in dB as a function of time, thus providing a uniform echo amplitude across depth, as illustrated in Figure 3.2(b).

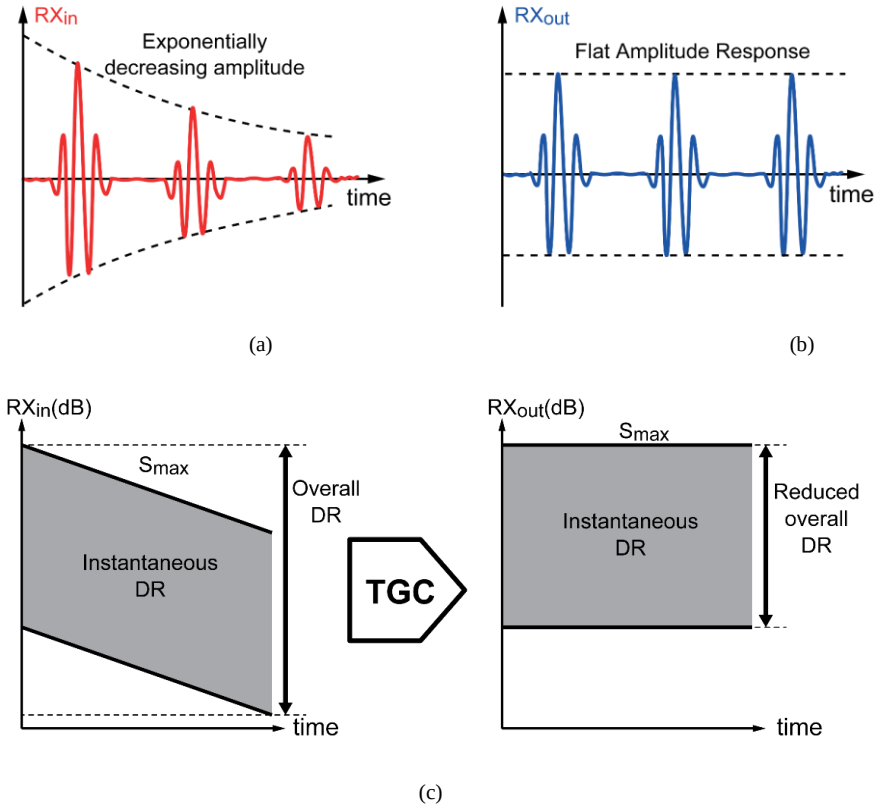
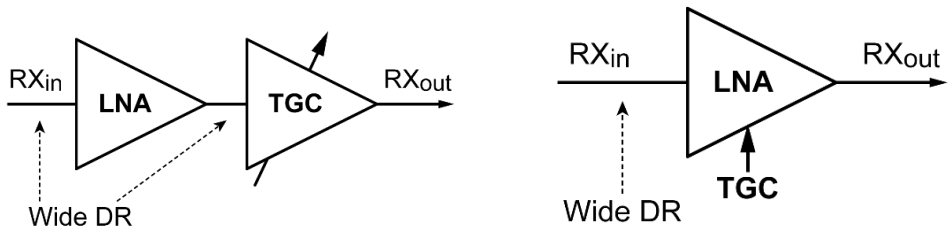


Figure 3.2 (a) RX signal before time-gain compensation (TGC); (b) RX signal after TGC; (c) RX input and output signal range as a function of time with ideal time-gain-compensation.

The impact of TGC on the signal DR is further illustrated in Figure 3.2(c), which shows how the range of echo-signal levels (the instantaneous DR) varies as a function of time (or, equivalently, depth) before and after TGC, demonstrating that the time-dependent attenuation is corrected for, thus reducing the overall DR to a level similar to the instantaneous DR. In conventional ultrasound systems, TGC is typically performed after the LNA [15], as shown in Figure 3.3(a), implying that a power-hungry LNA is required that is capable of handling the full DR of the echo signal at its output.

In this chapter, we present an LNA with a built-in continuous TGC function that mitigates this problem, as shown in Figure 3.3(b) [16]. The LNA is a transimpedance amplifier (TIA) optimized to amplify the signal current of a capacitive micro-machined ultrasound transducer (CMUT). We demonstrate its integration into a 64-channel ASIC for a CMUT-based ICE probe, as shown in Figure 3.1(b). While the LNA has been designed for application in an ICE probe, the presented amplifier architecture is applicable to ultrasound front-ends for miniature ultrasound probes in general.

This chapter is organized as follows. Section 3.2 reviews the existing approaches for TGC. Section 3.3 describes the proposed TIA architecture. The circuit implementation details of the TIA are presented in Section 3.4. Electrical measurements and imaging experiments are presented in Section 3.5. The chapter ends with a comparison with the state-of-the-art and conclusions.



(a) (b)

Figure 3.3 (a) block diagram of the conventional solution of an LNA followed by a TGC amplifier; (b) block diagram of the proposed LNA with embedded TGC function.

3.2 Comparison of TGC Circuits

Various approaches have been taken to realize amplifiers suitable for TGC. They can globally be divided into two groups: amplifiers with discrete gain steps and amplifiers with continuous gain control.

Amplifiers with discrete gain steps approximate the ideal exponentially varying gain by a number of discrete gain steps that are sequentially applied. An important advantage of this approach is that the gain steps can be accurately defined by means of a digitally-programmable resistive feedback network, as illustrated in Figure 3.4(a) [17]–[21], a digitally-programmable capacitive feedback network [12], [13], [22], or a digitally-programmable current-steering feedback network [23]. Moreover, the gain steps can be divided among multiple amplifier stages, with course gain steps realized in the low-noise amplifier (LNA) at the input of the receive signal path, which enables the realization of highly power-efficient amplifiers [12], [19]. Switching from one discrete gain step to the next,

however, is typically associated with a switching transient that can lead to artefacts in the ultrasound image at a depth that corresponds to the gain-switching moment. Such artefacts can be made negligible by making the gain steps small [20], but this requires a large number of gain steps to cover the gain range, leading to a complex circuit that requires substantial die area.

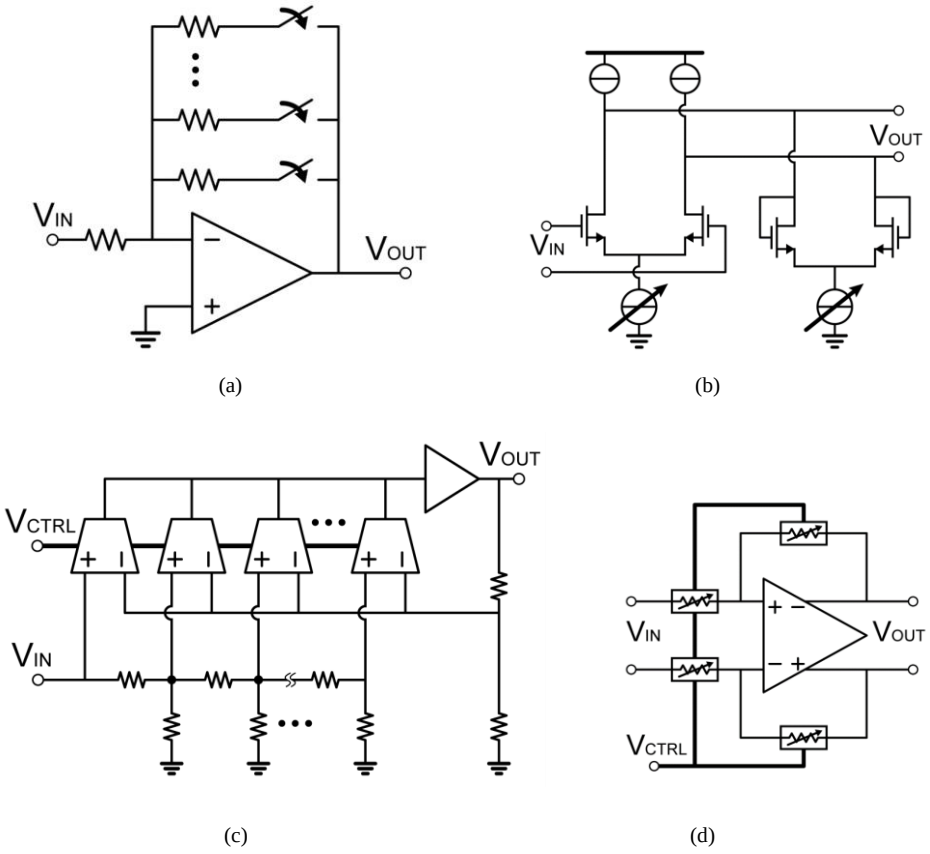


Figure 3.4 Circuits to realize time-gain compensation: (a) amplifier with discrete gain steps [17]-[21]; (b) amplifier with time-varying biasing [24]; (c) amplifier that interpolates between the outputs of a resistive ladder attenuator [29]; (d) amplifier using a feedback network with MOS variable resistors [23].

Amplifiers with continuous gain control are also referred to as variable-gain amplifiers (VGAs) and typically have a gain that can be set by an analog control input, typically a control voltage. The gain tends to depend (approximately) exponentially on the control voltage, giving a linear-in-dB gain control. By ramping the control voltage linearly as a function of time, the gain can be swept across a desired range to realize TGC without the disadvantages associated with discrete gain steps. The many ways in which this can be

realized can be roughly divided into two categories: amplifiers with an approximately exponential transfer function, and amplifiers with interpolation between discrete gain steps.

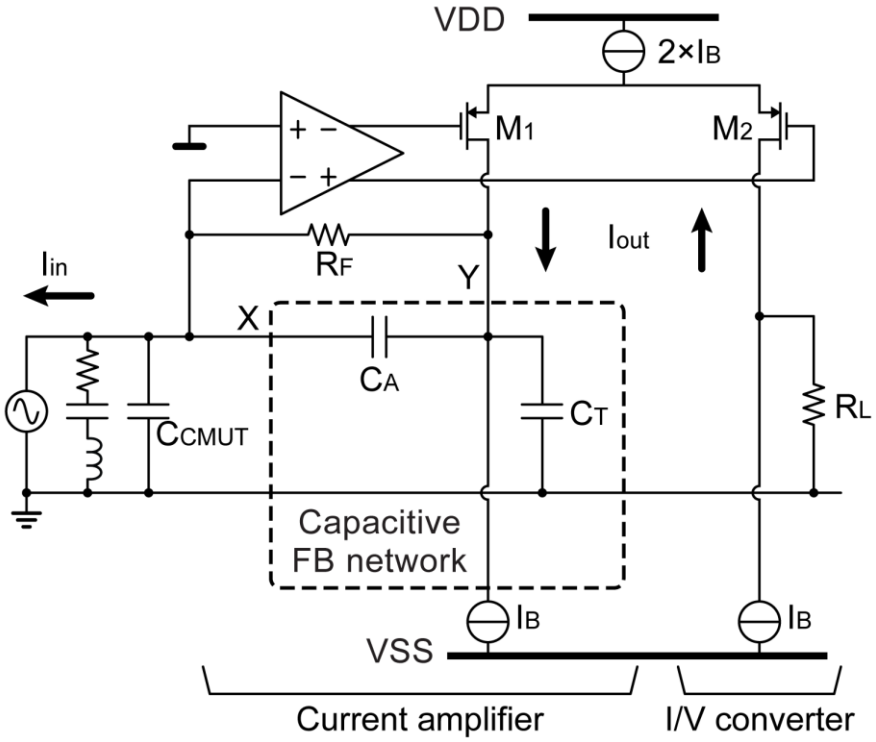


Figure 3.5 Simplified circuit diagram of the proposed TIA with a fixed-gain capacitive feedback network.

Amplifiers with an approximately exponential transfer function typically exploit the non-linear characteristics of MOS or bipolar transistors to realize variable gain. This can be done, for instance, by changing the operating point of a differential pair as a function of a gain-control voltage, leading to a variable transconductance. Combined with a load with an impedance that is also dependent on the control-voltage, for instance, by changing the operating point of diode-connected transistors as a function of the same control voltage, an amplifier with a non-linear transfer function is obtained, as shown in Figure 3.4(b) [24], [25]. However, this non-linear transfer function only approximates an exponential across a limited gain range, and tends to be sensitive to process, supply voltage and temperature (PVT) variations. Multiple stages can be cascaded to extend the range [26], [27].

Another approach to approximate an exponential transfer function is to use the exponentially increasing output voltage of a positive-feedback amplifier during a well-defined time window [28]. This approach, however, requires that the signal is sampled at the amplifier's input,

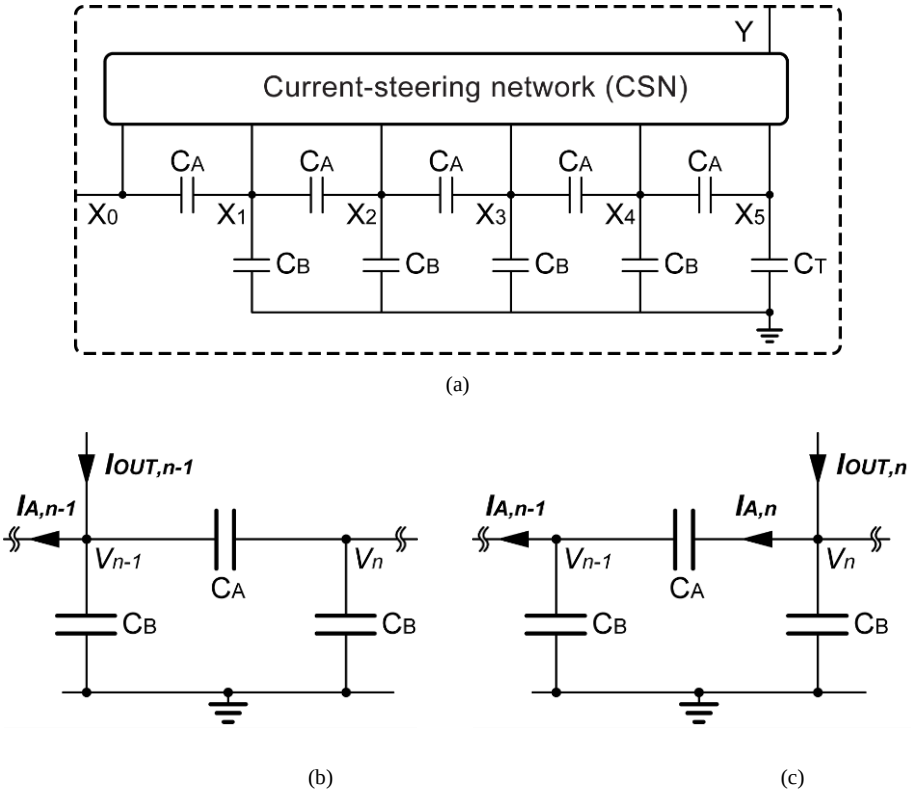


Figure 3.6 (a) Capacitive ladder feedback network with CSN to realize variable gain; (b) an arbitrary section of the ladder network, with a feedback connection to node $n-1$, and (c) to node n.

allowing each successive sample to be amplified using the positive-feedback amplifier, and the gain to be varied from sample to sample by changing the positive-feedback time window.

A TGC amplifier topology with interpolation between discrete gain steps has been reported in [29], [30]. As illustrated in Figure 3.4(c), the input signal is attenuated by a resistive ladder network, each section of which provides a fixed attenuation step in dB. These attenuated signals are fed to an amplifier with multiple input stages, the bias currents of which are controlled in order to gradually change from one step to the next. Another topology that employs multiple inputs stages with controlled biasing has been reported in [31], where the attenuating network is part of the feedback of the amplifier, and the input stages directly connect to the input in order to provide not only variable gain, but also simultaneously varying input noise and signal swing.

Interpolation between discrete gain steps can also be achieved by smoothly changing the components values in a passive attenuator network by including MOS transistors that act as

variable resistors, as illustrated in Figure 3.4(d) [23], [32]. Special biasing circuits are needed in order to mitigate PVT dependence.

A third approach to achieve interpolation between discrete gain steps is to use a differential pair as a current-steering device. In [33], a differential pair at the output of an amplifier directs a fraction of the output current back to the input, and a fraction towards the output. Thus, the current gain of this amplifier can be continuously controlled through the voltage applied to the differential pair. In an amplifier with two parallel input stages, [34] uses current steering to control how much of the output current of the current produced by these input stages are added to the output.

Compared to the prior art, the amplifier proposed in this work has three appealing features. Firstly, it provides continuous TGC, avoiding the switching artefacts associated with discrete gain steps. Secondly, as the TGC function is realized in the LNA, it does not rely on a preceding (fixed-gain) LNA to obtain a good noise figure and/or to obtain a suitable input impedance, like in e.g. [23], [29], [30], [35]. Such a fixed-gain LNA has an output DR that equals the large input DR, which tends to be associated with additional power consumption in the output stage to achieve acceptable distortion at the largest signal levels, or with additional power consumption to reduce noise in the stage after the LNA if the LNA's gain is kept limited to avoid distortion. Thirdly, as it relies on capacitor ratios to define the gain, it avoids the additional noise associated with a resistive feedback network, and the PVT dependence of approaches that rely on non-linear device characteristics.

3.3 Architecture of the TIA with TGC

3.3.1 Current Amplifier based TIA

As mentioned, the proposed TIA has been designed to interface with a CMUT transducer. Such a transducer consists of a flexible micro-machined membrane that forms one of the electrodes of a parallel-plate capacitor. In response to an incoming pressure wave, the membrane is moving, leading to a small change in the capacitance. When the CMUT is DC biased, this change can be detected as a signal current [36]. The CMUT can then modeled as a signal-current source I_{in} shunted by a capacitance C_{CMUT} modeling the transducer's electrical capacitance, and a resonator representing its mechanical resonance, as shown in Figure 3.5. The transducer used in this work is operated at 5 MHz and has a capacitance of 15 pF.

To detect the signal current, a low-noise amplifier with a low input impedance is needed, making a TIA is a suitable choice [37]. In this work, an input-referred noise level of 2 pA/√Hz and a maximum signal current of 100 μA is targeted. A TIA with resistive feedback is commonly used [38], but does not readily support the widely variable gain needed for TGC. Moreover, resistive feedback contributes additional noise.

Therefore, instead, we use a TIA based on a current amplifier with capacitive feedback as a starting point, based on [39]. As shown in Figure 3.5, this TIA consists of a current amplifier with a gain defined by capacitors C_A and C_T, followed by a resistive load R_L that turns the amplified current into an output voltage. A high-ohmic feedback resistor R_F serves to set the DC operating point and plays a negligible role at the signal frequencies of interest. A loop amplifier senses the input voltage V_X so as to maintain a virtual ground at the input. As a result, the input current I_{in} is integrated on capacitor C_A, leading to a voltage V_Y across capacitor C_T, and an amplified output current

$$I_{OUT} = \left(1 + \frac{C_T}{C_A}\right) I_{IN} = \alpha I_{IN} \qquad (3\text{-}1)$$

Thus, the circuit provides a current gain of $\alpha = 1 + C_T/C_A$. We use this current gain mechanism to implement the required 40 dB gain range, as will be discussed shortly.

In contrast with [39], in which a single-ended loop amplifier and a source follower with a resistive load are used, we employ a fully-differential loop amplifier, and a differential pair (M1 and M2) that provides equal currents of opposite polarity to the feedback network and to R_L, to convert the amplified current to an output voltage. To avoid clipping, the bias current I_B should be larger than the maximum amplified current. The resulting overall transimpedance is $(1 + C_T/C_A)R_L$. This differential topology helps to reduce power-supply sensitivity and increases output voltage headroom.

3.3.2 Capacitive Ladder Feedback Network

Although variable gain could be realized by adjusting C_T/C_A, this would require a large capacitor ratio to achieve a 40 dB range, and dense gain steps to minimize switching artefacts between the gain steps. This would be unattractive in terms of die size and complexity. Therefore, as shown in Figure 3.6(a), we realize gain steps covering a wide range by means of a ladder structure, and then interpolate between these steps by means of a current-steering network.

Ignoring the interpolation for now, let us assume that the feedback node Y is connected to one of the nodes of the ladder network X_n ($0 \leq n \leq 5$ in our design). The ladder capacitors C_A, C_B and C_T are dimensioned such that the capacitance to ground at each node X_n equals C_T, which implies

$$C_B + \frac{C_A C_T}{C_A + C_T} = C_T \Rightarrow C_B = \frac{C_T^2}{C_A + C_T} \qquad (3\text{-}2)$$

We will now show that this choice causes every ladder section to contribute an additional gain factor $\alpha = 1 + C_T/C_A$. If the feedback is connected to node X_0, the output current

$I_{OUT,0}$ equals I_{IN}, corresponding to a gain of 1 ($= \alpha^0$). The ladder network then merely forms an additional capacitive load at the input. If the feedback is connected to X_1, the topology is the same as in Figure 3.5, and the output current equals $I_{OUT,1} = \alpha I_{IN}$.

Now consider a feedback connection to an arbitrary node X_{n-1}, associated with an output current $I_{OUT,n-1}$, as shown in Figure 3.6(b), and a feedback connection to the next node X_n, with output current $I_{OUT,n}$, as shown in Figure 3.6(c). Given that the feedback network is a linear passive network, the current $I_{A,n-1}$ flowing back towards the input and the voltage V_{n-1} at node X_{n-1} must be equal, implying

$$I_{A,n-1} = I_{OUT,n-1} - sC_T V_{n-1} = I_{A,n} - sC_B V_{n-1} \quad (3\text{-}3)$$

where $I_{A,n}$ is the current flowing in Figure 3.6(c) through the capacitor CA connecting node X_{n-1} to node X_n. This current can also be expressed in terms of $I_{OUT,n}$:

$$I_{A,n} = \frac{C_A}{C_A+C_T} I_{OUT,n} - s\frac{C_A C_T}{C_A+C_T} V_{n-1} \quad (3\text{-}4)$$

where the first term represents the fraction of $I_{OUT,n}$ that would flow to node X_{n-1} if V_{n-1} would be zero, and the second term represents the current flowing from node X_{n-1} to node X_n if $I_{OUT,n}$ would be zero. Substituting (3-2) and (3-4) into (3-3) gives

$$I_{OUT,n} = \left(1 + \frac{C_T}{C_A}\right) I_{OUT,n-1} = \alpha I_{OUT,n-1} \quad (3\text{-}5)$$

which proves by induction that $I_{OUT,n} = \alpha^n I_{IN}$.

Thus, by an appropriate choice of the capacitor values, exponential gain steps can be realized without requiring large capacitor ratios. In our implementation, we adopted a 5-section ladder network with $\alpha = 2.5$ (i.e. gain steps of 8 dB covering 40 dB) realized using integer multiples of a unit capacitor C_U: $C_A = 10C_U$, $C_B = 9C_U$ and $C_T = 15C_U$. This allows for a compact and well-matched layout. The value of C_U should be sufficient to keep the voltage

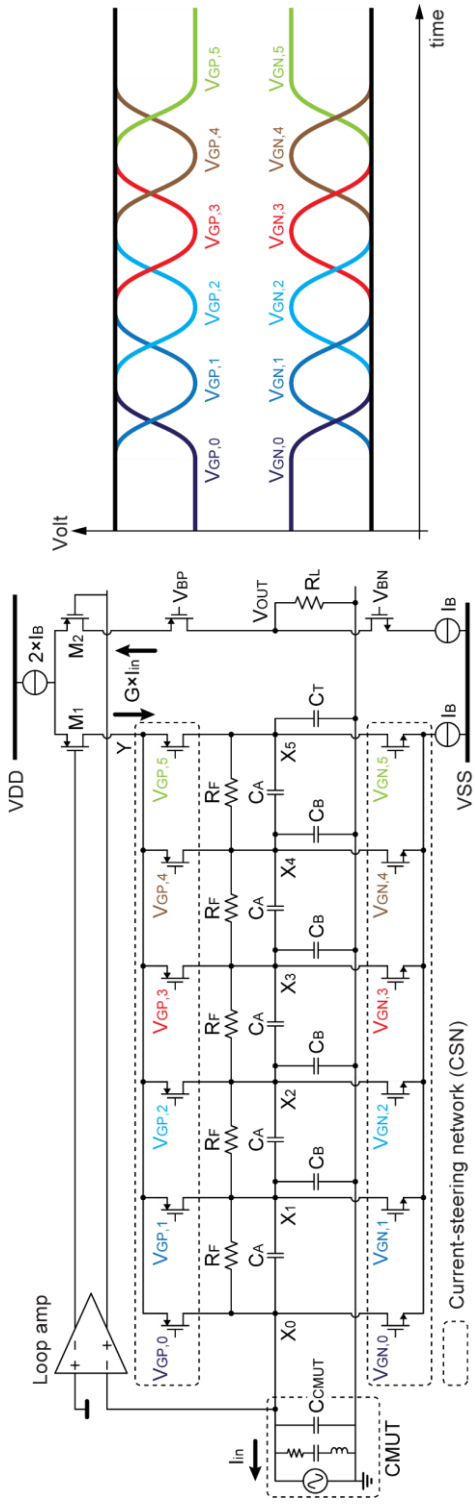
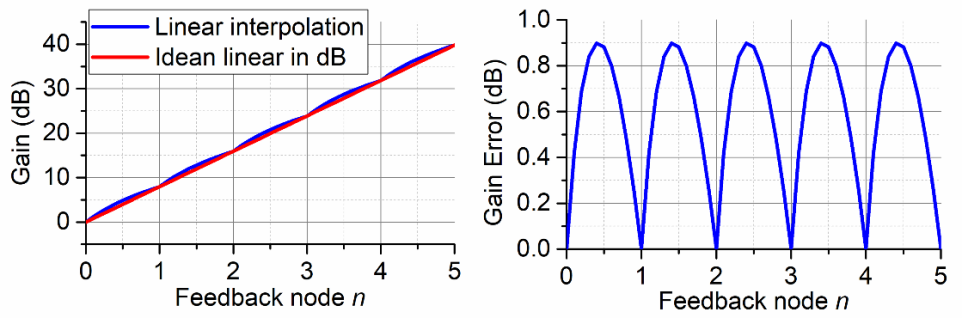


Figure 3.7 (a) Circuit diagram of the proposed TIA; (b) the gate-control voltages for the CSNs for continuous gain control.

swing in the network limited, and to make the impact of parasitic capacitance on the gain negligible. We use 0.3 pF to limit the swing to 360 mV at a maximum I_{IN} of 100 µA at 5 MHz.

3.3.3 Interpolation by means of Current Steering

To interpolate between the gain steps of the ladder network, we propose a current steering network (CSN) as shown in Figure 3.7(a). A set of PMOS transistors directs the feedback current at node Y to the ladder nodes X_n. The feedback current is initially steered completely to the input node X0, by providing a lower gate voltage $V_{GP,0}$to the corresponding PMOS transistor, as shown in Figure 3.7(b). The feedback current then gradually shifts from node to node, by alternately pulling down the gate voltages $V_{GP,n}$, effectively linearly interpolating between the exponential gain steps of the ladder network. Finally, the feedback current is steered entirely to the last tap, providing maximum gain. To bias the circuit, a complementary NMOS CSN, with similar complementary gate-drive voltages $V_{GN,n}$, steers a bias current I_B to the nodes of the feedback network. High-ohmic resistors R_F in the feedback network prevent charge accumulation due to small current differences between the CSNs, without affecting the in-band AC current gain.



(a) (b)

Figure 3.8 (a) Gain as a function of the selected feedback node Xn, for linear interpolation and for an ideal linear-in-dB curve; (b) Corresponding gain error relative to the linear-in-dB curve.

The CSN provides an approximately linear interpolation between exponential gain steps. The resulting error with respect to an ideal linear-in-dB (exponential) gain curve is shown in Figure 3.8. A ladder network consisting of 5 sections with a gain step of 8 dB each has been chosen to achieve a gain error less than 1 dB, in line with the requirements of the imaging application. This can be reduced by increasing the number of ladder sections. Note that the sharp dips in the gain-error curve in Figure 3.8(b) are due to the ideal linear interpolation

applied. The actual implementation using PMOS transistors and smoothly-varying gate voltages as illustrated in Figure 3.7(b) will lead to less sharp transitions in the gain-error curve.

3.3.4 Noise Analysis

To be able to detect the smallest echo signals at the highest gain, the TIA's noise contribution should not exceed that of the transducer. At the high end of the gain range, the noise contribution of the load resistor, the output differential pair and the bias-current sources is negligible, because they are attenuated by the 40 dB current gain when referred to the input. The feedback network, due to its capacitive nature, does not contribute in-band noise. This leaves the loop amplifier as the dominant noise source. Its input-referred voltage noise appears at the virtual ground and leads to an equivalent input current noise due to the total impedance to ground at the input. This impedance is dominated in our design by the CMUT capacitance of about 15 pF, and amounts to about 2 kΩ at 5 MHz. To achieve an equivalent input current noise below 1.5 pA/√Hz, the loop amplifier's input voltage noise should be below 3 nV/√Hz. Note that this noise levels only needs to be achieved at the highest gain level. At lower gain levels, the input signal is bigger, and so proportionally larger noise can be accepted without loss of SNR. Achieving this noise level in a power-efficient manner is one of the key design objectives for the loop amplifier implementation, as will be elaborated in the next section.

3.4 Circuit Implementation

3.4.1 Gain-Control Circuit

To generate the gate-control voltages $V_{GP,n}$ and $V_{GN,n}$ for the CSNs in Figure 3.7(b), an external gain-control voltage V_{TGC} is compared to a set of reference voltages generated using a stack of cascaded PMOS differential pairs, as shown in Figure 3.9. The reference voltages $V_{REF,i}$ are generated using a resistive divider.

Thus, as V_{TGC} is swept, the tail current is steered from drain to drain. The drain currents are mirrored to diode-connected PMOS and NMOS transistors at appropriate common-mode levels to generate $V_{GP,n}$ and $V_{GN,n}$, respectively, resulting in the voltages shown in Figure 3.7(b) when V_{TGC} is linearly ramped down.

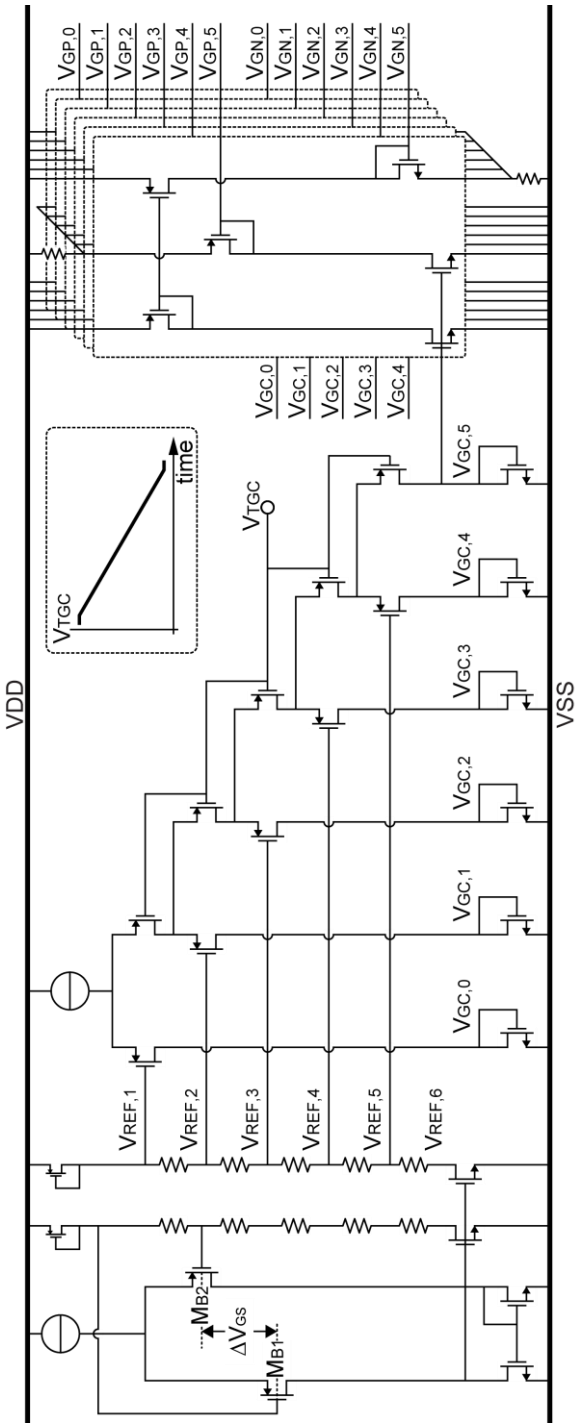


Figure 3.9 Circuit diagram of the gain control circuit

In this circuit, all PMOS differential pairs have identical sizes and have bulk connections to the source to mitigate the body effect. The bias current of the gain-control circuit is chosen such that the bandwidth of the circuit is sufficient to track the required V_{TGC} transient, while avoid excess bandwidth, as this would add undesired in-band noise to the signal path. The bias current for the resistive ladder is generated using the bias circuit shown in the left-hand side of Figure 3.9. This bias circuit employs a feedback loop to generate a current proportional to the difference in gate-source voltage ΔV_{GS} of ratioed PMOS transistors M_{B1} and M_{B2}. The bias circuit employs a replica of the resistive ladder, so that the voltage steps between the reference voltages equal ΔV_{GS}, making the current division in the PMOS differential pairs as a function of V_{TGC} insensitive to process and supply variations.

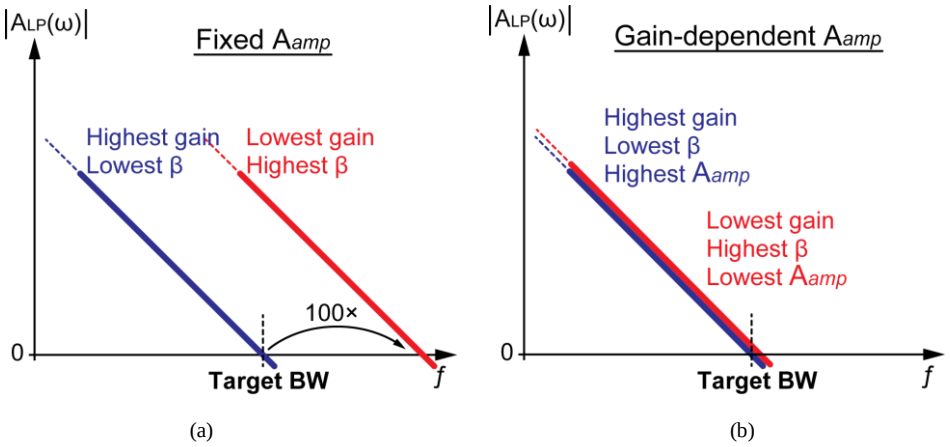


Figure 3.10 Magnitude of the loop-gain as a function of frequency, showing (a) a strongly gain-dependent unity-gain frequency for a fixed-gain loop amplifier, and (b) a constant unity-gain frequency for a loop amplifier with variable gain.

3.4.2 Loop Amplifier Design

A key challenge in the design of the loop amplifier is to maintain sufficient loop gain in the presence of the widely-varying current gain. We analyze the loop gain by breaking the feedback loop at the input of the loop amplifier. The resulting loop-gain $A_{LP}(\omega)$ consists of the product of the loop amplifier's voltage gain $A_{amp}(\omega)$ and the transfer function from the output of the loop amplifier back to the input:

$$A_{LP}(\omega) = A_{amp}(\omega) \cdot \frac{g_{m,out}\beta}{j\omega C_{in}} \qquad (3\text{-}6)$$

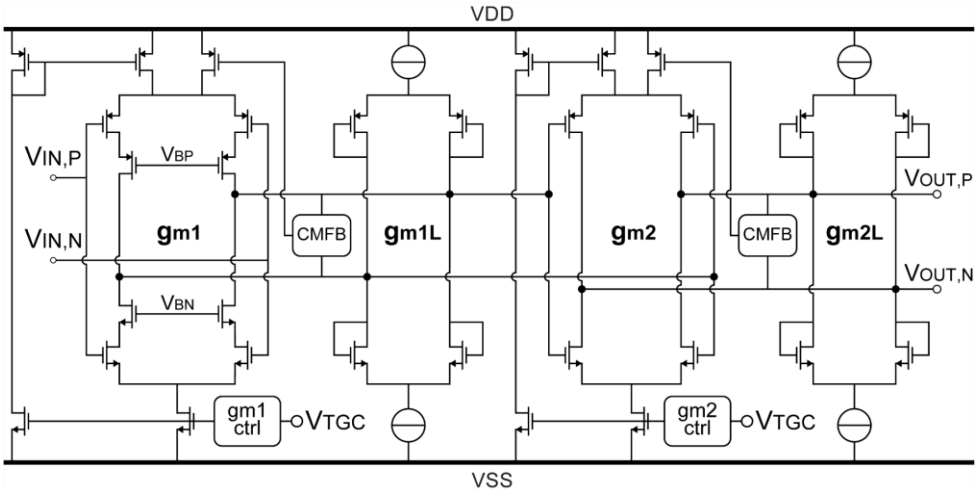


Figure 3.11 Circuit diagram of the loop amplifier.

where $g_{m,out}$ is the transconductance of the differential pair M1,2 (see Figure 3.5), β is the fraction of that differential pair's output current that makes it back to the input, and C_{in} is the total capacitance at the input, which is dominated by the CMUT capacitance C_{CMUT}. The fraction β is related to the closed-loop current gain, which in Section 3.3.2 has been shown to be αn. While the closed-loop current gain is independent of C_{in}, because C_{in} is at the virtual ground in the closed-loop configuration, C_{in} does influence the fraction β. However, if $C_{in} \gg C_T$, we can approximate the input as being shorted to ground by C_{in}, and the factor β is then by good approximation the inverse of the current gain α^n. If we assume that the loop amplifier has a constant gain and a wide bandwidth, i.e. that $A_{amp}(\omega)$ is constant across the frequency range of interest, this implies that for a 40 dB variation in current gain, the unity-gain frequency of $A_{LP}(\omega)$, which sets the closed-loop 3 dB bandwidth, would vary by a factor 100, as illustrated in Figure 3.10(a). In order to achieve enough bandwidth at the highest current gain, which corresponds to the lowest β, we would obtain a bandwidth that is 100 times larger than needed at the lowest current gain, which corresponds to the highest β. To realize this, the loop amplifier would need to have an unrealistically wide bandwidth.

Therefore, instead, we employ a loop amplifier whose gain $A_{amp}(\omega)$ is adjusted to compensate for the varying β. For the highest current gain (i.e. the lowest β), we make the DC gain of the loop amplifier roughly 100 times higher than for the lowest current gain (i.e. the highest β). This gives the loop an approximately constant unity-gain frequency, corresponding to an approximately constant closed-loop 3 dB bandwidth, as illustrated in Figure 3.10(b). Any poles in the loop amplifier should be sufficiently above this frequency to maintain stability.

Since the required gain-bandwidth product of the loop amplifier is hard to realize with a single-stage amplifier, we use a cascade of two stages, as shown in Figure 3.11. A fully-

differential amplifier structure is adopted. The first stage consists of a current-reuse input stage with diode-connected load transistors, resulting in a gain set by the transconductance ratio g_{m1}/g_{m1L}. The transconductance of the input stage g_{m1} is defined by the tail current, which is shared by the NMOS and PMOS pair to improve power efficiency [40]. This tail current is varied as a function of the gain-control voltage V_{TGC} (details provided in Section 3.4.3) to obtain the required variable gain. Besides maintaining constant bandwidth, this scheme also saves power, by ensuring that the input stage is biased at the highest current level only at the high end of the gain range, where the lowest input noise is required, in line with the noise requirement discussed in Section 3.3.4. For lower gain levels, at which a higher input noise is acceptable, the bias currents are reduced.

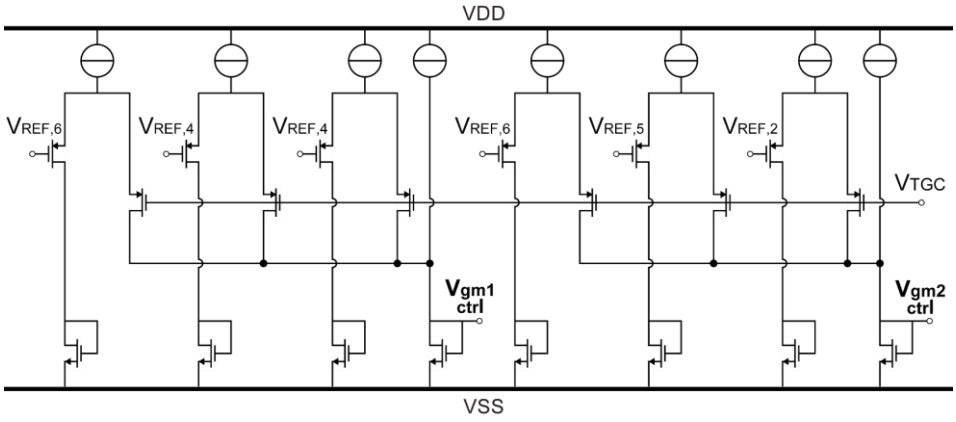


Figure 3.12 Circuit diagram of the transconductance-control circuit.

At the chosen bias point, the input transistors suffer from relatively low output impedance and large gate-drain capacitance, which degrades the gain and increases the input-referred noise. To mitigate these effects, cascade transistors are employed.

A similar second stage provides additional gain g_{m2}/g_{m2L}. In this case, the input is a current-reuse stage without cascoding for simplicity. Again, a tail current dependent on V_{TGC} is used to obtain the overall desired variable gain. Each stage has its own common-mode feedback circuit (CMFB) to maintain a proper DC biasing point.

3.4.3 Transconductance-Control Circuit

The circuit that generates the bias currents for the loop amplifier as a function of V_{TGC} is shown in Figure 3.12. A current steering mechanism similar to that used in the Gain-Control Circuit (Figure 3.9) is employed, in which V_{TGC} is compared to reference voltages by means of differential pairs. For each stage of the loop amplifier, three PMOS differential pairs are used of which the tail currents add to the bias current when V_{TGC} drops below the respective reference voltage. The tail current levels and reference voltage levels (derived from the

resistive divider shown in Figure 3.9) have been chosen based on simulation to obtain a near-constant closed-loop bandwidth and sufficient phase margin.

3.5 Experimental Results

3.5.1 Experimental Prototype

The ASIC has been fabricated in 0.18 μm HV BCDMOS process. The ASIC consists of 64 RX and TX channels, each of which interfaces with one element of a 64-element CMUT transducer array. Each RX channel consists of the proposed TIA and a cable driver [41], and is powered by a ±0.9 V analog supply and a 1.8 V logic supply. Each TX channel has a programmable high-voltage (HV) pulser to generate pulses with a maximum amplitude of ±30 V, and a HV transmit/receive (T/R) switch to protect the low-voltage RX circuits during pulse transmission. Details of the TX-channel circuitry have been reported in [42]. The channels are arranged in two rows with 32 blocks in each row. This arrangement enables direct pitch-matched connection to the 64-element CMUT transducer array. Figure 3.13 shows a photograph of the chip. The proposed TIA occupies an area of 0.12 mm^2.

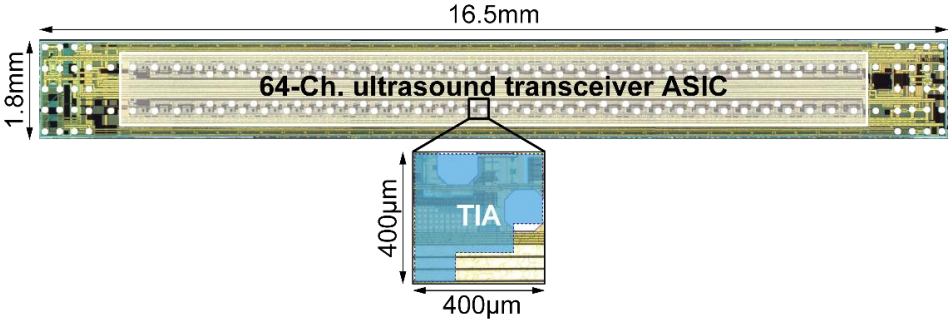
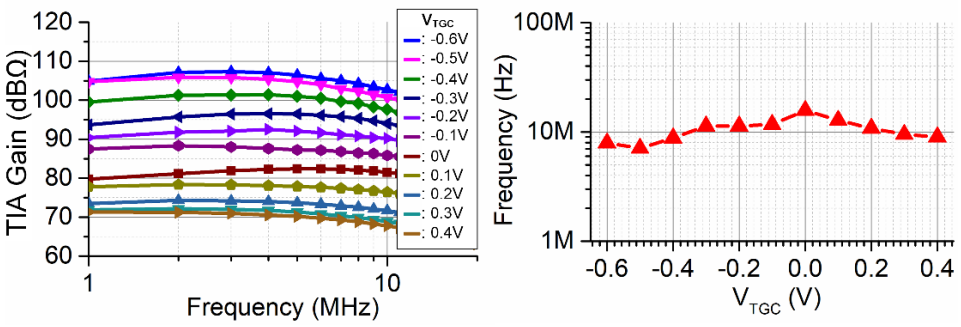


Figure 3.13 Chip micrograph of the 64-channel transceiver ASIC, with inset showing the element-level TIA.

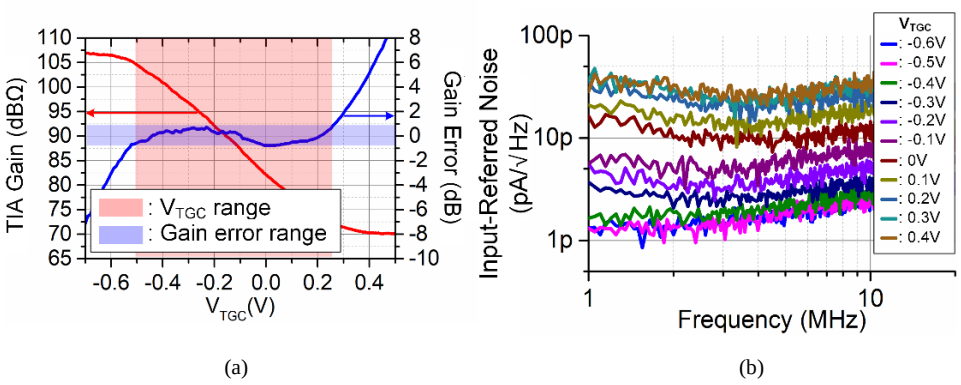
3.5.2 Electrical Characterization Results

To measure the TIA's transfer function, an input current was generated by applying a voltage signal to a 15 pF off-chip capacitor, which mimics the CMUT capacitance, connected to the TIA's input. Figure 3.14(a) shows the measured transfer function over the whole gain range. As shown in Figure 3.14(b), the -3 dB bandwidth varies between 7.1 MHz and 15.7 MHz across the gain range. Compared to the gain variation of almost 40 dB, the bandwidth is kept relatively constant, in good agreement with the designed adaptive gain operation of the loop amplifier.



(a) (b)

Figure 3.14 (a) Measured transfer function, and (b) corresponding -3dB bandwidth as a function of V_{TGC}.



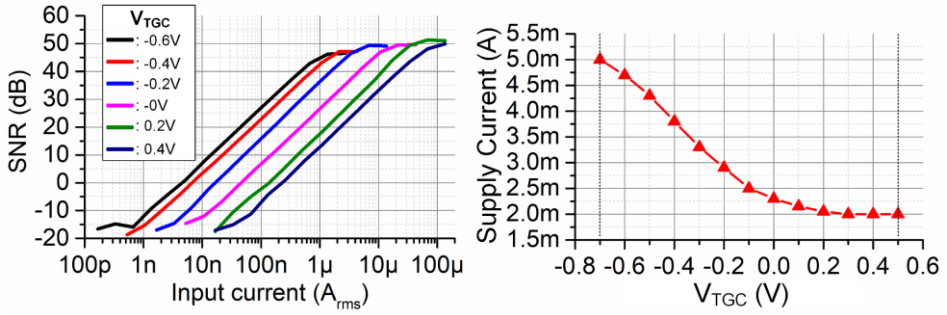
(a) (b)

Figure 3.15 (a) Measured gain at 5 MHz as a function of V_{TGC}, with the associated error compared to a linear-in-dB curve; (b) input-referred noise spectrum

Figure 3.15(a) shows the TIA gain at 5 MHz as a function of the TGC control voltage (V_{TGC}). Note that, as expected, the gain decreases with increasing values of V_{TGC}, which in combination with a V_{TGC} that decreases with time leads to the desired gain that increases with time. The TIA gain can be varied continuously across a 37 dB range. The corresponding gain error with respect to an ideal linear-in-dB curve is less than ±1 dB across the middle 33 dB of the gain range.

The input-referred noise of the TIA was determined by connecting the same off-chip capacitor at the input of the TIA, measuring the output noise, and dividing it by the measured transfer function. The resulting input-referred noise spectra for different values of V_{TGC} are shown in Figure 3.15(b). The noise floor is 1.7 pA/√Hz at 5 MHz at the highest gain, which is comparable to the CMUT noise floor. The measured spectra also demonstrate that the noise

floor increases for lower TIA gains, as expected due to the adaptive biasing of the loop amplifier. At the lowest gain, the noise floor is about 30 pA/√Hz at 5 MHz. This increase of about 25 dB is less than the expected increase in the signal level of about 40 dB. Therefore, the signal-to-noise ratio (SNR) is not degraded by this gain-dependent noise floor.



(a) (b)

Figure 3.16 (a) Measured SNR as a function the signal amplitude for different values of V_{TGC}; (b) measured supply current as a function of V_{TGC}.

This is confirmed by the DR measurement shown in Figure 3.16(a), which shows the measured output SNR as a function of the input signal current for different values of V_{TGC}. The overall input DR, defined as the ratio between the input level at which1 dB compression occurs at the lowest gain and the input level at which the SNR reaches zero at the highest gain, amounts to 82 dB. The variable gain reduces this to 46 dB at the output. As expected, due to the adaptive biasing, the TIA supply current also changes in a gain-dependent manner, as shown in Figure 3.16(b). Assuming a linear variation of V_{TGC} as a function of time to cover the gain range, the variable supply current leads to an average power consumption of 5.2 mW.

Figure 3.17 shows the measured transient behavior of the continuous TGC operation. A continuous sinusoidal input current with a frequency of 7 MHz and an exponentially decreasing amplitude, and a corresponding ramp signal are applied to the TIA's input and the gain-control port, respectively. The measured output has an approximately constant and smoothly-compensated output swing. The gain error extracted from the output amplitude variation is less than ± 1 dB, demonstrating the intended continuous linear-in-dB TGC operation.

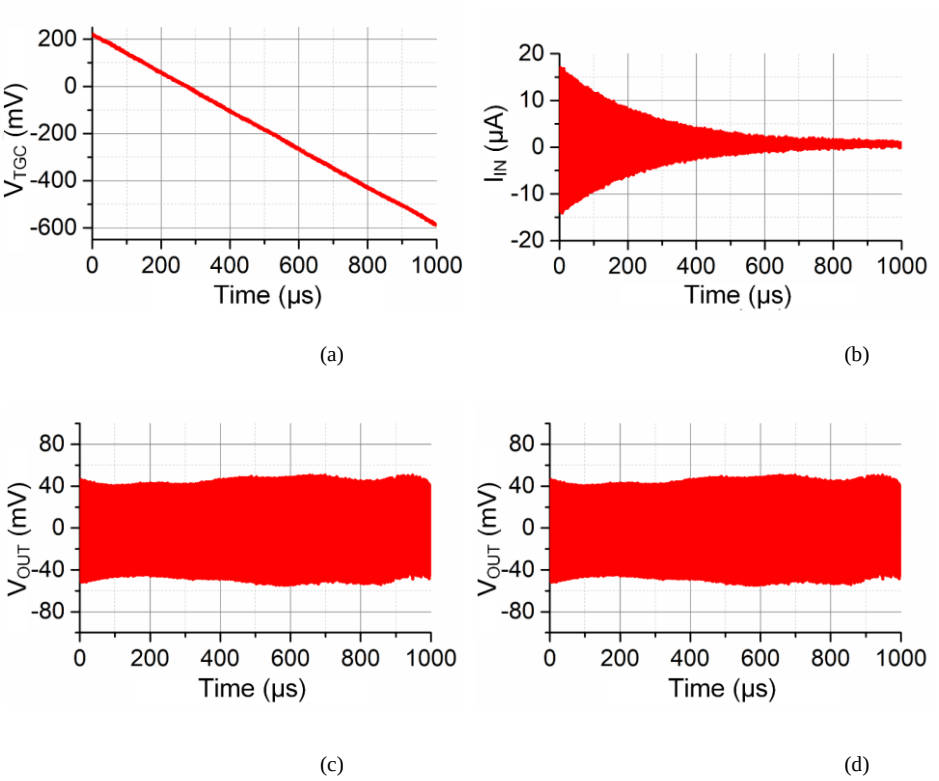
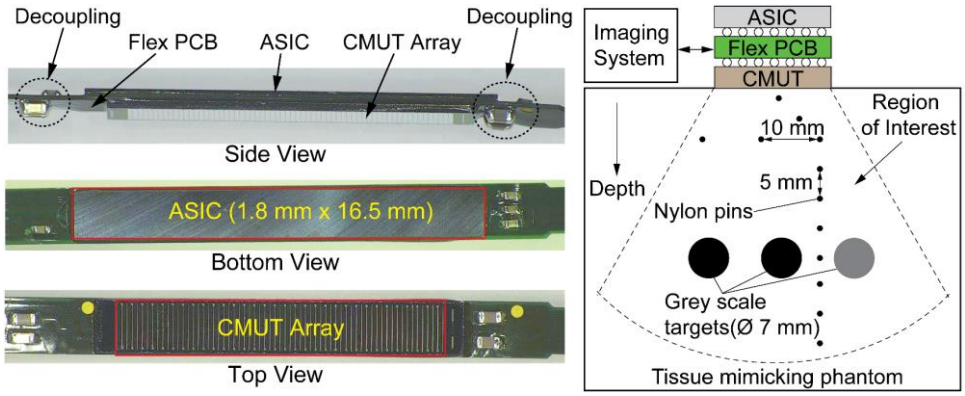


Figure 3.17 Measured transient TGC operation: (a) applied TGC control voltage; (b) applied exponentially decreasing input signal; (c) measured output signal; (d) corresponding error with respect to a linear-in-dB gain curve.

3.5.3 Acoustical Experiments

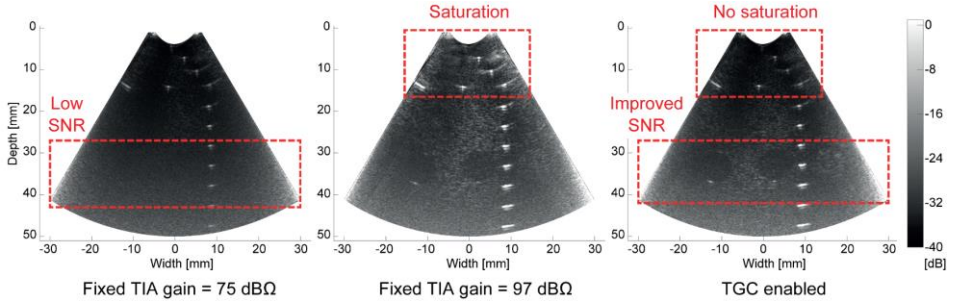
Figure 3.18(a) shows a fabricated prototype in which the ASIC and CMUT have been flip-chip bonded on a Flexible Printed Circuit Board (flex PCB). Each TX/RX channel on the ASIC directly interfaces with a CMUT element. The TIA outputs, buffered by the cable drivers, go to a Verasonics imaging system (Verasonics Inc., Redmond, WA) [43] to record the received echo signals. The flex PCB also connects the power supplies, with local decoupling capacitors, to the ASIC, as well as digital control signals, which are provided by an FPGA.

The test-bench for imaging experiments is shown in Figure 3.18(b). The implemented prototype is placed at the surface of a tissue-mimicking phantom (GAMMEX SONO404) with an attenuation coefficient of 0.5 dB/cm/MHz. The phantom contains nylon wires acting as point reflectors and grey-scale targets to evaluate the SNR in the image.



(a) (b)

Figure 3.18 (a) Implemented prototype; (b) overview of the measurement setup used for acoustic characterization.



(a) (b) (c)

Figure 3.19 Phased-array B-Mode images with a ±45° opening angle, obtained with (a) fixed low gain, (b) fixed high gain, (c) the proposed continuous TGC operation.

Figure 3.19 shows ±45° phased-array B-mode images of the phantom with 64-channel TX and RX operation. Figure 3.19(a) is obtained using a fixed TIA gain of 75 dBΩ. As this gain is optimized for the near field, the circular grey-scale targets at larger depth are hardly distinguishable. When the gain is fixed at a higher value of 97 dBΩ to improve SNR at larger depth (Figure 3.19(b)), the RX signal at the shallow depths suffers from saturation, leading to a too bright image. With continuous TGC, these issues are mitigated, leading to a higher-quality image in which no saturation occurs and the grey-scale targets can be clearly distinguished from the surrounding speckle pattern (Figure 3.19(c)). This imaging experiment successfully demonstrates the continuous TGC capability of the prototype.

TABLE 3-1 PERFORMANCE SUMMARY AND COMPARISON

	This work	[22]	[46]	[47]	[48]	AD8332 [44]	VCA2617 [45]
Process	0.18 μm HV BCDMOS	0.18 μm HV BCDMOS	0.18 μm HV CMOS	0.35 um CMOS	BCD-SOI	-	-
BW	7MHz	16MHz	10MHz	40MHz	11MHz	100MHz	50MHz
LNA type	TIA	TIA	TIA	TIA	TIA	Voltage amp	Voltage amp
Max gain	107dBΩ	119dBΩ	116dBΩ	106dBΩ	78.4dBΩ	68.5dB	38dB
Full gain range	37dB	12dB	12dB	0dB	0dB	48dB	48dB
Gain error(1) (gain range)	± 1dB (33dB)	± 3dB(2) (12dB)	± 3dB(2) (12dB)	-	-	± 0.3dB (42dB)	± 0.9dB (37dB)
Gain control	Continuous	Discrete	Discrete	Fixed gain	Fixed gain	Continuous	Continuous
Transducer capacitance	15pF	0.7pF	2 pF	0.09pF	9.2pF	-	-
Input referred noise	1.7pA/√Hz @5MHz	2.0pA/√Hz @13MHz	0.41pA/√Hz @ 5MHz	0.31 pA/√Hz @ 20MHz	5.1pA/√Hz @10MHz	0.74 nV/√Hz @5MHz	4.1nV/√Hz @5MHz
Power consumption	5.2mW	0.42mW	1.4mW	0.8mW	1mW	138mW	52mW
NEF'(3)	0.78(4)	1.23(4)	2.7	-	0.55	-	-

(1) Maximum deviation from the ideal linear-in-dB curve across the mentioned gain range

(2) Estimated from the discrete gain step

(3) NEF' = $p_{n,in}\cdot\sqrt{Power_{tot}}$ [mP·√(mW/Hz)] [46] where $p_{n,in}$ is the input-referred acoustic pressure noise spectral density averaged inside the passband

(4) Calculated by referring the measured noise to an equivalent pressure noise using the estimated transducer sensitivity

TABLE 3-1 compares the proposed TIA with the prior art. Compared to commercial LNAs with continuous TGC function [44], [45], >10× lower power consumption is achieved. While some of this difference may be attributed to the proposed circuit architecture, it should be noted that these parts have quite different noise and bandwidth specifications, and are not intended for in-probe integration. Compared to prior in-probe TIAs, which employ discrete

steps or fixed gain [22], [44]–[48], comparable performance is obtained, but with much wider gain range and without the imaging artefacts associated with gain switching.

3.6 Conclusion

This chapter has presented a low-noise TIA with continuous TGC for ultrasound imaging applications. The TIA employs a capacitive ladder feedback network and interpolation by means of current steering to provide linear-in-dB gain control. The proposed architecture combines LNA and TGC functionality in a single feedback loop, leading to better power efficiency than solutions that employ a fixed-gain LNA followed by a TGC stage, in which the LNA needs to be able to handle the full input DR at its output. In order to accommodate the large variation in the feedback factor, a current-reuse loop amplifier with adaptive biasing has been introduced, which provides approximately constant closed-loop bandwidth and saves power by allowing higher input noise at the lower part of the gain range.

Compared to prior in-probe TIAs, which employ discrete steps or fixed gain, competitive noise efficiency and a wider gain range are obtained without gain-switching transients. The presented electrical measurements demonstrate continuous gain control that is linear-in-dB to within ±1 dB. Imaging results obtained in combination with a 64-element CMUT transducer show reduced imaging artefacts and highlight that the presented topology is a promising solution for future in-probe ultrasound ASICs.

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CHAPTER 4

FRONT-END ASIC WITH HIGH-VOLTAGE TRANSMIT SWITCHING AND RECEIVE DIGITIZATION

This chapter is based on the publication: M. Tan, C. Chen, Z. Chen, J. Janjic, V. Daeichin, Z.-Y. Chang, E. Noothout, G. van Soest, M. D. Verweij, N. de Jong and M.A.P. Pertijs, "A Front-End ASIC with High-Voltage Transmit Switching and Receive Digitization for 3D Forward-Looking Intravascular Ultrasound Imaging", IEEE J. Solid-State Circuits, vol. 53, no. 8, pp. 2284-2297, Aug. 2018.

4.1 Introduction

Coronary artery disease is caused by atherosclerosis of the coronary arteries of the heart [1]. It has become one of the most common causes of death worldwide [2]. Intravascular ultrasound (IVUS) imaging, using an ultrasound transducer mounted at the tip of a catheter, is an important tool for the visualization, diagnosis and treatment of atherosclerosis [3].

Conventional IVUS catheters are side-looking (SL) devices that provide a 2D cross-sectional image of the vessel wall. An ultrasound transducer mounted at the tip of the catheter is excited by high-voltage pulses to generate an acoustic pulse, and the resulting echo signals are processed to form the image. IVUS catheters employ either a mechanically-rotating single-element transducer [4], or 64 elements folded around the tip of the catheter [5, 6]. Mechanical

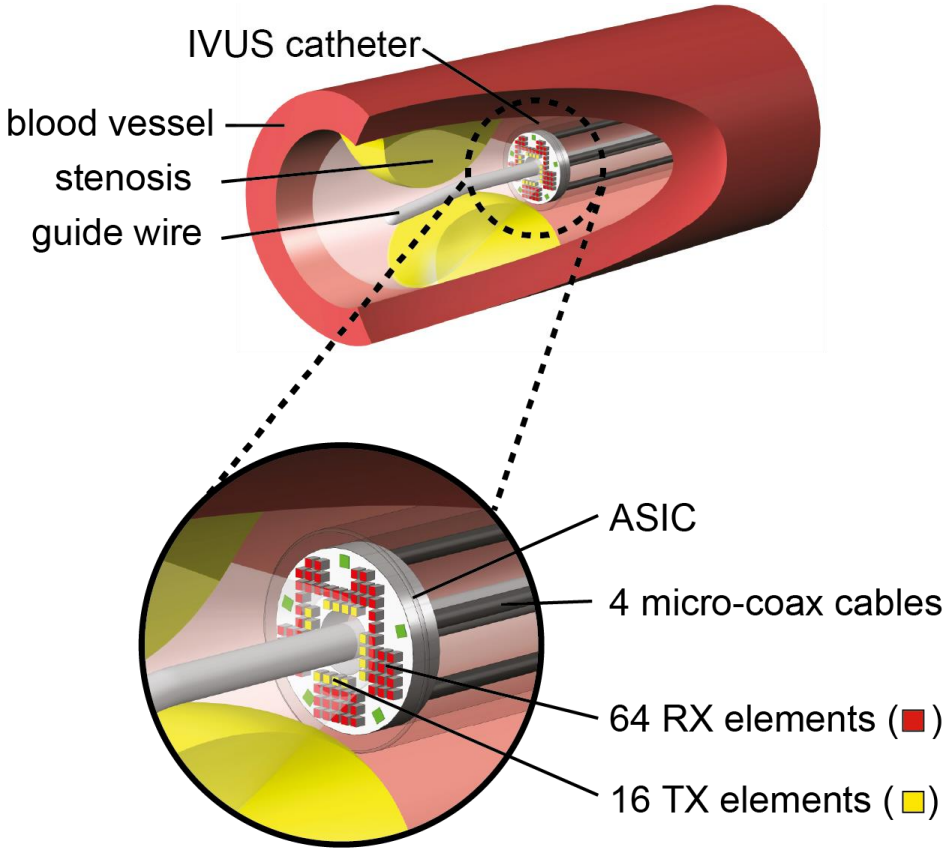

Figure 4.1 A conceptual diagram of the forward-looking IVUS catheter.

rotation is complex to implement, and relatively slow, leading to motion artefacts in the image [7], while the use of a transducer array comes with an electrical interconnect challenge due to the limited number of cables that can be accommodated in a catheter shaft.

A severe case of coronary artery disease is a chronic total occlusion, a condition in which atherosclerotic plaque completely blocks the vessel. Successful recanalization of such occlusions using guidewires is associated with improved left ventricular function and reduced mortality [8, 9]. For this type of lesions, forward-looking (FL) imaging is required, since imaging ahead of the catheter tip can help to distinguish between plaque and normal vessel wall during the crossing procedures, hence reducing the risks of dissections and vessel perforation [3].

Early implementations of FL-IVUS catheters are based on the scanning motion of a FL single-element transducer [10, 11] or a rotating single element oriented at 45° angle [12]. Both implementations require rotation and multiple acquisitions to construct a 2D image, and are sensitive to motion artifacts. In order to achieve real-time forward-looking 3D imaging without rotation, a circular transducer array [13, 14], or a 2D transducer array [15] can be

placed at the tip of the catheter. However, connecting the resulting relatively large number of elements (50-100) using micro-coaxial cables within the catheter diameter of < 2 mm is extremely challenging.

ASICs for FL-IVUS have been reported that employ pulsers and multiplexers to reduce the number of cables, but these still require at least 13 connections [13, 14, 16]. Moreover, they communicate the received echo signals to the imaging system in an analog form, which is relatively susceptible to interference and not amenable to digital multiplexing or data-reduction approaches. Also, the use of wireless data transmission has been proposed to reduce the cable count [17], but the integration of the required antenna on a catheter is challenging, and successful wireless operation on a catheter is yet to be demonstrated.

This paper presents a front-end ASIC that requires only 4 micro-coaxial cables to interface with a total of 80 piezoelectric transducer elements fabricated on top of the ASIC: 64 receive (RX) elements and 16 transmit (TX) elements [18]. In contrast with prior work, the ASIC digitizes the received echo signals locally, allowing their transmission to an external imaging system in a robust form, and demonstrating the feasibility of in-probe digitization within the stringent size, power and interconnect constraints of a FL-IVUS probe. The ASIC has been designed for FL-IVUS, but the presented approaches to in-probe digitization, cable-count reduction and high-voltage switching are equally applicable in a SL-IVUS probe, or in other miniature probes, such as intra-cardiac echography (ICE) catheters.

Figure 4.1 illustrates conceptually how the ASIC will be mounted at the tip of a catheter. The ASIC will be laser-cut into a donut shape, with an outer diameter of 1.5 mm and an inner hole of 0.5 mm for the guide wire. The ASIC enables synthetic aperture imaging, in which acoustic pulses are transmitted using one or multiple TX elements, and the resulting received echoes are recorded by one RX element at a time. Expanding on our earlier publication [18], which reports preliminary results obtained using a test transducer array that is connected to the ASIC using wire bonds, this paper presents a detailed description of the design and new experimental results obtained with transducer elements integrated on top of the ASIC. This

TABLE 4-1. Key parameters of the applied transducer elements.

Size	80 µm × 80 µm
Resonance Frequency	13 MHz
-3 dB Bandwidth	44% (10 MHz ~ 16 MHz)
Impedance at Resonance	0.7 pF // 5 kΩ
Transmit Efficiency	0.4 kPa/V @ 6 mm
Receive Sensitivity	4 µV/Pa

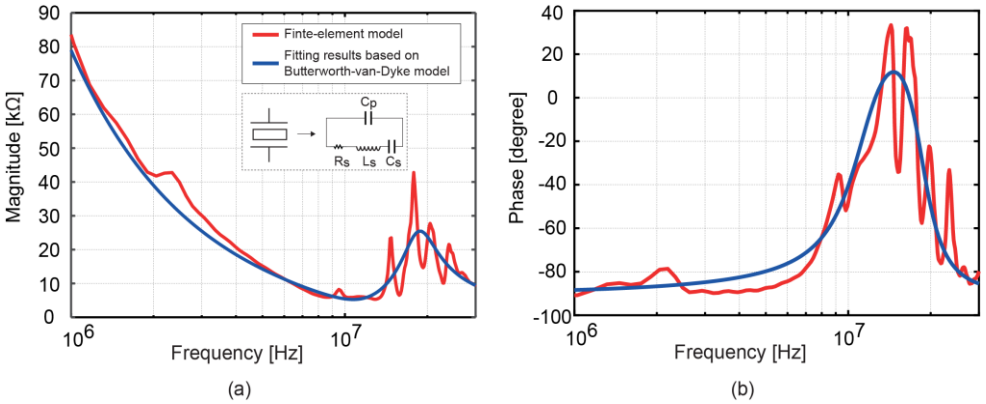

Figure 4.2 Simulated impedance characteristics obtained using finite-element modeling, and the fitting results based on the Butterworth-van-Dyke model; (a) magnitude versus frequency; (b) phase versus frequency.

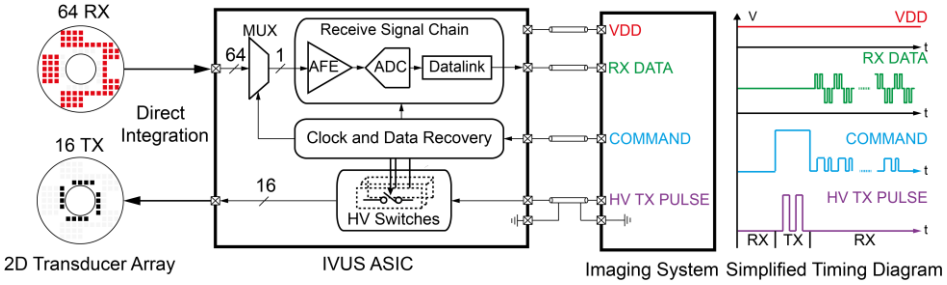

Figure 4.3 Block diagram of the IVUS ASIC.

chapter is organized as follows. Section 4.2 describes the proposed system architecture. Section 4.3 discusses the details of the circuit implementation. Sections 4.4 and 4.5 present the experimental results and conclusions.

4.2 System Architecture

4.2.1 Transducer Array

FL-IVUS probes have been reported that apply a ring-shaped transducer array based on Capacitive Micromachined Ultrasonic Transducers (CMUTs) [13, 14] or a 2D matrix array based on piezo-electrical (PZT) transducers [15]. These designs either have a relatively low signal to noise ratio or require a large number of cables to be integrated. To overcome these limitations, we have developed a PZT-based matrix transducer with a total of 80 elements only needing 4 coaxial cables to be integrated inside a catheter. The transducer elements for

transmit and receive are separated (16 for TX and 64 for RX), as illustrated in Figure 4.1. The transducer array built on top of the ASIC uses the approach described in [19].

We employ 80 µm × 80 µm transducer elements with a pitch of 100 µm. The center frequency of these elements is 13 MHz. This is lower than the frequencies typically used in SL-IVUS devices, which operate at 20 MHz or above [5, 6]. The chosen frequency is comparable to earlier FL-IVUS designs, e.g. [14, 20], and trades off resolution for larger penetration depth as required in forward-looking imaging. The -3 dB bandwidth of the elements is 44% (10 MHz ~ 16MHz). The impedance characteristic of the transducer elements has been simulated using finite-element analysis software (PZFlex LLC, Cupertino), as shown in Figure 4.2. This simulation includes the whole transducer stack (PZT, matching layer, ASIC, glue, ground foil). Since the element thickness of 80 µm is close to the wavelength (100 µm), various mode vibrations occur in the different layers, resulting in fluctuations of the impedance as function of the frequency. To obtain a lumped-element model suitable for circuit simulation, we approximate the electrical impedance around resonance by a Butterworth-Van Dyke lumped-element model (also shown in Figure 4.2), which captures the main resonance mode and the element's electrical capacitance. The parameters of this model are obtained by means of least-squares curve fitting on the simulated impedance data. The transducer's impedance at resonance is approximately 0.7 pF // 5 kΩ. The elements have a measured transmit efficiency of 0.4 kPa/V at 6 mm from the transducer. Their measured receive sensitivity is around 4 µV/Pa. To generate sufficient acoustic pressure to be able to detect the low backscattered signal from blood [21] at an imaging depth suitable for FL-IVUS, transmit voltages on the order of 30 V are required. Table 4-1 summarizes the key parameters of the applied transducer.

While a matrix of transducer elements covering the full ASIC would be best for imaging, we leave out elements to make space for five bond pads, which provide electrical connections (one of which is a ground) to four micro-coaxial cables. In the prototype presented in this paper, the ASIC is connected using wire bonds on the same side as the transducer elements, but these can be replaced in the future by through-silicon vias to realize more convenient connections on the back side of the ASIC. Elements are also omitted in the center of the ASIC to make room for the catheter's guide wire.

The 80 elements are divided into 16 transmit (TX) elements and 64 receive (RX) elements. The transmit elements are located around the guide wire hole, while the receive elements cover a larger aperture and determine the lateral imaging resolution. This partitioning allows the receive circuitry to be implemented using compact low-voltage circuitry, while the number of high-voltage circuits associated with the transmit elements, which occupy a relatively large die size, is kept limited.

4.2.2 ASIC Architecture

Figure 4.3 shows the top-level architecture of the proposed ASIC. The ASIC consists of three main parts: 1) high-voltage (HV) switches, 2) a receive signal chain, and 3) a clock and data recovery circuit.

The HV switches are responsible for exciting the 16 TX elements using HV pulses in order to generate enough acoustic pressure. Several implementations of on-chip HV pulsers have been reported that can serve this purpose [22, 23]. Pulsers employing a resistive pull-up to a HV supply [13] are simple and area-efficient but are relatively power hungry due to the current flowing through the pull-up resistor. A push-pull architecture [22] is more power-efficient but requires more HV transistors to implement a level shifter to control the pull-up transistor and thus occupies more die area. An alternative to using on-chip pulsers is to use on-chip switches to route an externally-generated HV signal (HV TX PULSE in Figure 4.3) to selected transducer elements [24]. This approach reduces the on-chip power dissipation and allows the use of arbitrary transmit waveforms. We present an area-efficient HV switch implementation, by means of which one or more of the TX elements can be connected via a TX cable to the imaging system. This allows for the implementation of a synthetic-aperture transmit scheme, in which each of the 16 TX elements are successively pulsed, or, alternatively, a plane-wave transmit scheme, in which multiple TX elements are pulsed simultaneously.

The receive signal chain is responsible for transferring the received echo signals to the imaging system. In contrast with prior analog approaches [13, 14], we digitize the echo signals locally. In order to do so, we connect one of the 64 RX elements via an analog multiplexer and an analog front-end circuit to an ADC. This allows for the implementation of a synthetic-aperture receive scheme, in which the echo signals received by the 64 RX elements are digitized in 64 successive pulse-echo sequences. Combined with the synthetic-aperture transmit scheme, a complete synthetic-aperture image can be obtained in 1024 (16 × 64) sequences. The estimated volume frame rate is on the order of 100 fps for an imaging depth of 8 mm. While this is sufficient for our application, higher frame rates could be achieved by using multiple analog front-ends and ADCs and less multiplexing. This, however, comes with the challenges of increased die size and output data rates.

The analog front-end circuit amplifies the echo signal with a programmable gain to match it to the input range of the ADC. To detect the low backscattered signal from blood, an ultrasound system requires a dynamic range (DR) of at least 70 dB [21]. The DR of the receive signal chain can be lower than this, because the beamforming operation that combines the 16 × 64 receive signals to form the image enhances the DR. In the case of full synthetic phased array imaging, the DR will increase by $\sqrt{(16 \cdot 64)}$, or 30 dB, while other imaging schemes can provide even more [25]. To reach an overall DR of 80 dB, we aim for a DR of 50 dB per channel. Considering this DR requirement and the 13 MHz transducer center

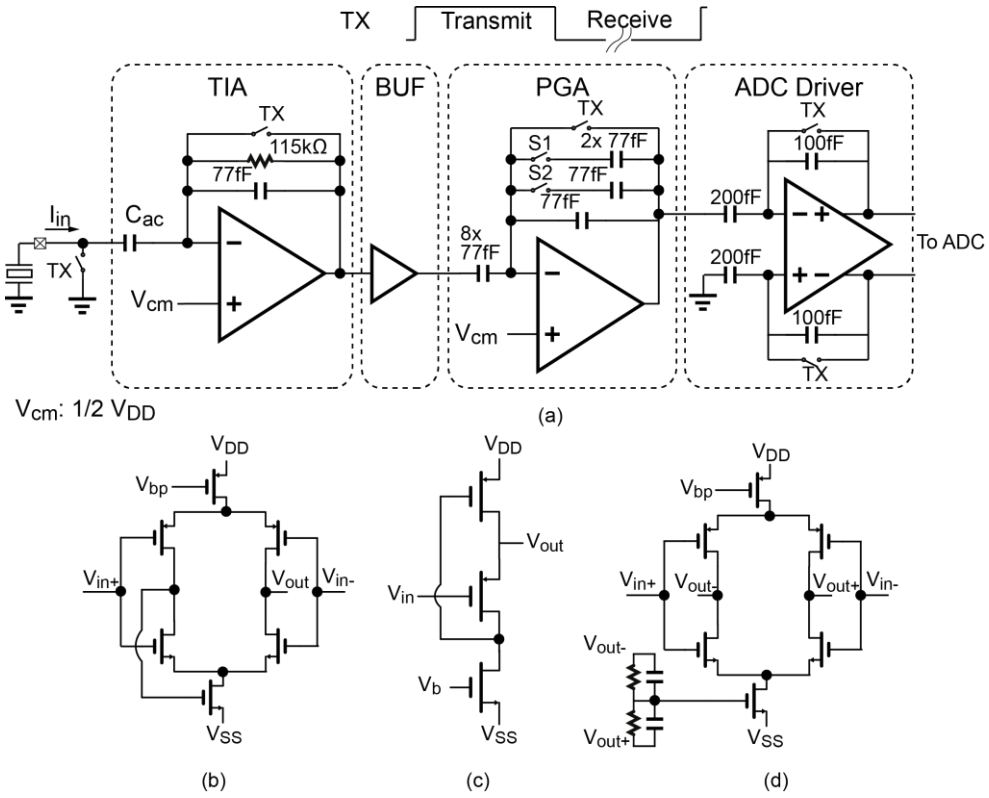

Figure 4.4 Circuit diagrams of (a) the analog front-end; (b) the OTA used in both the TIA and the PGA; (c) the buffer stage; and (d) the OTA of the ADC driver.

frequency, a 60-MS/s 10-bit SAR ADC is adopted. The ADC's output data is transmitted serially to the imaging system using a load-modulation-based data link (RX DATA).

The clock and data recovery circuit is responsible for extracting the ADC sampling clock and the pulse-width encoded configuration data, including the switch and gain settings, from a COMMAND signal generated by the imaging system during the RX phase. This same signal is also used to distinguish between the TX and the RX phases. During TX, the line is pulled to 5 V by the system, providing a supply voltage for the HV transmit circuit, as will be discussed in Section 4.3.4. In addition to the three mentioned cables (HV TX PULSE, RX DATA and COMMAND), a fourth cable provides the ASIC with a supply voltage (VDD) of 1.9 V.

The ASIC enables rapid reconfiguration of the selection of elements used for RX and TX, aiming for application in high-frame-rate volumetric imaging of the carotid artery. Control logic, programmed through row-level and element-level logic, determines whether an element participates in a given transmit and/or receive cycle. Element-level memory, which

can be pre-loaded through a shift register, allows the selection of active elements to be rapidly changed between successive transmit/receive cycles.

4.3 Circuit Implementation

4.3.1 Analog Front-End

Figure 4.4a shows the circuit diagram of the analog front-end (AFE), which converts the signal current of the selected RX element to a differential input voltage for the ADC. It consists of a trans-impedance amplifier (TIA), a buffer stage (BUF), a programmable-gain amplifier (PGA) and an ADC driver. Note that the multiplexer at the input has been omitted in this figure for simplicity.

The TIA is used to amplify the signal current I_{in} produced by the small PZT elements. Considering, as shown in Figure 4.2, the relatively high source resistance (~5 kΩ) and the small capacitance (~0.7 pF), a trans-impedance amplifier (TIA) is a power-efficient circuit topology. We opt for a single-ended TIA in view of the inherently single-ended nature of the transducer elements, due to the common ground electrode shared by all elements. A fully-differential implementation would require more area, while the benefit of lower harmonic distortion is not critical in our application, since harmonics are out-of-band and will be filtered out. The TIA senses the signal current I_{in} and converts it into an output voltage. A feedback resistor of 115 kΩ sets the trans-impedance gain, while a feedback capacitor of 77 fF ensures stability and sets the -3 dB bandwidth to 18 MHz.

To make the DC biasing of the TIA's virtual ground independent of that of the transducer, a coupling capacitor C_{ac} of 5.6 pF is used. This allows the transducer to be shorted to ground during the TX phase and connected to the TIA during the RX phase, without voltage transients that lead to parasitic acoustic transmissions. During the TX phase, the TIA's feedback network is shorted, thus keeping the amplifier in unity-gain feedback and preventing parasitic on-chip coupling of the HV transmit pulse from affecting the receive path.

A current-reuse operational transconductance amplifier (OTA) is employed to increase the power-efficiency of the TIA, as shown in Figure 4.4b [26]. The applied differential architecture allows the use of a tail-current source that isolates the signal-path from interfering signals superimposed on the supply voltage. The OTA is biased at 220 µA to ensure that the TIA's bandwidth covers the transducer's bandwidth and that the input-referred noise of the receive signal chain is dominated by the transducer (whose in-band rms noise is around 4.4 nA) rather than the TIA. The OTA's non-inverting input is biased at a mid-supply reference voltage V_{cm}, using a resistive divider (not shown).

The PGA is implemented as an inverting amplifier with a switchable capacitive feedback network, which provides a gain of 6 dB, 12 dB or 18 dB. This programmability allows the amplitude of the received signal to be adjusted to the input range of the ADC. The PGA has a constant input capacitance of 616 fF. The programmable gain is realized by switching the feedback capacitors, from 308 fF at the lowest gain setting to 77 fF at the highest gain setting. The architecture of the OTA is similar to that used in the TIA. It is biased at 220 µA for gain accuracy and linearity. In order to prevent the PGA's input capacitance (616 fF) from loading the TIA, a flipped voltage follower (BUF) biased at 110 µA [27], shown in Figure 4.4c, is employed as a buffer stage.

Finally, a fully-differential amplifier is implemented to convert the single-ended voltage to a differential voltage and drive the ADC's input sampling capacitors of 2 pF. To relax the bandwidth requirements on this amplifier, as will be discussed below, the ADC employs two pairs of time-interleaved sampling capacitors, so that one sampling clock period, i.e. roughly 16.6 ns, is available for settling, rather than only a fraction of the sampling period. This still requires a bandwidth of 66 MHz, which is realized in a power-efficient way by adopting a modest gain of 2 and using a fully-differential current-reuse OTA, shown in Figure 4.4d, biased at 400 µA. This OTA provides a differential output voltage to the ADC with a peak-to-peak range of 1.2 V.

Like the TIA, the PGA and the ADC driver are both switched in unity-gain feedback during the TX phase. This blocks interference from the TX signal and provides a well-defined DC biasing for the capacitive feedback networks. The complete receive path consumes approximately 950 µA and provides an overall trans-impedance gain of 112 dBΩ, 118 dBΩ or 124 dBΩ for the three PGA gain settings.

4.3.2 ADC

Local digitization of the receive echo signals helps to provide a robust digital output. Pipelined ADCs and delta-sigma ADCs have been reported for ultrasound applications with suitable power consumption levels [28, 29, 30]. However, these designs require a die area that exceeds what is available in our application [28, 29], or are implemented in advanced technology nodes that do not offer the high-voltage devices required in our design for the transmit switches [29]. Considering the stringent requirement of power and area, and the

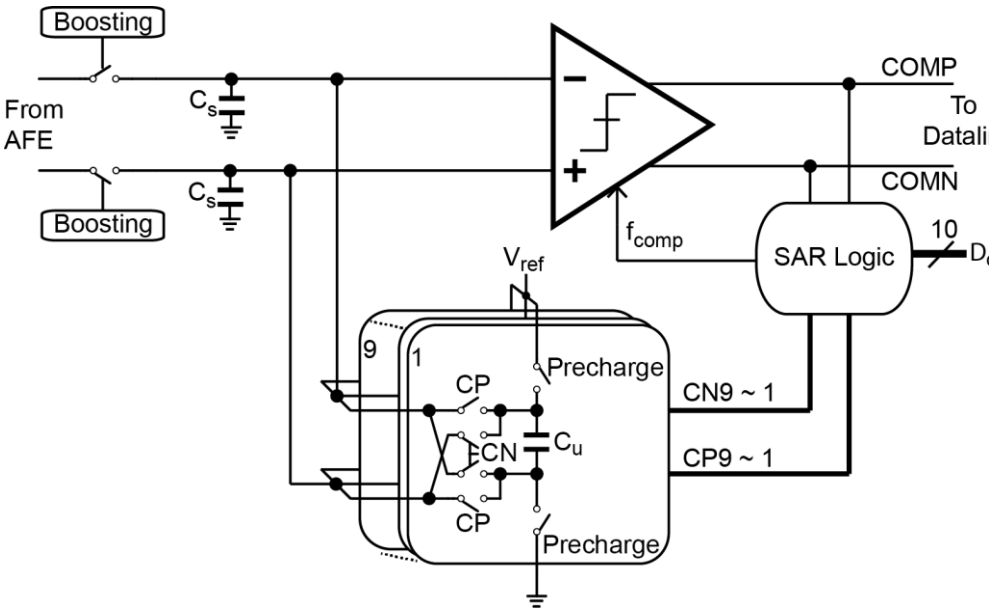

Figure 4.5 Simplified circuit diagram of the ADC.

relatively modest DR requirement, a SAR ADC is a good choice for our application in 0.18 µm HV CMOS technology. A 60 MS/s 10-bit SAR ADC is employed which can be implemented in a power-efficient manner and is well matched to the 50 dB DR. Moreover, it allows asynchronous operation, which eliminates the need of an external oversampled clock and thus reduces the system complexity.

In a conventional charge-redistribution SAR ADC, the voltage on the capacitive DAC (CDAC) needs to settle to the required accuracy (errors within +/- 0.5 LSB) before the comparator makes a decision. Less than 1.7 ns would be available for the CDAC to settle to the reference voltage and the comparator and SAR logic to finish the decision. Allocating more time for the CDAC settling would reduce the power consumption of the reference buffer but more power-hungry and faster digital logic (comparator and SAR logic) would be required. A 10-bit charge-sharing SAR ADC, in contrast, can be implemented using only 67 unit capacitors, and relaxes the settling requirements of the reference buffer [31]. Therefore, we employ a charge-sharing SAR ADC in this work.

Figure 4.5 shows a simplified circuit diagram of this SAR ADC. The differential analog input signal is first sampled on the sampling capacitors C_S. In the meanwhile, the CDAC is pre-charged by an on-chip reference buffer to generate 9 binary-scaled reference charges which will be used to quantize the signal charge. To determine the most significant output bit, the comparator evaluates the polarity of the voltage on C_S. Based on this, the largest CDAC capacitor is connected either in parallel (CP) or anti-parallel (CN) to C_S, causing the associated reference charge to be added to or subtracted from the charge on C_S. The

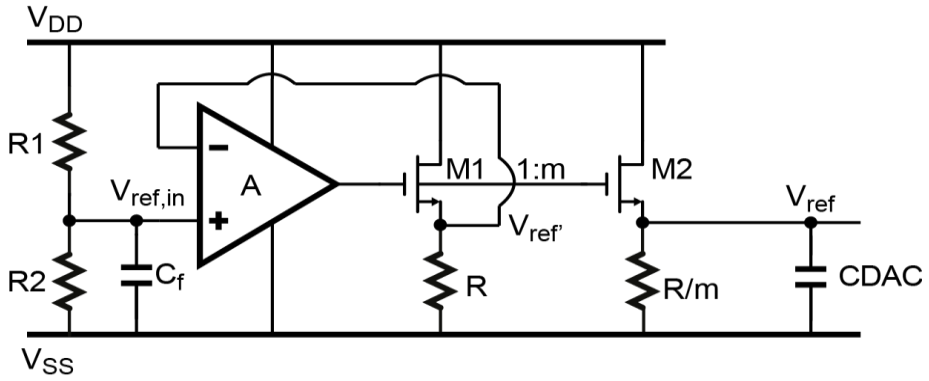

Figure 4.6 Circuit diagram of the reference buffer.

comparator then again evaluates the polarity of the voltage on C_S to determine the next bit. This successive approximation process continues until all 10 bits have been determined, and is controlled by the SAR logic, whose differential outputs CP1-CP9 and CN1-CN9 are used to control the switching of the CDAC. By using sampling capacitors C_S of the same size as the total CDAC capacitance and a reference voltage of 0.3 V, the desired differential input voltage range of 1.2 V is obtained [31].

The implemented CDAC consists of 67 unit capacitors (not shown in detail in Figure 4.5), 63 of which are pre-charged to the reference voltage to create the 6 most-significant binary-scaled reference charges (32:16:8:4:2:1). Of the remaining 4 unit capacitors, one is pre-

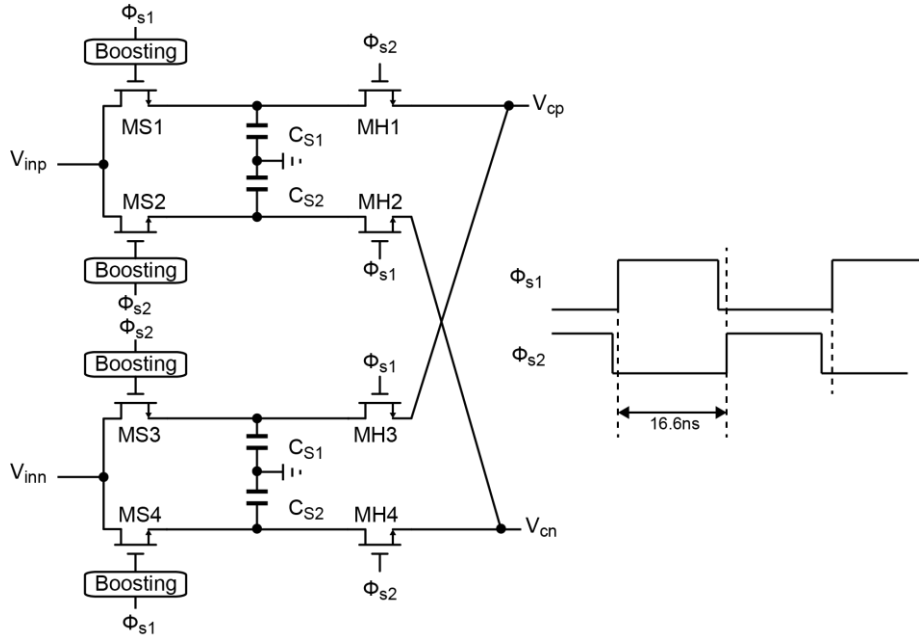

Figure 4.7 Circuit diagram of two-path time interleaved sampling.

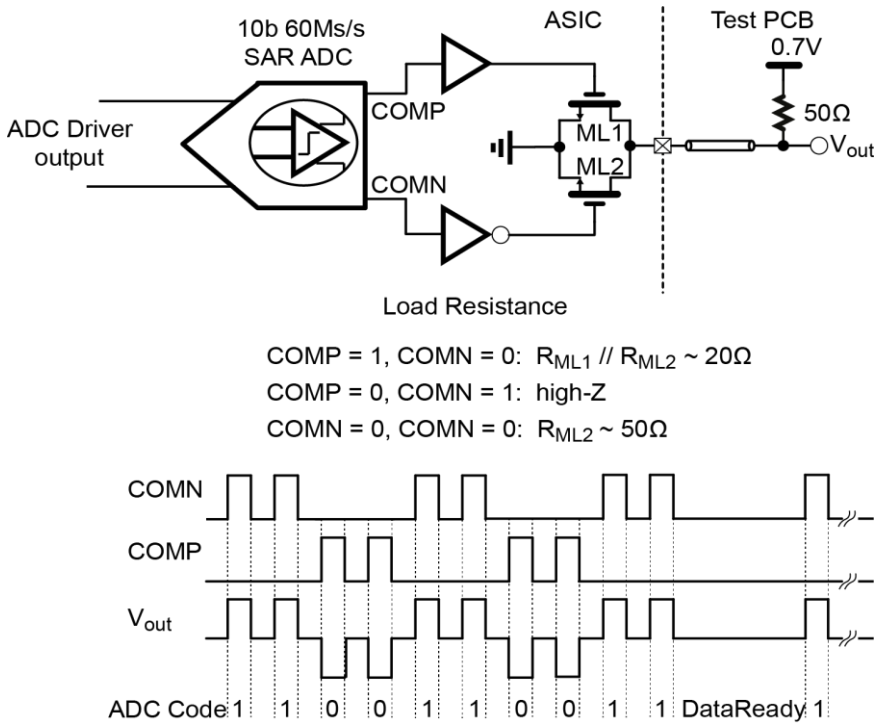

Figure 4.8 Circuit diagram and waveforms for the load modulation datalink.

charged to the reference voltage, after which successive charge redistribution with the other 3 is used to create the 3 least-significant reference charges (0.5:0.25:0.125) [31]. A unit capacitor C_U of 32 fF is used to meet the 10-bit matching requirement, taking into account both matching between the unit capacitors and the effect of parasitic capacitance of the switches controlled by CP and CN shown in Figure 4.5. This leads to total CDAC capacitance of 2 pF. As said, the sampling capacitors Cs are of the same size. The associated kT/C noise is well below the LSB step of the ADC.

A self-timed architecture is implemented for the SAR logic to avoid the need of an oversampled clock. Via the COMMAND line, an external 60 MHz clock is used to trigger the start of the conversion. The comparator clock is generated by asynchronous SAR logic. In order to increase the linearity of the input sampling switches, the drive signal of these NMOS switches is boosted to achieve an over-drive voltage of ~1.3 V [32]. The power consumption of the ADC is fully dynamic and amounts to 2.8 mW.

Figure 4.6 shows the schematic of the reference buffer. A reference voltage $V_{ref,in}$ of 0.3 V is derived from the supply voltage VDD by means of a resistive divider comprised of R1 and R2. While this means that any variation in VDD results in a variation of $V_{ref,in}$ with an attenuation of only 6× (16 dB), this is not problematic, since the chip's supply voltage is directly provided from the system side via one of the four cables (see Figure 4.3). There, a voltage regulator is used to stabilize the DC value of the supply voltage. To prevent high-

frequency signals on the supply from coupling into the reference voltage, an on-chip bypass capacitor C_f is included. An OTA and a source follower form an op-amp which is configured as a unity-gain stage and forces $V_{ref'}$ equal to $V_{ref,in}$. A scaled replica stage comprised of M2 and R/m, charges the CDAC in an open-loop manner to a reference voltage V_{ref} that tracks $V_{ref'}$ and hence $V_{ref,in}$. The scale factor m = 10 is chosen to ensure sufficient CDAC settling. Only 39 µA is consumed in the OTA and 60 µA in the source follower comprised of M1 and R. 600 µA is consumed in the replica stage to ensure low enough output impedance for sufficient CDAC settling.

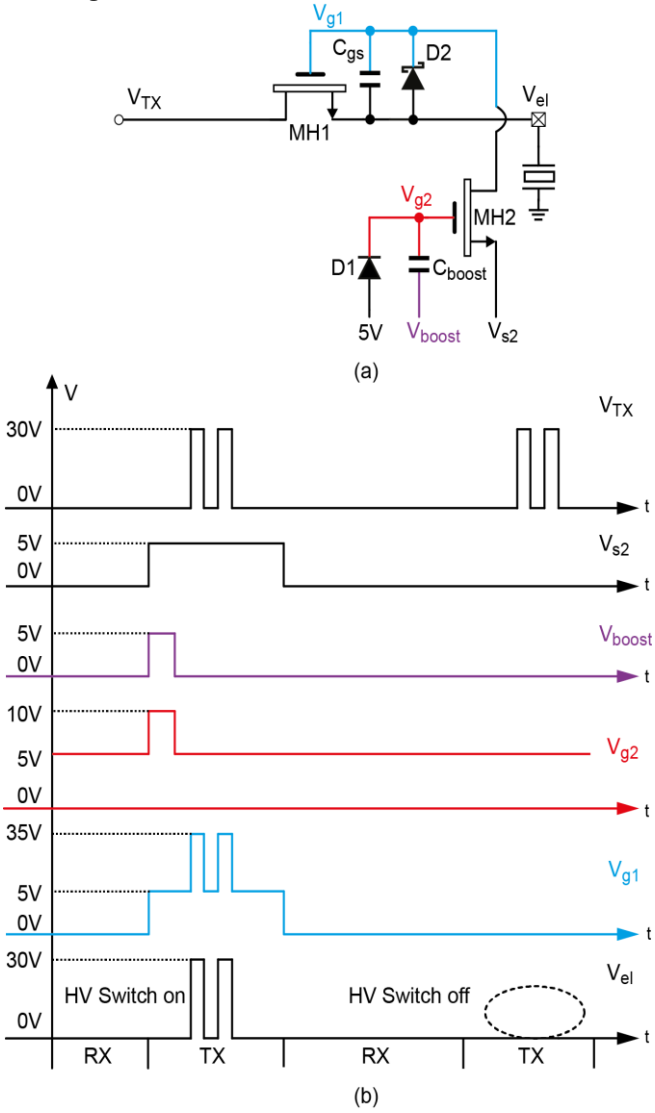

Figure 4.9 (a) Conceptual diagram of the high-voltage switch circuit; (b)The associated timing diagram.

In order to reduce the power consumption of the ADC driver, a two-path time-interleaved sampling scheme is employed to reduce the bandwidth requirement of the ADC driver. The associated schematic and timing diagram are shown in Figure 4.7. In every clock cycle, one pair of sampling capacitors connects to ADC driver, making a full 16.6 ns available for settling, while the charge stored on the other pair is digitized.

4.3.3 Load-Modulation Datalink

To transmit the ADC's 10b output code through a single cable, a conventional implementation is to serialize the 10-b code using an oversampled clock generated on-chip with a power-hungry phase-lock-loop (PLL) or delay-lock-loop (DLL). Instead, to simplify the circuitry and reduce the on-chip power dissipation, the ADC output code is transmitted asynchronously by means of load modulation. Figure 4.8 shows the principle. The comparator's asynchronous differential outputs COMP and COMN represent the output code. Two differently-sized NMOS load-modulation switches are driven by the comparator outputs, resulting in three different loads resistances. Together with a 50Ω pull-up resistor on the system side, this forms a resistive divider on which a three-level waveform can be observed from which the ADC bits can be recovered. The supply voltage to which the pull-up resistor is connected is a trade-off between signal swing and power consumption. A voltage of 0.7 V was chosen experimentally (see Section 4.4.1), which leads to an on-chip power consumption associated with the data transmission of about 2.7 mW, comparable to the power consumption of the remaining building blocks.

4.3.4 High-Voltage Bootstrapped Switch

The HV switches serve to pass a transmit pulse generated by the imaging system to selected transducer elements during the TX phase. Earlier implementations of HV switches employ either level-shift circuits [22, 23] or bootstrapped capacitors [24] to provide overdrive to turn

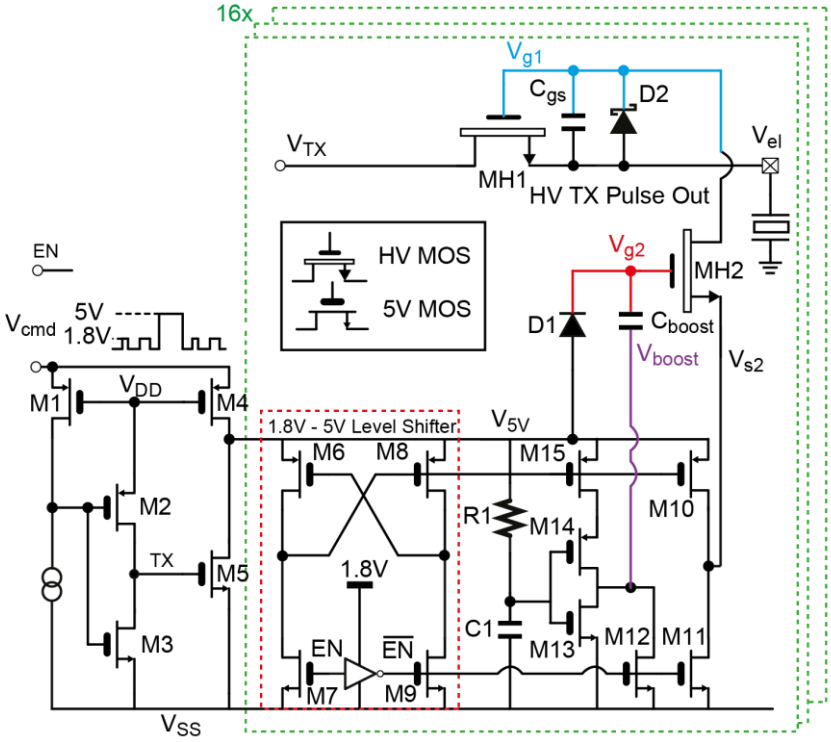

Figure 4.10 Circuit diagram of the high-voltage switch and the control signal generator.

on a high-voltage MOS transistor. A level-shift circuit translates a low-voltage switch-control signal to the voltage level at which the switch operates, and tends to require a HV supply, which is not available in our system. A bootstrapped switch is a better match. It employs a capacitor at the gate of a HV MOS transistor which is charged up to turn on the switch when the voltage level is low. The capacitor then maintains the overdrive when the voltage level increases, thus keeping the switch on. In [24], a switch is described that employs back-to-back connected transistors to provide bi-directional isolation. However, to turn on and off these transistors, two additional HV MOS transistors and several HV diodes are needed per switch, which requires significant die size.

In this work, we limit ourselves to unipolar pulses, so that back-to-back isolation is not required, allowing an implementation using only one HV switch transistor MH1 to connect the transmit element (V_{el}) to the off-chip HV pulser (V_{TX}), as shown in Figure 4.9a. To turn on MH1, a bootstrap capacitor C_{gs} is charged to 5 V through transistor MH2. This happens when VTX is still low, at the start of the TX phase. To turn on MH2, its gate voltage V_{g2} is pumped to approximately 10 V, while its source voltage V_{S2} is pushed to 5 V, as shown in Figure 4.9b. The 10 V at the gate is generated by charging a capacitor C_{boost} to 5 V and then pushing the voltage V_{boost} at its bottom plate to 5 V. Because MH2 is now turned on, C_{gs} will be charged to V_{S2} (5 V). Once C_{gs} has been charged, MH2 is switched off by dropping V_{boost},

thus isolating the charge on C_{gs} and keeping MH1 switched on. HV transmit pulses on the TX line can then be passed to the transducer element. The bootstrap capacitor C_{gs} of 1.7 pF is sized such that MH1 maintains enough overdrive even if some charge is lost when the TX line goes high due to parasitic capacitance at node V_{g1}. A Zener diode D2 protects the gate of MH1. After the TX phase, MH1 is turned off by dropping V_{S2}, which causes C_{gs} to be discharged through MH2. A diode D1 then precharges C_{boost} for the next TX cycle. To prevent the switch from turning on during the TX phase, V_{boost} and V_{S2} are simply kept low, as illustrated in the second TX phase in Figure 4.9b.

In order to generate the 5 V control signals V_{boost} and V_{S2} needed for the HV switch, a control signal generator is required, shown in Figure 4.10. The required 5 V level is derived from the COMMAND line. When the voltage V_{cmd} on that line is pulled to 5 V by the system to identify the start of the TX phase, M4 pulls the V_{5V} line up to 5 V. If V_{cmd} is between VSS and VDD, i.e. during the RX phase, this is detected by the circuit consisting of M1-3, which turns on M5 to pull V_{5V} to ground, completely turning off the HV switch circuit. As said, the HV switch MH1 is turned on by pulling V_{boost} and V_{S2} to 5 V during the TX phase. Whether

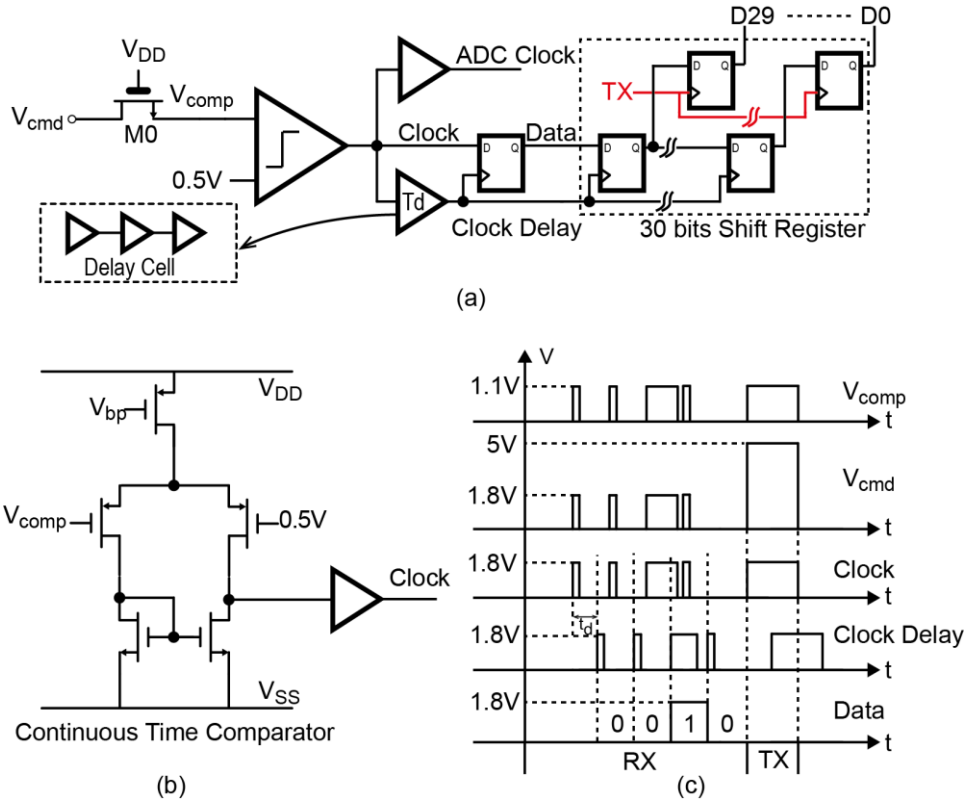

Figure 4.11 Circuit diagrams of (a) clock and data recovery circuit; (b) the continuous-time comparator; (c) associated timing diagram.

this happens is determined by a 1.8 V logic enable signal EN, provided by the chip's

configuration shift register. With the help of a 1.8 V-5 V level shifter consisting of M6-9, this enable signal drives transistor M10 to pulling up V_{S2}. The shorter pulse on V_{boost} is generated by M12-15, R1 and C1, where the time required to charge C1 through R1 determines the duration of this pulse, which is set to approximately 20 ns. When EN is low, V_{S2} and V_{boost} are pulled down by M11 and M12, respectively, preventing the switch from turning on. Although the V_{5V} is pulled down to 0 V during the RX phase, the diode D1 prevents C_{boost} from being discharged.

4.3.5 Clock and Data Recovery Circuit

Besides providing a 5 V level during the TX phase, the COMMAND line also provides a clock for the ADC, and, in the form of PWM-encoded data, configuration bits that are loaded into a shift register to control the RX multiplexer, the gain of the AFE, and the EN signals of

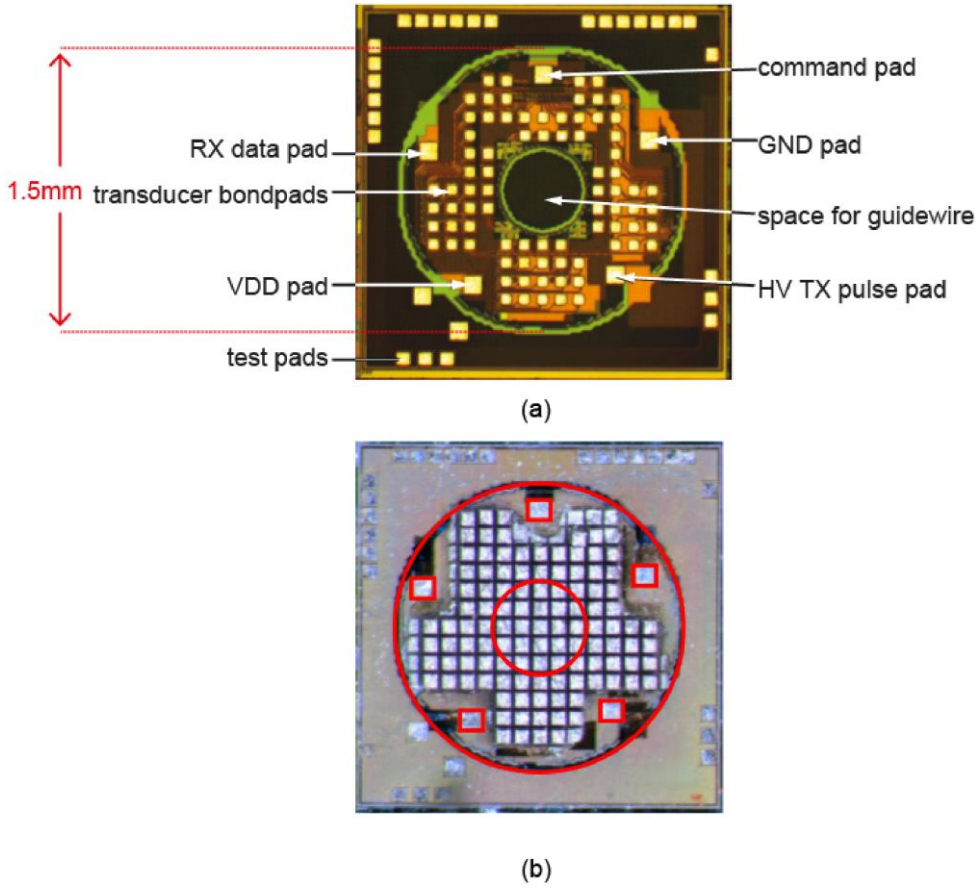

Figure 4.12 (a) Chip micrograph (b) Micrograph of prototype ASIC with transducer array on top.

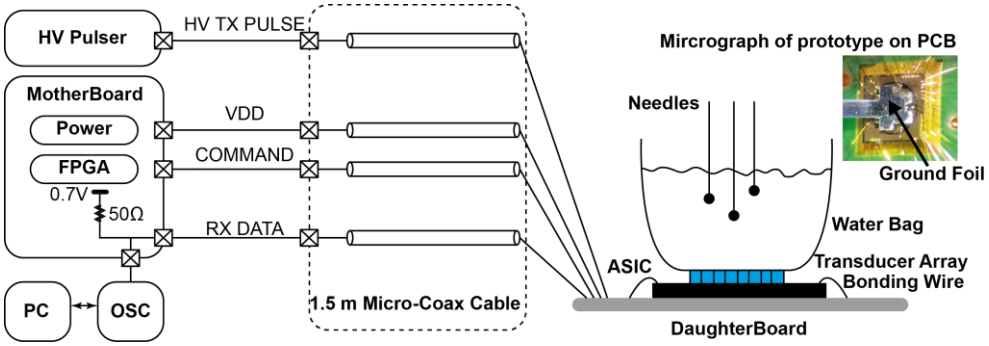

Figure 4.13 Schematic diagram of the acoustical experimental setup.

the TX switches. In order to recover the clock and data from the COMMAND line, the 5 V pulses are first clamped to protect the following low-voltage circuitry, and then, the extracted PWM signal is demodulated into a clock and data, as shown in Figure 4.11a. A 5 V NMOS transistor M0 limits the V_{cmd} signal to VDD - V_{th}, where V_{th} is the transistor's threshold voltage, after which a simple continuous-time comparator, shown in Figure 4.11b, turns the signal into proper logic levels. The comparator is biased at 190 µA to make sure that the latency of the comparator will not affect the duty cycle of recovered PWM signal. The rising edges of the resulting signal are used to trigger the ADC.

To decode the data bits, the signal level is sampled at half a clock cycle after the rising edge, as shown in Figure 4.11c. To do so, a delayed version of the signal is used to clock a flip-flop. This delayed version is also used as the clock for the chip's 30-bit shift register. In order to prevent the current state of the chip from being affected by the loading of new data into the shift register, the shift register output is buffered by a second set of flip-flops, which are clocked by the TX signal (obtained from the HV switch circuit, see Figure 4.10). Thus, new configuration data only becomes active at the start of the succeeding TX phase.

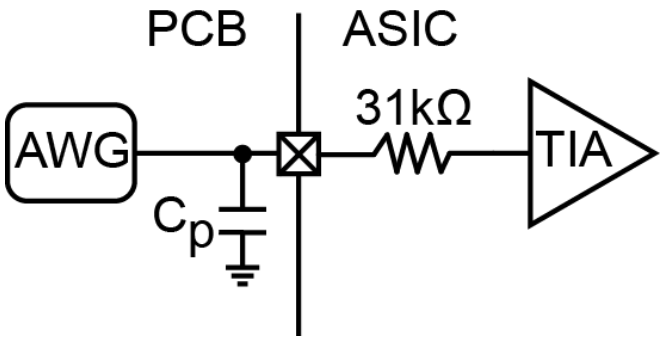

Figure 4.14 Method of applying a test current to the TIA input.

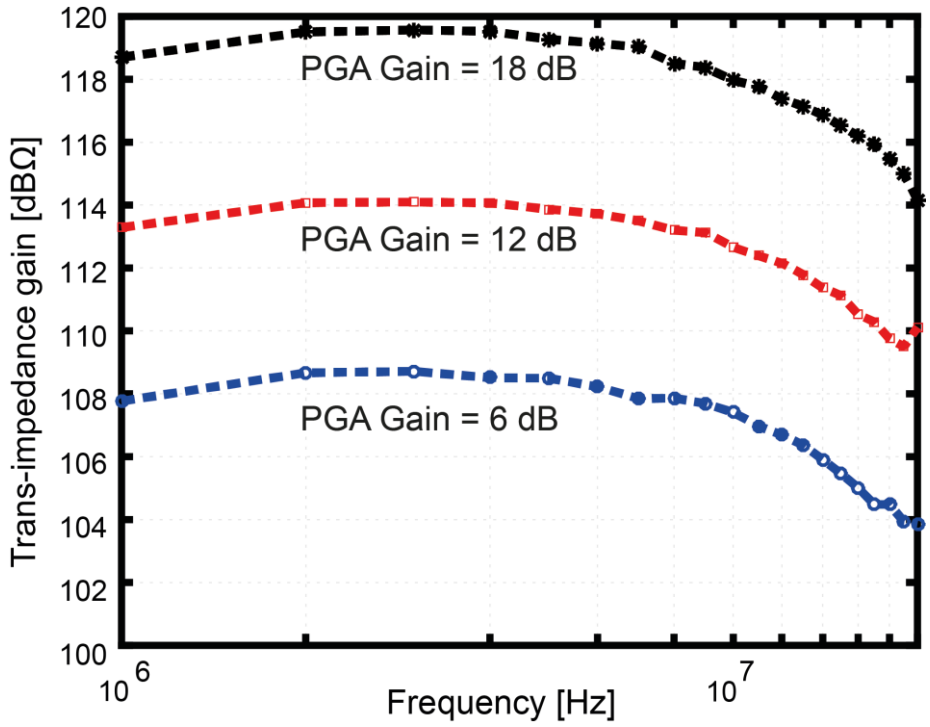

Figure 4.15 Measured transfer function of the ASIC receive signal chain for different PGA gain settings.

4.4 Experimental Results

4.4.1 Experimental Setup

The ASIC has been realized in a 0.18 µm high-voltage BCDMOS process with a total area of 2 × 2 mm^2, as shown in Figure 4.12a. The circular layout has a 1.5 mm outer diameter and a central hole with a 0.5 mm diameter, so that it can be laser-cut into a donut shape to fit at the tip of a catheter. Five bond pads provide electrical connections for the four micro-coaxial cables; 80 bond pads are positioned to connect to transducer elements. The die area around the donut is used for test circuits, which are not connected in the acoustical measurements reported below. These test circuits contain digital buffers that provide a parallel 10-bit ADC output (D_{out} in Figure 4.5), as well as a test bondpad through which an electrical test signal can be applied to the analog front-end.

Figure 4.12b shows a fabricated prototype with the transducer array built on top of the ASIC using the approach described in [19]. The bond pads on the ASIC that provide electrical connections to the transducer elements are equipped with gold bumps using a wire-bonding tool. After this, an epoxy layer is applied to ASIC that is grinded down to expose the gold,

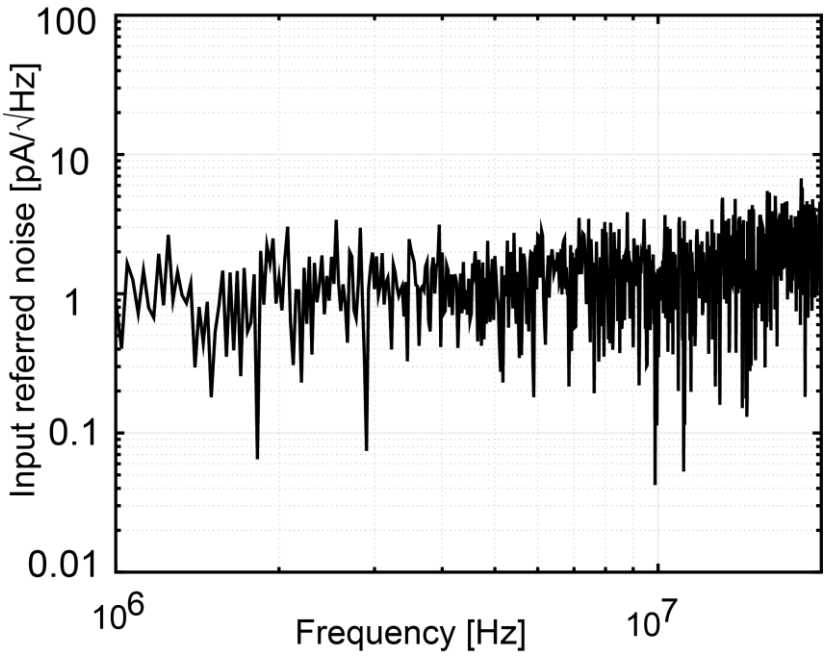

Figure 4.16 Measured input-referred noise of the receive signal chain.

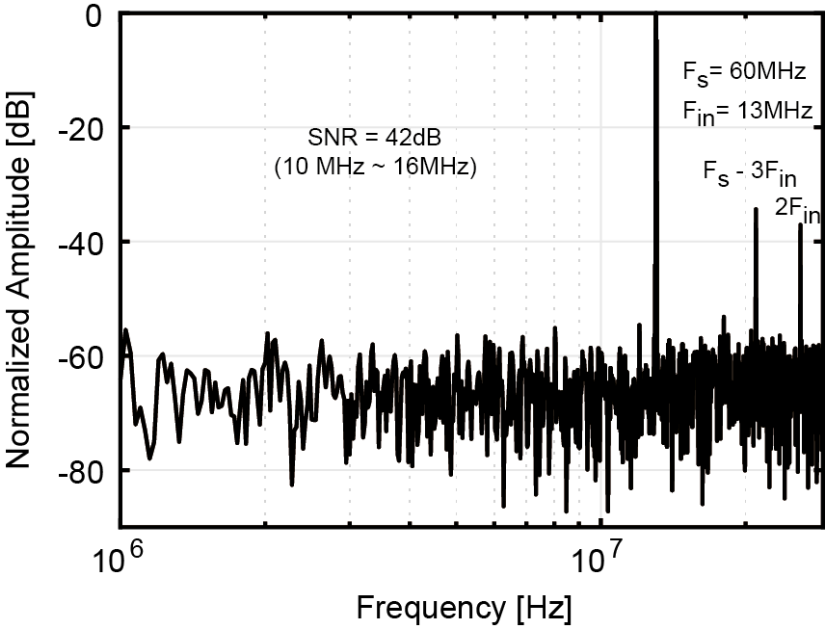

Figure 4.17 Measured output spectrum of the receive signal chain for a 13 MHz sinusoidal input signal.

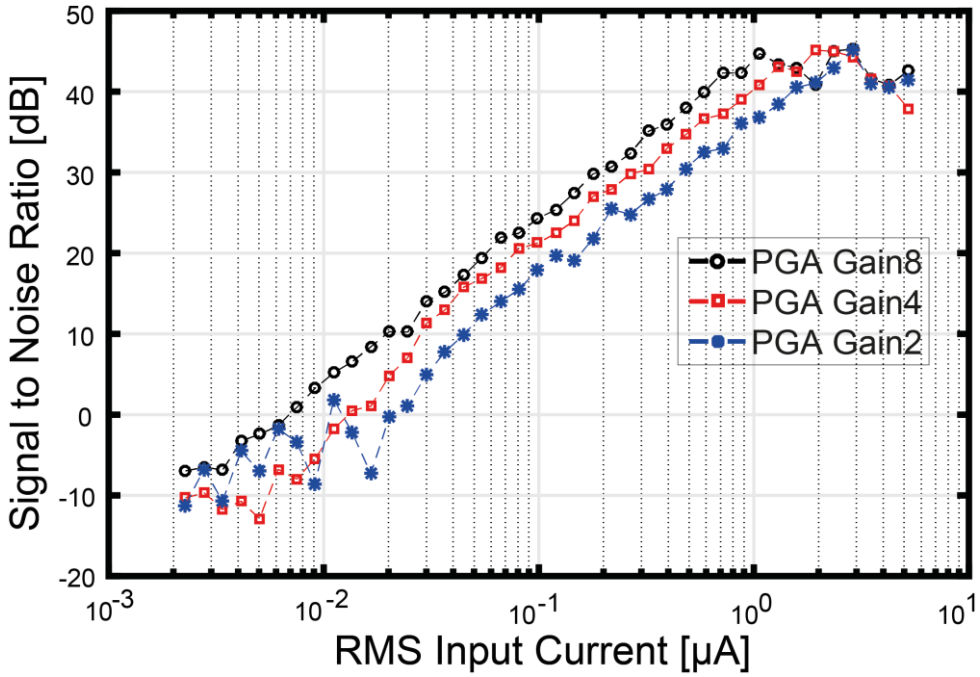

Figure 4.18 Measured dynamic range of the ASIC receive signal chain for different PGA gain settings.

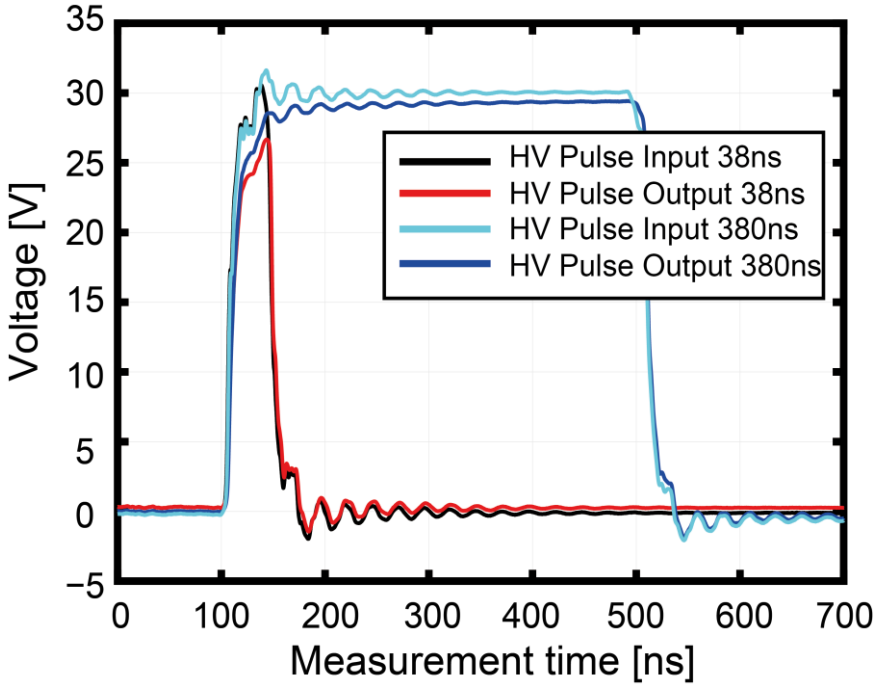

Figure 4.19 Measured high voltage pulse input, and output at one TX transducer pad in different pulse width.

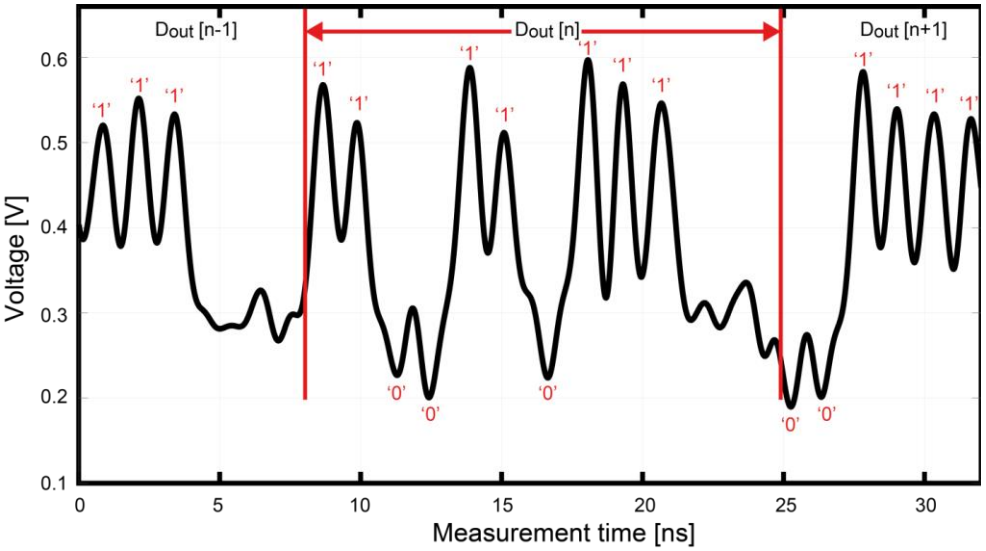

Figure 4.20 Measured load modulation signal.

thus providing reliable electrical contacts for the transducer elements. The acoustic stack consisting of a backing layer, a piezo-electric material (PZT) and a matching layer (with a total thickness of approximately 160 µm) is glued on top of the grinded epoxy layer, which is cut into the desired 100-µm-pitch array pattern using a diamond saw. Finally, the array is covered with an aluminium foil that forms the common ground electrode of the elements.

Figure 4.13 shows a block diagram of the experimental setup. The ASIC is wire-bonded to a daughter board PCB. The ground foil is connected to the ground of the ASIC and the PCB. The ASIC's 4 cable connections are connected to four headers on the daughter board which are then connected through 1.5-m long micro-coaxial cables (AWG 42) to a mother board. The serial output of the ADC is captured by a high-speed oscilloscope with 1 GHz bandwidth (DL9710L, Yokogawa) and processed in MATLAB on a PC. The test signals are connected to the mother board through headers. The high-voltage pulse is provided by an external pulser (AVTech, AVR40, Avtech Electrosystems Ltd.). The mixed-voltage multi-functional command line is generated by an FPGA and an analog switch (ADG719, Analog Device) which is used to pull the line to 5 V. The switch control signal and 60 MHz PWM signal are generated by the FPGA.

4.4.2 Electrical Measurements

In order to characterize the receive signal chain, an external test voltage was applied to the ASIC's analog test input, which is connected on chip via a 31 kΩ resistor to the TIA input to produce a test current, as shown in Figure 4.14. This ensures that the parasitic capacitance (C_p) associated with the PCB trace and the on-chip bond pad do not affect the test current applied to the TIA. Figure 4.15 shows the measured transfer function of the receive signal

chain for the three gain settings. The measured trans-impedance gain ranges from 108 dBΩ to 119 dBΩ with a gain step of 5.7 dBΩ and is 4-5 dBΩ lower than the design target because of the limited open-loop gain of the OTAs in the AFE.

The measured input-referred noise spectrum is shown in Figure 4.16. The slight increase at higher frequencies is due to the roll-off of the transfer function (see Figure 4.15). The total input-referred in-band (10 MHz to 16 MHz) rms noise is 4.8 nA in which the thermal noise of the 31 kΩ resistor is also included. While comparable to the 4.4 nA noise level of the transducer, this noise level is larger than the design target. A possible cause of this is coupling of the transient supply currents drawn by the ADC and the logic to the input of the LNA via the ground connection of the chip, which in this design also serves as the connection to the transducer's ground foil. This coupling can be reduced in the future by connecting the ground foil to the ground bond pad on the chip, rather than via the PCB.

A sinusoidal input signal was applied to evaluate the signal-to-noise ratio (SNR) and the linearity of the receive signal chain. The measured spectrum shown in Figure 4.17 illustrates a 42 dB in-band (10MHz to 16MHz) SNR and ~37 dB HD2. The dynamic range measurement results are shown in Figure 4.18. The measured dynamic range, accounting for the programmable gain, is around 53 dB, sufficient for the IVUS application.

The high-voltage switch was designed to transmit 30 V pulses at a frequency of 13 MHz (pulse width of 38 ns) for a PZT device with a parasitic capacitance of 0.7 pF. Figure 4.19 shows the measured high-voltage pulse input and high-voltage pulse output of one selected channel in the high-voltage switch array. A 380 ns HV pulse is applied to show the highest voltage amplitude that the chip can provide, which is 29.3 V. A 38 ns pulse is also applied.

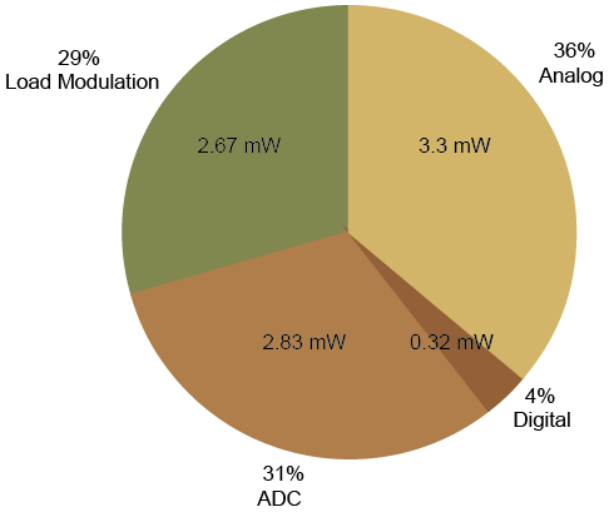

Figure 4.21 Power breakdown of the chip.

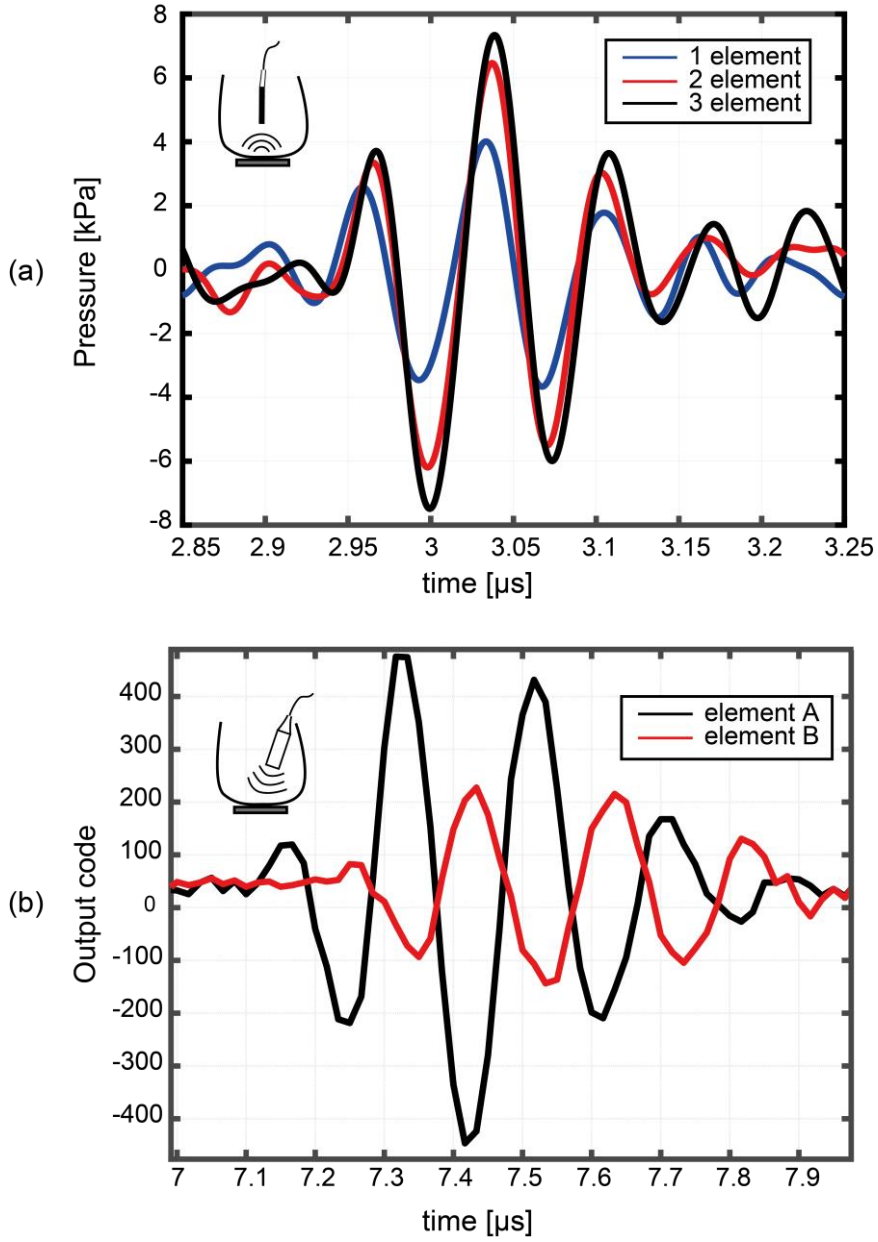

Figure 4.22 (a) Measured TX pressure versus number of excited elements. (b) Receive signal measured through two transducer elements.

The lower amplitude of the HV pulse output shown is caused by incomplete settling due to the large PCB parasitic. However, the transducer array used in the acoustical measurement is directly integrated on top of ASIC so that no additional parasitic are introduced and the HV pulse should be able to fully settle.

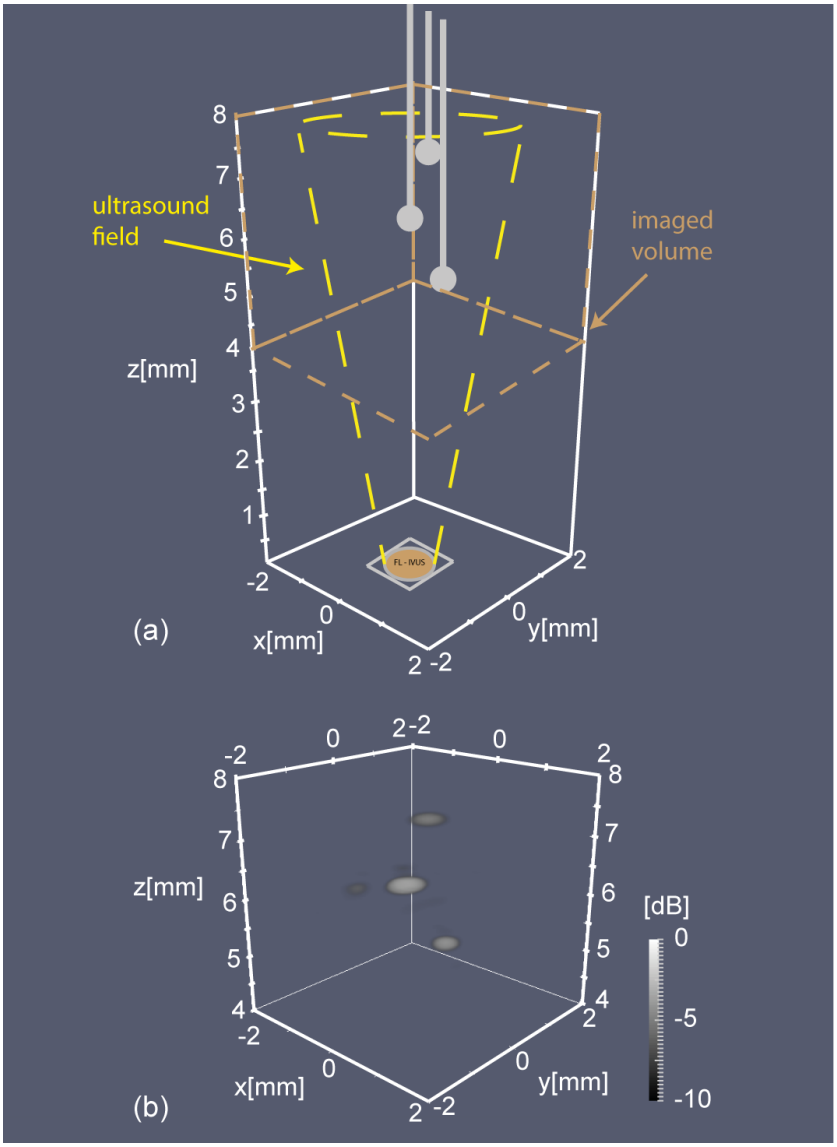

Figure 4.23 (a) 3-needle phantom setup. (b) 3-D image showing the position of the 3 needles.

Figure 4.20 shows the load-modulation output captured using the high-speed oscilloscope. Compared to the ideal waveform shown in Figure 4.8, the signal has clearly been low-pass filtered, partially due to the finite bandwidth of the oscilloscope. Nevertheless, the data bits can still be correctly extracted from the captured waveform. To do so, the captured waveform is first synchronized to the 60 MHz input clock and divided into chucks that corresponds to the 10 data bits of an individual sample. The data bits are then extracted by detecting the peaks in the waveform using MATLAB. By comparing the extracted data with the data

captured from the parallel test outputs, a bit error rate (BER) of approximately 0.2% is found, which hardly affects the SNR.

Figure 4.21 shows the power breakdown of the ASIC. The total power consumption is 9.1 mW, which is dominated by the power consumed by the ADC, the analog circuits (including the receive signal chain, the comparator in clock and data recovery circuits and the reference buffer) and the load modulation datalink.

4.4.3 Acoustic Measurements

To perform acoustic measurements, a water bag was mounted on top of the fabricated prototype, as shown in Figure 4.13. Selected channels of the high-voltage transmit chain were excited and the pressure was measured using a hydrophone (SN1302, Precision Acoustics) suspended in the water 5 mm above the transducer array. The measured TX pressure for increasing number of excited elements is shown in Figure 4.22a, showing, as expected, a peak pressure that increases roughly proportionally with the number of excited elements.

To test the receive functionality acoustically, a single element 5 MHz transmit transducer (PA865, Precision Acoustics) was placed under an angle in the water above the transducer array generating short acoustic pulses. Two receive elements were selected to receive the acoustic signal as shown in Figure 4.22b. The time delay between the recorded signals is consistent with the fact that the transmitter was placed at an angle, leading to different arrival time of the acoustic pulse on the two elements.

In order to show the 3D imaging capability of the prototype, a 3-needle phantom was placed in the water above the transducer array (Figure. 4.23a). The 16 transmit transducers were excited simultaneously by 30-V pulses of 30 ns to generate a TX beam. The echo signals from 64 receive transducers were then recorded sequentially. A 3D image showing a dynamic

TABLE 4-2. System-level comparison with prior work

	[13]	[14]	[6]*	This work
Transducer Type	CMUT	CMUT	PVDF	PZT
Process	0.35μm HV CMOS	0.35μm HV CMOS	3 μm CMOS	0.18μm HV BCD
Core chip size	1.4 mm Φ	2.1 mm Φ	4 x (0.86 mm × 1.65 mm)	1.5 mm Φ
Supply voltage	3.3 V	3.3 V	10 V	1.9 V(V_{DD}) + 5 V(V_{cmd})
#Transmit	56	64	64	16
#Receive	48	56	64	64
Center frequency	20 MHz	12 MHz	20 MHz	13 MHz
Reveive output	analog	analog	analog	digital
Receive bandwidth	40 MHz	n/a	27 MHz	16 MHz
Dynamic Range	50 dB	n/a	n/a	53 dB
Transmit circuit	pulser	pulser	pulser	switch
Max.transmit amplitude	25 V	12.5 V	10V	30 V
Power consumption	20 mW	n/a	30 mW	9.1 mW
#Cables	13	13	7	4

* [6] is a side-looking IVUS design with 4 separate chips connected to a 64-element array.

range of 10 dB (Figure. 4.23b) was reconstructed by means of delay-and-sum beamforming of the received echo signals. The three needle heads can be clearly recognized in the image. For the central needle, side-lobe artifacts are visible close to the main signal. These artifacts are present for all the needles but since the central needle reflects most of the signal, only there the artifact is visible in the 10 dB dynamic range image. Note that better image quality can be obtained by employing synthetic aperture also in TX, and by applying more sophisticated reconstruction techniques. This, however, is beyond the scope of this paper.

A comparison of our ASIC performance and characteristics with the prior art is provided in Table 4-2. The designs described in [13] and [14] employ ring-shaped CMUT transducer arrays with separate RX and TX elements. The on-chip circuitry includes per-element receive amplifiers, multiplexers and buffers that provide 4 parallel receive outputs, as well as pulsers with the associated control logic. The design described in [6] is for a side-looking IVUS probe, in which four ASICs are connected to a 64-element PVDF array. Each ASIC includes 16 receive amplifiers and transmit pulsers, with a single differential current-mode receive output shared by the four ASICs. A unique feature of our work is that it not only includes a receive front-end, but also an ADC and a load-modulation datalink. Rather than employing on-chip pulsers, we use on-chip high-voltage switches, which connect selected TX elements to a pulser on the system side, thus reducing the on-chip power dissipation. Our ASIC features the lowest cable count and the lowest power consumption, and is the first to provide a digitized output signal.

4.5 Conclusion

This chapter has presented a front-end ASIC for 3D intravascular ultrasound imaging which interfaces with 16 transmit elements and 64 receive elements using only four 1.5 m micro-coaxial cables. The chip has 1.5 mm diameter donut-shaped lay-out to facilitate placement around the guide-wire of a catheter. A multi-functional mixed-voltage command line is used to transmit clock, data and a power supply for the HV switches through only one cable. A load-modulation-based data transmission scheme is used to transfer the ADC's 10-b output asynchronously through one cable. A high-voltage switch array with a compact and power-efficient circuit-level implementation allows 16 transmit transducers to be excited through one cable. To overcome the challenges of limited area- and power-constraints, an inverter-based analog front-end and a charge-sharing SAR ADC have been implemented. The effectiveness of these techniques has been successfully demonstrated in a 3D ultrasound imaging experiment.

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CHAPTER 5

LOW-POWER RECONFIGURABLE TRANSCEIVER ASIC FOR WEARABLE ULTRASOUND PATCHES

This chapter is based on the publication: M. Tan et al., "A 16- to 64-Channel Low-Power Reconfigurable Transceiver ASIC for CMUT-based Wearable Ultrasound Patches", in preparation for submission.

5.1 Introduction

Smart body patches are becoming a valuable tool in medical diagnostics. These wearable devices allow for continuous monitoring of body parameters, giving patients valuable health insights without help from hospitals and care-takers, consequently enabling them to stay longer in their home environment and reduce the cost of healthcare [1]. For instance, in [2], a disposable health patch has been reported that can monitor heart rate using ECG, breathing rate using bio-impedance measurements, and blood oxygen saturation using photoplethysmography (PPG). Other body patches like wearable thermometers [3] and wearable humidity sensors [4] measure temperature and humidity at the skin. These patches are limited to detecting only surface body parameters.

To obtain information about phenomena deeper inside the human body, imaging modalities such as X-ray, magnetic resonance imaging (MRI), computed tomography (CT), and ultrasound imaging are typically used. Among these, the use of ultrasound is an attractive option for integration into wearable body patches, as it is harmless and miniaturizable in a

cost-effective manner [5]. Conventional ultrasound probes used in hospitals are connected to bulky and expensive cart-based imaging machines. Handheld probes that connect to mobile devices [6, 7] are increasingly being adopted, but are not able to provide continuous monitoring of body parameters because their cost, size and power consumption are not yet suitable for integration into wearable devices.

Several wearable ultrasound devices have been reported, for applications including bladder monitoring [8], blood flow measurement [9] and monitoring of bone-fracture healing [10]. These devices, however, employ conventional transducer technology and discrete electronics, making them relatively bulky and uncomfortable. To make the step to wearable ultrasound patches, several innovations are needed, including the development of low-cost flexible and stretchable ultrasound transducer technology [11-14], packaging solutions that provide a durable acoustic contact to the skin [15, 16], and the development of low-power electronics that can interface with the transducer and communicate wirelessly with mobile devices.

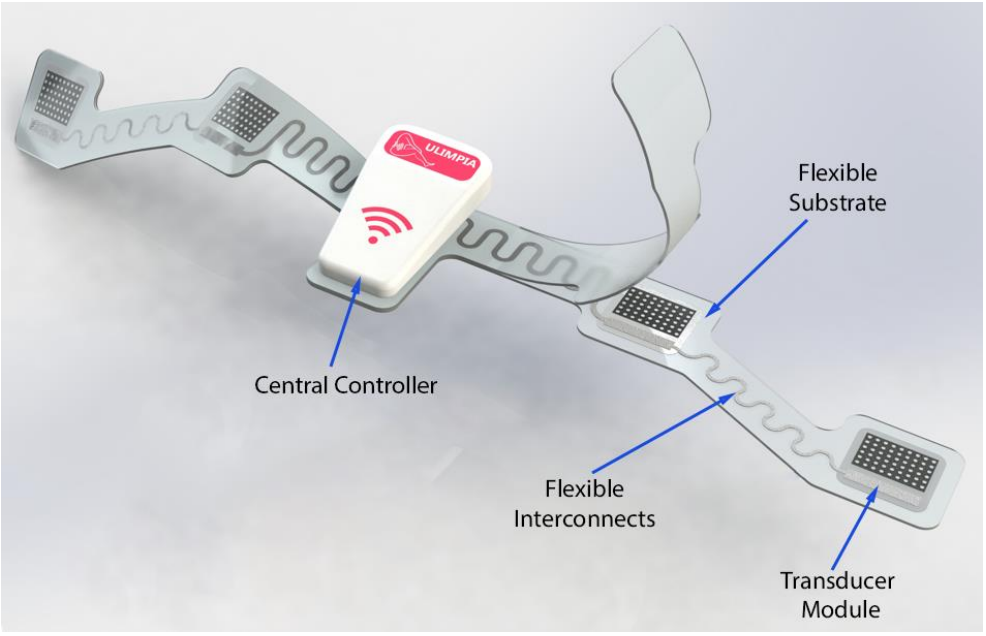

Figure 5.1 Conceptual diagram of a wearable ultrasound monitoring patch.

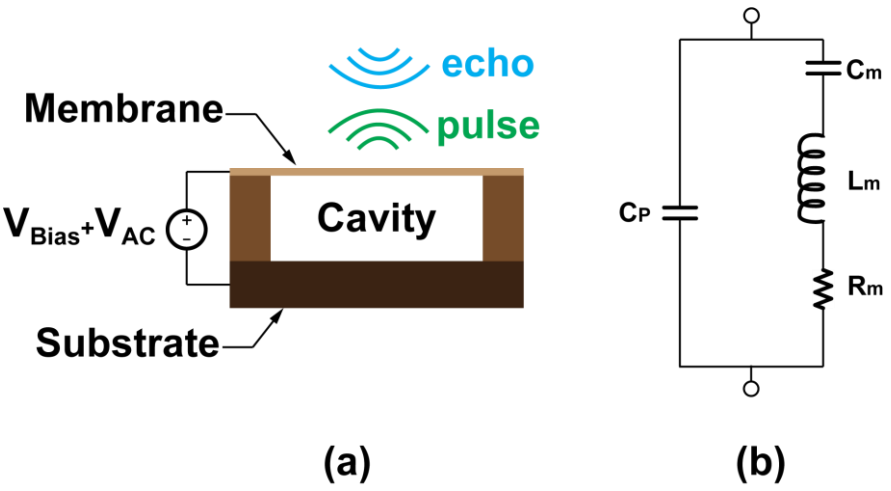

Figure 5.2. a) Simplified structure of a CMUT cell; b) equivalent Butterworth-van-Dyke model of the CMUT.

In [16], a stretchable conformal ultrasound device has been presented for monitoring of the central blood pressure. In [11], a stretchable ultrasonic phased array transducer has been proposed to monitor deep-tissue hemodynamics. However, bench-top equipment was used for signal acquisition and processing, connected to the transducers via cables. Similarly, other flexible ultrasonic arrays [12-14] rely on external power-hungry imaging systems, leaving the design of suitable interface electronics as an open challenge.

Application-specific integrated circuits (ASICs) have been proven to be a suitable solution for both portable ultrasound probes and catheter-based probes [7, 17-18]. However, their application in wearable ultrasound devices so far has been limited. In [19], a battery-powered system has been proposed with an ASIC, transducer array and off-chip electronics to measure body-fat composition. The usage of an off-chip power-hungry ADC and wired communication via USB, and the small number of transceiver channels (only 7) limit the range of medical applications.

In this work, we propose a reconfigurable ASIC that can serve a variety of wearable ultrasound applications. Different applications may require different operating frequencies, transducer array topologies, imaging modes and imaging algorithms. Instead of designing an ASIC for each application, having a reconfigurable ASIC architecture that can be used for multiple applications allows for a shorter evaluation time and is more cost-effective. In recent years, reconfigurable ASICs including element-level high-voltage (HV) pulsers [20] or HV switches [21] have been proposed to provide programmable transmit beamforming patterns. In [22], element-level receivers have been reported to achieve row- or column-parallel connection by grouping low-noise-amplifiers (LNAs) in a row or column. However, those designs are tailored for only one specific type of transducer, which limits the range of

Table 5-1. Impedance characteristics of the low-frequency (LF) and high-frequency (HF) CMUT used in this work.

Transducer type	C_p [pF]	C_m [pF]	L_m [uH]	R_m [kΩ]	Resonance Frequency (MHz)
LF	118.8	56.1	68	1.6	2.58
HF	18.9	9.24	44	4	7.9

applications. This work, in contrast, aims to serve multiple transducer types and configurations with a single design.

Figure 5.1 shows how the proposed ASIC can be applied in a wearable patch configuration. The envisioned patch contains several transducer modules connecting to a central controller via flexible and stretchable interconnects. In each transducer module, an ultrasound transducer array with its interface ASIC is placed on top of a flexible substrate. Besides, local digital signal processing can be implemented in an FPGA or ASIC to perform data reduction. The central controller includes an MCU that controls the transducer modules, a blue-tooth low energy (BLE) radio that communicates with mobile devices, and a battery that provides power for the whole system.

This paper is organized as follows. Section 5.2 describes the proposed system architecture. Section 5.3 discusses the details of the circuit implementation. Section 5.4 and 5.5 present the measurement results and conclusions.

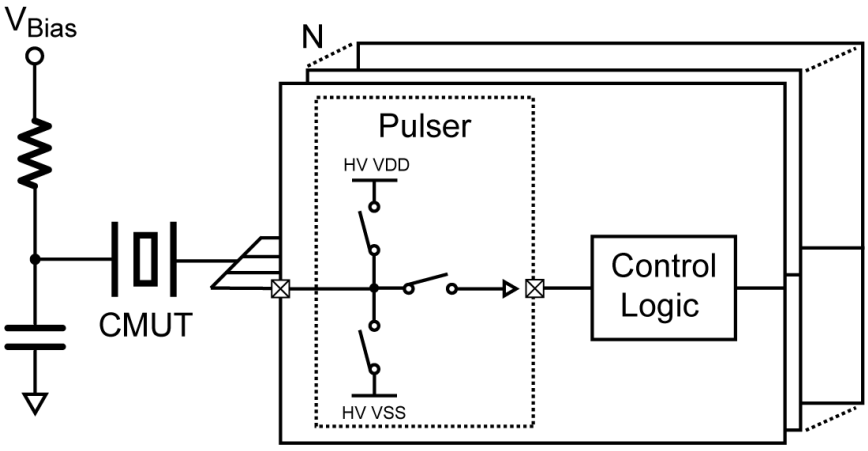

Figure 5.3. Block diagram of *N* parallelized pulsers driving one CMUT element.

5.2 System Architecture

5.2.1 Transducer Characteristics

In the last two decades, capacitive micro-machined ultrasound transducers (CMUTs) have developed into an attractive alternative to conventional PZT-based transducers in terms of performance and fabrication costs [23]. A CMUT element, or "drum", consists of a micro-machined flexible top plate sitting on top of a fixed bottom plate over a vacuum gap, as shown in Figure 5.2. A DC bias voltage (V_{Bias}) is applied across the CMUT to establish an electric field in the cavity, which allows for electrostatic transduction. An AC voltage V_{AC}, typically a pulse with an amplitude of tens of Volt, superimposed on V_{Bias}, can be used to generate an acoustic wave, while returning echo signals can be detected as charge displacement on the CMUT capacitance. The DC bias voltage typically ranges from 40 V up to 160 V [24-26].

The design and dimensions of a CMUT drum depend on parameters such as the targeted centre frequency, bandwidth, and sensitivity. As CMUT drums are often much smaller than the desired aperture of an acoustic transducer element, multiple drums are combined (connected in parallel) to form one transducer element. As a result, CMUTs designed for different applications differ significantly, including their electrical characteristics, calling for a reconfigurable front-end design that can accommodate these differences.

The Butterworth-van-Dyke (BVD) lumped-element model is commonly used to describe the equivalent electrical impedance of piezoelectric transducers as well as CMUTs around their resonance frequency [27-28]. As shown in Figure 5.2, the model includes a motion branch consisting of L_m, C_m, and R_m and a parallel capacitor C_p representing the dielectric property of the CMUT. Table 5-1 lists these parameters for the two types of CMUTs used in this work to demonstrate the reconfigurability of the ASIC: a low-frequency (LF) and a higher-frequency (HF) CMUT. The LF CMUT has around 6 times larger parasitic capacitance and 4 times smaller centre frequency compared to the HF CMUT.

5.2.2 Reconfigurable HV Pulsers

Driving different transducer elements with a wide range of impedance levels and centre frequencies can be done in different ways. For instance, a brute-force approach is to design a pulser that is strong enough to drive the worst-case load, which is not power- and area-efficient when lighter loads need to be driven. Another way is to make the output transistors switchable according to the load conditions. However, when there is a need to interface multiple elements with light load, such an approach would also not be area-efficient. Here, we propose a reconfigurable HV pulsing scheme by dynamically parallelizing pulser channels. A transducer element that represents a heavy load (i.e., a large capacitance and/or

a high driving frequency) is driven by connecting multiple pulsers in parallel, while multiple lighter loads can be driven by the same set of pulsers.

Figure 5.3 shows N HV pulser channels connected in parallel that drive a CMUT element. Noting that the impedance of most CMUT transducers is dominated by their parallel capacitance C_p, the pulsers can be considered to drive a capacitive load. Assuming the parasitic capacitance at the output of the HV pulsers is negligible, the maximum frequency that the pulser can operate at scales inversely proportional to its load capacitance. Therefore, the driving capability of each pulser can be expressed by the product P_{fC} of the pulse frequency and the load capacitance, with a unit of MHz·pF. For a CMUT with a capacitance of C_p and a central frequency of f_c, the number of HV pulsers that need to be parallelized will be:

$$N = \frac{f_c \cdot C_p}{P_{fc}} \tag{5-1}$$

For instance, an HV pulser with a driving capability of 144 MHz·pF can drive a HF CMUT element without parallelizing channels, while a LF CMUT element can be driven by three of those pulsers connected in parallel.

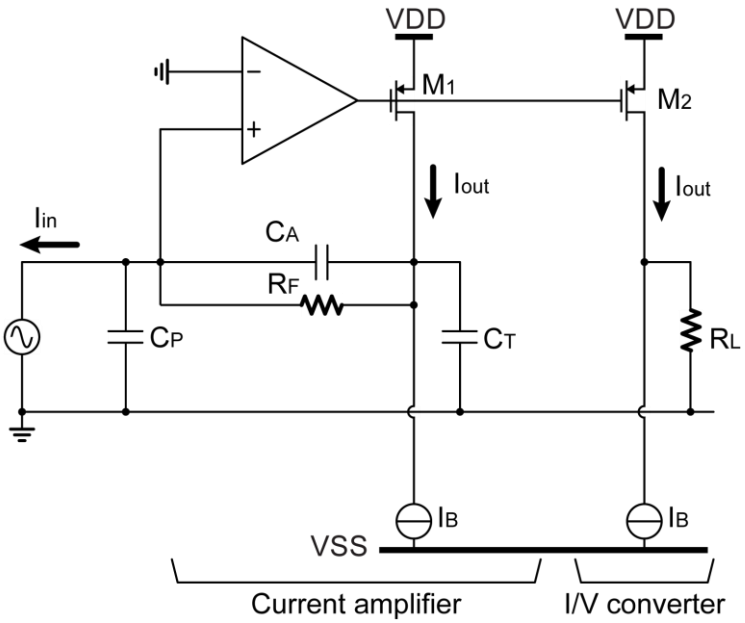

Figure 5.4 Simplified block diagram of the TIA architecture used in [29].

5.2.3 Reconfigurable Low-Noise Amplifiers

Similar to the reconfigurable HV pulsers, there are also different ways to make LNAs reconfigurable to interface with different transducer elements. One way is to design the amplifier to meet the bandwidth and noise requirements for the worst-case load, which is not power and area-optimized for lighter loads. Another way is to make the biasing current tuneable for different bandwidth and noise requirements. However, this approach is not area-efficient to interface small transducer elements with light load. Therefore, we also employ a channel-parallelizing scheme, enabling a reconfigurable LNA to drive a large transducer element or multiple small elements.

Since the impedance of the CMUT is dominated by its parallel capacitance and the acoustic echo signal is converted to signal charge, LNAs with trans-impedance amplifier (TIA) topologies have been used [20, 29]. Here, we will adopt the topology shown in Figure 5.4 [29], which is based on a current amplifier (CA) that provides an amplified version of the signal current:

$$I_{out} = \left(1 + \frac{C_2}{C_1}\right) I_{in} = G \cdot I_{in} \tag{5-2}$$

which is copied to a load resistance R_L to create trans-impedance gain. Compared to TIAs with resistive feedback, this topology offers better noise efficiency [30]. Moreover, it provides the possibility to implement variable gain to implement time-gain compensation

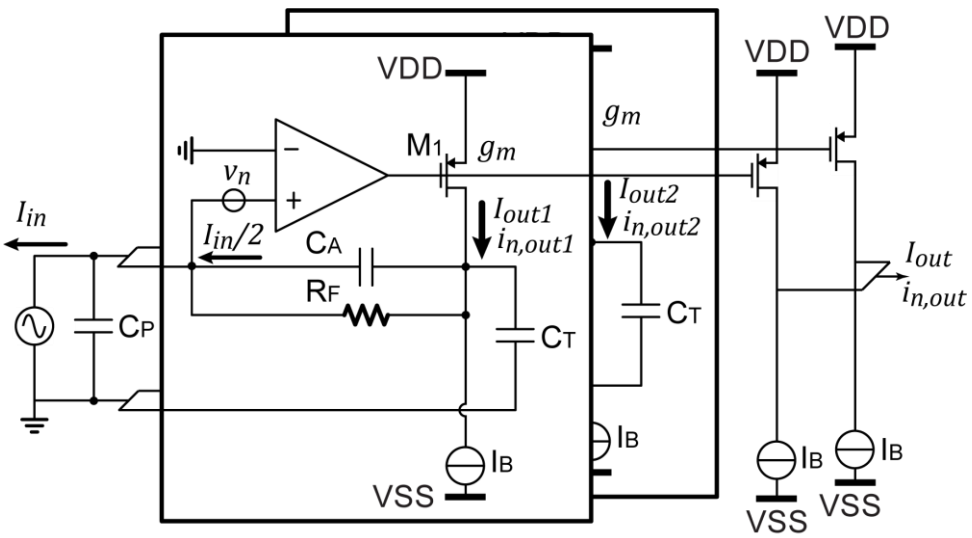

Figure 5.5 Simplified block diagram of the two parallelized CAs interfacing with one CMUT element.

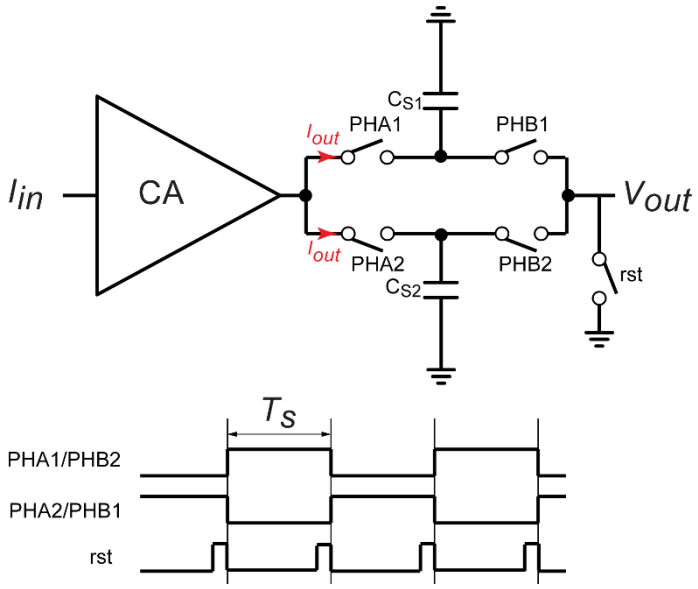

Figure 5.6 Block diagram of the boxcar sampling scheme (single-ended version shown for simplicity).

[29]. The reconfiguration approach described below, however, is also applicable to other TIA topologies. In Figure 5.4, the CMUT is modelled as a current source in parallel with its intrinsic capacitance C_p. The unity-gain frequency of the loop gain, which determines the closed-loop 3-dB bandwidth, is approximately [29]:

$$\omega_u = \frac{A \cdot \beta \cdot g_m}{C_p} \tag{5-3}$$

where A is the gain of the loop amplifier (which is assumed to have a bandwidth larger than ω_u), β is the feedback factor and g_m is the transconductance of M1. Figure 5.5 shows two parallelized CAs with their virtual grounds connected to the CMUT and their outputs summed in the current domain. At the common virtual ground, there are two feedback loops charging the input capacitor. If the two CAs match well, each loop is equivalently driving half of C_p. Therefore, the closed-loop bandwidth can be expressed as:

$$\omega_u = \frac{A \cdot \beta \cdot 2 \cdot g_m}{C_p} \tag{5-4}$$

More generally, for an N-fold parallelized CA, the close loop bandwidth will be:

$$\omega_u = \frac{A \cdot \beta \cdot N \cdot g_m}{C_p} \tag{5-5}$$

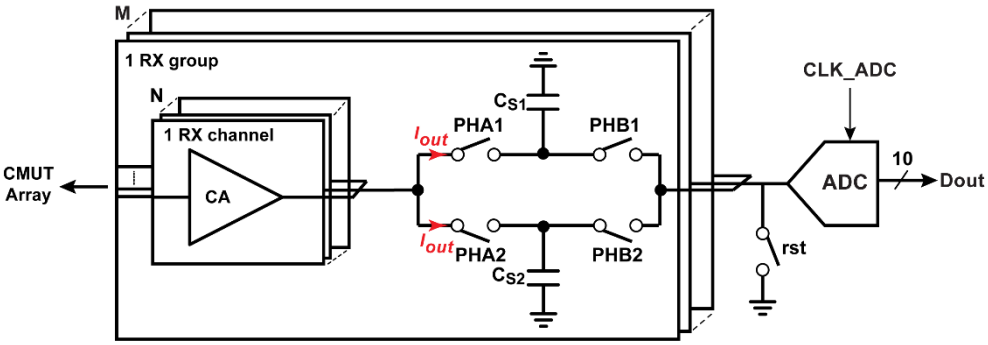

Figure 5.7 Block diagram of the multiple boxcar-sampling channels interfacing with multiple CAs and one ADC (single-ended version shown for simplicity).

The closed-loop bandwidth of the CA should be larger than the transducer centre frequency. Therefore, like for the HV pulser, the driving capability of a given CA design can be expressed as the product $P_{fc}$of the transducer centre frequency and load capacitance that it is designed for. The number of CAs that need to be parallelized to drive a given CMUT with capacitance C_p and centre frequency f_c can be calculated based on (5-1). When parallelizing CAs, which implies that multiple loop amplifiers are connected in parallel to the one input, it is crucial to know how signal and noise are amplified. In Figure 5.5, assuming there is no mismatch between the two parallelized CAs and the output currents will be summed without any losses, each CA will absorb half of the input current and thus the summed output current will be the same as that in the single-CA case. Therefore, the signal gain of the 2-fold parallelized CA case will be the same as that of a single CA. In the single-CA case, assuming $C_p \gg C_2$, the noise gain of the loop amplifier noise v_n to output current is:

$$G_n = j\omega\left[\left(1+\frac{C_2}{C_1}\right)C_p + C_2\right] \approx j\omega\left(1+\frac{C_2}{C_1}\right)C_p \tag{5-6}$$

The equivalent input-referred current noise is:

$$i_{n,in} = v_n\,\frac{G_n}{G} \approx v_n \cdot j\omega C_p \tag{5-7}$$

When two CAs are connected in parallel with their virtual grounds shorted to each other, the loop amplifier noise v_{n1}^2 and v_{n2}^2 will be averaged, leading to a total noise of $(v_{n1}^2 + v_{n1}^2)/2$. Noting that the signal gain is the same as in the single-CA case and assuming $v_{n1}^2 = v_{n2}^2 = v_n^2$, the total input-referred noise current will $\sqrt{2}$ times smaller than that of the single-CA case. Therefore, putting N CAs in parallel will increase the bandwidth by a factor of N with the same mid-band gain and reduce the input-referred current noise by a factor of $\sqrt{N}$. However, there are some noise sources that cannot be averaged in the CA, for instance, the

current noise of the feedback resistor R_F and the biasing current I_B. These noise sources add uncorrelatedly to the input-referred current noise, deteriorating the noise reduction factor.

5.2.4 Reconfigurable Digitization

The LNA output (or combined outputs) will be digitized by an ADC. As a rule of thumb [31], the sampling frequency should be 4 to 10 times higher than the transducer centre frequency. To enable reconfigurable digitization for different transducer centre frequencies, several options are possible:

- Time-interleaving the signals of multiple channels at the input of one ADC [32-33]. This can be done if the ADC sampling rate is higher than what is needed per channel, implying that the number of ADCs is less that the number of channels.

- Multiplexing one ADC to serve multiple channels if the ADC sampling rate matches with what is needed per channel. This will lead to frame-rate loss compared to a scenario in which each channel has its own ADC [34].

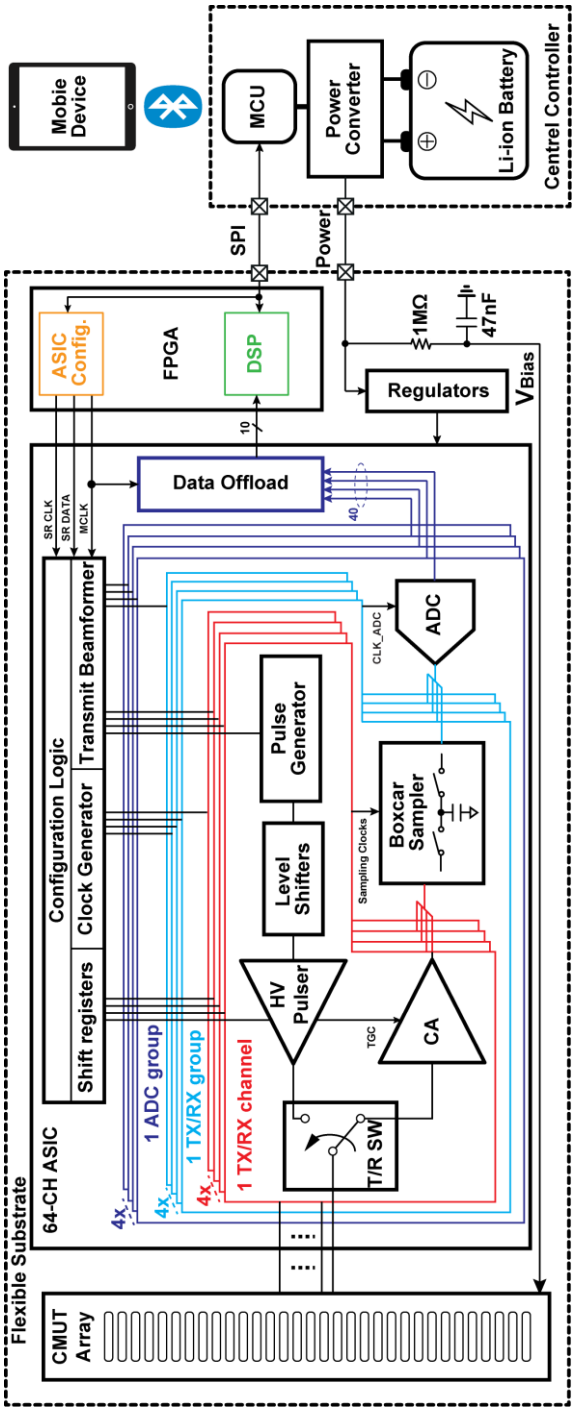

Figure 5.8 Overview of the ASIC architecture.

- Time-interleaving multiple ADCs to serve one higher-BW channel if the ADC sampling rate is lower than what is needed per channel, implying that the number of ADCs is more than the number of channels [35].

To arrive at a reasonable trade-off between complexity, output data rate and frame rate, we apply the first option for the LF transducer and the second for the HF transducer, implying that a reconfigurable sampling network is required. In conventional sampling networks, the output voltage of the front-end circuitry is typically sampled on a capacitor and then digitized [34, 36-38]. This approach tends to be power-hungry as it requires driving the sampling capacitor with sufficient bandwidth to allow settling within a fraction of the ADC's clock period [34]. Instead, we adopt the boxcar sampling scheme proposed in [39-40], as it reduces the power consumption and naturally fits with the current-mode output of our CA-based LNA.

Figure 5.6 shows a single-ended boxcar sampler and the associated timing diagram. The input current I_{in} is amplified by a CA with gain A, and integrated alternately on two sampling capacitors C_{S1} and C_{S2}. The integration will last for a clock period T_S. After that, the sampling capacitor is disconnected from the CA and connected to the ADC. Before the next integration cycle starts, the sampling capacitor is discharged through a reset switch. This scheme saves power compared to voltage-mode sampling, and, moreover, provides anti-aliasing filtering which helps reducing noise folding [40].

To enable the reconfigurable digitization, multiple boxcar-sampling channels are used. Figure 5.7 shows that one ADC interfaces with *M* RX groups, each of which contains a boxcar sampler and *N* RX channels consisting of CA front-ends. These RX channels can be connected in parallel, as discussed in Section 5.2.3, depending on the CMUT impedance and centre frequency. Their outputs are shorted to perform current summation. The summed signal currents are then integrated onto the sampling capacitors. Clocked by CLK_ADC, the ADC is shared by the boxcar samplers of *M* RX groups. If the ADC sampling frequency matches with what is needed per channel, only one of the boxer samplers and the corresponding RX channels will be connected to the ADC to perform digitization in every receive period. If the ADC sampling frequency is *M* times higher than what is needed per receive channel, all boxcar samplers connect to the ADC in a time-interleaved manner such that one ADC can serve for *M* boxcar samplers and the associated RX channels.

5.3 Circuit Implementation

5.3.1 ASIC Architecture

Based on the proposed reconfigurable HV pulsers, LNAs and digitization, a prototype ASIC designed to interface with a CMUT array of 16 up to 64 elements is presented, along with

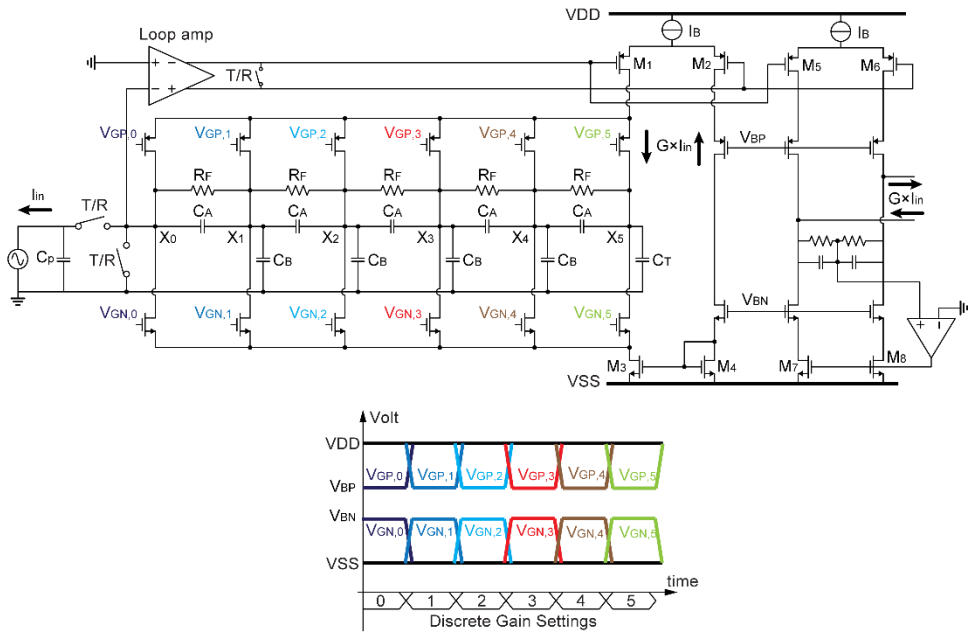

Figure 5.9 Block diagram of the low-noise current amplifier.

the associated peripheral electronics, as shown in Figure 5.8. The CMUT array either consists of 16 LF transducer elements or 64 HF elements which are DC biased at V_{Bias} via a shared low-pass RC network. By parallelizing TX/RX channels, the ASIC can interface with both arrays. One TX/RX channel is designed to interface with one HF transducer element. The T/R switch and the HV pulser in each TX/RX channel have been described in [41] in detail. To interface with an LF transducer element, which has higher capacitance, 4 TX/RX channels are connected in parallel in a TX/RX group. At the input, this is done by wire-bonding their inputs to the same PCB pad that connects with one LF transducer element. By employing the abovementioned reconfigurable digitization scheme, 4 TX/RX groups connect to one 40 MS/s ADC via reconfigurable sampling networks such that the ADC can digitize echo signals from one HF transducer element or from 4 LF transducer elements simultaneously. The 10-bit outputs from 4 ADCs are transferred to an FPGA via a data-offload block with a 10-bit data bus which runs at a 160 MHz clock frequency such that all the ADC data can be transferred simultaneously. The 160 MHz master clock (MCLK) is generated in the FPGA and distributed to the data-offload block, the HV transmit beamformer and the clock generator that generates clock signals for the boxcar samplers and ADCs. The HV transmit beamformer, which has been described in [41], determines the start time of the pulses generated by each HV pulser, achieving different delay profiles for acoustic beam steering and focusing. Configuration data for the HV pulser, the LNA, and the ADC are stored in a shift register (SR) which is updated via clock (SR_CLK) and data (SR_DATA). The ASIC,

CMUT array, FPGA, and regulators are integrated on top of a flexible PCB. After post-processing the received ADC data from the ASIC to reduce the data rate, the FPGA transfers the processed data to the MCU in the central controller via a low-speed SPI interface. Further data processing or analysis can be done in the MCU such that the data rate is small enough to use low-energy Bluetooth for communication with mobile devices.

5.3.2 Low-Noise Current Amplifier

The low-noise CA is similar to that presented in [29], and is shown in Figure 5.9. The topology is similar to that of Figure 5.4, except that a ladder-type feedback network is used to create programmable gain, and that the amplified signal current is generated using a differential pair $M_{1,2}$ with current-mirror load $M_{3,4}$, rather than the single-ended configuration of Figure 5.4. In contrast with [29] and Figure 5.4, the output current is not turned into a voltage using a load resistor, but copied out using a replica differential pair $M_{5,6}$. Combined with load current sources $M_{7,8}$, this provides a fully-differential output current to drive the boxcar sampler. Cascode transistors biased at voltages V_{BN} and V_{BP} help to make the output current insensitive to voltage swing at the feedback network and output nodes. To regulate the output common-mode voltage, a CMFB circuit, consisting of a common-mode sense circuit and an error amplifier, controls the load current sources. The programmable gain is realized by means of a switchable ladder feedback network [29]. The capacitors in the ladder network are sized to have a six gain steps of 8 dB, ranging from 0 dB to 40 dB. The gain is set by steering the drain currents of M_1 and M_3 into one of the taps of the ladder network using a set of current-steering transistors controlled by voltages $V_{GP,0..5}$ and $V_{GP,0..5}$. At the lowest gain (setting 0), $V_{GP,0}$ and $V_{GN,0}$are pulled to V_{BP} and V_{BP} respectively while the remaining NMOS and PMOS are turned off such that all feedback current is steered to the input node, leading to a current gain of 0 dB. As the discrete gain setting increases from 0 to 5, the feedback current steers to different taps of the capacitor ladder network by alternately turning on the PMOS and NMOS switches, as shown in the timing diagram in Figure 5.9.

The programmable gain can be used for time-gain-compensation (TGC), i.e. to compensate for the attenuation that the acoustic waves experience as they travel through tissue by amplifying the first echoes, which have higher amplitudes, less than the weaker later echoes [42]. In principle, this current-steering topology can be used to realize continuous gain control by employing gradual transitions at the gates of the current steering differential pairs, as described in [29]. Here, for simplicity, we use discrete, digitally-controlled gain steps instead. When multiple channels are connected in parallel, their outputs are connected in parallel to the same sampling network, performing the signal summation. During the transmit phase, the CA inputs and outputs, and the loop amplifier outputs are shorted to prevent disturbance of the biasing point caused by HV pulsing. When a channel is disabled, its biasing current is disabled. Besides, the LV T/R switch is disconnected, and the CA virtual ground

is shorted to ground such that the enabled channel will not have extra loading from the disabled channel.

5.3.3 Sampling Network

To enable the reconfigurable digitization discussed in Section 5.2.4, a flexible sampling network that dynamically connects the ADC to the front-end is necessary. Figure 5.10a shows the block diagram of the sampling network with connections to CA and ADC. Each RX group with four CAs connects to one sampling block. Each sampling block contains two time-interleaved sampling capacitors C_{S1} and C_{S2} such that the CA output signal is boxcar-integrated for a full sampling period on either C_{S1} or C_{S2} while the ADC digitizes the charge

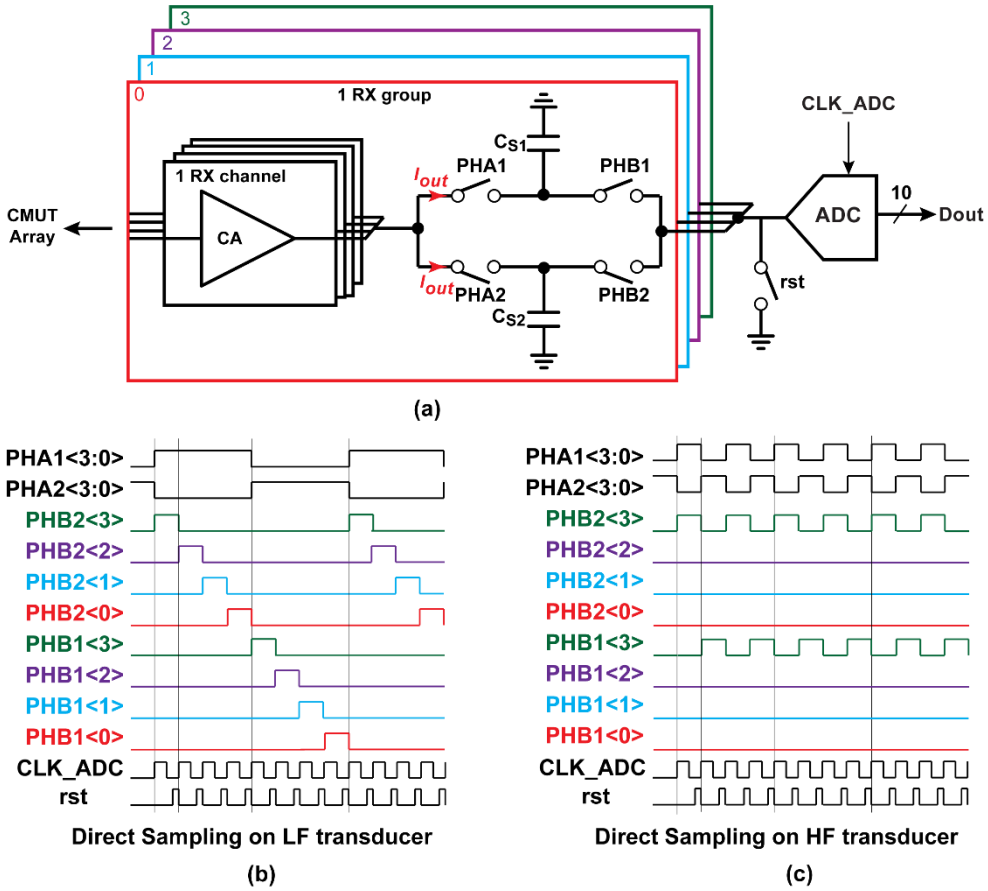

Figure 5.10 Block diagram of the sampling block and timing diagram of different sampling modes. (single-ended version shown for simplicity).

stored on the other capacitor. The sampling switches are controlled by PHA1<3:0>, PHA2<3:0> while the switches that connect sampling capacitors to the ADC are controlled by PHB1<3:0> and PHB2<3:0>, as shown in Figure 5.10a.

Figure 5.10b shows the timing diagram of the time-interleaving mode for the LF transducer, in which the ADC runs at higher frequency to digitize echo signals from multiple transducer elements simultaneously. Thus, the 40 MS/s ADC can be time-multiplexed to digitize 4 RX channel with each channel being sampled at 10 MHz. As shown in Figure 5.10b, the sampling switches controlled by PHA1<3:0> and PHA2<3:0> are toggling at 10 MHz such that CA output current will be integrated on the 4 groups of sampling capacitors for 100 ns. The 40 MS/s ADC can then sequentially digitize the charge stored on the C_{S1} or C_{S2} of the 4 groups by toggling PHB1<3:0> and PHB2<3:0> one-by-one every 25 ns. Figure 5.10c shows the timing diagram of the direct sampling mode for the HF transducer in which the ADC only digitizes echo signal from one transducer element at a time. In this mode, the sampling switches controlled by PHA1<3:0> and PHA2<3:0> are toggling at 40 MHz while only one of the 4 sampling capacitors will be connected to the ADC for conversion by configuring control signals PHB1<3:0> and PHB2<3:0>. For instance, the timing diagram shown in Figure 5.10c indicates that only sampling block<3> will be connected to the ADC.

The sizing of the sampling capacitor C_s determines the trans-impedance gain of the boxcar sampler from the amplified signal current at the CA's output to a voltage at the input of the ADC. The ADC input full scale $V_{FS,ADC}$ can be expressed as

$$V_{FS,ADC} = \frac{i_{in,p-p} \cdot G \cdot T_s}{C_S} \tag{5-8}$$

where $i_{in,p-p}$ is the maximum peak-to-peak signal current, G the CA's current gain, and T_s the boxcar integration time. The input peak-to-peak signal current depends on the application

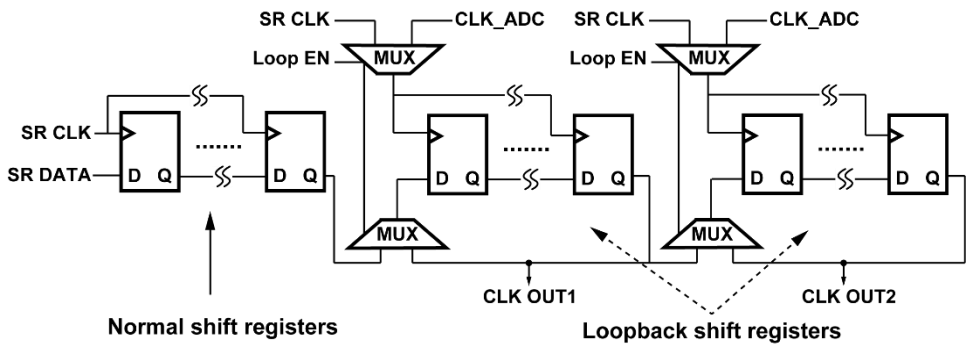

Figure 5.11 Block diagram of the loop-back shift register.

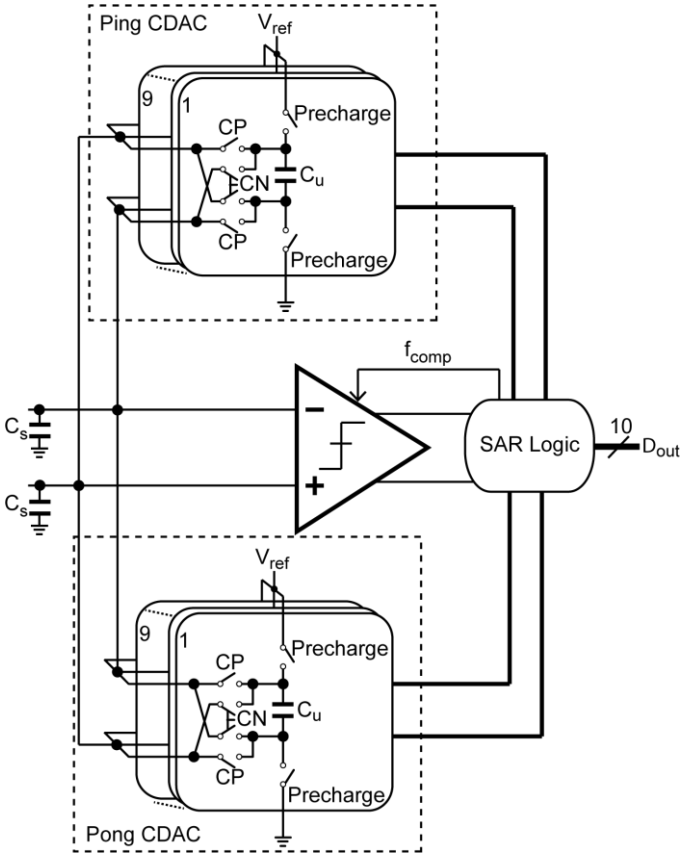

Figure 5.12 Block diagram the 10-bit charge-sharing ADC.

and transducer sensitivity and can be as large as 100 µA [29]. To handle this at the smallest CA gain of 0 dB, C_S is sized at 2.4 pF, leading to an ADC input full range of 1 V when the sampling frequency is 40 MHz. At a lower sampling frequency, the maximum detectable input signal current will be lower than 100 µA. For instance, when the sampling frequency is 10 MHz, the detectable $i_{in,p-p}$ is 25 μA, which is still acceptable.

5.3.4 Control Logic

As shown in Figure 5.10, each sampling block requires 6 clock signals which all require stable edges and close to 50% duty cycle. Besides, those signals should be programmable to support different sampling modes. To flexibly generate these clock signals, a loop-back shift register (LBSR) clocked by the ADC sampling clock is used. As shown in Figure 5.11, the LBSR is initially in normal loading mode in which data is shifted from left to right by configuring the shift register clock to SR_CLK and each shift register input to the output of

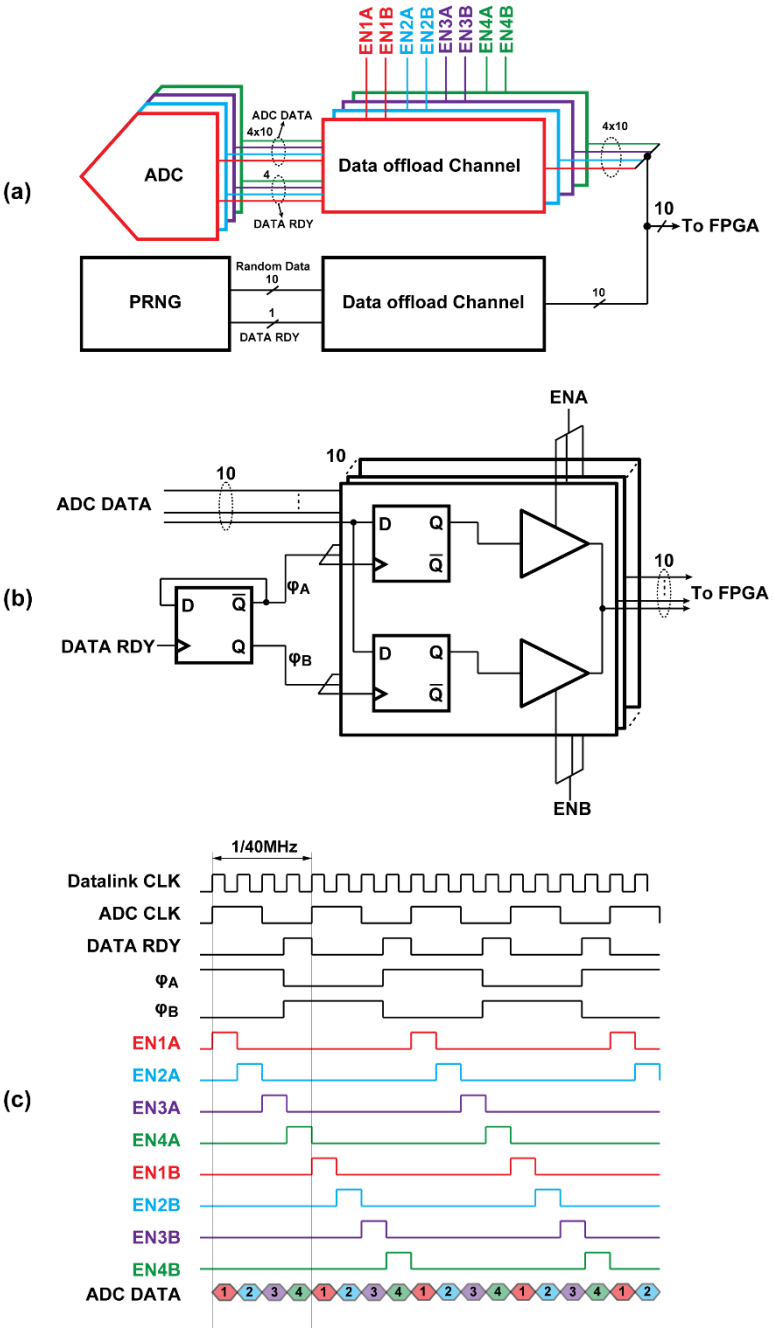

Figure 5.13 (a) Block diagram of the datalink; (b) circuit diagram of a data offload channel, and (c) associated timing diagram.

the preceding stage. In the loop-back mode, the SR is clocked by the ADC sampling clock CLK_ADC and its output is connected to the input such that the pre-loaded data will be shifted in a loop. Thus, a control signal will be generated synchronous to the sampling clock with a pattern defined by the pre-loaded data, allowing clock patterns such as those in Figure 5.10 to programmed. Similarly, the ADC sampling clock itself is also derived with such a LBSR driven by the system clock. For instance, if the pre-loaded data pattern is 11001100 and the LBSR is driven by 160 MHz, the output will be a 40 MHz clock with a well-defined duty cycle and stable rising and falling edges.

5.3.5 ADC

The required resolution of the ADC is determined by the dynamic range (DR) of the CA output. With the help of TGC, the ADC input will roughly see the instantaneous DR of the incoming echo signal, ranging from 40 dB to 50 dB depending on the application. In view of this modest DR requirement and the mentioned sampling rate of 40 MS/s, a SAR ADC is a suitable choice in the 180 nm technology used. Since the boxcar sampler is applied to integrate the signal current, digitization in the charge domain is preferred. Therefore, a 10-bit 40 MS/s charge-sharing SAR ADC is employed. Figure 5.12 shows a circuit diagram of the charge-sharing SAR ADC which has been described in detail in [36]. It consists of a pair of ping-pong capacitive DACs (CDACs) which are pre-charged to an external reference voltage before the conversion starts. The sampling cap is connected to the pre-charged ping or pong CDAC whose charge will be used to neutralize the signal charge in 9 successive approximation steps. This is done in a time-interleaved manner, which means that the ping CDAC and pong CDAC are alternately pre-charged or connected to the sampling cap. Each CDAC contains 67 unit capacitors, leading to 1.5 pF total capacitance. Asynchronous SAR logic, driven by the differential output of the dynamic comparator, is applied to eliminate the need for an external high-speed clock. The offset of the dynamic comparator is calibrated in the background while the SAR logic is running.

5.3.6 Data Offload

Data offloading can be done by first serializing and encoding the data using a high-speed clock and then transmitting it to the FPGA using an LVDS driver, reducing the number of interconnects [36]. In our wearable ultrasound patch, we prefer to avoid the Gb/s data rates and associated power consumption and, instead, employ parallel data bus to transfer ADC data. Figure 5.13a shows a block diagram of the data offload circuit that combines the parallel outputs of 4 ADCs on one 10-bit data bus by time-interleaving the data using a 160 MHz clock. In order to generate a stable version of the ADC output data with sufficient timing margin in spite of the variable timing associated with the self-timed SAR logic, each ADC output and its data-ready signal is connected to a datalink channel that contains a ping-pong sample-and-hold circuit, as shown in Figure 5.13b. Two 10-bit registers, clocked by divided

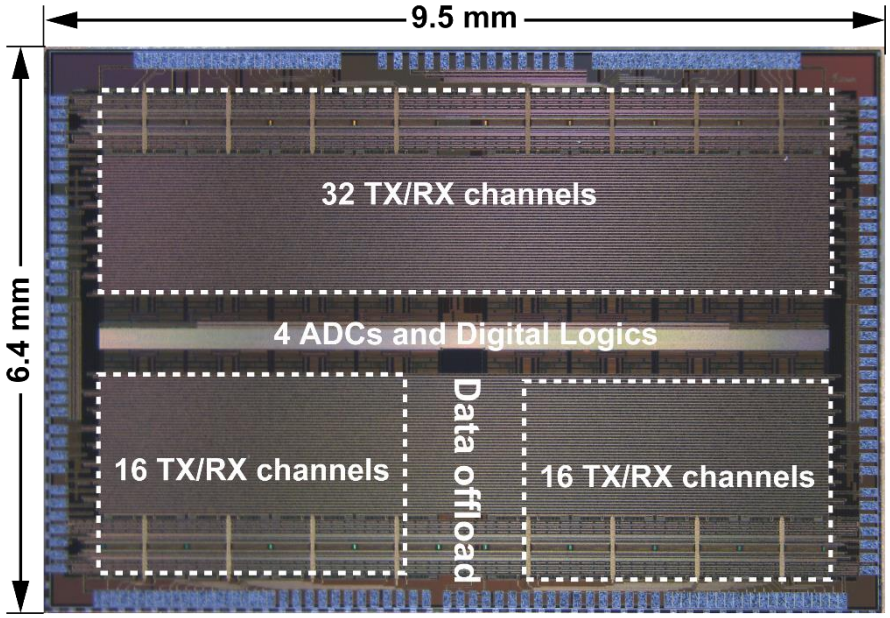

Figure 5.14 Micrograph of the ASIC.

versions of the data-ready signal φA and φB, alternately sample the ADC output data and hold it for a 50 ns period. Within that period, two tri-state buffers, controlled by enable signals ENA and ENB, drive the data onto the output data bus during the right 12.5 ns interval.

The timing diagram in Figure 5.13c shows how the enable signals of the four datalink channels are interleaved. These signals are generated using a loop-back shift register that allows for a programmable pulse width ranging from 12.5 ns to 50 ns. This allows the datalink to transfer four channels simultaneously, as shown in Figure 5.13c, but also one or two channels at a lower data rate if desired. Moreover, all tri-state buffers can be disabled by setting all the tri-state buffer enable bits to be low such that multiple ASICs can be placed in parallel with a shared data bus. Thus, in principle, multiple ASICs can be combined to interface with e.g., a 128-channel or 256-channel transducer array. To evaluate the bit error of the proposed data offload circuit, an additional data offload channel is used to transfer test data generated by a pseudo-random number generator (PRNG) with pre-determined seed.

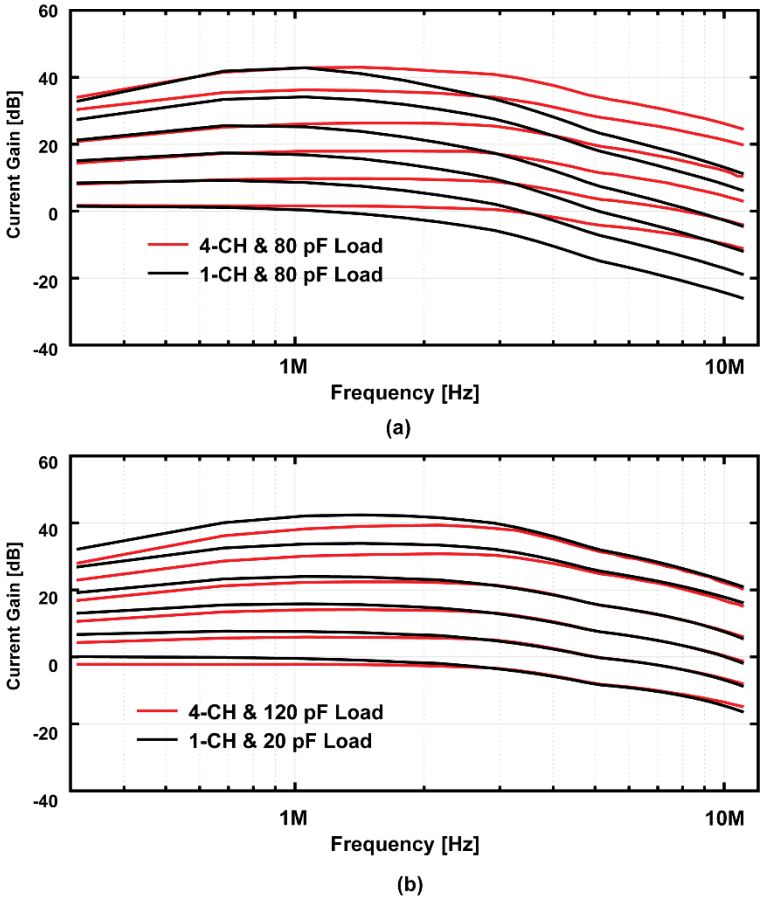

Figure 5.15 Measured current gain transfer function with (a) a single channel CA and 4 CA channels in parallel, loaded with an 80 pF input capacitor. (b) single channel CA loaded with a 20 pF input capacitor and 4 CA channels in parallel loaded with a 120 pF input capacitor.

5.4 Experimental Results

5.4.1 Experimental Prototype

The ASIC has been fabricated in TSMC 180 nm HV BCDMOS technology with a size of 9.5 x 6.4 mm^2, as shown in Figure 5.14. The 64 TR/RX channels with each channel including the TX beamformer, HV pulser, low-noise CA, and biasing circuits, are separated into two rows of 32 TX/RX channels. The ADCs, sampling blocks and associated loop back shift

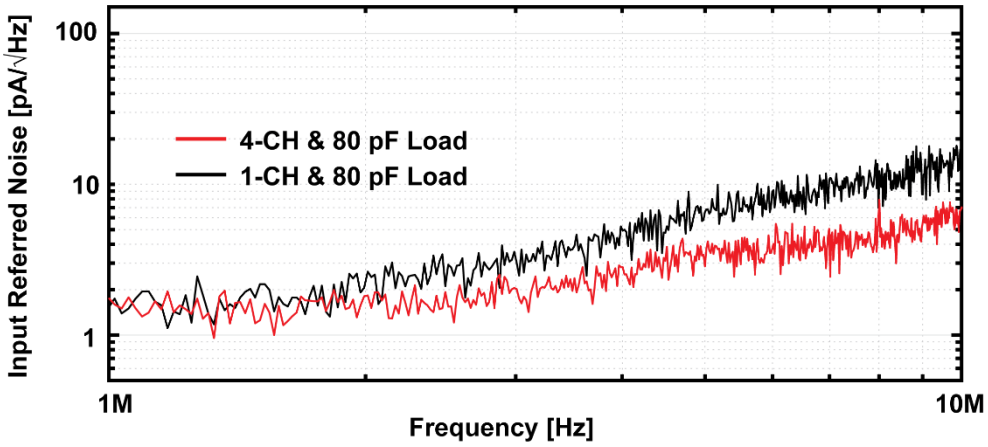

Figure 5.16 Measured input-referred noise at the highest gain setting with a single CA channel and 4 CA channels in parallel, loaded with an 80 pF input capacitor.

registers are located in the centre of the ASIC and placed close to each TR/RX block. The datalink is placed in the middle of the bottom row and close to the associated bond pads.

5.4.2 Electrical Characterization Results

To characterise the electrical performance of the receive signal chain, a sinusoidal input signal current was applied to the CA input through an 80 pF off-chip capacitor that mimics the CMUT capacitance. Figure 5.15a shows the measured transfer function for the six gain settings, both for a single CA channel and for four CA channels connected in parallel, with a 3-dB bandwidth of 1.6 MHz and 4-MHz, respectively. In theory, the bandwidth of the 4-fold parallelized CAs should be 4 times larger than that of the single channel. However, the routing parasitic capacitance at output of the CA is charged along with the sampling capacitor during the integration phase. This parasitic capacitor remains charged and will share charge with the sampling capacitor in the next integration cycle, effectively forming a IIR low-pass filter. This additional limiting factor reduces the bandwidth scaling factor of the proposed channel-parallelizing scheme. Figure 5.15b shows the measured transfer function for 120 pF and 20 pF input capacitors that are closer to the capacitance of the LF and HF CMUT shown in Table 5-1. The 3-dB bandwidth for 120 pF is around 4 MHz which is larger than the centre frequency of LF CMUT. However, the 3-dB bandwidth for 20 pF is only 3.6 MHz which is lower than the centre frequency of HF CMUT. This problem can be solved by reducing the layout routing parasitic or resetting the parasitic capacitor along with the sampling capacitor.

The input-referred noise is obtained by dividing the measured output-referred noise by the measured transfer function. Figure 5.16 shows the input-referred noise spectrum in the

maximum gain setting, again both for a single CA channel and for four CA channels connected in parallel. At 2.5 MHz, the input-referred current noise density is 2.7 pA/√Hz for the single-channel case versus 1.7 pA/√Hz for the 4-channel case, indicating a noise reduction factor of 1.6, which is a bit lower than the theoretical value of 2. As discussed in Section 5.2.3, this is caused by the noise sources that have non-negligible contribution and

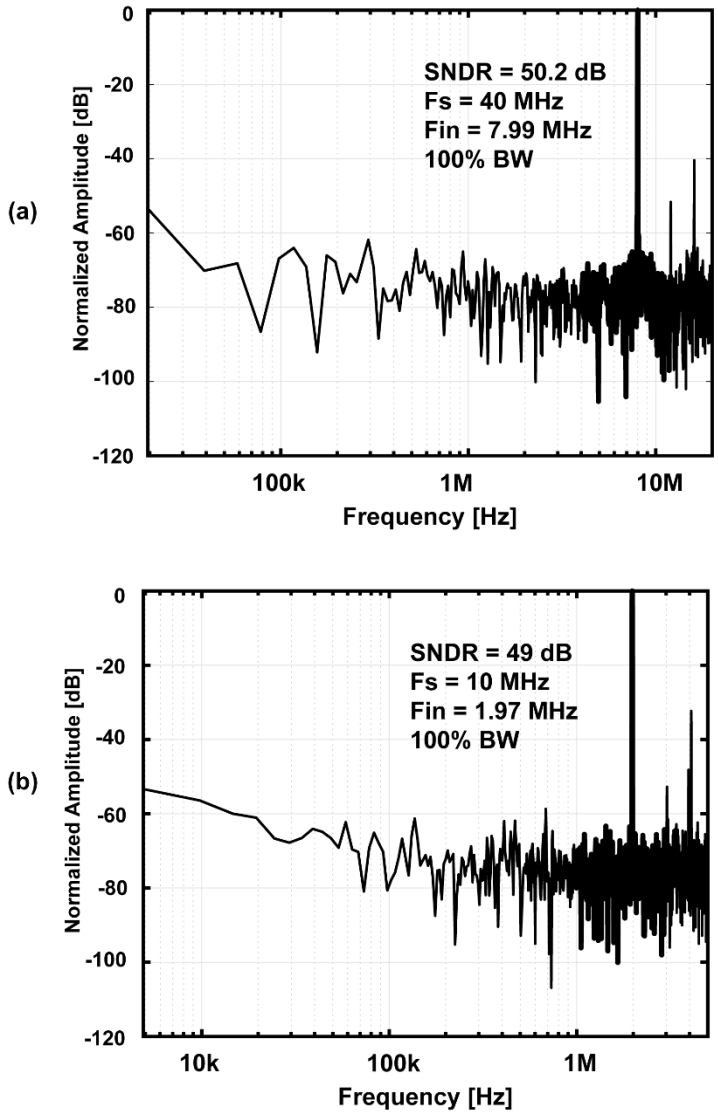

Figure 5.17 Measured ADC output SNDR at two different sampling rates: (a) 40 MS/s; (b) 10 MS/s.

cannot be averaged by connecting CA in parallel. The measurement results are in good agreement with simulations.

A sinusoidal input signal was applied to evaluate the SNDR of the signal chain. The ADC was running at 40 MS/s while the sampling network was configured to be either 10 MS/s for the LF transducer or 40 MS/s for the HF transducer. As shown in Figure 5.17, both sampling modes achieve around 50 dB SNDR within an 100% bandwidth, where the AFE dominates the noise floor. To evaluate the HV pulser, a 120 pF off-chip capacitor that mimics the LF capacitance was used as the load. Figure 5.18a shows the output waveform of a 3-cycle 3 MHz pulse with one pulser channel to four parallelized pulsers connected to the capacitor, indicating the effectiveness the proposed channel-parallelizing scheme. Figure 5.18b shows

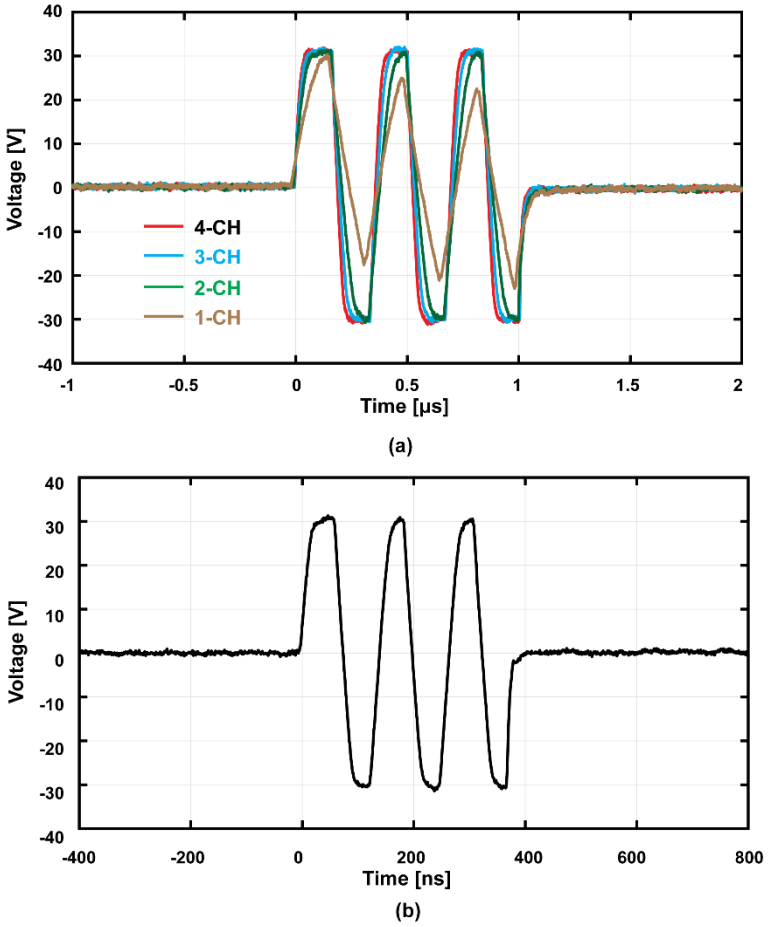

Figure 5.18 Measured pulser output with (a) 1 to 4 pulser channels connected to a 120-pF load pulsed at 3 MHz; (b) 1 pulser channel connected to a 20-pF load pulsed at 8 MHz.

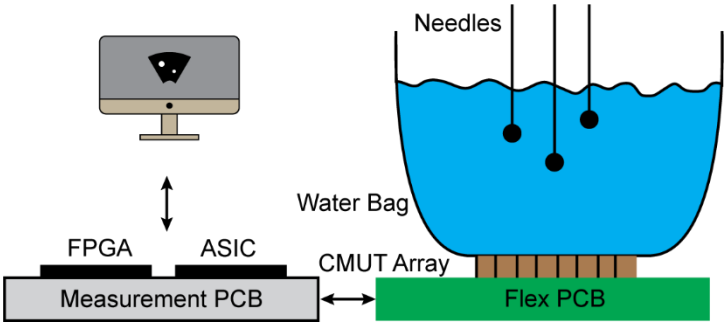

Figure 5.19 Block diagram of the acoustic measurement setup used for the HF CMUT array.

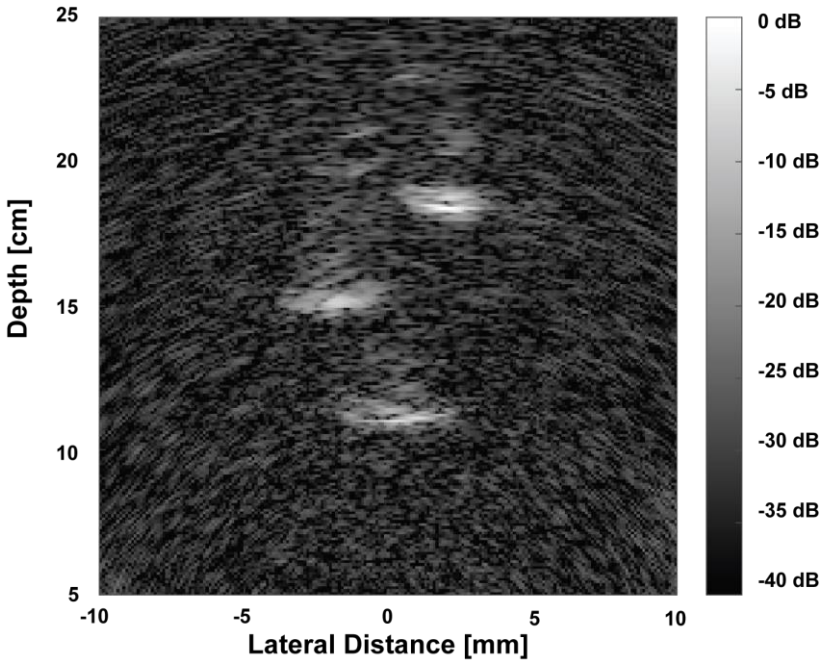

Figure 5.20 2-D cross-sectional B-mode image obtained using the HF CMUT array showing the position of the 3 needles.

the output waveform of a 3-cycle 8 MHz pulse with one pulser channel driving 20 pF load that is equivalent to the load capacitance of HF transducer.

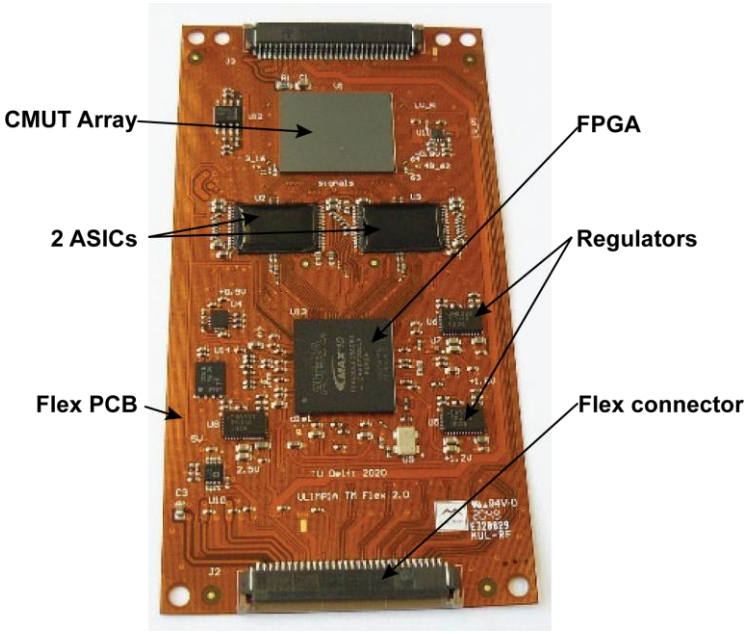

Figure 5.21 Prototype of a wearable ultrasound body patch with ASICs, FPGA and LF CMUT array integrated on top of a flex PCB.

5.4.3 Acoustical Experiments

To perform acoustic measurements, the prototype ASIC was interfaced with both a HF and LF CMUT array with element impedance characteristics shown in Table 5-1. A 48-element HF CMUT array was connected to 48 transceiver channels of one prototype ASIC. As shown in Figure 5.19, the CMUT array was mounted on top of a flex PCB which is connected to the measurement PCB. The FPGA (MAX10, Intel Corp., CA, USA) receives the digitized echo signals and transfers them to a PC for image processing. A water bag with three needles immersed in the water was placed on top of the CMUT array. A 2-D B-mode image, shown in Figure 5.20, was obtained with a full synthetic aperture acquisition scheme, in which the 48 elements are pulsed one-by-one and the digitized echo signals received by the 48 elements are captured successively to perform delay and sum beamforming. The image clearly shows the position of the 3 needles in a 40 dB display dynamic range.

As an additional demonstrator, a prototype wearable ultrasound patch for bladder monitoring has been fabricated, consisting of two ASICs, a LF CMUT array, an FPGA (MAX10, Intel Corp., CA, USA) and peripherals integrated on a flex PCB, as shown in Figure 5.21. The LF CMUT array contains 32 elements, each of which is interfaced by 4 parallelized ASIC transceiver channels. Each ASIC includes 64 transceiver channels, which means 2 ASICs are

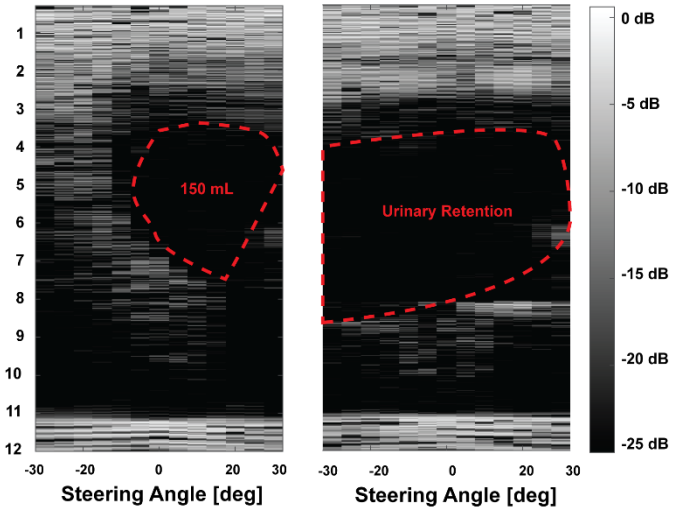

Figure 5.22 2-D cross-sectional image of the intravesical urine volume measurement phantom.

needed. The prototype patch was evaluated with two tissue-mimicking intravesical urine volume measurement phantoms (Kyoto Kagaku Co. Ltd., Kyoto, Japan). One phantom mimics a urinary retention condition in which the bladder is full of urine, while the other phantom mimics a bladder filled with 150 ml urine. B-mode images for the two phantoms were obtained by transmitting steered plane waves at 13 angles ranging from -30 degree to 30 degree and receiving the resulting echoes with one of the 32 elements, as shown in Figure 5.22. The resulting images clearly show the bladder region and are in good agreement with the reference images provided in the phantom manual [43], demonstrating the feasibility of using the fabricated patch for bladder-volume monitoring.

5.5 Conclusion

This paper has presented a reconfigurable transceiver ASIC which can interface 16- to 64-element transducer arrays for wearable ultrasound body patches. It employs a channel-parallelizing scheme that groups multiple HV pulser and LNA channels in parallel to achieve different driving capabilities and noise performance, such that transducer arrays with different centre frequencies and impedance levels can be interfaced. Reconfigurable digitization based on a flexible boxcar sampling network and a charge-sharing SAR ADC has been proposed to digitize receive channels with different bandwidths. The effectiveness of these techniques has been evaluated using several prototypes. Electrical characterization of the ASIC shows the expected bandwidth enhancement and noise reduction through channel-parallelizing. Acoustic measurements show the capability of the proposed ASIC to

interface with both LF and HF CMUT arrays. A prototype wearable ultrasound patch for bladder volume monitoring has been fabricated and demonstrated.

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CHAPTER 6

CONCLUSIONS

6.1 Main Contributions

- Proposed an HV pulser topology with embedded T/R switching functionality, reducing the required number of area-consuming HV transistors (Chapter 2).

  By embedding the T/R switch into the HV pulser, the number of required HV transistors is reduced. Besides, a compact back-to-back bi-directional isolation scheme is implemented with only 1 HV transistor, achieving further die area reduction.

- Proposed an LNA topology with embedded continuous time-gain compensation functionality (Chapter 3).

  An LNA topology with continuously variable gain to compensate for the time-dependent attenuation of the received echo signal has been proposed. Employing a capacitive ladder feedback network and a current-steering circuit, the LNA achieves a linear-in-dB gain range of 37 dB. In addition, a variable-gain loop amplifier based on current-reuse stages maintains constant bandwidth in a power-efficient manner. It achieves a gain error below ±1dB and a 1.7pA/√Hz noise floor and consumes 5.2mW from a ±0.9V supply.

- Implemented an ASIC for an ICE probe with pitch-matched element-level transceivers (Chapter 2, Chapter 3).

  The HV pulser presented in Chapter 3 and LNA presented in Chapter 4 have been integrated into a 205 µm-pitch matched layout for a 64-element 2-D ICE probe. The total area of the ASIC is 1.8 mm × 16.5 mm, which is suitable to be placed in a 9-Fr ICE catheter. The fabricated prototype, with the CMUT array and the ASIC flip-

chip bonded on top of a flexible PCB, has been evaluated acoustically with a tissue-mimicking phantom.

- Demonstrated that digitization is possible within the size and power constraints of an IVUS probe (Chapter 4).

  We have successfully demonstrated a front-end ASIC for a forward-looking IVUS probe. The ASIC consumes only 9 mW and includes a 10-bit 60-MS/s SAR ADC as well as an AFE and HV switches within a 1.5-mm diameter circular die area.

- Implemented an ASIC requiring only 4 cables to interface with a transducer array of 16 TX and 64 RX elements (Chapter 4).

  To interface with a 2-D transducer array and minimize cable usage, an ASIC that requires only 4 cables has been proposed and successfully demonstrated. The ASIC employs a multi-functional mixed-voltage command scheme that merges power supply, clock, and data on a single cable. Moreover, load-modulation-based data transmission is applied to transfer the digitized echo signal to the imaging system, and HV multiplexing to perform synthetic-aperture imaging.

- Proposed a method to make an ultrasound transceiver reconfigurable to allow it to interface with different transducers and serve different applications (Chapter 5).

  By dynamically parallelizing transceiver channels, different transducer elements with different center frequencies and capacitances can be driven. To flexibly digitize the echo signal, a reconfigurable sampling network has been proposed, allowing one ADC to digitize multiple channels and echo signals from different transducer elements.

- Implementation of a reconfigurable ASIC for a wearable ultrasound patch (Chapter 5)

  A prototype ASIC has been implemented in TSMC 180nm HV BCD technology for a wearable ultrasound patch. The ASIC contains 64reconfigurable transceiver channels that can interface with different transducer elements with the parasitic capacitance and center frequency ranging from 2 MHz to 8 MHz and 20 pF to 120 pF. A wearable ultrasound patch prototype with ASICs, transducer array, and

periphery building blocks integrated on top of a flexible PCB has been built and evaluated acoustically with a bladder phantom.

6.2 General Conclusions

- The use of separate transducers for TX and RX avoids the need for T/R switches and allows the TX circuity and RX circuity to be optimized independently, leading to a more power and area-efficient design. Therefore, this is an important option to consider, provided that the resulting separate TX and RX apertures are acceptable from an imaging perspective.
- The design and simulation of ASICs for miniature ultrasound devices, such as ultrasound catheters and patches, should consider the effects of supply and interconnect non-idealities because of the limited space for decoupling-capacitor placement and solid power routing. For instance, a simulation test bench for the ASIC should include the inductance associated with the supply connections by identifying the current return loops and then estimating their inductance.
- Considering the limited area, stringent power budget, and the limited number of cables of a catheter-based probe, the challenge in implementing on-chip digitization is not only in designing an energy-efficient ADC, but also in designing auxiliary building blocks, e.g., an ADC driver, a reference buffer, and clock distribution. Besides, for a massively parallel ADC array, energy-efficient datalinks, proper power supply, and clock distribution are more crucial than the ADC design.
- Channel multiplexing is the simplest way to reduce cable count, but it also reduces the achievable frame rate.
- The fact that the bandwidth of a typical micro-coaxial cable used in ultrasound probes exceeds that needed by a single RX channel can be exploited to reduce cable count.
- An ASIC that is integrated closely with the transducer array can help to match the transducer impedance, enhancing the SNR and thus imaging quality.

- A reconfigurable ASIC with ultrasound transceivers capable of interfacing with different transducers can be applied in multiple imaging applications, paving the way towards a platform technology for wearable ultrasound patches.
- A wearable ultrasound patch includes an ASIC and other peripheral building blocks. To achieve overall optimal energy efficiency, an energy-aware application-specific system architecture is necessary.

6.3 Future Work

- HV pulser for better imaging quality

  Chapter 3 has demonstrated a bipolar HV pulser with programmable frequency and number of pulses for a catheter-based probe. More programmability can be integrated to facilitate various imaging enhancing techniques. For instance, the pulse amplitude can be made tuneable for the transmit aperture apodization to reduce sidelobes [1]. To enable tissue harmonic imaging, the HD2 of the pulse should be minimized [2], which requires a pulser with a balanced rising edge and falling edge. The ultimate target is to build a highly programmable and digitally controlled smart HV pulser for catheter-based probes that provides the maximum degree of freedom for the imaging system.

- Co-optimization of ultrasound ASICs and imaging algorithms

  The link between the performance of an ultrasound ASIC (HV pulse amplitude, NF, bandwidth, gain of the AFE, etc.) and the final image quality (frame rate, resolution) is difficult to identify. However, this link can be evaluated through simulations by implementing an ASIC behavioural model and then combining it with an ultrasound simulation program, for instance, Field II [3, 4], the k-Wave toolbox [5], etc. The trade-offs associated with the design choices in the ASIC and the imaging algorithm can thus be directly evaluated from simulated images, making it possible to arrive at optimal choices in a more systematic way.

- Further exploring the reconfigurability of ultrasound ASICs

  Nowadays, to evaluate ultrasound imaging algorithms, transducer array configurations, transducer characterization, etc., research imaging systems, such as the Verasonics imaging systems [6] or the ULA-OP system [7], are usually applied to interface with the transducer array. However, the cable loading effects in such a

configuration introduces non-idealities in the signal chain, especially for CMUT arrays. Besides, for 2-D transducer arrays with a small element pitch, the cable loading effect is severer, and it is challenging to fan out all the elements with sufficiently low crosstalk and routing mismatch. Having a reconfigurable ASIC architecture that can be closely integrated with a 1-D or 2-D transducer array and that provides amplified analog or even digitized output signals would be beneficial. It would allow the imaging system to access each transducer element with minimized cable loading effects such that various imaging algorithms and array configurations can be accurately evaluated.

- Advanced packaging solutions for ultrasound ASICs

Since ultrasound ASICs need to excite the ultrasound transducer with high-voltage (tens of Volts) pulses, a high-voltage process is needed, which currently limits the feature size to 90 nm or larger. However, the deep sub-micron CMOS process is more favourable for the implementation of ADCs and advanced digital beamforming techniques. Advanced packaging solutions provided by foundries allow multiple dies to be integrated on top of each other. One possible scenario is that CMUTs or PMUTs are integrated on top of a HV transceiver die, either monolithically or by means of die-to-die bonding, while another die includes high-performance ADCs and advanced DSP units. The two dies can be stacked vertically using through-silicon-vias (TSVs) [8], thus boosting the integration density and reducing the form factor.

- System-on-chip (SoC) for wearable ultrasound patch

A wearable ultrasound patch is directly powered from a battery and wirelessly communicates with mobile devices. A customized SoC with an integrated power management unit tailored for ultrasound applications, a digital post-processing unit (e.g., beamforming and/or envelop detection) to reduce the overall data rate, and a Bluetooth Low Energy unit to transfer the processed data would be beneficial to achieve optimized energy efficiency and minimized form factor.

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SUMMARY

This thesis describes the design, prototyping and experimental evaluation of transceiver ASICs (application-specific integrated circuits) for catheter-based ultrasound probes and wearable ultrasound patches.

Chapter 1 introduces the motivation of this thesis work and the background of the targeted applications. Catheter-based ultrasound probes, including intra-cardiac echocardiography (ICE) probes and probes for intravascular ultrasound (IVUS), are conventionally implemented by connecting a transducer array at the tip of the catheter through a bundle of micro-coaxial cables, leading to signal attenuation and distortion. Besides, the number of elements in a 1-D or 2-D transducer array may exceed the number of cables that can be accommodated in the catheter shaft, calling for solutions to reduce the cable count. Integrating ASICs close to the transducer array at the catheter tip is promising to address these issues. However, the small diameter of the catheters brings challenges to the design of the ASICs. This chapter reviews these challenges and the state-of-the-art of the associated solutions. In addition, wearable ultrasound patches (WUPs) are also reviewed. A WUP that is intended to operate for several days on the surface of the human body should meet several requirements: it should be comfortable, conformal, energy-efficient and wireless. To date, research efforts have been focused on the design of comfortable and conformal transducer arrays, while challenges in designing energy-efficient interface electronics have not been addressed. As for catheter-based probes, ASICs can provide a suitable solution to realize the electronics of WUPs.

To reduce the loading effect of micro-coaxial cables in an ICE probe based on capacitive micro-machined ultrasound transducers (CMUTs), an ASIC prototype including element-level high-voltage (HV) pulsers and low-noise transimpedance amplifiers (TIAs) has been implemented. The design of the HV pulser is described in **Chapter 2**. The ASIC is equipped with programmable HV pulsers that can generate ±30-V return-to-zero (RZ) and non-RZ pulses. The pulsers employ a compact back-to-back isolating HV switch topology that employs HV floating-gate drivers with only one HV MOS transistor each. Further die-size reduction is achieved by using the RZ switches also as the transmit/receive (T/R) needed to pass received echo signals to low-voltage receive circuitry. On-chip digital logic clocked at

200 MHz allows the pulse timing to be programmed with a resolution of 5 ns, while supporting pulses of 1 cycle up to 63 cycles. Each pulser with embedded T/R switch and digital logic occupies only 0.167 mm2. The pulser successfully drives an 18-pF transducer capacitance at pulse frequencies up to 9 MHz, which is suitable for ICE applications.

The low-noise TIA in the ASIC prototype for a CMUT-based ICE probe is described in **Chapter 3**. Apart from the low-noise amplification, the proposed design provides continuously variable gain to compensate for the time-dependent attenuation of the received echo signal. This time-gain compensation (TGC) compresses the echo-signal dynamic range (DR) while avoiding imaging artifacts associated with discrete gain steps. Embedding the TGC function in the TIA reduces the output DR, saving power compared to prior solutions that apply TGC after the low-noise amplifier. The TIA employs a capacitive ladder feedback network and a current-steering circuit to obtain a linear-in-dB gain range of 37 dB. A variable-gain loop amplifier based on current-reuse stages maintains constant bandwidth in a power-efficient manner. Together with the HV pulser described in Chapter 2, the chip has been implemented in 0.18-μm HV Bipolar-CMOS-DMOS (BCD) technology and occupies an area of 1.8 mm × 16.5 mm, suitable for integration into an 8-F catheter. The prototype has been evaluated successfully with a 7.5 MHz 64-element CMUT array, with B-mode images of a tissue-mimicking phantom showing the benefits of the TGC scheme.

Besides reducing the loading effect from micro-coaxial cables, ASICs play an important role in achieving cable-count reduction, which is crucial for 3-D imaging catheters, such as forward-looking IVUS probes. In **Chapter 4**, circuit techniques are proposed to implement a prototype ASIC which only requires 4 cables to interface with a 2D piezoelectric transducer array. The ASIC is intended to be mounted at the tip of a catheter and has a circular active area with a diameter of 1.5 mm on top of which the 2-D 13-MHz transducer array with 64 receive (RX) elements and 16 transmit (TX) elements is integrated. The TX elements are connected to HV pulses generated by the imaging system using compact HV switch circuits. The received echo signals from RX elements are locally multiplexed, amplified, digitized and then transferred to the system using an energy-efficient load-modulation datalink. A multi-functional command line provides the required sampling clock, configuration data, and supply voltage for the HV switches. The ASIC has been realized in a 0.18-μm HV BCD technology and consumes only 9.1 mW. Acoustical measurements demonstrate the 3-D imaging capability of the prototype IVUS probe.

To address the challenges in interface electronics for WUPs, a prototype ASIC is presented in **Chapter 5**. The ASIC contains 64 reconfigurable transceiver channels that can interface with different transducer elements by employing channel-parallelizing techniques. Each transceiver channel is designed to drive a high-frequency (HF) CMUT element with small capacitance. To drive a low-frequency (LF) CMUT element with relatively large capacitance, multiple transceiver channels are parallelized to achieve a higher driving capability and lower input-referred noise. The received echo signals are digitized by four 10-bit SAR ADC. A

flexible boxcar-based sampling network allows each ADC to digitize multiple low-bandwidth receive channels or a single high-bandwidth receive channel. A parallel digital data interface is used to off-load the output data of the four ADCs to an FPGA. The ASIC has been realized in a 0.18-μm HV BCD technology. Acoustical measurements demonstrate the capability of the ASIC to interface with both the LF and HF transducer array.

Finally**, Chapter 6** summarizes the original contributions and conclusions of the thesis work. Recommendations for future work are presented, including: 1) HV pulser design for better imaging quality; 2) co-optimization of ultrasound ASICs and imaging algorithms; 3) further exploration of the reconfigurability of ultrasound ASICs; 4) advanced packaging solutions for ultrasound ASICs; 5) systems-on-chip (SoCs) for wearable ultrasound patches.

SAMENVATTING

Dit proefschrift beschrijft het ontwerp, de prototypen en experimentele evaluatie van een zend- en ontvangst ASIC (Applicatie-Specifiek Geïntegreerd Circuit) voor op katheter-gebaseerde ultrasone sondes en draagbare ultrageluid pleisters.

Hoofdstuk 1 introduceert de motivatie voor dit proefschrift en de achtergrond van de beoogde applicaties. Ultrasone sondes gebaseerd op katheters, waaronder intra-cardiale echocardiografie (ICE) sondes en sondes voor intravasculair ultrageluid (IVUS), worden conventioneel geïmplementeerd door een array transducent te verbinden met de kathetertip door middel van een bundel micro-coaxiale kabels. Deze kabels leiden tot verzwakking en vervorming van het signaal. Daarnaast kan het aantal kabels dat nodig is voor een 1-D of 2-D array transducent te groot zijn om in de schacht van een katheter te passen. Dit vraagt om oplossingen die het aantal kabels reduceren. Een veelbelovende oplossing is het integreren van ASIC's dicht bij de kathetertip. De smalle diameter van de katheters brengt echter ook uitdagingen voor het ontwerp van de ASIC's met zich mee. Dit hoofdstuk bespreekt deze uitdagingen en de state-of-the-art van de bijbehorende oplossingen. Daarnaast worden ook draagbare ultrageluid pleisters (WUP's) besproken. Een WUP die bedoeld is om meerdere dagen te werken op het menselijk lichaam moet aan verschillende vereisten voldoen: het moet comfortabel zijn, conformeren, energie-efficiënt en draadloos. Tot op heden heeft onderzoek zich vooral gericht op het ontwerp van comfortabele en conformerende array transducenten, terwijl de uitdagingen in het ontwerpen van energie-efficiënte interfaces nog niet bekeken zijn. In het geval van sondes gebaseerd op katheters kunnen ASIC's een passende oplossing bieden voor de elektronica van WUP's.

Om het belastende effect van een micro-coaxiale kabel in een ICE-sonde die gebaseerd is op micro-gefabriceerde ultrasone transducenten (CMUT's) te verminderen, werd een prototype ASIC geïmplementeerd met daarop hoogspannings-pulsers en transimpedantie versterkers (TIA's) met een laag ruisniveau. Het ontwerp van de hoogspannings-pulser wordt beschreven in **hoofdstuk 2**. De ASIC is uitgerust met programmeerbare HV pulsers die return-to-zero (RZ) en niet return-to-zero pulsen kunnen genereren. De pulsers maken gebruik van een compacte HV-schakelaar back-to-back topologie met HV zwevende-gate aansturing met elk maar één HV MOS transistor. Verdere oppervlakte vermindering wordt bereikt door de RZ-schakelaars ook te gebruiken als zendt/ontvangst (T/R) schakelaars, die nodig zijn om de ontvangen signalen over te brengen naar de laagspannings-ontvangstcircuits. Digitale logica op de chip, geklokt op 200 MHz, zorgt ervoor dat de pulstiming met een resolutie van 5 ns te programmeren is terwijl tegelijkertijd pulsen van 1 cyclus tot 63 cycli lang ondersteund

worden. Elke pulser met ingebouwde T/R schakelaar en digitale logica heeft een oppervlakte van maar 0.167 mm2. De pulser stuurt succesvol transducenten met een 18 pF capaciteit aan op pulsfrequenties tot 9 MHz, wat geschikt is voor ICE-applicaties.

De ruisarme TIA in het ASIC-prototype voor een ICE-sonde gebaseerd op CMUTs wordt beschreven in **hoofdstuk 3**. Naast de ruisarme versterking, biedt het gepresenteerde ontwerp continue variabele versterking om te compenseren voor de tijdsafhankelijke verzwakking van het ontvangen echosignaal. De tijd-versterking compensatie (TGC) comprimeert het dynamisch bereik (DR) van de echosignalen maar voorkomt de beeldartefacten die verbonden zijn met discrete versterkingsstappen. Door de functionaliteit van de TGC in de TIA onder te brengen wordt het DR van de output gereduceerd, wat vermogen bespaard ten opzichte van eerdere oplossingen waarbij de TGC na de ruisarme versterker wordt toegepast. De TIA maakt gebruik van een capacitief ladder feedbacknetwerk en een stroomsturingscircuit om een lineair-in-dB bereik van 37dB te verkrijgen. Een lusversterker met variabele versterking gebaseerd op stroom hergebruikende fasen zorgt voor een contante bandbreedte op een vermogens-efficiënte manier. De chip is samen met de HV pulser beschreven in hoofdstuk 2 geïmplementeerd in een 0.18-μm HV Bipolar-CMOS-DMOS (BCD) technologie en neemt een actieve oppervlakte in beslag van 1.8 mm × 16.5 mm, geschikt voor integratie in een 8-French katheter. Het prototype is succesvol geëvalueerd met een 7.5 MHz CMUT array met 64 elementen, waarbij B-mode beelden van een weefsel-nabootsende fantoom de voordelen laten zien van het TGC ontwerp.

Naast het reduceren van de belasting die micro-coaxiale kabels vormen, spelen ASIC's een belangrijke rol in het reduceren van het aantal kabels, wat cruciaal is voor 3-D beeldvormede sondes, zoals vooruitkijkende IVUS-sondes. In **hoofdstuk 4** worden circuit technieken gepresenteerd voor een prototype ASIC die het mogelijk maken met maar 4 kabels een 2D piëzo-elektrische array transducent aan te sluiten. De ASIC is bedoeld om op de tip van een katheter gemonteerd te worden en heeft een cirkelvormige actieve oppervlakte met een diameter van 1.5 mm, waar bovenop een 2-D 13-MHz array transducent met 64 ontvangst (RX) en 16 transmit (TX) elementen geïntegreerd zijn. De TX-elementen worden verbonden met HV-signalen die gegenereerd worden door een beeldvormingssysteem door middel van compacte HV-schakelcircuits. De ontvangen echosignalen van de RX-elementen worden lokaal gemultiplext, versterkt en gedigitaliseerd, en vervolgens overgedragen aan het beeldvormingssysteem met een energie-efficiënte belastings-modulerende datalink. Een multifunctionele commando-kabel voorziet de chip van de benodigde bemonsteringsklok, configuratie data en voedingsspanning voor de HV-schakelaars. De ASIC is gerealiseerd in een 0.18-μm HV BCD technologie en verbruikt maar 9.1 mW. Akoestische metingen demonstreren het vermogen van het prototype IVUS-sonde om 3-D beelden te maken.

Om de uitdagingen in interface elektronica in WUPs aan te pakken, wordt een prototype ASIC gepresenteerd in **hoofdstuk 5**. De ASIC bevat 64 her configureerbare zendontvangst kanalen die kunnen koppelen met verschillende transducenten door kanaal-parallelliserende

technieken te gebruiken. Elk zendontvangst kanaal is ontworpen om een hoogfrequent (HF) CMUT-element met een kleine capaciteit aan te sturen. Om een laagfrequent (LF) CMUT-element met een relatief grote capaciteit aan te sturen kunnen meerdere zendontvangstkanalen parallel worden gebruikt voor een sterker aansturingsvermogen lagere input-gerefereerd ruis. De ontvangen echosignalen worden gedigitaliseerd door een 10-bit SAR ADC. Een flexibel op boxcar gebaseerd bemonsteringsnetwerk zorgt ervoor dat elke ADC meerdere kanalen met lage bandbreedte of een enkel ontvangstkanaal met hoge bandbreedte kan digitaliseren. Een parallelle digitale data interface wordt gebruikt om de data van vier ADC's over te brengen naar een FPGA. De ASIC is gerealiseerd in een 0.18-μm hoogspanning BCD-technologie. Akoestische metingen demonstreren het vermogen van de ASIC om te werken met zowel LF als HF array transducenten. Tot slot geeft **hoofdstuk 6** een samenvatting van de wetenschappelijke bijdragen en conclusies van dit proefschrift. Verder worden er aanbevelingen gedaan voor toekomstig werk, waaronder: 1) een hoogspannings pulser ontwerp voor betere beeldkwaliteit; 2) het tegelijk optimaliseren van ultrageluid ASIC's en beeldvormingsalgoritmes; 3) verdere verkenning van de herconfigureerbaarheid van ultrageluid ASIC's; 4) geavanceerde behuizingsoplossingen voor ultrageluid ASIC's; 5) Systemen-op-chip (SoC) voor draagbare ultrageluid pleisters.

List of Abbreviations

2-D	Two-Dimensional
3-D	Three-Dimensional
ADC	Analog-to-Digital Converter
AFE	Analog Front-End
ASIC	Application-Specific Integrated Circuits
AWG	Arbitrary Waveform Generator
BCD	Bipolar-CMOS-DMOS
BER	Bit-Error-Rate
BLE	Bluetooth Low Energy
BUF	Buffer
BVD	Butterworth-Van-Dyke
BW	Bandwidth
CA	Current Amplifier
CD	Cable Driver
CDAC	Capacitor Digital-to-Analog Converter
CMFB	Common-Mode Feedback
CMOS	Complementary Metal-Oxide-Semiconductor
CMUT	Capacitive Micromachined Ultrasound Transducers
CTO	Chronic Total Occlusion
CVD	Cardiovascular Diseases
DAC	Digital-to-Analog converter
DLL	Delay-Locked Loop
DMOS	Double-diffused MOS
DR	Dynamic Range
DSP	Digital Signal Processing
ECG	Electrocardiography
FDSOI	Fully Depleted Silicon on Insulator

FL	Forward-Looking
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
GBW	Gain-Bandwidth product
HD	Harmonic Distortion
HF	High-Frequency
HV	High-Voltage
IC	Integrated Circuits
ICE	Intracardiac Echocardiography
IIR	Infinite Impulse Response
IVUS	Intravascular Ultrasound
LBSR	Loop-back Shift Register
LF	Low-Frequency
LNA	Low-Noise Amplifier
LSB	Least-Significant Bit
LUT	Look-Up Table
LV	Low-Voltage
LVDS	Low-Voltage Differential Signaling
MRI	Magnetic Resonance Imaging
NDE	Non-destructive Evaluation
NEF	Noise-Efficiency Factor
NF	Noise Figure
NRZ	Non-Return-to-Zero
OTA	Operational Transconductance Amplifier
PA	Power Amplifier
PCB	Printed Circuit Board
PDMS	Polydimethylsiloxane
PGA	Programmable Gain Amplifier
PLL	Phase-locked Loop
PMU	Power Management Unit
PMUT	Piezoelectrical Micro-machined Ultrasound Transducer
PPG	Photoplethysmography
PRF	Pulse Repetition Frequency
PRNG	Pseudo-Random Number Generator
PVDF	Polyvinylidene Fluoride

PVT	Process/Voltage/ Temperature
PWM	Pulse Width Modulation
PZT	Lead zirconate titanate
SAR	Successive Approximation Register
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
TEE	Transoesophageal Echocardiography
TGC	Time-Gain Compensation
TIA	Trans-Impedance Amplifiers
TR	Transmit/Receive
TSV	Through-Silicon-Vias
TTE	Transthoracic Echocardiography
TX	Transmit
US	Ultrasound

LIST OF PUBLICATIONS

Journal Articles

M. Tan, E. Kang, J. S. An, Z. Y. Chang, P. Vince, T. Mateo, N. Senegond, and M. A. P. Pertijs "A 64-channel transmit beamformer with ±30-V bipolar high-voltage pulsers for catheter-based ultrasound probes," *IEEE J. Solid-State Circuits*, vol. 55, no. 7, pp. 1796–1806, 2020.

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M. Tan, E. Kang, J. An, Z. Chang, P. Vince, T. Matéo, N. Sénégond, and M. A. P. Pertijs, "An Integrated Programmable High-Voltage Bipolar Pulser with Embedded Transmit/Receive Switch for Miniature Ultrasound Probes," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 9, pp. 79-82, Sept. 2019.

M. Tan, C. Chen, Z. Chen, J. Janjic, V. Daeichin, Z.-Y. Chang, E. Noothout, G. van Soest, M. D. Verweij, N. de Jong and M.A.P. Pertijs, "A Front-End ASIC with High-Voltage Transmit Switching and Receive Digitization for 3D Forward-Looking Intravascular Ultrasound Imaging", *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2284-2297, Aug. 2018.

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M. Tan *et al.*, "A 16- to 64-Channel Low-Power Reconfigurable Transceiver ASIC for CMUT-based Wearable Ultrasound Patches", in preparation for submission.

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