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DOI
10.1016/j.microrel.2022.114830

Publication date
2022

Document Version
Final published version

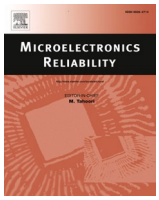
Published in
Microelectronics Reliability

Microelectronics Reliability 139 (2022) 114830

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel



Review paper

Board level vibration test method of components for automotive electronics: State-of-the-art approaches and challenges

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ARTICLE INFO

Keywords:
JEDEC standards
Board level reliability
Board level vibration test
PCB dynamic response
Wafer level chip scale packages
Ball grid array packages

ABSTRACT

Board level vibration testing is intended to assess prediction of the reliability of solder joint interconnects that are formed between electronic components and printed circuit boards (PCB). Frailties in the stress test experiment might lead to false board level reliability (BLR) evaluations. Therefore, it is essential to have a well-characterized board level vibration test method. Currently, there is no industrial test standard that prescribes board level vibration test method for electronic components at the PCB level. This paper examines the vibration test standards that are currently available in the industry and their applicability at the solder joint interconnect level. Next to that, it surveys the state-of-the-art board level vibration test setups and their impact on PCB dynamic loading and reliability at solder joint-PCB interface. It collates research on major building blocks of a board level vibration test method that includes vibration measurement techniques, PCB assemblies under test, board mounting schemes, operating environments, fault detection systems, and vibration test stress conditions that are currently used in the domain of solder joint level vibration testing. The findings from this paper are expected to reveal pitfalls and challenges while setting up board level vibration test experiments for electronic components. In addition, this paper attempts to identify research efforts that are required to make board level vibration testing a more credible means for assessing solder joint reliability. Outcomes from this study can further be used to guide future board level vibration specifications for electronic components.

1. Introduction

With the continuous expansion of electronic equipment in innovative application areas, reliability solutions are going beyond electronic circuitry and package level. Electronic components are mostly mounted on printed circuit boards (PCB) to realize final functionality. These boards can incorporate additional stresses onto components that are placed on them.

Therefore, it is pivotal to assess the interaction of PCB and the electronic packages under test. Usually, board level reliability testing is employed to characterize the mechanical and thermo-mechanical robustness of solder attachments that are formed in between electronic components and PCBs. It is also called second level reliability in the [1]. Several reliability levels are depicted in Fig. 1.

The solder joint attachments in automotive applications are prone to experience mechanical vibrations at various frequencies and temperatures. It can result in another failure mode than the failures generated solely by abrupt mechanical shocks. Such vibration events can transfer the energy to the PCB assemblies via board supports and cause electrical faults in the PCB assemblies mounted inside the housing. Therefore, the reliability of electronic components is assessed by using the board level vibration tests.

A typical experimental test setup of a board level vibration test is shown in Fig. 2. A well-implemented PCB level vibration test methodology should comprise of the following experimental test setup related elements: (i) Vibration measurement sensors (such as accelerometers), (ii) standardized test board (PCB), (iii) controlled vibration test load parameters (e.g. stress profile, etc.), (iv) electrical fault monitoring techniques, (v) test environmental conditions (Fig. 3).

To design a sturdy board level vibration test methodology, it is essential to understand the impact of each of these elements on the stability of the PCB dynamic response and the characteristic lifetime of

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https://doi.org/10.1016/j.microrel.2022.114830
Received 6 August 2022; Received in revised form 7 October 2022; Accepted 13 October 2022
Available online 25 October 2022

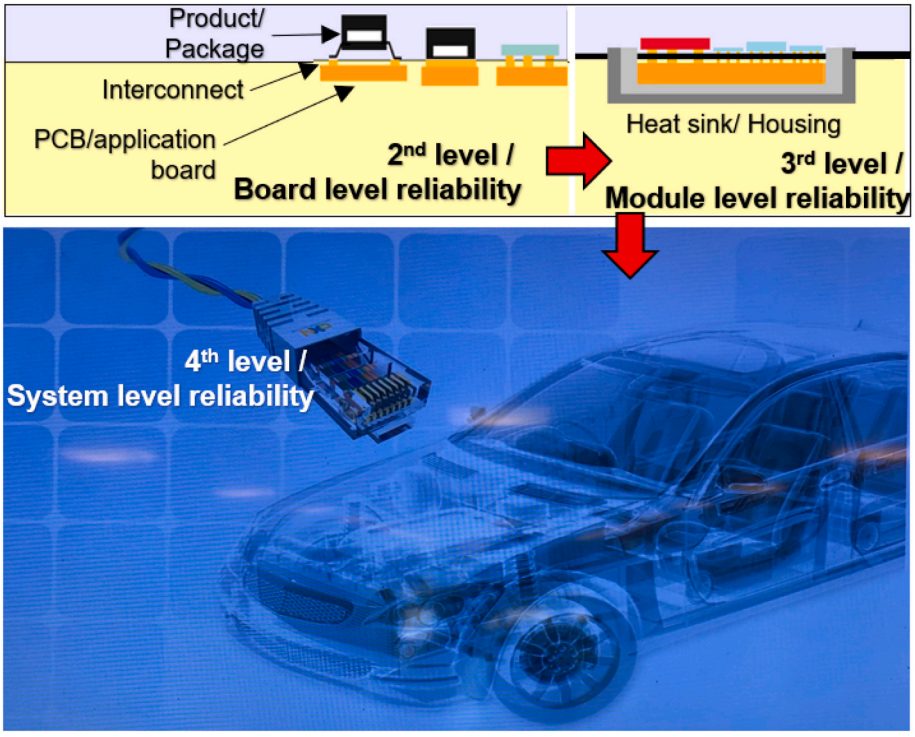

Fig. 1. Overview reliability levels: Board level reliability vs other reliability levels [1].

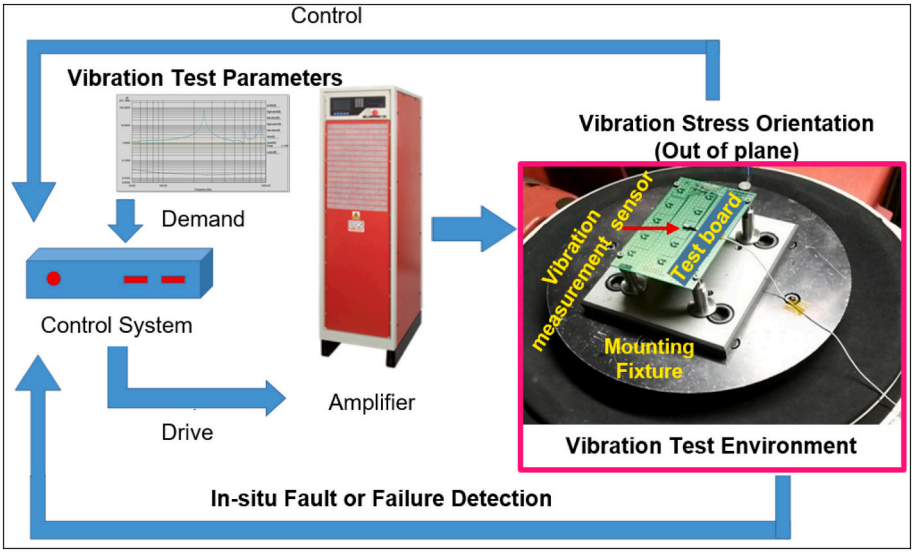

Fig. 2. Typical board level vibration test setup.

solder joints. Otherwise, unintended stress artifacts from the experimental test setup itself might overstress or under-stress components at the board level.

Presently, several papers, for example [2–7] can be found reporting board level vibration test results and PCB dynamic response results. In general, solder joint reliability is in the spotlight, and literature on the methodology and stability of the vibration test method itself is sparse. In [2,3], some of the test control settings linked to vibration testing, such as sweep rate and applied stress level are studied.

This paper aims to assess all test apparatus related domains (in Fig. 3) that define a rigorous and rugged board level vibration test procedure. These vibration testing conditions include PCB vibration measurement methods, board under test, board fixture schemes, board orientation, vibration energy levels, test environments, and electrical failure detection systems. This paper also highlights work revealing numerous pitfalls linked to the vibration test methodology and offers case studies representing good practices associated with board level vibration test analysis.

2. Board level vibration test theory

This section specifies the use of some simplified analytical relationships to enable an understanding of stresses experienced by solder joints during board level vibration testing. These stresses are well described by the vibration response of the board under test. It can be used as an indirect indication of stresses undergone by components at board level.

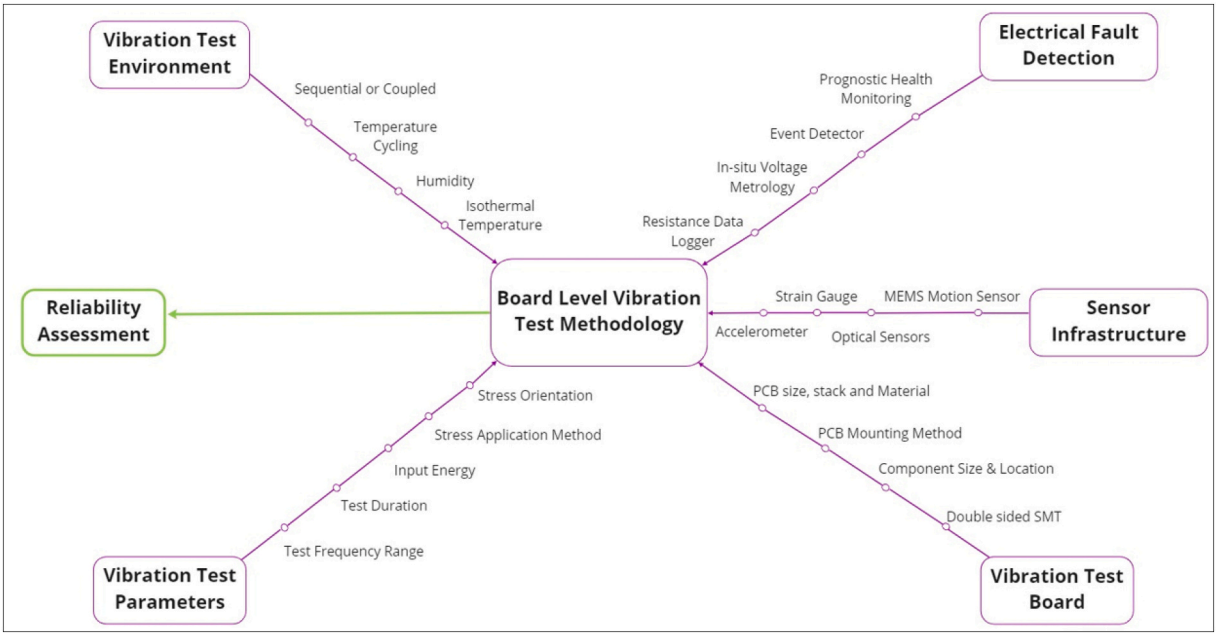

Fig. 3. Mind-map of a board level vibration test methodology.

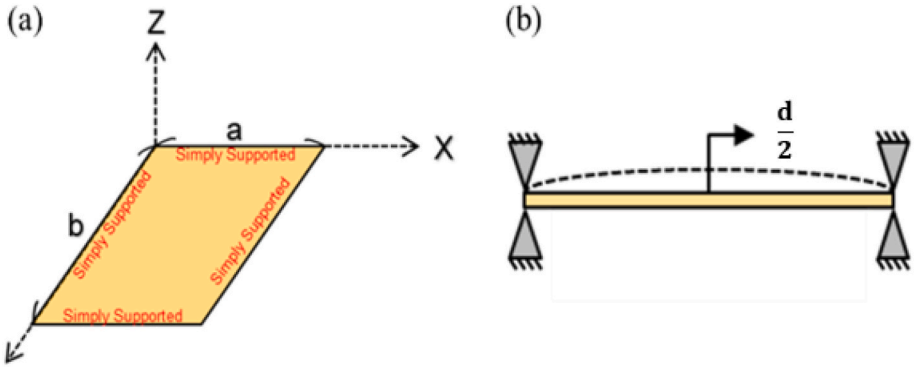

Fig. 4. Boundary condition assumption of PCB plate: (a) Top view (b) side view.

A board level vibration response of any PCB assembly consists of resonance frequency (f_0) and peak-peak displacement (d). According to Steinberg [8], the resonance frequency of a PCB can be expressed as follows:

$$f_0 = \lambda \left(\frac{1}{a^2}+\frac{1}{b^2}\right)\sqrt{\frac{Eh^3}{12\rho(1-\upsilon^3)}} \tag{1}$$

where, E is the Young's modulus of PCB, h is the board thickness, ρ and, υ refer to the metal density and Poisson's ratio respectively. λ is clamping constant, a and b represent length and width of the PCB respectively (as shown in Fig. 4).

Then, peak-peak displacement (d) at the center of the PCB during its first resonance state is defined by the following equation [9]:

$$d = \frac{a}{2\pi^2 f_0^2} \tag{2}$$

where, f_0 is the resonance frequency of the PCB, and, a is the peak acceleration measured during PCB resonance. In this equation, the motion of test board is assumed to be sinusoidal in time.

These equations can be further expressed in terms of the global PCB strains (ε). These equations are derived from classic beam theory, neglecting the effects due to the Poisson's ratio of a bent plate, or to the electronic packages.

$$\varepsilon = \frac{6hd}{2L^2} = \frac{3hd}{L^2} \tag{3}$$

where, L is the unsupported length of the PCB. Now, PCB strains can be linked to the stress (S) experienced by the test board system. It can be described as follows:

$$\varepsilon = \frac{S}{E} \tag{4}$$

where, E is the flexural modulus of a given PCB assembly. Once the stresses are known, the following relation [8] can be considered to estimate the fatigue life span of solder joints in application.

$$\frac{N_1}{N_2} = \left(\frac{S_2}{S_1}\right)^b \tag{5}$$

where, N is the number of stress cycles to produce a solder fatigue failure, and, b is the vibration fatigue exponent. N can also be extracted by the failure distribution generated from the board level vibration reliability tests. Whereas, b can be determined for solder joints by using the typical physical properties for solder alloys.

The stress (S) can also be directly linked to the strain, acceleration, or

Table 1
Overview of industrial vibration test standards.

Test standard	Scope description	Axes nr.	Test parameters (stress level, frequency range, test time)	Standardized board level vibration sensor?	Vibration test environment prescription?	Standard test board?
JESD22-B103-B [10]	Non-automotive	3	0.001–20G 0.0626–6.27 G_{rms} 20-2000 Hz 0.5 h/axes	No	No	No
IEC 60068-2-64 [11], IEC 60068-2-6 [12] (Spectrum A.3, IEC 60749) Category 1	Automobile chassis	3	3.38G_{rms} 10–1000 Hz 8–33 h/axes	No	No	No
IEC 60068-2-64 [11], Spectrum A.3 Category 2a,2b,2c	Automobile engine compartment, body	1	0.67–1.1G_{rms} 5–200 Hz 8–33 h	No	No	No
ISO 16750-3 [13] (4.1.2.4/5)	Automobile body, unsprung masses	3	2.71G_{rms} 10–1000 Hz 8 h/axes	No	Yes	No
MIL-STD-810G [14] & MIL-STD-883 [15] (MIL-E-5400,MIL-T-5422, Method 514.6)	Automobile wheels	3	1.4–2.24G_{rms} 5–500 Hz 2–33 h/axes	No	No	No
GMW 3172 [16] (9.3.1.1/2/3)	Automobile engine, transmission, sprung/unsprung	3	2–12.96G_{rms} 10–2000 Hz 16–44 h/axes	No	No	No
JEITA ED-4701/400 [17]	Non-automotive	3	20G 100–2000 Hz 0.8–96 h	No	No	No
JIS D 1601 [18]	Automobile parts	3	0.5–50G 33–400 Hz 8 h/axes	No	No	No

displacement of the PCB assembly. Furthermore, assuming electronic PCB assembly under test to be a linear system, the number of fatigue cycle can be directly linked to the time (T) [8].

$$\frac{T_1}{T_2} = \left(\frac{d_2}{d_1}\right)^b \tag{6}$$

$$\frac{T_1}{T_2} = \left(\frac{\varepsilon_2}{\varepsilon_1}\right)^b \tag{7}$$

$$\frac{T_1}{T_2} = \left(\frac{a_2}{a_1}\right)^b \tag{8}$$

Eq. (8) can also be considered for setting up a board level vibration qualification test for a given PCB assembly that are typically used in automotive applications. For example, suppose that T_2 is the vehicle operation time (T_2=T_{USER}) and ($a_2 = a_{USER}$) represents the peak acceleration measured in the automotive field test data. Then, the peak acceleration applied in the lab environment ($a_1 = a_{LAB}$) can be substituted in Eq. (8) to find the desired board level vibration test time period ($T_1 = T_{LAB}$).

3. Overview of vibration test standards in industry

Currently, there is no board level vibration test method in the semiconductor industry intended to assess and compare the vibration performance of electronic component technologies in an accelerated test environment, where the vibration of a circuit board causes product failure. It is ascribed to the fact that there is no standardized test board and test methodology to provide a reproducible reliability assessment while duplicating the failure modes that are observed during the product life cycle.

In spite of this, several international standards prescribing vibration testing of electronic equipment are available. These test specifications are commonly called qualification standards and are summarized in Table 1. However, these test specifications do not directly cover the board level test configuration that comprises a standardized test board.

Test specifications listed in Table 1 are typically framed to align technical discussions between supplier and customer on the number of failing units during qualification testing and their failure mechanisms. The most common frameworks in the electronics industry are as follows: (i) The Joint Electron Device Engineering Council (JEDEC), (ii) International Electrotechnical Commission (IEC), (iv) International Organization for Standardization (ISO), (v) Military Standards (MIL-STD), (vi) Japan Electronics and Information Technology Industries Association (JEITA), (vii) Institute of Printed Circuits (IPC).

Some of the above-mentioned test standards are the basis for other important test standards in the electrical and electronics industry, e.g. include, the Automotive Electronics Council (AEC), Japanese Industrial Standard (JIS), General Motor Worldwide (GMW). The JEDEC is known to stipulate test standards for the qualification of silicon integrated circuits. The JESD22-B103-B [4] is related to the vibration variable frequency and is typically intended for the evaluation of component(s) for use in electrical equipment. It is not suitable for components mounted on PCBs. Similarly, other specifications such as IEC, ISO, JEITA, and MIL do not directly cover the solder joint reliability risks of electronic components at the board level.

These test standards provide potential vibration test strategy and vibration load parameters such as stress orientation, sample size, test time, vibration stress type, level, and excitation frequencies. However, they do not necessarily intend to establish a baseline for potential investigative efforts in package-board interface technologies.

There is no consensus between these test specifications. For instance, several stress levels are prescribed for the same automotive application. Also, these test standards do not define some of the key building constituents of a board level vibration test. For instance, guidelines linked to the vibration characterization sensors, PCB type, board mounting arrangement during test execution, environmental conditions, and electrical failure detection equipment and criterion are not formalized in these test specifications. Hence, it is required to understand the impact of these building elements on the PCB vibration response and solder joint reliability performance of components.

4. Vibration measurement sensors

Resonance characterization of the test object is usually the first step in vibration testing. PCB vibration properties such as resonance

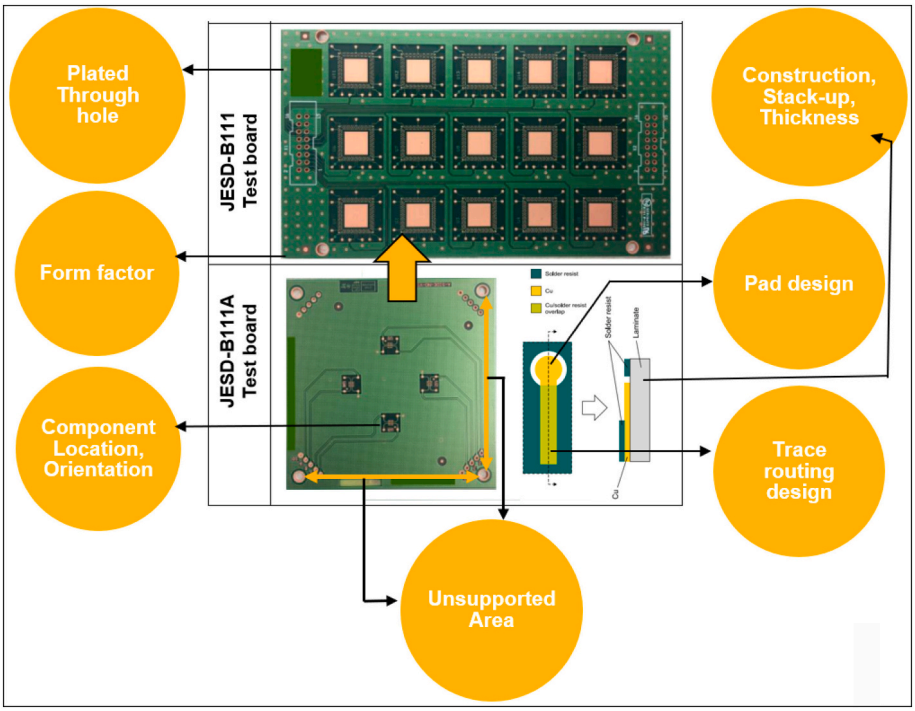

Fig. 5. Test board design related factors impacting board level vibration test results [37,38].

frequency, peak-peak displacement, relative displacement, and strains are known to influence the lifespan of solder joint interconnects [19]. Therefore, a good understanding of the PCB dynamic response is essential in predicting the board level vibration test performance of electronic components.

Transducers used for measuring the PCB vibration spectrum during board level vibration testing can be broadly categorized into two groups [19]: Contact-based measurement sensors and Contactless-based measurement sensors.

Contact-based measurement approach includes a large variety of sensors such as accelerometers [2], strain gauge [20], etc. On the other hand, contactless measurement sensors use optical sensor-based techniques such as LASER Doppler Vibrometer (LDV) [19], Digital Image Correlation (DIC) [21]. The following transducer characteristics are identified to be significant: (i) Signal measurement range, (ii) sensitivity for dynamic loads, (iii) transducer resonance, (iv) transducer mass, and (v) operational complexity.

In general, accelerometers are utilized to characterize the PCB vibration spectrum during board level vibration tests [2]. Standard piezoelectric accelerometer measurements offer a high measurement range, are cost-effective, and provide easy installation advantages that justify its wide usage. However, a piezoelectric accelerometer can perturb the dynamic response of a PCB [19]. Hence, it calls for considerations to standardize the vibration measurement setup that enables precise vibration recordings of the test board assembly.

[19] investigated accelerometer and LDV measurement techniques by carrying out controlled swept sine board-level vibration excitations for circuit board assemblies with different form factors and electronic component types. The results showed that LDV allows a more accurate measurement solution than the standard piezoelectric accelerometer used in that study.

Amongst others, the relative mass of an accelerometer used with respect to the weight of a moving PCB target is identified to be one of the major factors responsible for the alteration of the PCB dynamic motion which is verified by the Finite Element simulations [19]. A larger measurement deviation between the LDV and accelerometer is observed for boards containing smaller wafer level chip scale packages (WLCSP) than that of bigger ball grid array (BGA) type packages [19]. This advocates to use a contactless based measurement solution or employ lightweight accelerometers ($\leq$0.2 g), weighing comparable to that of a small WLCSP component.

Similarly, [2] showed a minor impact of using a miniature type, lightweight piezoelectric accelerometer (0.2 g). The accelerometer reduced the resonance frequency by 2 to 4 Hz, depending upon the PCB thickness. Hence, it shows a similar trend when compared to the results from [19]. Another recent study [20], observed deviations and shifts in the PCB dynamic motion that were tested at different labs. Such discrepancy is induced by the mass of the accelerometers used in this study.

Other than the conventional piezoelectric type accelerometers, commercially available MEMS IC-based accelerometers are also used in a few studies [22,23]. Such accelerometer is soldered onto a small PCB coupon with some surface mount components to realize their functionality. The coupon is usually mounted on the test board by applying epoxy resin adhesives. The impact of this accelerometer assembly on the tested PCB vibration motion is not discussed in these studies.

Another PCB vibration measurement approach is conducted by [24]. It also involves micro-electromechanical systems (MEMS) type accelerometers for monitoring board vibration motion. MEMS-based acceleration meter uses a capacitive sensing principle that produces a voltage that is dependent on the distance between two planar surfaces. However, such accelerometers require a microcontroller and other SMD components for further signal processing. Also, these components need to be soldered onto the test board surface and it is not preferred in some cases.

In [25,26], Lall et al. extracted PCB strains with a DIC method using high-speed cameras at 100,000 fps. The board is coated with a speckle pattern. A geometric point on this pattern is tracked before and after loading to calculate the PCB displacement and deformation. The experimentally obtained PCB resonance frequency is validated by the FEM results. A similar technique is used in [27,28].

Other studies such as [20] have used strain gauges to measure the PCB dynamic response during board level vibration testing. In [20], two triaxial-based strain gauge sensors are mounted to measure the peak

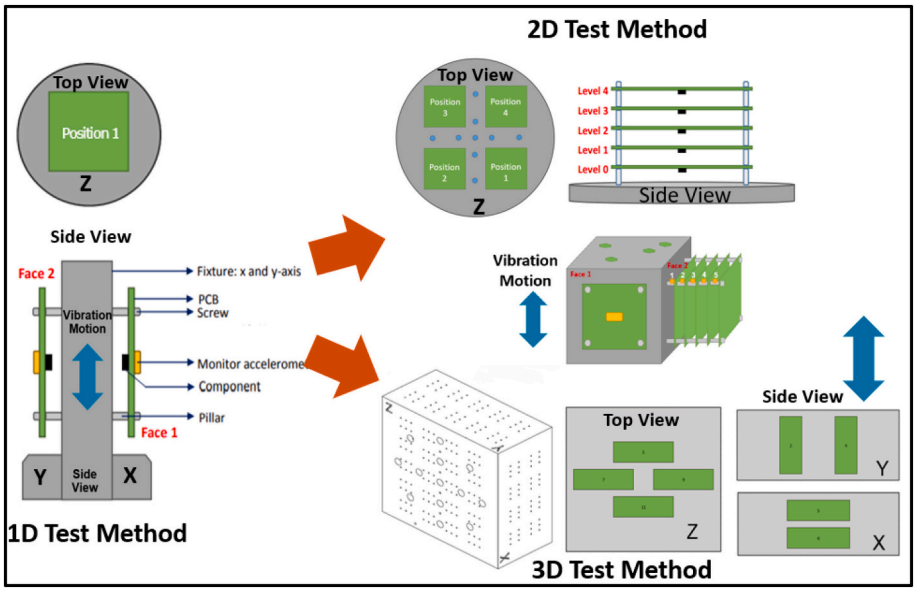

Fig. 6. Overview of PCB mounting strategies [22].

strain values. The measured peak strain values complement well with the FEM outcomes.

To conclude, it is evident that the industry is inundated with a large range of PCB vibration measurement sensors. There is a lack of standard on the PCB vibration measurement methodology. The impact of some of these measurement techniques is known to influence the solder joint lifespan. Hence, it is inflaming for the standardization of the board response measurement method.

5. Test board

The test board is an important ingredient of any board level vibration test method. Differential flexure between the component and circuit board during vibrations causes failure in the surface-mounted electronic components. Hence, it acts as the primary driver of the stress experienced by the solder joint interconnects during accelerated vibration testing.

Failures induced in a device under vibration test are a strong function of the PCB mounting strategy, and following test board design related factors (as depicted in Fig. 5): (i) Form factor, (ii) unsupported area, (iii) thickness, construction material & stack-up, (iv) pad design & surface finish, (v) component location and orientation, (vi) trace routing design, (vii) plated through hole and via in pad design, (viii) double-sided or Single-sided assembly. It advocates for standardization of the test board design. Consequently, it is important to start reviewing several test board designs found in the literature.

5.1. Test board designs

A pre-eminent board level vibration test methodology comparing the impact of both PCB form factor and material stack-up on the circuit board vibration characteristics is presented in [9]. It analyzed and benchmarked PCB board responses of the test board layouts described in the JESD-B111A [29] (square shaped) and JESD-B111 (rectangular shaped) Board Level Drop Test Method of Components for handheld products [30]. It is found that the resonance frequency of the JESD-B111A is greater than the JESD-B111 test board.

Similar results are observed by Thukral et al. [31] during board level drop testing [30]. In addition, the peak-peak displacement of the JESD-B111A is lower than the JESD-B111 type board design. Similar to [2], this study also showed changes in the PCB spectrum with minor changes in the PCB stack-up.

CALCE Research Center at the University of Maryland investigated the effect of PCB material on the solder interconnect reliability [32]. Results show that the stiff polyimide-based PCB assembly is more reliable when compared to the FR4 board assembly.

Next to that, the effect of package types, such as WLCSP and BGA packages, on the PCB vibration motion is also investigated. It shows that PCB design concerted with the package under test is key in determining the PCB vibration spectrum.

Study [2] on the JESD-B111 PCB assembly showed that the components located at the center of the board failed before the components placed at other locations on the board. This is linked to inhomogeneous stress experienced by these components. The components placed in the center of the PCB experience maximum flexure and strains at the solder interconnects.

Other than the JESD-B111A and JESD-B111 PCB types, customized PCB layouts sizing from 77 mm to 305 mm with thicknesses varying from 1 mm to 2 mm are also found in several other investigations [33–35]. It includes board designs that can contain 4 components and 1 component on the PCB to allow homogenous stress transfer to all stressed components on the board. 1 component test board design enables understanding of stress applied to the solder interconnects [36]. Investigations with 12, 7, and 5 component board layouts can also found in [37–39] respectively. These boards also induced solder cracks in PBGA type packages.

In [39], the study showed that the Non-Solder Mask Define (NSMD) type pad design outperforms the SMD type pad design. Uppalapati et al. [28] exposed the high sensitivity to the trace routing design underneath the component and plated through hole location.

Board level vibration testing is a statistical-based reliability approach. It implies that multiple samples are stressed and involve vibration testing of components on several PCB assemblies. Therefore, other than the test board design aspect, the consequences of testing one PCB to another PCB shall also be considered. Otherwise, boards might have different mechanical properties that induce distinctive stresses onto the component. This part is studied by Thukral et al. [36] and limited strain variation from PCB to PCB is reported.

5.2. PCB mounting strategy

The test board assembly under vibration test is rigidly fastened on

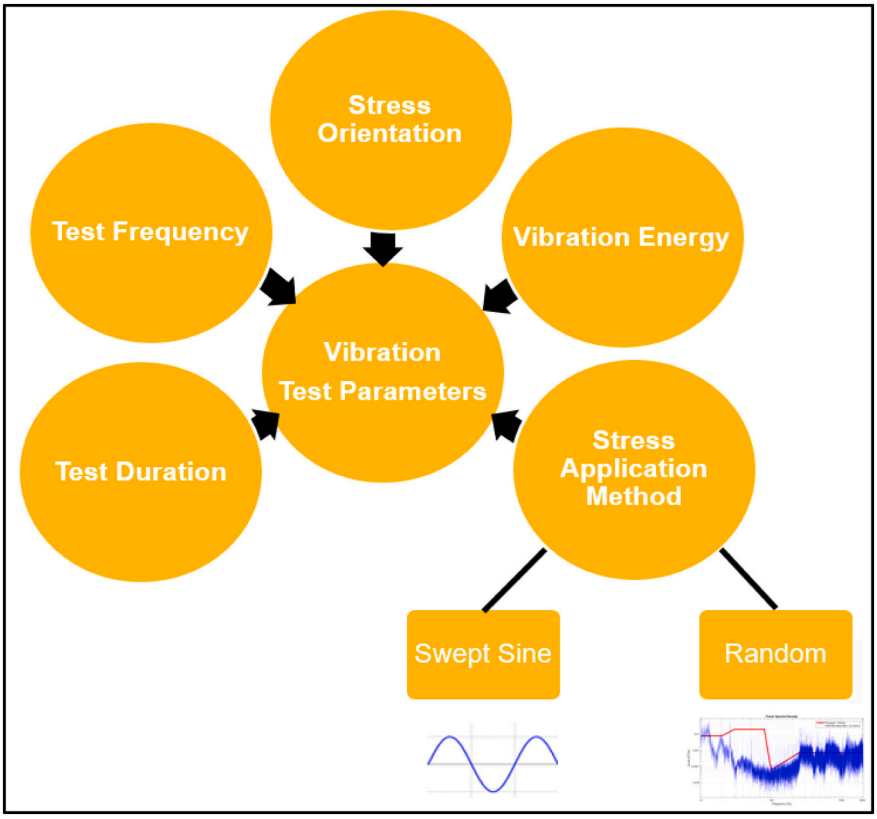

Fig. 7. Overview of vibration test parameters impacting board level vibration tests.

the vibration fixture platform in such a manner that electronic components receive the full-specified vibration energy level during vibration testing. Fig. 2 shows a typical vibration test apparatus. It contains a base vibration fixture plate that is designed to couple the motion from a vibration source to the test board assembly in an undistorted manner.

One such example of a vibration test fixture is reported in [36]. Vibration fixture characterization results showed no distortions at the multiple PCB mounting locations. It indicates that there is no relative movement between the vibration equipment head and the specimen fixture base plate during vibration testing.

Most of the boards are found to be bolted to some type of support standups and others are plug-in types [8]. Such mounting methods can be majorly classified as point-supported or edge-supported configurations. Some of these clamping conditions are studied in [40] and concluded that the clamping condition of the PCB is necessary to validate that PCB is subjected to homogenous stress.

In addition, a few studies are done on assessing the impact of increasing the amount of PCB clamping screws and standups [20,41]. They influence the PCB excitation response during vibration testing and hence affecting the damage levels at the solder joint interconnects.

Several PCB mounting structures that allow simultaneous PCB testing can be readily found in literature [36,39]. Besides [36], there is not much data showing the impact of this mounting structure on the stress transferred onto the component.

In [36], three vibration test methods (1D, 2D & 3D shown in Fig. 6) have been compared by measuring the PCB vibrational dynamics. It is revealed that the non-rigid type vibration test fixture strategies might alter the stress transferred to the component in all three vibration axes. It can lead to a false reliability prediction. The results show that both 1D and 3D techniques can be used as complementary to one another depending upon the allowed mass limit of the shaker system and stress levels involved.

Most of the work performed so far reaches numerous non-standardized test board design variants and well-known solder alloys of fairly simple packaging technologies. However, the correlation to the fails observed in the application is missing, implying that the solder joint prediction part is not yet mature in board level vibration testing.

6. Vibration test parameters

The board level vibration test severity is determined by the combination of all the following vibration test variables as shown in Fig. 7: (i) Stress orientation, (ii) vibration stress application method, (iii) vibration energy density, (iv) test duration, (v) test frequency range. Each test parameter is described separately as follows.

6.1. Stress orientation

All vibration test specifications described in Table 1 prescribe a vibration test sequence applied in each of the mutually perpendicular axes of the test object. Having said that, some studies investigating the impact of stress orientation can be found. In [42], the effects of different vibration directions on the damage of BGA under vibration loading conditions are examined. Other than the mutually perpendicular axes, boards are also tested with other inclination angles, involving 45° and 30°. It is found that strain accumulation near the solder joint occurs faster when boards are arranged in horizontal axes.

6.2. Vibration stress application method

The vibration stress can be applied in the following two ways: Swept sine test and Random vibration test. Both test methods are commonly suggested in the vibration test specifications that include the JEDEC Vibration, Variable Frequency specification, JESD22-B103-B [10]. Random vibration is unique in a way that all of the frequencies are present and excited at the same time, and at any instant of time. On the

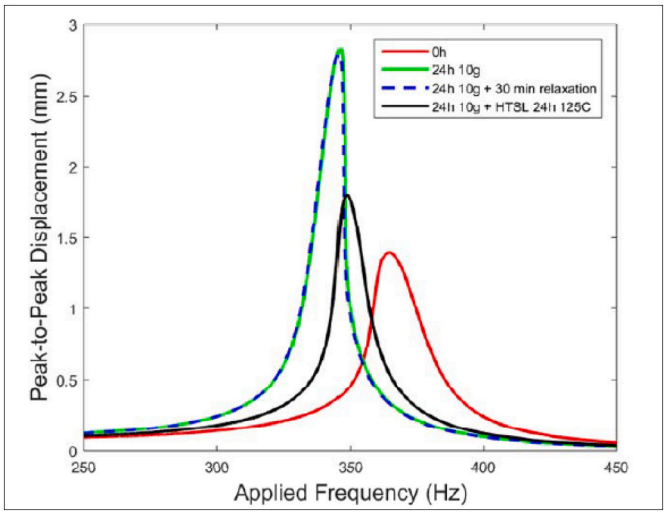

Fig. 8. Impact of test duration on board level vibration response [8].

other hand, swept sine tests involve sine wave signal driven into the vibrator, and the frequency of the sine wave changes with time, i.e. it sweeps.

Random vibration can excite several individual resonances of the sub-elements present in a system at the same time. These resonances can interact with one another and create failures different from the fatigue failures generated in swept sine tests. Random vibration more closely represents the true loading conditions in which the electronic systems must operate [8]. On the other hand, sinusoidal vibrations can be found in objects that rotate or oscillate, such as electric motors, engines, etc. It is useful in extracting the dynamic response of various types of structures individually. Furthermore, it is more often used to sweep through the resonant points as part of the damage accumulation process [14,15].

In [39,43], both swept sine and random vibration testing are assessed using BGA components. It is concluded that component location and failure mechanism are not the same. Most of the solder joint fatigue studies employ swept sine tests. Depending upon the acceleration level used in these tests, a mix of wear-out type and infant type failures are seen in swept sine tests. To conclude, both tests can induce failures in the solder joint interconnects and the test acceleration factor largely depends on the applied vibration energy that is described next.

6.3. *Vibration energy*

The vibration energy is one of the key test parameters in determining the amount of stress applied to a component. Hence, it influences the test acceleration factor of a board level vibration test. The peak level or magnitude of the input vibration signal can be expressed in three ways: Acceleration, velocity, or displacement.

The swept sine type vibration testing is found in a myriad of studies [2,37]. The peak acceleration levels used in these investigations range from 0.5 g to 20 g. Roucou et al. [2] investigated the impact of peak acceleration on the JESD-B111 type board dynamic response. The acceleration is varied from 1 g to 10 g and found that the PCB peak-peak displacement increases with the increased input energy. It does not impact the resonance behavior of the test board.

Next to that, it is of key importance to understand the effect of this increased acceleration on the induced failure mechanism and integrity of the test board itself. PCB cracks are seen when 10 g acceleration is

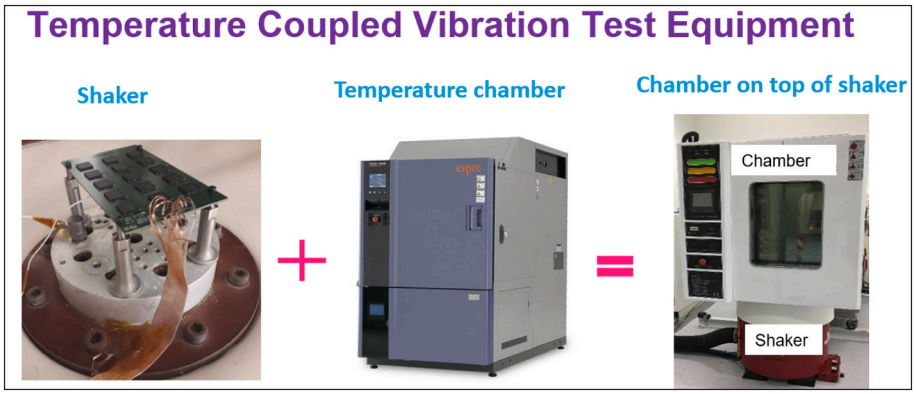

Fig. 9. Typical vibration test equipment for combined temperature-vibration testing.

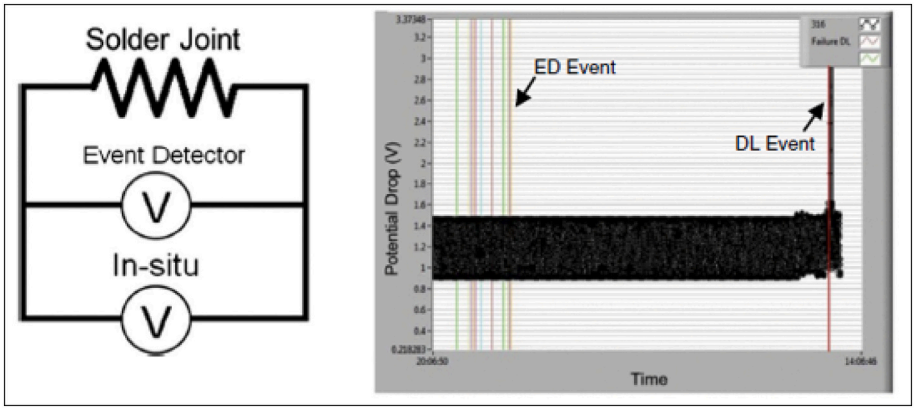

Fig. 10. Comparison of event detector (ED) vs high speed data logger (DL) solder joint monitoring techniques [52].

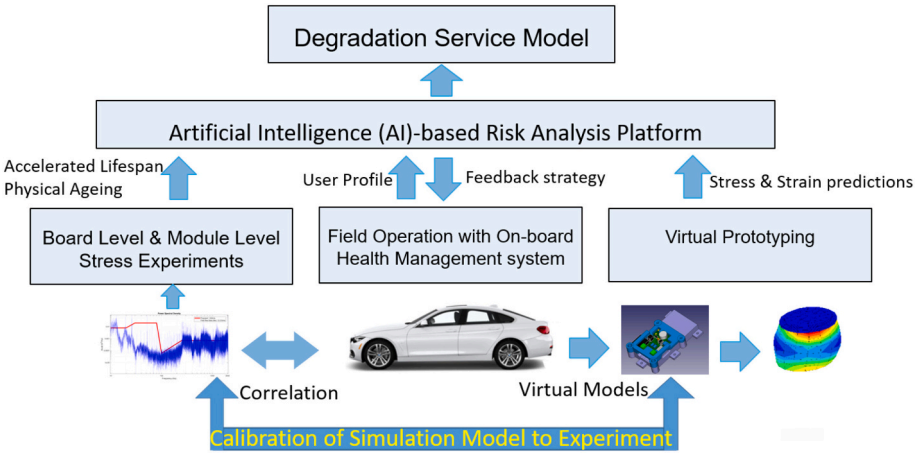

Fig. 11. Board level vibration test concept for future automobiles with on-board health management unit.

applied. Other investigations have shown similar outcomes [26,44].

Similarly, [39] showed the impact of increased acceleration level from 0.5 g to 5 g on a PCB similar to JESD-B111 with 5 BGA components placed on top of it. Solder cracks are found after swept sine tests with acceleration levels less than 5 g.

A random vibration signal involves a waveform that encloses frequencies whose amplitudes and phases vary randomly. The random aspects of magnitude require a value that relates to probability. It is expressed in Power Spectral Density (PSD). It describes the average power applied in the 1 Hz bandwidth of a particular frequency. It is usually specified with tolerances. The total power is obtained by adding the power of each of these 1 Hz bands and giving rise to a total G_{rms} (root mean square value).

Random vibration service test conditions are prescribed as an optional stress method in the JESD22-B103-B [10]. Amongst others, some board level vibration test studies have used random vibration stress [38,43]. One of these studies [38] involved random vibration testing of 10x10mm and 16x16mm BGA electronic packages. It employed G_{rms} values from 22 to 32 and observed that the stress on solder joints is dependent upon the size and location of electronic components.

In general, the selection of the vibration energy needs to be carefully negated against the test duration to minimize PCB damage and prevent overstress of components.

6.4. Test duration

There are various test standards (shown in Table 1) that prescribe vibration test duration from 30 min to 44 h. These are usually aimed at characterizing the ability of the electronic equipment under test to survive and operate at some specified vibration levels over a defined frequency range and life cycle. These tests are usually performed for a sufficient amount of duration to demonstrate this requirement.

However, in a board level vibration test, test duration should be sufficient enough to accumulate the necessary stress cycles to induce damages in the PCB-solder joint interface of the semiconductor package under test. Although this may give rise to changes in the PCB vibration spectrum and hence the stability of a vibration test setup. It has been unraveled in some studies that are summarized as follows.

Roucou et al. [2] examined the influence of swept sine vibration test duration that is stressed at 10 g acceleration level. A modification in the PCB (JESD-B111 board layout) resonance frequency and peak-peak displacement is observed after 24 h of the test (depicted in Fig. 8). The natural frequency is dropped by 20 Hz and the peak-peak displacement is increased by a factor of two.

Other swept sine type vibration studies involve test duration in terms of sweep cycles [2,41]. It can also be converted in time duration given that the sweep speed is known. It can be linear such as 1 oct/min which implies that the frequency doubles in every minute. In [2], the impact of sweep rate, when varied from 0.5 oct/min to 5 oct/min is also investigated. The variation in PCB vibration characteristics is shown to be within the reproducibility of the measurements. Therefore, the sweep rate does influence the resonance frequency of the PCB.

6.5. Test frequency range

Test frequency range is defined as the difference between the indicated minimum frequency and maximum test frequency at which the test board is excited by mechanical vibrations. Test frequency is described in all of the vibration test methods listed in Table 1. These are usually based on the service conditions described in these test standards.

Several tests to fail type sinusoidal vibration studies [2,45] have used test frequency range in such a manner that the resonance of the test board assembly under test is within the test frequency spectrum. In [2], the frequency sweeping is restricted by ±20 % of the resonance frequency. Another study [41] employed a similar approach of dwelling the sinusoidal vibration stress around resonance frequency of the PCB under test. Such investigations generated solder joint cracks.

A large variety of test frequency ranges are found in the literature. It ranges from 10 Hz to 2000 Hz. Some of the test studies used the test frequency range specified in the JESD22-B103-B [10].

To summarize, the effects of these vibration test parameters to various test board designs and application variables is not yet fully understood. The correlation of accelerated vibration test parameters used in board level vibration testing and vibration stresses experienced by components in automotive applications is not yet available (Table 2).

7. Test environments

In some applications, such as automotive, PCB assemblies with solder joints are subjected to combined vibrations and environmental loadings that include temperature and humidity. Although it represents the real environment, the ability to predict the lifetime of solder joints in a combined loading environment is still a challenge. It is due the fact that the vibration test setup can itself be influenced by varying temperature conditions.

The mechanical properties of the test board and solder alloy materials are temperature sensitive. Several PCB vibration spectrum and solder joint reliability assessments under vibration couple thermal loading environments are available in the literature. It is studied in [46] that included SAC105 type solder alloy. It is revealed that the crack length increases with increased temperatures.

Table 2
Overview of case studies on board level vibration tests.

Board level vibration test domains	Classifications	Examples
Vibration measurement sensor	Contact based	• Wide range of accelerometers [2,19], strain gauge [20], semiconductor ICs [22,23], etc.
	Contact less	• LDV [19], DIC [21], etc. • No recommendation on signal sample rate, range, etc.
Vibration test board	PCB construction and material	• JESD22-B111/B111A [29,30] • Others PCB size ranging from 77 mm to 305 mm with thicknesses varying from 1 to 2 mm [33–35] • No recommendation on PCB material
	Component placement and location	• Symmetrical [27] or Non-symmetrical [2] • No guideline on component orientation
	PCB mounting strategy	• Point supported with 4–8 screws [20,32] • Edge supported [33] • Simultaneous test strategies [36]
Vibration stress test parameters	Vibration stress application method	• Swept sine type vibrations [2] • Random type vibrations [8]
	Vibration input energy level	• Categorized based on service condition [10] • Swept sine: Peak acceleration range: 0.001-20G [10–16] • Random: RMS acceleration ranging: 0.06-32G [10–18]
	Excitation frequency range	• Frequencies ranging from 2 Hz to 2000 Hz [10–18]
	Sweep rate (for swept sine only)	• Sweep rate used vary from 0.5 to 5 oct/min [2]
	Test duration	• Components are either tested to fail [2] or • Service condition dependent [10] • Test time during from 0.5 to 44 h/axes [10–17]
	Stress orientation	• 3 axial tests (X,Y & Z) [10] • Uniaxial tests (X/Y/Z) [11] • Inclined angled. Example: 45° and 30° [42]
Vibration test environment	Relative humidity	• 30 %–60 % [2]
	Temperature	• Isothermal conditions [44] • Temperature cycling conditions [33]
Electrical fault detection	Failure criteria	• Daisy chained resistor based (JEDEC, etc.) [29] • Functional fails and others
	Fault detection and prediction methods	• Event detector [52] • In-situ voltage metrology [53] • Data-driven prediction methods [58]

Maniar et al. [35], performed High Cycle Fatigue (HCF) experiments on standardized specimens of the SAC alloy. It is concluded the number of cycles to failure decreases with the increase in temperature. Similar failure mechanisms occurred at both room temperature and 125 °C.

In [47], thermal cyclic loading is combined with the vibration testing analysis of SAC305 solder assemblies. The temperature is varied from −40 °C to 125 °C within an hour and it is combined with the random vibration loading of 7.5 Grms. It is presented that the effect of mechanical vibration loading dominates the thermal loading environment.

Vijayakumar et al. [48] analyzed the impact of isothermal aging on the vibration performance of SAC105 and SAC305 solder alloys. An aging temperature of 55 °C is used for 6, 12, and 24 months. It is shown that the aging temperature has a direct impact on the lifetime of solder joints. Deleterious effects are seen on the mechanical properties of these solder alloys. It is revealed that SAC105 is the least resistant to the temperature aging stresses.

In [33], BGA type packages are stressed to temperature cycling superimposed on random vibration environments. The temperature profile used in this study varies from −50 °C to 150 °C. It is concluded that the damages under combined temperature and vibration loading are at least 10 times more damaging than the expectations from the linear damage approximation.

In some papers, inverse trends are observed. For example, in [49], SAC305 solder interconnects are exposed to mechanically coupled thermal tests. It is revealed that the life of solder joint interconnects increases at higher temperatures. Different failure mechanisms are observed at higher temperatures when compared to the failures at room temperature.

Roucou et al. [2] discovered the impact of temperature and humidity on the PCB vibration response. The relative humidity is varied between 30 % and 60 % and is found to have no impact on the PCB vibration spectrum. Then, the temperature is varied from 17 °C to 47 °C, and observed lower resonances at higher temperatures. At the same time, peak-peak displacement is increased with the temperature rise. Another study [41] showed a similar trend on the same board layout. However, the rate of change in resonance with respect to temperature is not the same. It revealed a faster failure rate when the temperature is increased.

Eckert et al. [50] investigated the solder joint fatigue model under combined vibration and temperature environments. A shift in the resonance frequency is observed while increasing the temperature. On the other hand, the PCB deflection is reduced at high temperatures. The failure analysis results showed solder joint fatigue failures.

Matkowski [22] also examined the impact of solder joint fatigue when 1206 and 0805 SMD are subjected to temperature-coupled random vibration environments. It is proven that the mechanical stress in conjunction with the thermo-mechanical loading environment is responsible for the acceleration of solder joint failures.

McMahon et al. [51] also investigated solder reliability of several PLCC and BGA type packages using a combined isothermal-vibration test equipment similar to the equipment shown in Fig. 9. A non-standard and customized test board is used. A first estimation of the relationship between micro-strain, resonance frequency, and driving acceleration level has been drawn in this work. It is concluded that the tested components showed the highest reliability at cold temperatures when compared to room temperature and hot temperatures.

Other than the PCB and solder alloys, it is important to note that the board level vibration test setup can also be temperature sensitive. It might interact with the PCB mounting strategy and hence influence the board level reliability performance of surface mount components. However, it has not been studied in the literature. Therefore, test setup validation needs to be exercised before performing temperature coupled vibration stress tests. Also, the interaction of module level elements with temperature loading is not articulated well in the literature. Finally, the acceleration model for combined vibration and thermal loading lifetime testing is not yet available for the current generation of electronic packages used in the automotive industry.

8. Electrical fault monitoring & analytical techniques

Board level reliability testing involves a daisy-chained component as a test vehicle [29,30]. A daisy-chained component can be described as a continuous and alternate conductive link between the PCB and the device under test. It allows in-situ electrical monitoring of failures in the daisy chain nets during reliability testing. Fault detection analysis can be broadly categorized in the following streams:

8.1. Failure detection systems

Several board level reliability test standards such as JESD22-B111 [29,30] have established guidelines for monitoring electrical opens in daisy-chained components. JESD22-B111 has also emphasized using event detectors or high-speed acquisition systems to capture the

electrical discontinuity in daisy chain components. Some daisy chain failure criteria with sampling rates are also prescribed in these specifications.

Typically, electrical cables are soldered onto the PCB under test for the in-situ electrical continuity test purposes [30]. The impact of such cables on the PCB vibration response under board level vibration testing is demonstrated in [2]. The investigation showed changes in the resonance frequency and a more prominent impact on the higher order resonance frequencies of the tested PCB assembly. The failure criterion followed the guidelines mentioned in the JESD22-B111 [30].

Duan et al. [52] studied the impact of failure criteria on the solder joint lifetime under board level thermo-mechanical tests. The following measurement techniques are examined in this study, event detector, and data logger. As shown in Fig. 10, the event detector showed failure events prior to the data logger (DL) system. It is observed that the event detector can catch the short intermittent type failure events, while the data logger can capture the degradation event under board level mechanical tests. So, depending upon the nature of failures, a suitable failure detection scheme shall be applied.

In [53], failure measurement capability analysis (MCA) study was conducted on a voltage-based in-situ metrology technique. This method is applied to the failures generated by mechanical shock tests. MCA test results met a recommended guideline that is typically accepted in the industry [54].

High-speed data acquisition systems are used in experiments such as [55]. In [55], the daisy chain resistance failure event is recorded over time. It displays the different damage and failure stages of solder joint interconnect. A ringing signature is reported here. A similar solder degradation process is found in [56]. Several stages of solder joint crack propagation are shown in this work. However, this signature is not always found in other investigations such as [26]. In [26], resistance data is also captured by using a high-speed data acquisition unit. A rapid increase in resistance is found for some of the resistance measurement plots presented in this study.

8.2. *Failure prediction systems*

Failure prediction systems compose of physical degradation monitoring process hardware and algorithms. Current board level reliability test standards in the industry do not prescribe guidelines for the damage accumulation and failure impending systems. It stems from the fact that these test specifications are based on the physics of failure and the statistical reliability approach is at its core.

With more and more electronics being applied in the life critical systems, the demand for prognostics and health management (PHM) techniques is on the rise. Although, the application of PHM technology is relatively new to the board level vibration test methodology. A few prognostics based studies in the domain of board level vibration testing can be found in literature [57].

In [57], the sensitivity of the two feature vectors are investigated for different strain gauge sensor signals on two different PCB assemblies. It showed that the feature vector can predict failure before all components fail on the test board. It also revealed a distinctive behavior of feature vectors when the majority of the population failed on the PCB under test. This is also called data-driven approach in the world of PHM [58]. An overview of other data-driven techniques and algorithms is provided in [58].

Gu, Barker and Pecht [59] unfolded a unique physics of failure model-based prognostics approach. An acceleration sensor is used and put into the failure fatigue model to obtain the Remaining Useful Lifetime (RUL) for a given strain gauge range. Strain range is extracted by using the cycle-counting algorithm. The analytical model is calibrated by the finite element analysis developed for calculating the strain at the solder interconnect level.

Besides board level vibration testing, some prognostic approaches are also presented in the board level temperature cycling testing domain. Zhang [60] unraveled such an approach for LED-like board level ceramic packages. Here, the temperature coefficient of resistance is correlated to the fatigue damage evolution in the solder joint prototypes. This method was validated by the physical failure analysis outcomes and FEM simulation predictions.

The current board level reliability test methods are not capable of providing precise RUL in temperature coupled vibration experiments. Moving forward, a combination of PHM techniques and sensors capable of measuring mechanical and thermo-mechanical degradation at solder joint – PCB interface will be required.

9. Recommendations & challenges

The current board level vibration test method studies are usually using either the JESD22-B111/B111A test boards or some other customized circuit boards. The correlation between these boards and final automotive application is not necessarily established. It is recommended to standardize PCBs that can enable the evaluation and comparison of vibration performance of electronic components used in automotive electronic modules. It is advised to use robust PCB designs that are not prone to early test board-related failures during vibration stresses. Also, a well-developed vibration characterization technique should be realized to minimize the impact on the PCB dynamic response and the stress on components. Next to that, the vibration tests are advocated to be performed in regulated environmental conditions such as temperature and relative humidity. Modeling can be used to verify some of the experimental test setup. Then, swept sine vibration tests can be used over random vibration testing because of its ability to compare the relative reliability performance electronic components. Finally, high-speed data acquisition systems such as failure event detectors or in-situ voltage metrology methods are preferred to detect the failure of daisy chained components.

Various subjects need to be improved in order to correctly reflect the stresses in complex and multi-fold loading scenarios in the field. These subjects include the interaction between the various vibration stress test parameters and module-level application effects. Hence, exemplifying the need for experimental test setup validation, standardization, and application driven vibration testing. This would require physical stress and degradation measurement systems on-board in automotive vehicles to determine a user profile. And the integration of the following subjects: reliability stress test experiments, virtual prototyping, and Artificial Intelligent (AI) based platforms can be imperative to predict reliability risks at the solder interconnect level. It can altogether create an on-board health management unit that can work as a virtual-intelligent twin for solder joints. It is pictorially described in Fig. 11.

10. Conclusions

Based on the assessment of the existing board level vibration test methodologies, the paper has identified this subject to be an evolving concept and requires further reliability research and protocol development in several areas. Substantial improvements are needed in directions linked to the standardization of the vibration test methodology. It involves standardization of the reliability stress test setup, understanding of the application mission profile and PHM methods to cope with the reliability challenges in the next generation of automotive electronics. With the future focused on providing reliability as a service, smart electronic devices integrated with embedded functional safety features will be required at the chip level. Such a system-on-chip solution may comprise of inbuilt stress sensing hardware equipped with the AI based software algorithms.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

Varun Thukral reports financial support was provided by NXP Semiconductors NV.

Data availability

Data will be made available on request.

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