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Failure quantitative assessment approach to MOSFET power device by detecting parasitic parameters

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With the emerging wide bandgap (WBG) semiconductor development, the increasing power density and efficiency of power electronic converters may cause more switching oscillation, electromagnetic interference noise, and additional power loss, further increasing the probability of device failure. Therefore, determining and quantifying the failure of a metal-oxide-semiconductor-field-effect transistor (MOSFET), which assembled using WBG semiconductor in some applications, is crucial to improving the reliability of a power converter. This study proposes a novel failure quantitative assessment approach based on MOSFET parasitic parameters. According to the two-port network theory, MOSFET is equivalent to some second-order *RLC* circuits composed of independent inductances, capacitances, and resistances in series. Then, the frequency-domain impedance associated with the physical failure of MOSFET is identified through frequency domain reflectometry. Accelerated aging and bond wires cut-off experiments are employed to obtain various quality states of the MOSFET device. Result shows that the MOSFET quality level and its number of bond wire lift-offs can be quantified effectively. Drain-to-source on-resistance ($R_{DS(on)}$) that normally represents the MOSFET quality shows a positive linear function relationship on drain-to-source parasitic resistance (R_D + R_S) during the quality degradation proceeding. This finding matches with the correlation established between $R_{DS\ (on)}$ and R_D + R_S in theory. Meanwhile, source parasitic inductance (L_S) increases with the severity of bond wires faults, and even the slight fault shows a high sensitivity. The proposed approach would be an effective quality screening technology for power semiconductor devices without power on treatment, which can effectively avoid the impact of junction temperature and test conditions (current and voltage) on test results, and does not need to design additional test circuits. The test frequency range we used in this approach was 10–300 MHz, which to some extent is suitable for providing an on-line quality monitoring technology for high-frequency WBG power devices manufacturing.

KEYWORDS

MOSFETs, quantitative assessment, parasitic parameters, quality level, bond wire fault, detection

1 Introduction

Power electronic converters are widely used in many critical power systems with high reliability requirements, including, but not limited to, many emerging fields, such as high-speed railway, electric vehicles, industrial frequency conversion, and renewable energy generation. Next generation power electronics are moving toward emerging wide bandgap (WBG) power device, such as silicon carbide (SiC) and gallium nitride (GaN), which have higher power density and higher conversion efficiency. However, the ultrafast switching characteristics (high dv/dt or di/dt) mean that the power device needs to withstand severe thermal-stress and switching oscillations, which is a serious challenge to reliability. Literature studies indicated that power electronic devices' failure accounts for more than 31% of the total failure distribution in the power converter system [1, 2], which is the highest of all failure types. As a widely used electronic power device, a metal-oxide-semiconductor-field-effect transistor (MOSFET) is one of the critical components of a power converter. In practice, MOSFET suffers from excess electrical-thermal-mechanical stresses under harsh and uncertain conditions for a long time, resulting in fatigue failure. The reliability of MOSFETs has become a vital limiting factor influencing the reliability of power inverters, which has aroused great research interest in the industry.

The priority important study is the origin of the failure in order to accurately predict the quality state of the power device. Generally, the failure of semiconductor devices can be categorized into two groups, namely, packaging-related failure and chip-related failure [3–5]. Packaging-related failure is one type of fatigue failure, which is caused by fatigue degradation of materials in long-term thermal aging. High-power devices are generally comprised of wire-welding packaging, which is composed of multilayered materials with different coefficients of thermal expansion (CTE). When thermal stress is applied to the MOSFET, each layer of the device will expand at different rates, specifically in the weak points of the solder joint and wire bond root. The CTE mismatch with temperature swing will generate thermomechanical stress in adjacent layers and lead to serious aging problems. Therefore, the most common failure modes are solder layer degradation and bond wire failure in wire welding packaging semiconductor power devices [6, 7]. Chip-related failure is mainly caused by electrical overstress, electrostatic discharge, hot-carrier injection, electric migration, and radiation effects [8]. The applied electrical overstress (high voltage and high current) leads to the degradation of gate oxide, which is the main failure mechanism for MOS-gated devices. The key to realizing the reliable detection of power devices is to identify the certain fault precursor.

Considerable research papers indicated that the commonly used reliability detection methods of power devices can be classified into two classes, namely, degradation precursors-based methods and morphology characteristics-based methods. Degradation precursors are usually obtained by directly measuring the voltage or current information between any one or two terminals or indirectly detecting the change of junction temperature T_j or thermal resistance Rth by establishing the relationship between temperature-sensitive parameters and T_j. Then, we compare the data with healthy devices to evaluate the quality level. The commonly degradation precursors are as follows: gate-emitter voltage (V_{GE}) [9], gate leakage current (I_G) [10], on-resistance ($R_{DS(on)}$) [11], collector–emitter saturated voltage ($V_{CE(sat)}$) [4, 12, 13], drain-source current (I_D) [14], short circuit current (I_{SC}) [15], junction temperature (T_j) [16], thermal resistance from junction to case (R_{th}) [17], and others. From a practical point of view, the switching duration of the MOSFET is in the nanosecond-level or microsecond-level range, so accurately identifying the changes of degradation precursors caused by device degradation is difficult. Before and after switching, the degradation precursors $V_{CE(sat)}$ and I_{SC} fluctuate greatly and are easily affected by the drain current. Meanwhile, the degradation precursors $R_{DS(on)}$, $V_{CE(sat)}$, I_D, I_{SC}, and Rth usually belong to temperature-dependent parameters, so the measurement accuracy largely depends on the T_j of the chip. Unfortunately, the T_j cannot be measured directly, and the stable control of junction temperature is also a hard technical problem. In the test, the fluctuation of junction temperature greatly affects the accuracy and stability of the test results, so we must spend more cost in the test system. V_{GE} and I_G change significantly only when one or more parallel power chips fail or all the bond wires on a chip liftoff. Thus, effectively detecting the degradation of the device or a part of bond wires damage caused by the long-term operation is difficult. Morphology characteristic detection technologies mainly include thermal imaging [18–21] (eddy current pulse thermal imaging, infrared imaging) and structural imaging (X-ray imaging, ultra-sound imaging) [22–24]. Thermal imaging can identify the location of potential damage by observing the temperature distribution of the power devices under a positive bias voltage. Structural imaging directly detects device inner defects by identifying the phase and amplitude of the reflected signals. The application of thermal imaging technology here is usually a destructive test, which requires the power device to remove the case to observe the temperature distribution. The thermal imaging technology cannot quantitatively evaluate the quality level of the power devices [18–21]. Structural imaging is a non-destructive testing technology, which can directly detect the appearance quality of bond wire and solder layer. However, estimating the

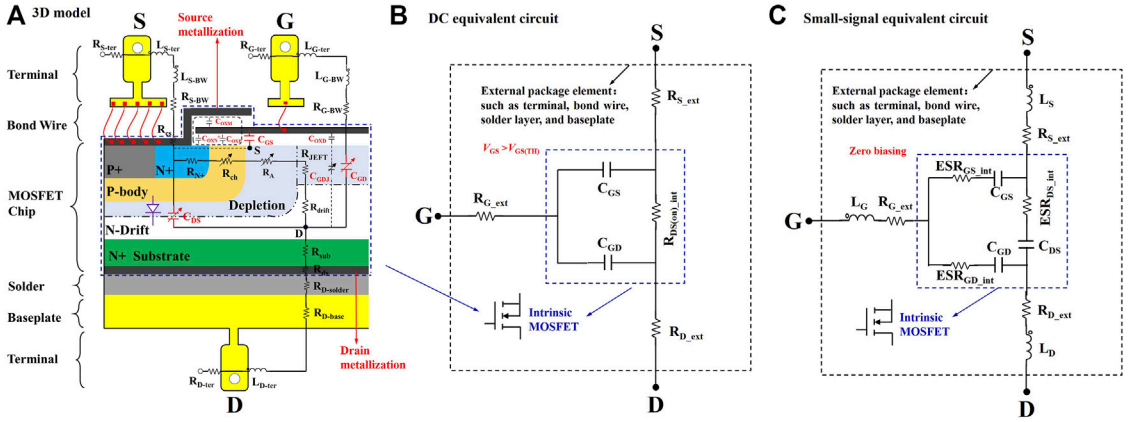

FIGURE 1
(A) Cross-section of a power MOSFET. **(B)** MOSFET DC equivalent circuit model. **(C)** MOSFET small-signal equivalent circuit model.

exact height of bond wire and solder layer in the Z-axis direction in advance is very difficult for users. Therefore, considerable time is needed to try to obtain the ideal imaging quality. Similarly, the structural imaging technology can not directly quantify the actual aging degree of the power devices. The penetration ability of the pulse ray is easily disturbed by the degradation of other material layers. If delamination exists between the epoxy molding compound (EMC) layer and the upper surface of MOSFET, then penetrating the lower interface of MOSFET for effective imaging is difficult for the pulse ray, resulting in a limited application. Compared to Si MOSFETs, the degradation detection approaches for WBG power devices (SiC MOSFETs) have not been widely reported in the literature due to the relative novelty of WBG devices. Therefore, it is urgent to develop a novel failure assessment approach based on exploring Si MOSFETS failure detection approaches to satisfy the requirements of rapid, nondestructive, and quantifiable detection of WBG power devices.

In this study, a failure quantitative assessment approach based on MOSFET parasitic parameters is proposed. According to the two-port network theory, MOSFET is equivalent to some second-order *RLC* circuits composed of independent inductances, capacitances, and resistances in series. According to the characteristics of the series resonant circuit, the impedance value at the self-resonant frequency is dominated by the resistive elements, whereas the impedance value at the high-frequency is dominated by the inductive elements. This notion provides a new idea that the physical failure of MOSFET can be mapped to the change of frequency domain impedance. This idea then inspires us to try to detect faults by identifying the changes of MOSFET frequency domain impedance at the specific frequency. Quantitative assessment experiments are designed according to the common failure modes of MOSFET. The purpose is to determine the specific parasitic parameters closely related to the quality level and the amount of bond wire faults by identifying the changes of parasitic parameters over the range of 10–300 MHz. Among all the WBG power devices, SiC MOSFETs are the most attractive, because they have great advantages in the field of high switching frequency. In addition, WBG devices have higher self-resonant frequency than Si MOSFETs, which means that it will be more suitable for the proposed two-port S-parameter characterization technique.

2 Methodologies

2.1 MOSFET small-signal equivalent circuit

Figure 1 illustrates the schematic of a cross-section of a half vertical-diffused MOSFET including the package structure and its equivalent circuit model. The equivalent circuit model under direct current (DC) condition is shown in Figure 1B. If $V_{GS} < V_{GS(TH)}$ (voltage threshold), then the effective channel length is not formed, whereas the MOSFET is off state, the drain-source output resistance $R_{DS} \approx \infty$. If $V_{GS} > V_{GS(TH)}$, then the channel is formed, $R_{DS} = \Delta V_{DS}/\Delta I_D$. As shown in Figure 1A, R_{DS} can be calculated as $R_{DS} = R_{S\text{-}ter} + R_{S\text{-}BW} + R_{DS\text{-}int} + R_{D\text{-}solder} + R_{D\text{-}base} + R_{D\text{-}ter}$, in which the intrinsic MOSFET drain-source resistance R_{DS_int} can be calculated as $R_{DS\_int} = R_{cs} + R_{N+} + R_{ch} + R_A + R_{JEFT} + R_{drift} + R_{sub} + R_{ds}$, where $R_{S\text{-}ter}$ is the source terminal resistance, $R_{S\text{-}BW}$ is the source bond wire resistance, R_{cs} is the metallization and source contact resistance, R_{N+} is the source resistance, R_{ch} is the channel resistance, R_A is the accumulation resistance, R_{JEFT} is junction field-effect transistor (JFET) resistance, R_{drift} is the drift region resistance, R_{sub} is the substrate resistance, R_{ds} is the metallization and drain contact resistance, $R_{D\text{-}solder}$ is the solder layer resistance, $R_{D\text{-}base}$ is the

baseplate resistance, and $R_{D\text{-}ter}$ is the drain terminal resistance. As described in [4], bond wire lift-off, metallization reconstruction or die-attach solder delamination leads to an increase in the MOSFET ON-state drain-source resistance $R_{DS(on)}$. In this study, $R_{DS(on)}$ is used as a comparative precursor parameter for package-related aging detection.

An ideal MOSFET chip can be equivalent to the constant and variable active devices, such as voltage-controlled current source, internal parasitic capacitances, internal parasitic series resistance, and anti-parallel body diode. The internal parasitic parameters include parasitic capacitances (drain-source capacitance C_{DS}, gate-source capacitance C_{GS}, and gate-drain capacitance C_{GD}) and parasitic series resistances (drain-source resistance ESR_{DS_int}, gate-source resistance ESR_{GS_int}, and gate-drain resistance ESR_{GD_int}). An additional equivalent series parasitic inductance may be included in the circuit. However, compared with the size of terminals and bond wires, the parasitic inductance of MOSFET is very small and can be ignored. The chip and external terminals are electrically interconnected through the aluminum bond wire packaging technology, which inevitably introduces the external packaging parasitic elements. 1) Parasitic inductances $L_{S\text{-}ter}$, $L_{G\text{-}ter}$, and $L_{D\text{-}ter}$ and parasitic resistances $R_{S\text{-}ter}$, $R_{G\text{-}ter}$, and $R_{D\text{-}ter}$ are generated from the gate, source, and drain terminals, respectively. 2) Parasitic inductances $L_{S\text{-}BW}$, $L_{G\text{-}BW}$ and parasitic resistances $R_{S\text{-}BW}$, $R_{G\text{-}BW}$ are generated from bond wires. 3) Parasitic resistances $R_{D\text{-}solder}$ and $R_{D\text{-}base}$ are generated from the solder and baseplate layers, respectively. The small-signal equivalent circuit model is simplified and the external parasitic inductances are combined into L_G ($L_{G\text{-}ter} + L_{G\text{-}BW}$), L_S ($L_{S\text{-}ter} + L_{S\text{-}BW}$), and L_D ($L_{D\text{-}ter}$) and the external parasitic resistances into R_{S_ext} ($R_{S\text{-}ter} + R_{S\text{-}BW}$), R_{G_ext} ($R_{G\text{-}ter} + R_{G\text{-}BW}$), and R_{D_ext} ($R_{D\text{-}solder} + R_{D\text{-}base} + R_{D\text{-}ter}$) to facilitate the analysis, as shown in Figure 1C.

2.2 Parasitic parameters as quality precursors

2.2.1 MOSFET quality states analysis with parasitic resistance

The MOSFET devices are typically packaged in discrete or power modules that provide heat dissipation and protection. The thermal mechanical stress caused by power loss and high thermal stress will accumulate in the die-attach layer, resulting in mechanical strain. If the strain exceeds the elastic region of the stress deformation characteristic, then cracks, voids, and material dislocations are produced in the die attach because of the great difference in the linear CTE of the materials (CTE for copper is 16–18, silicon is 2.6–3.3, and lead-free solder is 20–22.9 ppm/°C). From the existing literature study, $R_{DS(on)}$ is the most significant aging factor in MOSFETs [4, 11], [25–33]. Temperature elevation accelerates the degradation processes of semiconductor devices, and the Arrhenius equation can describe the influence of temperature. A relationship between the degradation rate D of $R_{DS(on)}$ and the average T_j of IGBTs can be described as [34]:

$$\boldsymbol{D} = \frac{\boldsymbol{d}_{\boldsymbol{R}_{\mathrm{DS(on)}}}}{dt} = \boldsymbol{C_0 e}^{\left(-\frac{\boldsymbol{E}_a}{\boldsymbol{K}_B \boldsymbol{T}_{javg}}\right)} \tag{1}$$

where C_0 is an Arrhenius constant, E_a is the activation energy, and K_B is a Boltzmann constant.

The degradation of $R_{DS(on)}$ should be a continuous process in a constant temperature accelerated aging test. Considering temperature changes as a function of time(t) in the aging process, the accumulated $R_{DS(on)}$ can be calculated as follows:

$$\boldsymbol{R}_{\mathrm{DS(on)}}(\boldsymbol{t}) = \boldsymbol{R}_{\mathrm{DS(on)\_init}} \cdot \boldsymbol{e}^{\int_0^t \boldsymbol{D}(t)dt} \tag{2}$$

where $R_{DS(on)\_init}$ is the initial $R_{DS(on)}$. The capacitor delta–connection can be converted into a star–connection, and the conversion method is shown in Figure 2A. The parasitic capacitances (C_{DS}, C_{GS}, and C_{GD}) and the parasitic series resistances (ESR_{DS_int}, ESR_{GS_int}, and ESR_{GD_int}) can be equivalent to a second-order *RLC* circuit composed of equivalent capacitances (C_S, C_G, and C_D) and equivalent resistances (R_{S_int}, R_{G_int}, and R_{D_int}) in series. Figure 2B shows a simplified MOSFET small-signal equivalent circuit in the form of capacitor star–connection, in which $R_S = R_{S\_int} + R_{S\_ext}$, $R_G = R_{G\_int} + R_{G\_ext}$, and $R_D = R_{D\_int} + R_{D\_ext}$.

$R_{DS(ON)}$ increases due to thermal overstress aging, and intermetallic growth and Kirkendall voids formation at the bond–pad and pad–attach interface at higher temperature. A simplified equivalent circuit for an aged power MOSFET is shown in Figure 2C, where the degradation of MOSFET can be equivalent to adding additional series resistance in the source–drain loop circuit, resulting in the increase of $R_{DS(on)}$ and ESR_{DS}. A direct positive relationship between aging time and capacitor equivalent series resistance *ESR* was proposed in [35,36], that is, the *ESR* increase with aging. Similar phenomenon happens for the MOSFET because it has built in capacitors between gate and source as well as between gate and drain [37–39]. *ESR*(t)-based Physics-of-Failure (PoF) equations are provided as follows:

$$\boldsymbol{ESR}(\boldsymbol{t}) = \boldsymbol{ESR}_{\boldsymbol{init}} \cdot \boldsymbol{e}^{\int_0^t \boldsymbol{k}(t)dt} \tag{3}$$

$$\boldsymbol{k}(\boldsymbol{t}) = \boldsymbol{k_0} \cdot \boldsymbol{e}^{-\frac{E_a}{K_B \cdot T}} \tag{4}$$

where ESR_{init} is the initial *ESR*; k(t) is the temperature-dependent degradation rate; k_0 is the Arrhenius constant. The MOSFET drain-to-source equivalent series resistance (ESR_{DS}) is associated with drain-to-source parasitic resistance ($R_D + R_S$) and can be described as follows:

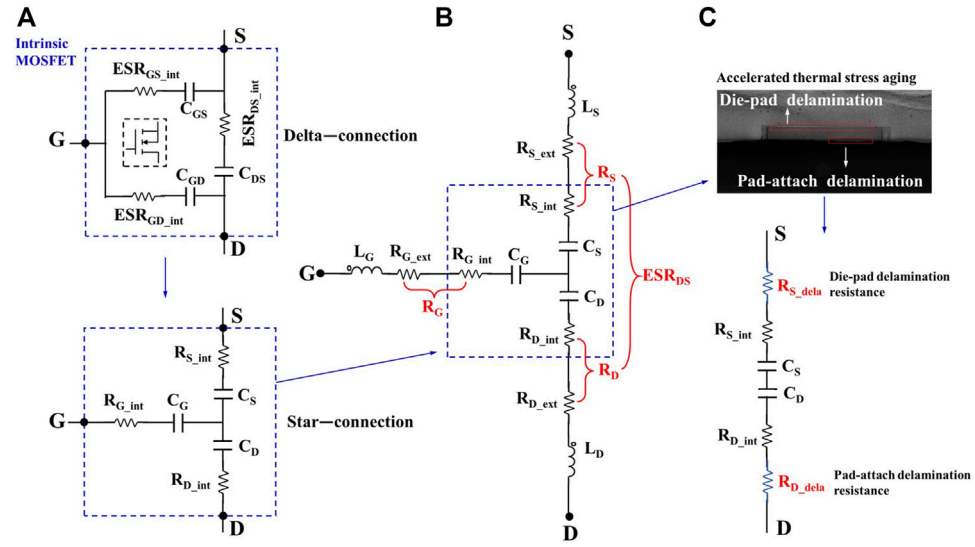

FIGURE 2
(A) Equivalent circuit of the parasitic capacitance (convert the capacitor delta connection to a star connection). **(B)** MOSFET small-signal equivalent circuit in the form of capacitor star connection. **(C)** Series resistances generated by bond–pad and pad–attach in the source-drain loop circuit.

$$ESR_{DS}(t) = R_D(t) + R_S(t) = R_{D\_init} \cdot e^{\int_0^t k_D(t)dt} + R_{S\_init} \cdot e^{\int_0^t k_S(t)dt} \quad (5)$$

where R_{D_init} is the initial R_D; R_{S_init} is the initial R_S; $k_D(t)$ and $k_S(t)$ are the temperature-dependent degradation rates of source and drain regions in MOSFET devices, respectively. We assume that the degradation rates of source and drain regions are the same in a constant temperature accelerated aging test. Eq. 5 can be modified as follows:

$$ESR_{DS}(t) = (R_{D\_init} + R_{S\_init}) \cdot e^{\int_0^t k_{DS}(t)dt} \quad (6)$$

In general, in a normal measuring condition, $R_{DS\ (on)}$ as the key evaluating parameter of MOSFET quality states is affected easily by the changes in chip junction temperature, gate-source voltage V_{GS}, and drain-source current I_D. Therefore, a fine $R_{DS(on)}$ measurement requires high consistency of test conditions [31]. By contrast, the parasitic resistances (R_S, R_G, and R_D) can be extracted with frequency domain reflectometry (FDR) technology without powering on the MOSFET [40,41]. Impressively, based on (2) and (6), $R_{DS(on)}$ (t) should show a similar exponential increasing trend as $ESR_{DS}(t)$. Then, a linear relationship between $(R_D + R_S)$ (t) and $R_{DS(on)}$ $_(t)$ can be established, as follows:

$$R_{DS(on)}(t) = A \cdot [R_D(t) + R_S(t)] + E \quad (7)$$

where A and E are undetermined coefficients. The calculated value of $R_{DS(on)}$ can be easily obtained with (7), whereas the parasitic resistances (R_D and R_S) are extracted with FDR technology. Then, the quality level or/and quality states of MOSFET can be quantified quickly.

2.2.2 MOSFET bond wire fault analysis with parasitic inductance

Middle and high-power MOSFETs are generally based on wire-welded packaging, which uses some parallel aluminum bond wires to improve the current carrying capacity for electrical interconnection between source and terminal. Figure 3 depicts a typical power MOSFET in a TO−247 discrete package showing the equivalent circuit of each region from source to drain terminal. Multiple parallel bond wires are distributed at the source of MOSFET to jointly carry current, which makes it challenging to identify the damage of some bond wires directly. Therefore, our research focuses on the source bond wire faults. However, since only one bond wire is distributed at the gate, the fault is catastrophic and does not require significant attention. A problem that cannot be ignored is that the existence of bond wire introduces large parasitic inductance. A simple estimation is made in [42], the inductance is estimated as "1-mm length equivalent to 1-nH inductance." In practice, 6 or 8 bond wires are usually used for interconnection. If the mutual inductance between parallel bond wires is ignored, then the total parasitic inductance of the bond wire can be simply calculated as $L/(6$ or $8)$. Figure 3 shows the RL equivalent circuit of a discrete MOSFET in

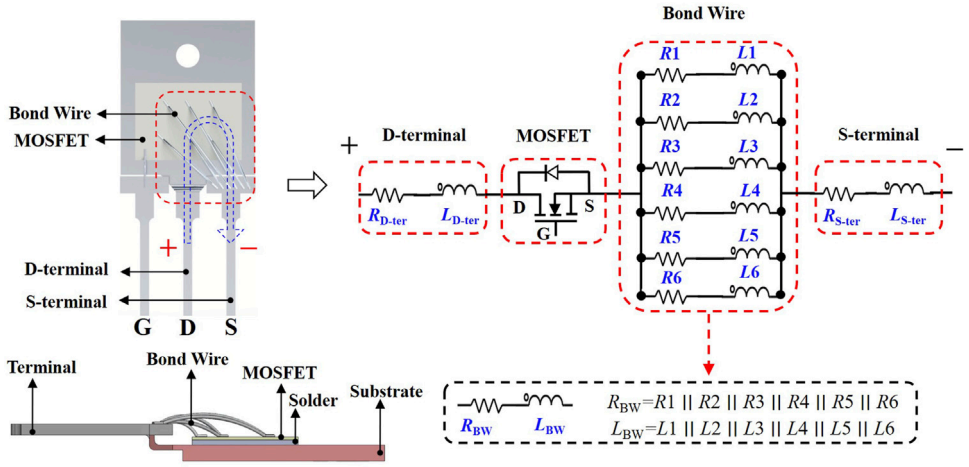

FIGURE 3
Simplified *RL* equivalent of a discrete MOSFET in TO–247 package.

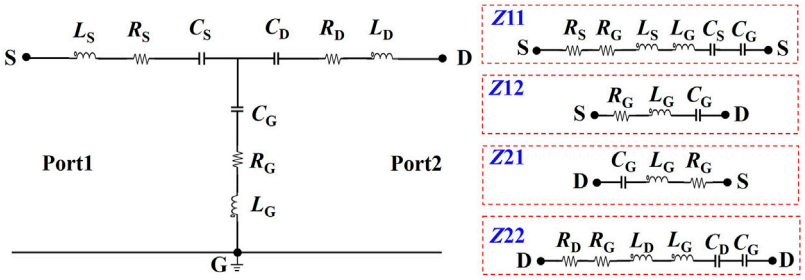

FIGURE 4
Two-port network representation of a MOSFET under zero biasing conditions.

the TO–247 package. Six parallel bond wires with different lengths exist between source and terminal, and each bond wire can be equivalent to a series circuit of resistance *R* and inductance *L*. L_{BW} = *L1*//*L2*//*L3*//*L4*//*L5*//*L6*. Bond wire fault will reduce the number of parallel inductors in the *RL* equivalent circuit of the bond wire, increasing parasitic inductance L_{BW}. Therefore, the change of parasitic inductance can be used to identify the health of the bond wire. In MOSFET small-signal equivalent circuit model (Figure 1C), the L_{BW} is merged in L_S. Thus, we can infer that L_S will increase with the increasing severity of the number of bond wire lift-off. The detailed simulation and measurement process to extract parasitic inductances L_S are reported in Section 3.3.

2.2.3 Parasitic parameter extraction approach

In this study, the FDR measurement is used to extract the parasitic parameters of MOSFET [40,41]. This method is a two-port characterization approach that allows three terminals of a power device to be connected at a time with a vector network analyzer (VNA). No floating terminal error is observed during the measurement, which provides high measurement accuracy. The MOSFET small-signal equivalent circuit is shown in Figure 4, whereas the source terminal is connected to the VNA Port 1, the drain terminal is connected to the VNA Port 2, and the gate terminal is connected to the VNA ground. Each of the two-port network *Z*-parameters Z_{11}, Z_{12}, Z_{21}, and Z_{22} can be equivalent to some second-order *RLC* circuits composed of independent inductances, capacitances, and resistances in series. Z_{11} is equivalent to the R_S–R_G–L_S–L_G–C_S–C_G series circuit, Z_{12} and Z_{21} are equivalent to the same R_G–L_G–C_G series circuit, and Z_{22} is equivalent to the R_D–R_G–L_D–L_G–C_D–C_G series circuit. Notably, as a standard form of a two-port network, the equivalent capacitances (C_G, C_D, and C_S) are star–connection in Figure 2B. The capacitor star–connection is converted to a delta–connection through (8)–(10) to extract the

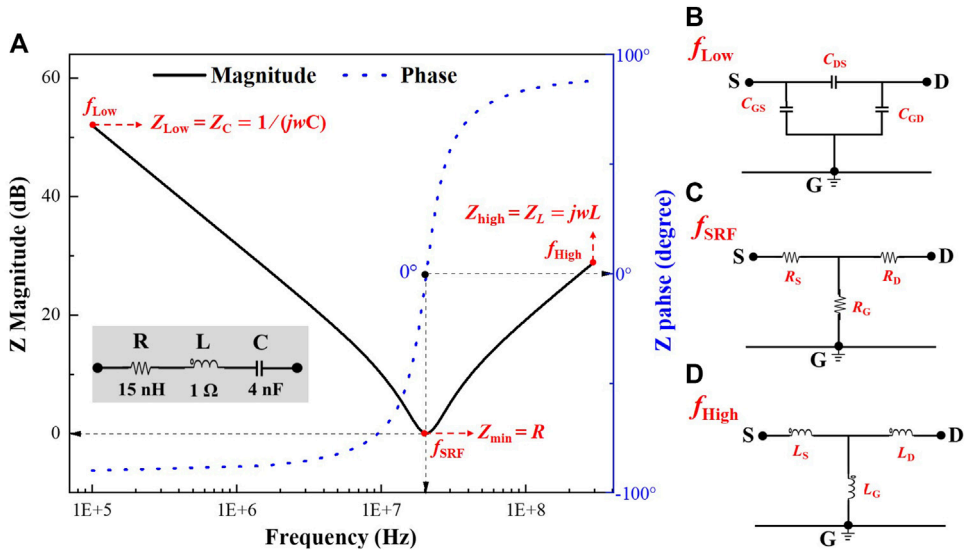

FIGURE 5
(A) Impedance magnitude and phase curve of series *RLC* circuit. **(B)** Two-port network representation of the MOSFET at low frequency f_{Low}. **(C)** Two-port network representation of the MOSFET at the self-resonant frequency fSRF. **(D)** Two-port network representation of the MOSFET at high frequency f_{High}.

parasitic capacitances (C_{GS}, C_{DS}, and C_{GD}). Figure 5A shows a typical impedance plot of a series *RLC* circuit, and the element values are L = 15 nH, C = 4 nF, and R = 1 Ω. The series *RLC* circuit impedance value can be expressed by (11), where $w = 2\pi f$ and f is the frequency. The effect of capacitive reactance and resistance can be neglected at high frequency f_{High}. The two-port network representation of the MOSFET can be simplified as Figure 5D, and L can be calculated using (12). At the self-resonance frequency f_{SRF}, inductive reactance and capacitive reactance cancel each other, showing pure resistance characteristics. The two-port network representation of the MOSFET can be simplified as Figure 5C. The resistive components can be determined at the f_{SRF}, and R is calculated from (13). According to the characteristics of a series self-resonance, the parasitic capacitance C can be obtained from (14).

$$C_{GS} = (C_G \cdot C_S)/(C_G + C_D + C_S) \quad (8)$$

$$C_{GD} = (C_G \cdot C_D)/(C_G + C_D + C_S) \quad (9)$$

$$C_{DS} = (C_D \cdot C_S)/(C_G + C_D + C_S) \quad (10)$$

$$Z = Z_C + Z_L + Z_R = R + \left(\frac{-1}{jwC} + jwL\right) \quad (11)$$

$$L = \left(imagZ_{High}\right)/w_{High} \quad (12)$$

$$R = Z_{min} \quad (13)$$

$$C = 1/\left(w_{SRF}^2 \cdot L\right) \quad (14)$$

Figure 6 shows the measuring principle of MOSFET two-port network and the VNA measurement system. To ensure the effective connection between MOSFET and VNA, we need to design a test fixture, which reserves three connection positions and ensures the low inductance connections between VNA and terminals. An effective test fixture needs to ensure 50 Ω impedance match on the transmission path and high isolation between input and output signals. The printed circuit board (PCB) test fixture composes two 50 Ω SMA adaptors, two 50 Ω microstrip lines, and a through-hole. The MOSFET is installed on the PCB test fixture and connected with VNA through SMA. The MOSFET source terminal is interconnected with VNA port 1, the MOSFET drain terminal is interconnected with VNA port 2, and the gate terminal is interconnected with the VNA ground through a PCB through-hole. De-embedding calibration is performed to remove the systematic errors caused by VNA itself, the test cables, adapters, and fixtures before scattering parameter (*S*-parameter) measurement. In this study, we use the 80502D calibration kit provided by Keysight for Short-Open-Load (SOL) to perform the VNA calibration. We also use PCB to design a new "Through" calibration element to extend the measurement plane to the device interface under the test (DUT) plane.

2.2.4 Experimental setup

An accelerated aging test is conducted using power and thermal overstress. The $R_{DS(on)}$ and parasitic parameters of MOSFET at different aging times are extracted, and the quality level of MOSFET is quantified by establishing the numerical correlation model between them. The bond

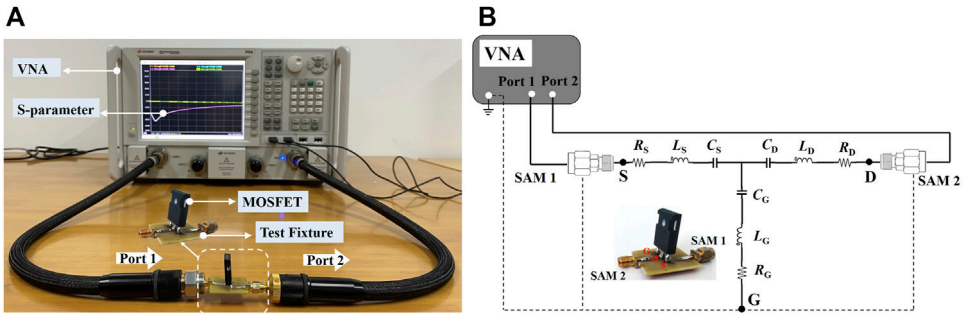

FIGURE 6
(A) Schematic diagram of the parasitic parameter two-port network extraction approach for a discrete MOSFET. **(B)** VNA measurement system, which is composed of one VNA, two test cables and the designed PCB test fixture.

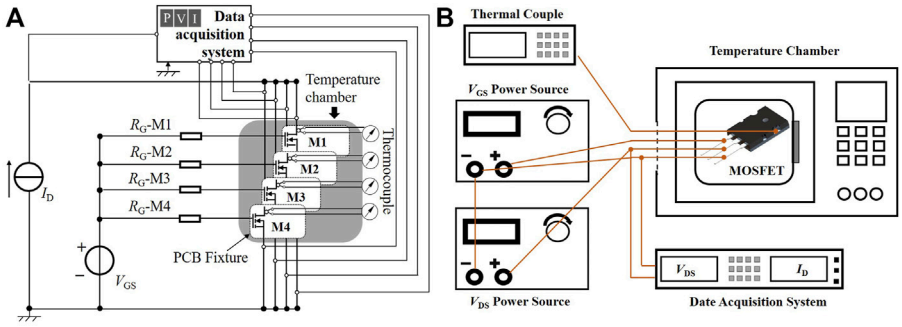

FIGURE 7
(A) Schematic of the accelerated aging experimental and **(B)** accelerated aging setup for MOSFET.

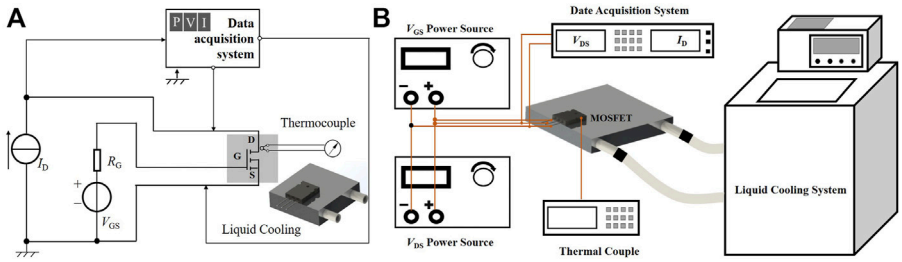

FIGURE 8
(A) Schematic of the $R_{DS(on)}$ test system and **(B)** $R_{DS(on)}$ test setup for MOSFET.

wire faults test is constructed by manually cutting off the bond wires. The parasitic parameters of MOSFET with various bond wire cut-off conditions are extracted, and the bond wire damage is quantified by establishing the numerical correlation model between parasitic parameters and the number of bond wires cut-off.

2.2.4.1 Aging

To determine how the parasitic resistance can effectively quantify the quality level of MOSFET power devices, an accelerated aging experimental platform, and the $R_{DS(on)}$ test platform are set up. Figure 7 depicts the schematic of the accelerated aging setup. The DUT, shown in Figure 7B, is

placed in an accelerated aging station to stress it electrically and thermally. The simultaneous stress is achieved by current flow and thermal during the on-state of the DUT. Figure 8 shows the schematic of the $R_{DS(on)}$ test setup. Multiple MOSFETs are aged for different times and are characterized by the $R_{DS(on)}$ test system and the two-port measurement system. A data acquisition system is used to collect the drain-to-source voltage V_{DS} and the drain-source current I_D to calculate $R_{DS(on)}$. A *k*-type thermocouple is attached to the surface of the MOSFET baseplate to measure the temperature during the accelerated aging in real-time, which is used to feedback and adjust the load current I_D. A liquid cooling system is used to keep the chip junction temperature stable during $R_{DS(on)}$ extraction after accelerated aging. The test steps are as follows:

Step 1: Extract the MOSFET $R_{DS(on)}$ at the desired conditions;

Step 2: Measure the S-parameters over a frequency range of 10–300 MHz, as shown in Figure 6;

Step 3: Convert the measured *S*-parameters to Z-parameters to calculate the parasitic parameters;

Step 4: Age the MOSFETs according to the above requirements;

Step 5: Repeat steps 1–4.

2.2.4.2 Bond wire fault

To reduce the experimental time, the approach of shearing off bond wires is demonstrated to simulate the fatigue of bond wires. In this study, a 1000 V N- channel power MOSFET in a TO–247 package (IXFK32N100P) is used to analyze the correctness of L_S as the precursor to identifying bond wire fault. First, we use laser equipment to remove the epoxy layer of MOSFET to expose the bond wire completely. Then, the bond wire faults are simulated by manually cutting off the bond wires individually, and the L_S is extracted by using the two-port *S*-parameter measurement system. The implementation steps are as follows:

Step 1: Remove the EMC with a laser device to expose the bond wires;

Step 2: Measure the *S*-parameters over a frequency range of 10–300 MHz;

Step 3: Convert the measured *S*-parameters to *Z*-parameters and calculate the initial parasitic inductance L_S;

Step 4: Cut off the bond wire to make a damage model;

Step 5: Repeat steps 2–4 until only one bond wire is left for the interconnection between the source and drain of the MOSFET.

3 Experimental results and discussion

3.1 Validation parasitic parameter extraction for MOSFET in TO-247

In this paper, a 400V N-Channel discrete MOSFET (IRFP340) in a TO–247 package is used to verify the two-port measurement technique. The values of Z_{11}, Z_{12}, Z_{21}, and Z_{22} can be calculated using Eqs 15–17 based on the two-port network. At a high frequency f_{High}, the contribution of capacitance and resistance to the *RLC* circuit impedance can be ignored, whereas the high-frequency impedance can be equal to the inductive reactance. Individual inductances L_S, L_G, and L_D can be extracted through Eqs 18–20. At the f_{SRF}, the contribution of capacitance and inductance to the *RLC* circuit impedance can be neglected. Individual resistances R_S, R_G, and R_D can be extracted using Eqs 21–23. The individual capacitances C_S, C_G, and C_D are obtained by plugging in the extracted L_S, L_G, and L_D to the f_{SRF} expression Eq. 14, respectively. Finally, the capacitor star–connection is converted to a delta–connection to extract C_{GS}, C_{GD}, and C_{DS} through Eqs 8–10. First, the *S*–parameter of the MOSFET was obtained from VNA measurement and converted into Z–parameters. Then, the parasitic inductances, capacitances, and resistances were accurately calculated from *Z*–parameters. After extracting the parasitic parameters, we also plug these values back into the established MOSFET two-port network model (as shown in Figure 4) for Advanced Design System (ADS) circuit simulation to verify the small-signal equivalent circuit and the general parasitic parameters extraction methodology. Figure 9 shows the frequency response curves of the *Z*-parameters obtained from ADS simulation and VNA experimental measurement. The ADS simulation curve (red dashed line) is in good agreement with the experimental value (black solid line), which validates the mathematical formulas and extraction approach mentioned in Section 2.2.3. In addition, the secondary validation approach is realized by comparing the extracted inductances from the proposed VNA measurement at the f_{High} with the MOSFET datasheet values. The parasitic inductances L_S and L_D obtained from the proposed two-port extraction technique are 12.358 and 5.262 nH, respectively. Considering the unavoidable measurement error, the extracted capacitances are consistent with the datasheet values (L_D = 5 nH, L_S = 13 nH, 6 mm from package and center of die contact), and the mismatch is 4.94% and 5.24%, respectively. The experimental results show that the proposed two-port network methodology is suitable for accurately extracting the parasitic parameters of discrete power MOSFETs.

$$\boldsymbol{Z}_{11} = \boldsymbol{X}_{L_S} + \boldsymbol{X}_{L_G} + \boldsymbol{X}_{R_S} + \boldsymbol{X}_{R_G} + \boldsymbol{X}_{C_S} + \boldsymbol{X}_{C_G} \tag{15}$$

$$\boldsymbol{Z}_{12} = \boldsymbol{Z}_{21} = \boldsymbol{X}_{L_G} + \boldsymbol{X}_{R_G} + \boldsymbol{X}_{C_G} \tag{16}$$

$$\boldsymbol{Z}_{22} = \boldsymbol{X}_{L_D} + \boldsymbol{X}_{L_G} + \boldsymbol{X}_{R_D} + \boldsymbol{X}_{R_G} + \boldsymbol{X}_{C_D} + \boldsymbol{X}_{C_G} \tag{17}$$

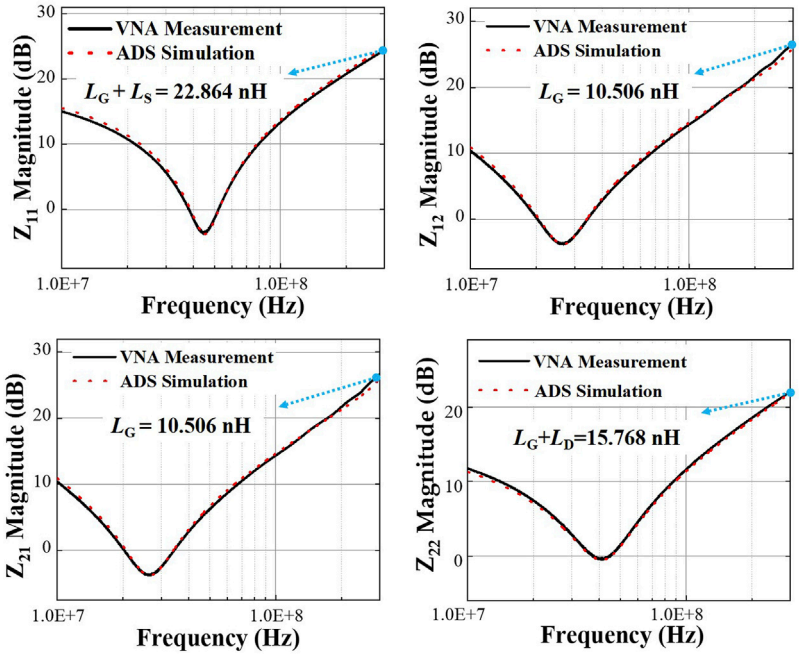

FIGURE 9
Z-parameters obtained from VNA experimental measurement and ADS simulation.

$$L_S + L_G = \mathbf{imag}\left(Z_{11\_High}\right)\Big/ w_{11\_High} \tag{18}$$

$$L_G = \mathbf{imag}\left(Z_{12\_High}\right)\Big/ w_{12\_High} \tag{19}$$

$$L_D + L_G = \mathbf{imag}\left(Z_{22\_High}\right)\Big/ w_{22\_High} \tag{20}$$

$$R_S + R_G = Z_{11\_min} \tag{21}$$

$$R_G = Z_{12\_min} \tag{22}$$

$$R_D + R_G = Z_{22\_min} \tag{23}$$

3.2 Quality level estimation of MOSFET

The IRFP340 N-Channel MOSFETs are installed on the PCB fixture and then placed in a temperature chamber at 100°C to perform aging. A 15 V DC gate-source voltage V_{GS} [$>V_{GS(TH)}$] is applied across the G–S terminals to turn on the MOSFETs fully, and a constant drain-source current I_D = 1.65 A is applied across the D–S terminals to generate sustained power stress during the accelerated aging procedure (Figure 7). The baseplate temperature of MOSFET reaches 190°C within 10 min, which is stabilized at (210 ± 2) °C, and the power loss is ≈5.14 W during the entire accelerated aging process. R_{DS} and parasitic parameters of the MOSFET are extracted as a reference before aging, the initial $R_{DS(on)}$ is approximately equal to 0.4023 Ω. A liquid cooling system is used to adjust the heat dissipation to keep the baseplate temperature of the MOSFET at (25 ± 0.1) °C, to ensure the stability of the chip junction temperature during the $R_{DS(on)}$ test. The V_{GS} is set to 10 V according to the test requirements from the datasheet, and the I_D is selected as 2.0 A while taking the measurements of $R_{DS(on)}$ using the data acquisition system.

Usually, MOSFETs are remarkably stable for a period before rapid degradation. The degradation process of $R_{DS(on)}$ is divided into two stages: the delay stage and the degradation stage. Like the results of the degradation of the formula (1), the $R_{DS(on)}$ variation is found to be exponential to a certain value. Table 1 summarizes the $R_{DS(on)}$ and parasitic parameters extracted at different aging times. Aged for 10 h, $R_{DS(on)}$ remains almost unchanged, indicating that the MOSFET is in the stable stage. When the cumulative aged time is 20 h, $R_{DS(on)}$ increases by 38.30 mΩ, indicating that the MOSFET is degraded. Therefore, the duration aged time is adjusted to 5 h to control the degradation speed of the MOSFET. The cumulative values of R_D + R_S and $R_{DS(on)}$ are highly consistent with the increase of aged time, as shown in Figure 10B, which conforms the assumption of (7). Meanwhile, R_D + R_S and $R_{DS(on)}$ have a quasi-linear positive correlation, this finding is consistent with our theoretical analysis in Section 2.2.1 However, the calculated change rate of R_D + R_S is 5%–6% higher than that of $R_{DS(on)}$ at different aging time. Since R_D + R_S is a newly proposed precursor, more studies are needed to support it to become an acceptable standard for quantifying the aging degree of MOSFETs. In the

TABLE 1 $R_{DS(on)}$ and parasitic resistances at different aged time.

Cumulative aged time (h)	$R_{DS(on)}$		$R_D + R_S$		R_G
	$R_{DS(on)}$ Ω	Quality level %	$R_D + R_S$ Ω	Change %	
0	0.4023	0.00	0.3103	0.00	0.6456
10	0.4053	0.75	0.3141	1.22	0.6373
20	0.4436	10.27	0.3576	15.24	0.6403
25	0.4700	16.83	0.3737	20.43	0.6403
30	0.5265	30.87	0.4246	36.84	0.6409
35	0.5950	47.90	0.4763	53.82	0.6372

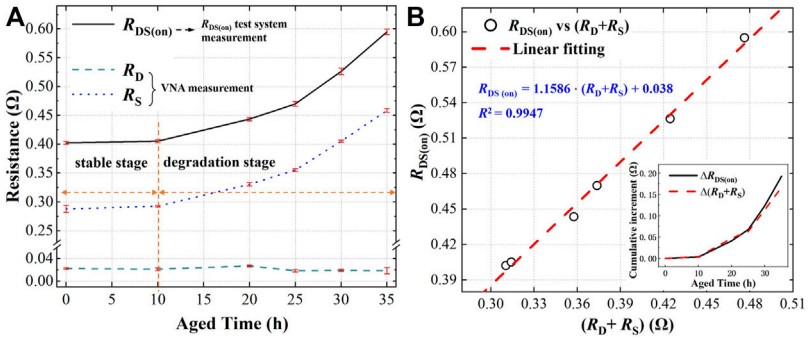

FIGURE 10
(A) Measured $R_{DS(on)}$, R_D, and R_S of MOSFET at different aging times ($R_{DS(on)}$ is measured by $R_{DS\ (on)}$ test system, R_D and R_S are extracted from the VNA measurement). **(B)** Relationship between $R_{DS(on)}$ and $R_D + R_S$.

power electronics industry, $R_{DS(on)}$ has been widely accepted as a general evaluation standard for qualifying MOSFETs' aging level. To visually describe the degradation degree of MOSFETs, $R_{DS(on)}$ can be quickly predicted through the fitting relationship between $R_D + R_S$ and $R_{DS(on)}$.

For power MOSFETs, the failure threshold can be considered as a 25% increase in $R_{DS(on)}$ relative to its initial value. The $R_{DS(on)}$ change ratio can be used to measure the approximate quality level of MOSFETs, quality level = $|$aged $R_{DS(on)}$—$R_{DS(on)\_init}|/R_{DS(on)\_init}$]. The quality level in the case of those aged 30 h is 30.87%, which is more than 25%. Figure 10B is drawn by using the data summarized in Table 1. It shows the relationship between $R_{DS(on)}$ and $R_D + R_S$ values. This relationship can be quantified by using the basic fitting tool in MATLAB, as shown in (24).

$$\mathbf{R_{DS(on)} = 1.1586 \cdot (R_D + R_S) + 0.038} \quad (24)$$

Once the initial $R_{DS(on)}$ and corresponding $R_D + R_S$ are known, the predicted $R_{DS(on)}$ and approximate quality level after accelerated aging can be easily determined from the $R_D + R_S$. Six new IRFP–340 MOSFETs (i.e., M1, M2, M3, M4, M5, and M6) are aged for different time durations using power and thermal overstress in a controlled environment to verify the accuracy of the fitting function (24) by applying similar stress. The $R_{DS(on)}$ of MOSFET M1 to M6 may be predicted by (24) using the $R_D + R_S$ values measured by VNA. A 1.92 A constant current I_D is applied across the drain-source terminals for extremely accelerated aging of the MOSFET, whereas the ambient temperature is 100°C. The power dissipation across each MOSFET is ≈6.97 W, and the baseplate temperature is stabilized at (235 ± 2) °C during the extremely accelerated aging procedure. M1, M2, M3, M4, M5, and M6 are aged according to the aging mentioned above process, including M1 aged for 10 h, M2 aged for 20 h, M3 aged for 30 h, M4 aged for 40 h, M5 aged for 50 h, and M6 aged for 60 h. Table 2 presents the measured $R_{DS(on)}$ values, measured $R_D + R_S$, $R_{DS(on)}$ values predicted using (24), and quality level. Owing to the sharp increment in $R_{DS(on)}$ of M6, the $R_D + R_S$ is significantly larger than other MOSFETs, and the quality level exceeds 100%. Therefore, this MOSFET can be considered damaged. The predicted $R_{DS(on)}$ of all MOSFETs except M6 is nearly equal to the actual measured $R_{DS(on)}$ value, whereas the maximum error percentage between them is less than 2%. The maximum error percentage of the predicted and the measured quality level is less than 3%, giving us sufficient confidence in our proposed quality level quantification approach.

TABLE 2 Comparison between predicted $R_{DS\ (on)}$ using (24) and measured $R_{DS\ (on)}$.

NO.	Aging condition	$R_D + R_S$ with VNA system			$R_{DS(on)}$ with $R_{DS(on)}$ test system		Comparison of $R_{DS(on)}$	
		Not aged (Ω)	Aged (Ω)	Predicted $R_{DS(on)}$ using (24) (Ω)	Not aged (Ω)	Aged(Ω)	Predicted quality level (%)	Measured quality level (%)
M1	235°C, 10 h	0.3077	0.3388	0.4354	0.3992	0.4305	7.85	7.49
M2	235°C, 20 h	0.3103	0.3663	0.4624	0.4037	0.4574	14.54	13.30
M3	235°C, 30 h	0.3133	0.3932	0.4936	0.4053	0.5025	21.78	23.98
M4	235°C, 40 h	0.3146	0.4952	0.6118	0.4063	0.6044	50.57	48.76
M5	235°C, 50 h	0.3122	0.5159	0.6357	0.4032	0.64555	58.10	60.54
M6	235°C, 60 h	0.3143	0.9528	1.1344	0.4034	1.0947	181.21(fail)	171.37 (fail)

However, in the case of M6, the predicted accuracy of (24) has a small deviation. The error between the actual measured $R_{DS(on)}$ and the predicted $R_{DS(on)}$ is 3.63%, and the error between the actual and predicted quality levels is 9.84%. Extreme thermal stress forces M6 to degrade seriously, resulting in very high $R_{DS(on)}$ (>3 × initial $R_{DS(on)}$), which makes it difficult to accurately control the chip junction temperature, so the measured value of R_{DS} will also have errors. However, although a mismatch exists between the predicted quality level and the actual measured quality level of M6, the serious degradation damage of the MOSFET can still be identified based on $R_D + R_S$. Compared with the $R_{DS(on)}$ precursor parameter highly dependent on T_j, V_{gs}, and I_D, the parasitic resistance without MOSFET power on the test proposed by us has better advantages in quantifying the quality level.

Figure 11 shows X-ray and C-SAM graphs of the four MOSFETs with different extremely aging times. In the X-ray photographs of M1–M4, the delamination regions are marked with red rectangles. From the X-ray image, the delamination of M1 and M2 only occurs between the source metal layer and epoxy layer, whereas the delamination of M2 is more evident. With the increase of extremely accelerated aging time, in M3 and M4, delamination occurs between the source metal layer and epoxy layer and between the drain metal layer and the solder layer. A slight "bulge" is observed on the top of M4, where the die is located, indicating that the epoxy layer is seriously separated from the die. Then, the die area is observed with C-SAM images. The yellow and red spots accompanied by the unexpected frequency responses observed on the surfaces indicate of delamination. Evidently, the yellow and red regions in M1–M4 increase, in turn, indicating that extremely accelerated thermal aging effectively forces the degradation of MOSFETs.

In summary, the impedance magnitude of MOSFET at the f_{SRF} carries the available and critical information strongly related to aging degradation. Using the linear fitting formula between $R_D + R_S$ and $R_{DS(on)}$, the quality level in MOSFET can be quickly identified by comparing the percentage change between predicted $R_{DS(on)}$ and initial $R_{DS\ (on)}$. This finding is a novel discovery, providing an effective quality screening technology for power semiconductor devices without power on treatment.

3.3 Bond wire fault quantitative assessment of MOSFET

Middle- and high-power MOSFETs generally use some parallel aluminum bond wires for the electrical path between the chip and the source terminal. For IXFK32N100P 1000V 32A N-channel MOSFET considered, for instance, six parallel bond wires with a diameter of 0.279 mm exist between the source-electric and source-terminal. Figure 12 shows the

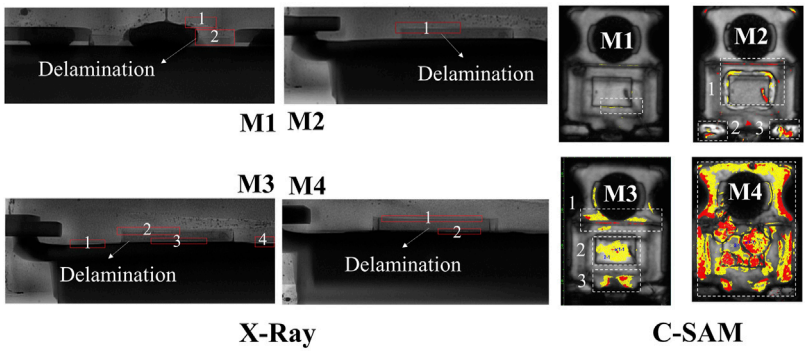

FIGURE 11
X-ray and SAM graphs of MOSFETs.

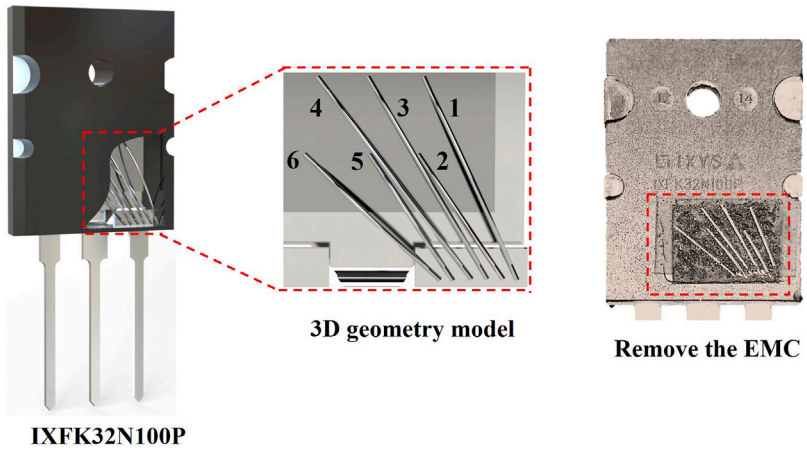

FIGURE 12
Internal structure of the MOSFET, whereas each bond wire is marked with serial number.

internal structure of IXFK-32N100P and the serial number marked on each bond wire. The damage model is established by cutting off the bond wire, including one bond wire fault (cut off No. 1), two bond wires fault (cut off No. 1 and No. 2), three bond wires fault (cut off No. 1, No. 2, and No. 3), four bond wires fault (cut off No. 1, No. 2, No. 3, and No. 4) and five bond wires fault (cut off No. 1, No. 2, No. 3, No. 4, and No. 5).

The position of six bond wire pads on the die and six pads on the source terminal is extracted from a dissembled package. The 3D geometry model of the MOSFET power device is established based on the actual size mapping, and the damage model is defined by cutting off the bond wires one by one. Then, the 3D model is imported into the Q3D-extractor finite element software to calculate the inductance of the commutation loop defined by the current path between the chip source and the source terminal. Figure 13 shows the source inductance $L_{\text{Source-BW}}$ with different amounts of bond wires cut-off. This indicates that an approximately positive correlation exists between the number of bond wire faults and $L_{\text{Source-BW}}$. When one or two bond wires are cut-off, the percentage change of $L_{\text{Source-BW}}$ is close to 1.46% and 7.09%, respectively. Even the slight degradation of the bond wire can still show high sensitivity. These results indicate that the proposed bond wire damage detection approach is reasonable.

In the MOSFET small signal-equivalent circuit model (Figure 1), the parasitic inductance of the source generated by bond wires is combined into L_S. Therefore, theoretically, the lift-off of source bond wires will directly and evidently cause the change of L_S. Figure 14 shows the Z-parameter frequency response curves of different bond wire faults. At high

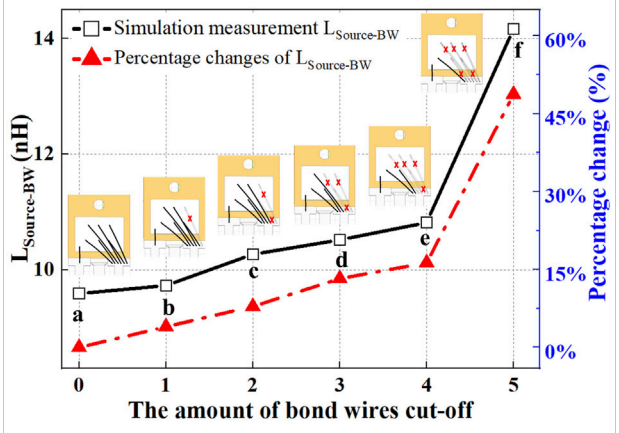

FIGURE 13
$L_{Source-BW}$ at different amounts of bond wires cut-off. a = 9.59 nH, b = 9.73 nH, c = 10.27 nH, d = 10.52 nH, e = 10.82 nH, f = 14.17 nH.

frequency f_{High}, Z_{11} ($Z_{11\_High} = L_S + L_G$) increases significantly with the number of bond wires cut off, but Z_{12} ($Z_{12\_High} = L_G$), Z_{21} ($Z_{21\_High} = L_G$), and Z_{22} ($Z_{22\_High} = L_G + L_D$) are almost unchanged. This case indicates that the parasitic inductance of the source rises with the increase of the number of bond wires cut-off, which is reflected in the increase of L_S. The ratios expressed as percentage change are calculated to define the degree of bond wire degradation. Percentage changes of Z_{11} and L_S are the different ratios of the measured value with the actual device compared with the initial value of the fault-free DUT. At 300 MHz, the percentage change in Z_{11}-parameters of each model is close to 1.90%, 4.04%, 6.66%, 8.67%, and 23.70%, respectively.

Figure 15 indicates that the L_S has an increment with the degradation of bond wires, which has the same change trend as the $L_{Source-BW}$ obtained by finite element analysis, and the offset is less than 0.5 nH. This finding further verifies the correctness of L_S extracted approach from the proposed two-port network measurement and the feasibility of L_S as a precursor. For ease of description, we define that 1 or 2 bond wires lift-off can be regarded as "slight fault," and 3, 4, or 5 bond wires lift-off is "serious fault." When 1 or 2 bond wires fail, L_S increases from 9.19 to 9.55 and 9.91 nH, 3.99% and 7.87% higher than the initial value, respectively. Notably, in the case of "slight fault," L_S shows sensitive changes and has good identifiability. This case means that the proposed approach can distinguish a slight fault with high discrimination. In the case of "serious fault," L_S increases sharply, and the percentage changes of L_S are 13.25%, 16.29%, and 48.71%, respectively. Therefore, regardless of a "slight fault"

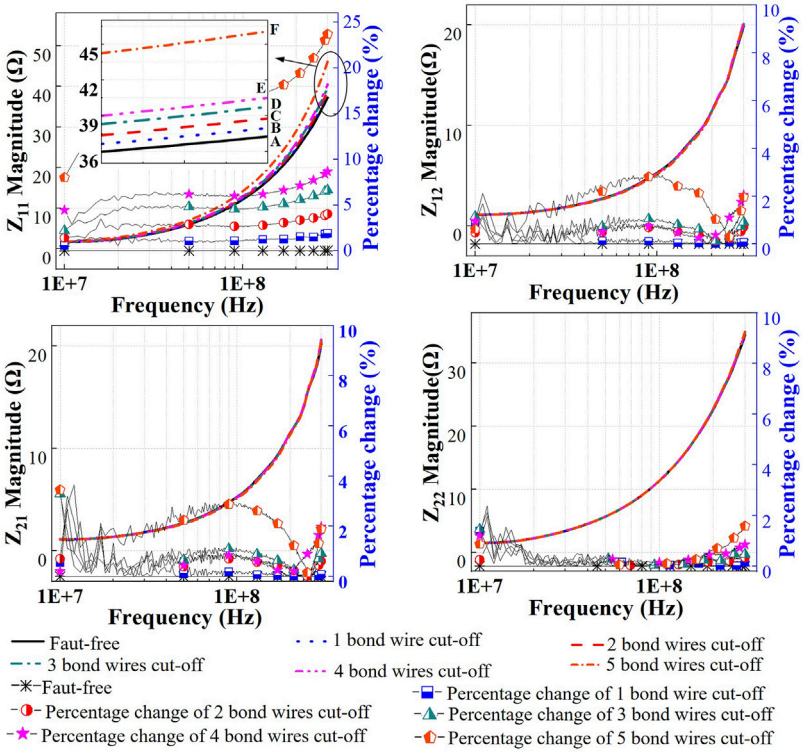

FIGURE 14
Z-parameters of IXFK32N100P MOSFET with different numbers of bond wire cut–off. (A = 37.24 Ω, B = 37.95 Ω, C = 38.74 Ω, D = 39.72 Ω, E = 40.47 Ω, F = 46.06 Ω).

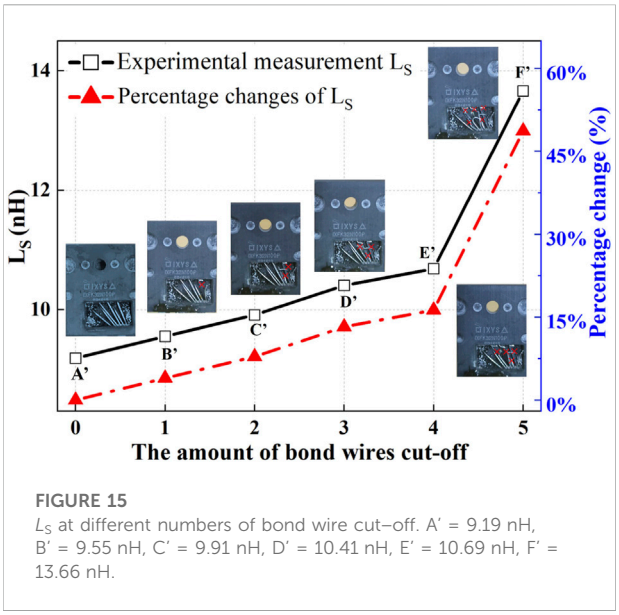

FIGURE 15
L_S at different numbers of bond wire cut–off. A′ = 9.19 nH, B′ = 9.55 nH, C′ = 9.91 nH, D′ = 10.41 nH, E′ = 10.69 nH, F′ = 13.66 nH.

or "serious fault," the source parasitic inductance has a high resolution as a precursor for bond wire damage detection. In conclusion, at high frequency, L_S is very sensitive to the fault of the bond wire, which provides a theoretical basis for establishing a novel bond wire reliability screening technology.

4 Conclusion

A novel failure quantitative assessment approach to MOSFET power device by detecting parasitic parameters is proposed in this study. The experimental results indicate that source-drain parasitic resistance increases with the increasing quality level and illustrates a quasi-linear positive correlation with $R_{DS(on)}$ in an error of less than 3%. Meanwhile, L_S increases with the fault number of bond wires. It has high sensitivity and can show a satisfactory recognition even for slight faults. Therefore, the aging degradation level (metallization reconstruction and die-attach solder delamination) and bond wire failure degree can be quantified by detecting the source-drain parasitic resistance and the source parasitic inductance, respectively.

WBG power devices are also packaged *via* wire-welding packaging process. Hence, the packaging failure are always caused by the solder layer degradation and bond wire failure. Since the junction capacitance of the WBG power device is smaller, it has a high f_{SRF}. Skin effect forces the increase in parasitic resistance of the conductors, so the source-drain parasitic resistance of the WBG power device is larger than that of the silicon power device. Theoretically, the proposed approach has higher recognition resolution when applied to WBG power devices.

Impressively, parasitic parameters can be obtained through domain measurement technology without turning on MOSFETs. Compared with the degradation precursors-based methods, the proposed approach can effectively avoid the influence of chip self-heating and external loading test parameters (such as source-drain current, gate-source voltage, and others) on testing results and is suitable for rapid quality screening of power devices. Moreover, the proposed approach can quantify the actual aging degree of the power devices compared with the morphology characteristics-based methods and quickly predict the type of package failure by identifying the changes of parasitic parameters in a single measurement. Providing an effective quality screening way for power devices and raising an on-line quality monitoring technology for the manufacturing process are promising [42].

Data availability statement

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding authors.

Author contributions

MY: Conceptualization, Data curation, Investigation, Methodology, Original draft. DY: Investigation, Review, Supervision, and editing. SH: Investigation, Methodology, and editing. MC: Conceptualization, Investigation, Methodology, and editing. JX: Methodology, Review, and Funding acquisition. KZ: Data curation; G-QZ: Investigation, Methodology, and Guidance.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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