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A Ring-Oscillator Sub-Sampling PLL With Hybrid Loop Using Generator-Based Design Flow

Zhongkai Wang[1*], Minsoo Choi[2], John Wright[1], Kyoungtae Lee[3], Zhaokai Liu[1], Bozhi Yin[1], Jaeduk Han[4], Sijun Du[5], Elad Alon[1]
[1]University of California, Berkeley, CA, [2]Samsung Semiconductor, Inc., San Jose, CA
[3]University of California, San Francisco, CA, [4]Hanyang University, Seoul, South Korea
[5]Delft University of Technology, Delft, Netherlands, *zhongkai@berkeley.edu

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***Abstract*—We present a ring-oscillator-based sub-sampling phase-locked loop (PLL) using a generator-based design flow. A hybrid loop with a delta-sigma ($\Delta\Sigma$) modulator is applied to reduce the loop filter (LF) area and the control ripple. The generator automatically produces the ring oscillator and PLL to meet the provided specifications. The 10-GHz PLL instance implemented in 28-nm planar process achieves RMS jitter of 299.5 fs and power of 9.9 mW from a 1-V supply.**

***Index Terms*—PLL, sub-sampling, ring oscillator, hybrid, PLL generator**

I. Introduction

High-performance phased-locked loop designs are a critical component for generating clean clocks for wireline communications, wireless communications, and processors. In addition to the stringent phase noise and jitter requirements, design time is a critical issue to meet the time-to-market [1]. A generator-based design flow is an attractive technique to reduce design time, as it enables engineers to quickly re-generate designs and physical layouts for different specifications and technologies.

Compared to LC-oscillator-based PLLs, ring-oscillator-based PLLs provide inferior jitter and phase noise performance due to the lack of resonate tanks. However, when these requirements are relaxed, ring-oscillator-based PLLs are preferable for their simplicity and smaller area. The sub-sampling PLL (SSPLL) [2] is a candidate to improve the phase noise performance of ring-oscillator-based PLLs, as the phase noise contribution of the charge pump is reduced with its large phase detector (PD) gain due to the high VCO output slope. However, the capacitors of the loop filter must be large to set the loop bandwidth and ensure loop stability, while a digital loop filter consumes less area and provides more programmablity.

A generator framework [1] was introduced to enable fast analog and mixed-signal (AMS) circuit designs using executable generators, which produces DRC- and LVS-clean schematics, layouts and test benches. Designers are allowed to codify their design procedures into design scripts for automatic design iteration loops, drastically reducing the design and validation time. [3] and [4] demonstrate the generator-based circuit design methodologies for a SerDes front-end and a LC-based PLL, which produce circuits that are comparable with manual designs. However, a ring-oscillator-based PLL using this design flow has not been presented.

In this paper, we present a SSPLL using a ring oscillator and hybrid loop to eliminate the bulky capacitor. In the hybrid loop architecture, the analog proportional path offers a fast response to meet the phase noise target, and the digital integral path provides frequency control with minimized ripple using a $\Delta\Sigma$ modulator. Furthermore, the PLL is produced with a top-down and bottom-up generator-based design flow similar to [4], demonstrating phase noise performance and power consumption comparable to manual designs.

The paper is organized as follows. Section II describes the architecture of the SSPLL and design of critical blocks. The system analysis and generator-based design flow are presented in Section III. Section IV summarizes the simulation results of the design, and Section V draws the conclusion.

II. PLL Architecture and Block Design

In an analog SSPLL, the loop filter is split into two parts: a resistor-based proportional path for phase locking and a capacitor-based integral path for frequency locking. While the capacitor usually consumes a large area, it can be replaced by a digital integral path, which can be smaller by taking advantage of technology scaling. To implement the digital integral path, the sub-sampling phase detector (SSPD) and dead-zone phase detector (DZPD) are connected to a comparator and flip-flop, respectively. The digital outputs are summed together and filtered by a digital integrator, which is followed by a voltage digital-to-analog converter (DAC) to control the frequency of the ring oscillator.

To avoid large area, the resolution of the DAC used in this design is limited to 9 bits. As the 9-bit DAC is too coarse to control the oscillator to get the precise frequency, the integral LF output dithers between several levels near the target frequency to reach the average desired voltage. When simulating the hybrid SSPLL with the DAC and target frequency of $10\ GHz$, the peak-to-peak ripple voltages observed on the proportional control voltage and the integral control voltage of the VCO are $23.8\ mV$ and $5.1\ mV$ respectively, as shown in Fig. 1. The ripples on the integral control and the proportional control will create in-band spurs on the phase noise and spectrum and increase the integrated RMS jitter.

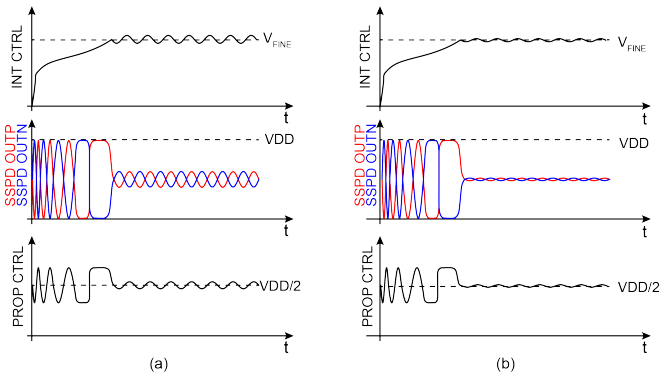

Fig. 1. Diagram of hybrid PLL integral control, SSPD outputs and proportional control (a) without and (b) with $\Delta\Sigma$ modulator.

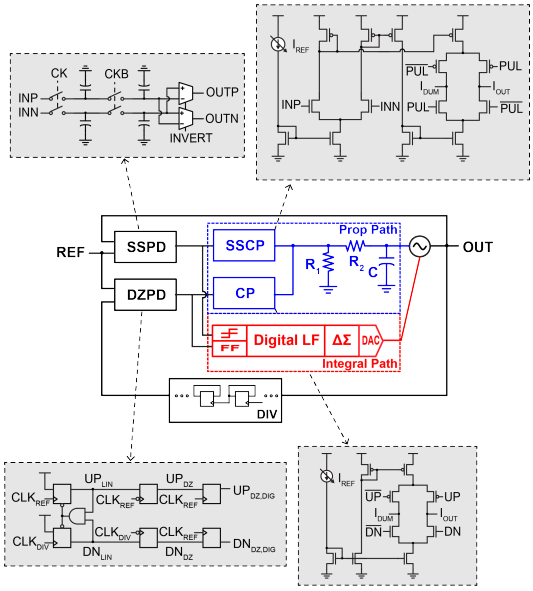

Fig. 2. PLL architecture.

Therefore, a $\Delta\Sigma$ modulator is inserted between the digital LF and DAC to realize a higher-resolution $\Delta\Sigma$ DAC to address this issue.

The architecture of the hybrid SSPLL is shown in Fig. 2, with detailed circuit diagrams of the sub-sampling phase detector (SSPD), sub-sampling phase detector (SSCP), dead-zone phase detector (DZPD) and charge pump (CP). The ring voltage-controlled oscillator (VCO) drives the SSPD and a divider chain. The SSPD compares the phases of the reference clock and the VCO output directly and drives the SSCP and a buffer to avoid kick-back noise and clock coupling from the following comparator. At the same time, the DZPD measures the frequency difference of the reference clock and the output of the divider chain to drive a CP and a synchronizing flip-flop.

In the proportional path, the currents of the SSCP and the CP are summed into the analog loop filter. The integral path adds the comparator and the FF outputs with programmable gains, and the added output is filtered by a digital integrator.

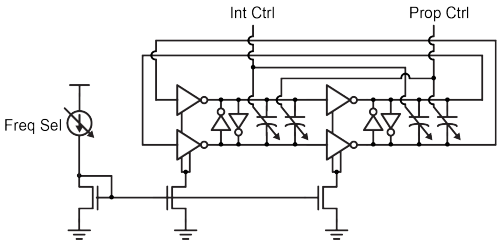

Fig. 3. Ring oscillator.

The integrator is connected to the $\Delta\Sigma$ modulator, which controls the VCO through a 9-bit DAC.

A. Ring Oscillator

Fig. 3 shows the circuit diagram of the ring oscillator. The VCO core includes four inverters with tail bias and four cross-coupled-pair inverters, which set the initial conditions and resolve DC latch-up [5]. The latch ratio, the ratio of the main inverter size and the cross-coupled inverter size, is set to 0.58 for the target technology to guarantee the stable start-up of the oscillator. The VCO structure includes three frequency control knobs to provide enough frequency control range and resolution. Two varactors for proportional and integral frequency tuning are added to the VCO core, with the proportional gain and integral gain being $110MHz/V$ and $450MHz/V$, respectively. The frequency band is selected by the tail current, with a total oscillation frequency range from 5.6 to 10.5 GHz.

B. Delta-Sigma Modulator

Considering the trade-offs among complexity, reliability, and performance, the PLL adopts a second-order $\Delta\Sigma$ modulator (Fig. 4 (a)) to reduce the quantization noise of the DAC. The feed-forward structure with extra input feed-in eliminates the observed DC components at the integrator outputs and the risk of instability. Figure 4 (b) shows the simulation and calculation results of the $\Delta\Sigma$ modulator, which pushes the quantization noise to higher band of the oversampling frequency. Therefore, after a low-pass filter with a corner frequency of ~ 60 MHz, the frequency error can be largely reduced, and the ripple caused by the frequency error becomes almost three times smaller than the original hybrid SSPLL.

III. Generator-Based Design Flow

The PLL is designed with a generator-based design methodology to speed up the design process and technology migration. First, the schematic and layout scripts are implemented for each block to create DRC- and LVS-clean layouts, which are then combined to create the top-level layout. The specifications of the blocks are derived from system design and analysis, and the building blocks are generated by sizing the devices directly or with an iterative loop method.

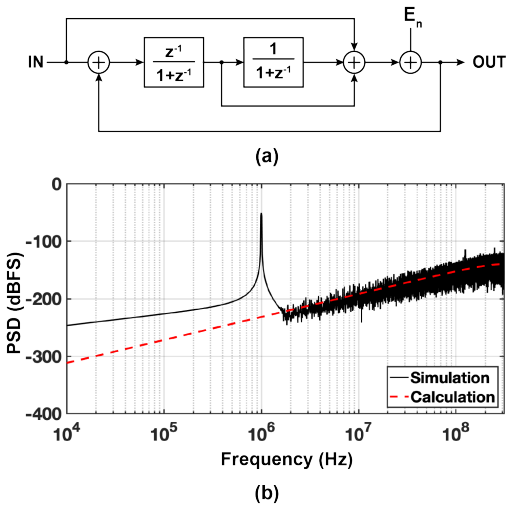

Fig. 4. (a) $\Delta\Sigma$ modulator and (b) its simulation and calculation results.

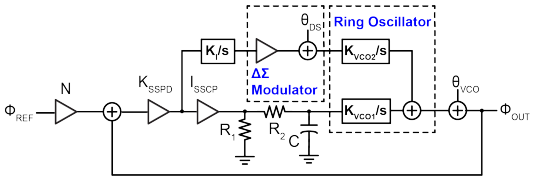

Fig. 5. PLL model.

A. System Analysis and Design

Fig. 5 shows the model of the PLL. The DZPD and CP are excluded in the model, as they are ineffective when the loop is locked. The SSPD and SSCP are modeled by K_{SSPD} and I_{SSPD}, and the integral path is replaced with a gain block K_I/s, followed by a buffer and filtered quantization noise θ_{DS} to model the $\Delta\Sigma$ modulator. The ring oscillator is modeled by the gain blocks of K_{vco1}/s and K_{vco2}/s to describe the proportional and integral gain, with the VCO phase noise modeled by a noise block θ_{vco}. In the SSPLL, the noise contribution of the CP is negligible. If we assume that the noise of the filtered $\Delta\Sigma$ modulator is low, the dominant noise sources are the reference clock and ring oscillator, and their noise transfer functions are shown in Equations 1 and 2.

$$\frac{\phi_{out}}{\phi_{ref}} = \frac{K_{pd}N(sI_{cp}R_1K_{vco1} + K_IK_{vco2})}{s^2 + sK_{pd}I_{cp}R_1K_{vco1} + K_{pd}K_IK_{vco2}} \quad (1)$$

$$\frac{\phi_{out}}{\phi_{vco}} = \frac{1}{s^2 + sK_{pd}I_{cp}R_1K_{vco1} + K_{pd}K_IK_{vco2}} \quad (2)$$

The oscillator phase noise is dominant when the loop bandwidth is small; otherwise, the reference noise dominates the PLL phase noise. Fig. 6 (a) shows the PLL jitter integrated from $1KHz$ to $100MHz$ versus the loop bandwidth for given reference phase noises and VCO phase noises. The optimal loop bandwidth is around $33MHz$, where the noise contributions of the ring oscillator and reference are equal. As

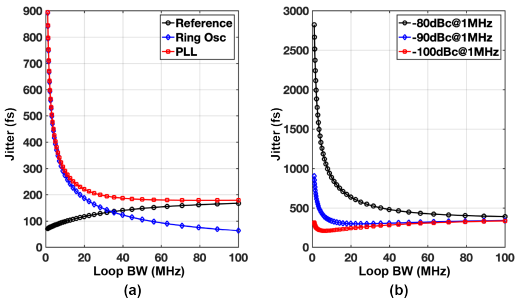

Fig. 6. (a) PLL, VCO and reference jitter versus loop bandwidth, and (b) PLL jitter versus loop bandwidth for VCO phase noises of -80dBc/Hz, -90dBc/Hz, and -100dBc/Hz at 1MHz offset frequency.

the phase noise from the reference is constant, the two design variables that would affect the PLL jitter are the VCO phase noise and loop bandwidth. Fig. 6 (b) shows the PLL jitter with different loop bandwidths under three VCO phase noise specifications at 1 MHz offset: $-80dBc/Hz$, $-90dBc/Hz$, and $-100dBc/Hz$. When the VCO phase noise decreases, the optimal loop bandwidth drops.

B. VCO Design

The main constraints of the ring oscillator are the oscillation frequency and phase noise. First, the ratio α of the main inverter to latch inverter is determined by the start-up condition and optimal phase noise performance [5]. If the size of oscillator is increased by β, the frequency of the ring oscillator is as shown in Equation 3, where N is the number of inverter stages, I_d is the current of the inverter, C_{int} is the internal capacitance, and C_{ext} is the load capacitance.

$$f_0 = \frac{I_d}{2N(C_{int} + \frac{C_{ext}}{\beta})V_{DD}} \quad (3)$$

Therefore, by up-sizing the ring oscillator core, the resonant frequency increases, which is limited by the intrinsic parasitic of the oscillator (Fig. 7 (a)). The phase noise [6] of the ring oscillator is as shown in Equation 4.

$$\mathcal{L}(f) = \frac{2kT}{I}\left\{\frac{1}{V_{DD} - V_t}(\gamma_N + \gamma_P) + \frac{1}{V_{DD}}\right\}\left(\frac{f_0}{f}\right)^2 \quad (4)$$

This is related to the current I, overdrive voltage $(V_{DD} - V_t)$ and noise factors γ_N and γ_P. Hence with a fixed ratio β, we can improve the ring oscillator phase noise by increasing the size of the whole design, which shows a trade-off between phase noise and power (Fig. 7 (b)). As shown in the design flow of Fig. 8, the unit VCO core size is first determined to ensure the start-up and phase noise performance, followed by two iteration loops to resize it to meet the target frequency and phase noise specifications.

IV. Simulation Results and Analysis

A SSPLL instance generated from this design methodology is implemented in a 28nm planar technology, as shown in

TABLE I
PERFORMANCE COMPARISON.

	[5]	[7]	[8]	[9]	[10]	This Work
VCO Structure	Ring	LC	LC	LC	Ring	Ring
Frequency	10 GHz	15GHz	18 GHz	14 GHz	5 GHz	10 GHz
Ref. Clk	625 MHz	1.875GHz	450 MHz	500 MHz	156.25 MHz	625 MHz
Power (mW)	7.6	46.2	29.2	45	15.4	9.9
Technology	65 nm	20 nm	16 nm	16 nm	65 nm	28 nm
Supply (V)	1.2	1.25/1.0	0.9/1.8	N/A	1.2	1.0
Area (mm^2)	0.009	0.044	0.39	0.35	0.06	0.089
RMS Jitter (Integration BW)	414 fs (10K-100M)	268 fs (100k-1G)	164 fs (1K-100M)	53.6 fs (1K-10M)	484 fs (1K-40M)	299.5 fs (1K-100M)
FOM_J (dB)	-238.8	-234.8	-241.0	-246.8	-234.4	-240.5

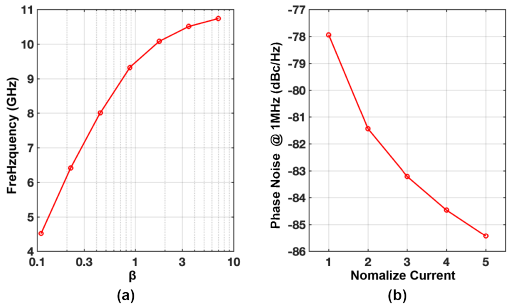

Fig. 7. (a) VCO frequency versus core and load ratio β, and (b) VCO phase noise at 1MHz offset versus normalized current.

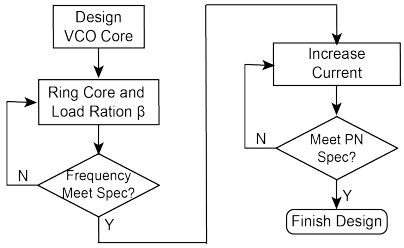

Fig. 8. Ring oscillator design flow.

Fig. 9, occupying an active area of $0.089mm^2$. The PLL output frequency ranges from 5.6 to 10.5 GHz. Fig. 10 shows the phase noise contributions of the blocks in the PLL, including the ring oscillator, the reference and its buffer, CP, and $\Delta\Sigma$ modulator. As expected, the ring oscillator and the reference are the main sources of phase noise. By setting the loop bandwidth to 40 MHz, limited by the $1/10$ of the reference, the RMS jitter of the PLL integrated from $1KHz$ to $100MHz$ is 299.5 fs. Fig. 11 compares the simulated spectrum of the PLL output with and without the $\Delta\Sigma$ modulator. The $\Delta\Sigma$ modulator reduces the VCO control line ripples and the spur by $11.2dB$. The total power of the PLL is $9.9mW$, which leads to a FOM value of $-240.52dB$. Table I compares the design with state-of-the-art PLLs operating at around 10 GHz. With reasonable RMS jitter performance and power consumption, the FOM value is comparable with other manual designs, which verifies the effectiveness of the generator-based design flow for the PLL.

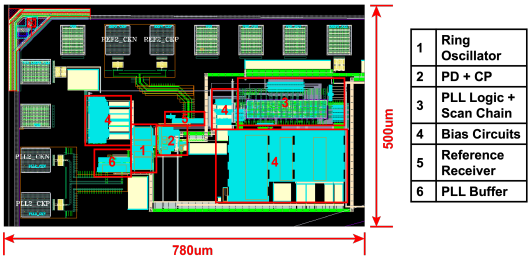

Fig. 9. PLL layout.

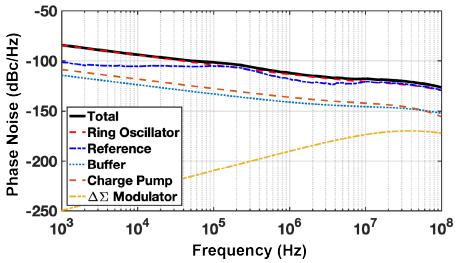

Fig. 10. Phase noise contributions of the blocks in the PLL.

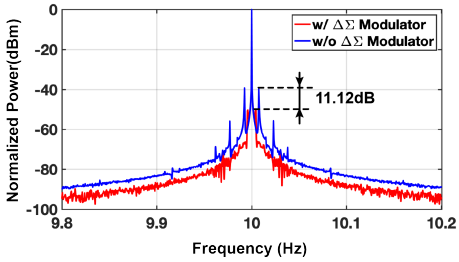

Fig. 11. PLL output spectrum with and without $\Delta\Sigma$ modulator.

V. Conclusion

This paper presents a hybrid SSPLL based on a ring oscillator. To minimize ripple on the frequency control, the digital integral path adopts a $\Delta\Sigma$ modulator. The PLL is produced with a top-down and bottom-up generator-based design flow, showing phase noise and power performance similar to manual designs.

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