A Versatile ± 25-A Shunt-Based Current Sensor With ± 0.25% Gain Error From − 40 ◦ C to 85 ◦ C

Tang, Zhong; Zamparette, Roger; Furuta, Yoshikazu; Nezuka, Tomohiro; Makinwa, Kofi A.A.

DOI
10.1109/JSSC.2022.3204520

Publication date
2022

Document Version
Final published version

Published in
IEEE Journal of Solid-State Circuits

A Versatile ±25-A Shunt-Based Current Sensor With ±0.25% Gain Error From −40 °C to 85 °C

Zhong Tang, *Member, IEEE*, Roger Zamparette, *Graduate Student Member, IEEE*, Yoshikazu Furuta, *Member, IEEE*, Tomohiro Nezuka, *Member, IEEE*, and Kofi A. A. Makinwa, *Fellow, IEEE*

***Abstract*— This article presents a versatile shunt-based current sensor for battery management applications. It digitizes the current-induced voltage drop across an external shunt resistor with the help of a 2nd-order delta-sigma (ΔΣ) ADC, whose summing node is implemented as a low-noise capacitively coupled amplifier. To compensate for the shunt's finite temperature coefficient (TC), the TC of the ADC on-chip voltage reference can be tuned. As a result, the sensor maintains high accuracy when used with low-cost high TC shunts, such as PCB traces, as well as with more expensive low TC shunts, such as metal-alloy resistors. Optimal gain flatness over temperature is achieved by a two-current room-temperature TC tuning scheme, which exploits the shunt's self-heating at high current levels. Fabricated in a standard 0.18-μm CMOS process, the current sensor occupies 0.36 mm^2 and draws 265 μA from a 1.8-V supply. Over the industrial temperature range (−40 °C to 85 °C) and a ±25-A current range, it achieves the state-of-the-art gain error (±0.25%) with both PCB (1.6 mΩ) and metal-alloy (2 mΩ) shunts. With these shunts, it achieves 5.3-mA/4.3-mA (rms) resolution in a 10-kHz bandwidth.**

***Index Terms*— Capacitively coupled amplifier (CCA), current sensing, delta-sigma (ΔΣ) ADC, PCB trace, temperature coefficient (TC), temperature compensation.**

I. Introduction

BATTERY management plays an important role in applications ranging from the Internet of Things (IoT) gadgets to electric vehicles [1]. It typically involves monitoring and controlling the battery state of charge (SOC) as well as the battery state of health (SOH) [2]. One way of determining SOC is by Coulomb counting, i.e., integrating current over time. To avoid error accumulation, this requires current sensors with low offset as well as low gain error [3], [4]. Battery SOH can be estimated by monitoring battery impedance at frequencies up to a few kilohertz [5], [6]. This can be done by injecting a small ac excitation current (voltage) into the battery and then measuring the resulting voltage (current) [7]. Current sensors for such applications should have kilohertz bandwidths and high resolution (e.g., 12 bit) to facilitate rapid calibration and accurate backend processing. Such bandwidths also facilitate the accurate detection of current transients [8].

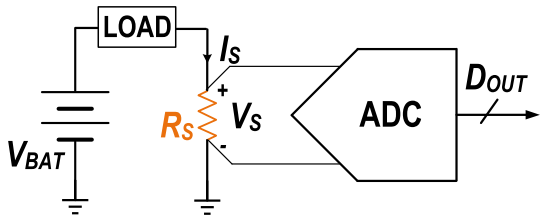


Fig. 1. Block diagram of a low-side sensing shunt-based current sensor.

Although current sensors based on magnetic field sensing can achieve large bandwidths [9], shunt-based current sensors are more accurate (<1%) [3], [4], [10], [11], [12], [13], [14], [15], [16]. As shown in Fig. 1, such sensors use an ADC to digitize the voltage drop Vs caused when a current I_S flows through a small shunt resistor R_S. The current can then be estimated from Ohm's law.

In a shunt-based current sensor, shunt resistance spread and temperature coefficient (TC) are important sources of error. While the former can be corrected by a one-point gain trim, the latter requires the use of a temperature compensation scheme (TCS), which increases system complexity. Although low-TC (tens of ppm/°C) metal-alloy shunts can be used, this comes at the expense of cost [13], [14], [15], [16]. Alternatively, low-cost metal shunts made from on-chip metal traces [3], package lead frames [4], and PCB traces [17], [18] can be used. Despite their large TC (∼0.4%/°C), gain errors of less than 1% over the industrial temperature range (−40 °C to 85 °C) can be achieved by combining them with temperature-compensated ADCs. However, only limited bandwidths (<1 kHz) have been reported [4], [11], [12]. Although shunt readout ADCs and amplifiers with higher bandwidths are commercially available [16], [19], they lack the TCSs needed for the accurate readout of low-cost metal shunts.

In this article, which is an extended version of [20], the design of a shunt-based current sensor with kilohertz bandwidth and a tunable TCS is presented. The latter ensures high accuracy with both low and high TC shunts. A low-cost room-temperature TC tuning scheme is also proposed. Over the industrial temperature range and a ±25-A current range, the sensor achieves the state-of-the-art gain error (±0.25%) with both PCB and low-TC shunts.

The rest of this article is organized as follows. Different TCSs for current sensors are summarized in Section II.

Manuscript received 15 May 2022; revised 26 July 2022; accepted 25 August 2022. Date of publication 21 September 2022; date of current version 28 November 2022. This article was approved by Associate Editor Jens Anders. *(Corresponding author: Zhong Tang.)*

Zhong Tang, Roger Zamparette, and Kofi A. A. Makinwa are with the Electronic Instrumentation Laboratory, Microelectronics Department, Faculty of Electrical Engineering, Mathematics and Computer Science (EEMCS), Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: z.tang-1@tudelft.nl).

Yoshikazu Furuta and Tomohiro Nezuka are with the Sensor R&D Division, MIRISE Technologies Corporation, Kariya, Aichi 448-8661, Japan.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2022.3204520.

Digital Object Identifier 10.1109/JSSC.2022.3204520

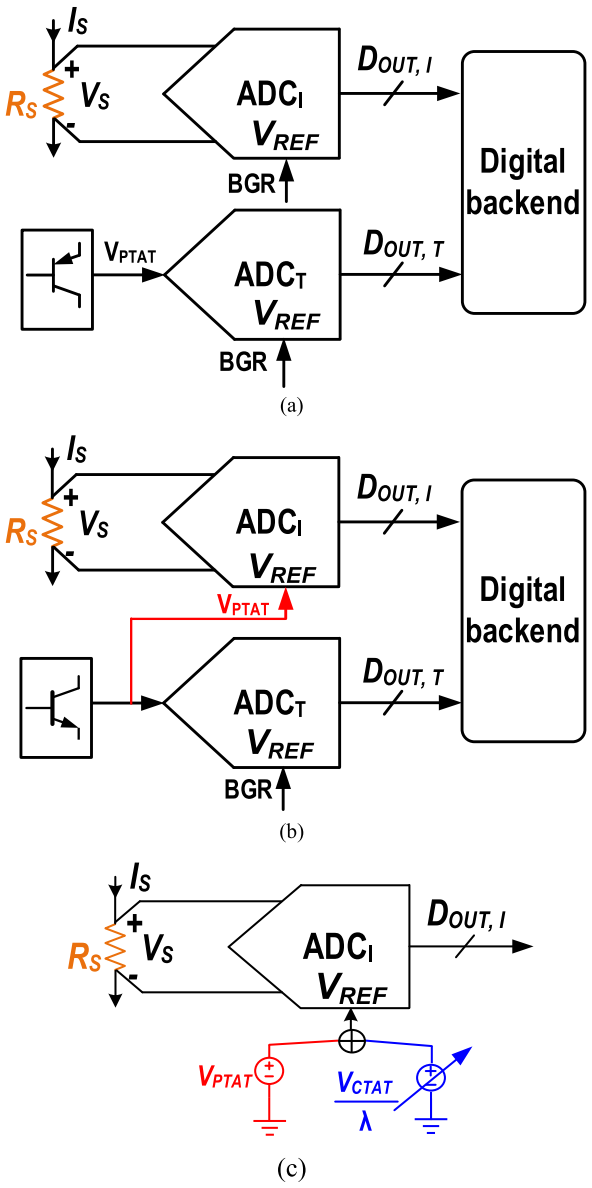


Fig. 2. (a) Block diagram of the TCS in [4]. (b) Block diagram of the TCS in [11]. (c) Block diagram of the TCS in [12].

Section III discusses the proposed tunable TCS and its circuit implementation. The proposed low-cost room-temperature TC tuning scheme is presented in Section IV. The measurement results are presented in Section V and compared with the state of the art. Finally, the conclusion is drawn in Section VI.

II. Review of Temperature Compensation Schemes

A. Digital TCS

As shown in Fig. 2(a), a straightforward way of compensating for the temperature dependence of a shunt is to place it in good thermal contact with an ADC that also contains a temperature sensor [4]. In this system, the shunt voltage V_S is digitized by an ADC_I with respect to a bandgap reference (BGR), while another ADC_T is used to sense the shunt's temperature. The shunt's temperature dependence can then be compensated in the digital domain. For a low-cost metal shunt (TC $\sim$ 0.4%/°C), however, the required temperature sensing inaccuracy is nontrivial: it should be less than 0.5 °C to avoid becoming the dominant source of error. In [4], a ±0.3% gain error over a ±36 A current range was achieved with a lead-frame shunt from −55 °C to 85 °C.

B. Hybrid TCS

To relax the required temperature sensing accuracy, a hybrid TCS is proposed in [11]. Instead of a BGR, a proportional-to-absolute-temperature (PTAT) voltage V_{PTAT} (∼0.33%/°C) is employed as an ADC_I reference. In this way, most of the shunt's TC (∼0.4%/°C) is compensated in the analog domain. The residual TC of ADC_I digital output $D_{\text{OUT},I}$ is then compensated in the digital domain with the help of a temperature sensor, whose accuracy, and thus complexity, can now be quite relaxed. With a simple temperature sensor (±1.2 °C error) and a PCB shunt, a gain error of ±0.35% over a ±12-A current range was achieved from −40 °C to 85 °C [11].

C. Analog TCS

To eliminate ADC_T completely, an analog TCS is proposed in [12], as shown in Fig. 2(c). Here, the reference of ADC_I is a PTAT voltage with a tunable TC. By adding a tunable complementary-to-absolute-temperature (CTAT) voltage (V_{CTAT}/λ) to a PTAT voltage, the TC of the reference can be tuned to match that of the shunt, resulting in a temperature-independent digital output. This approach requires only a single ADC and no further digital processing, leading to much lower power consumption and smaller area. After a batch calibration to determine the attenuation coefficient λ for a PCB shunt, a ±0.6% gain error over a ±15-A current range was obtained from −40 °C to 85 °C while consuming only 2.5 μW [12].

Compared to other TCSs, the analog TCS described in [12] offers the best power efficiency. However, this results in somewhat lower accuracy. Furthermore, it is not compatible with low-TC metal shunts.

III. Proposed TCS and Its Circuit Implementation

In this work, a flexible analog TCS is proposed, which ensures compatibility with both low-TC and low-cost shunts. It also employs a low-cost room-temperature TC tuning scheme to achieve improved accuracy (Section IV).

A. Proposed TCS

Fig. 3 shows the block diagram of the proposed current sensor. To compensate for the TC of a low-cost metal shunt, it employs a PTAT reference V_{REF} with a tunable TC

$$V_{\text{REF}} = V_{\text{PTAT}} \pm \frac{V_{\text{CTAT}}}{\lambda} \tag{1}$$

where λ can be tuned to match the TC of V_{REF} with that of the shunt. The PTAT reference V_{PTAT} is the difference of the base–emitter voltages (ΔV_{BE}) of two BJTs biased at different current densities, while V_{CTAT} is a base–emitter voltage V_{BE}. Since ΔV_{BE} has a large positive TC (0.33%/°C), only a small

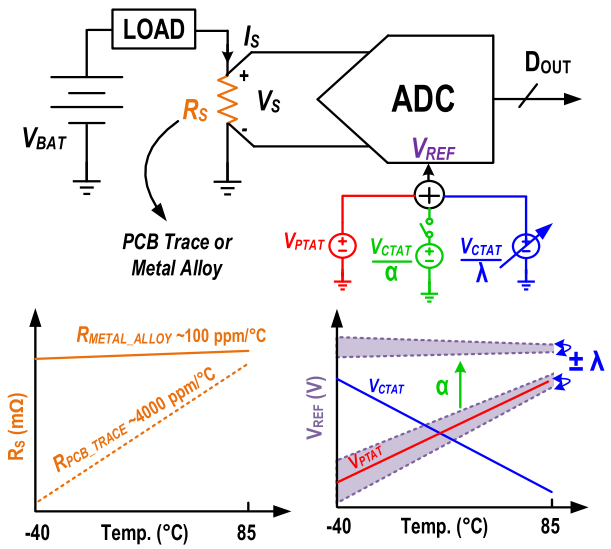


Fig. 3. Block diagram and TC compensation scheme of the proposed current sensor.

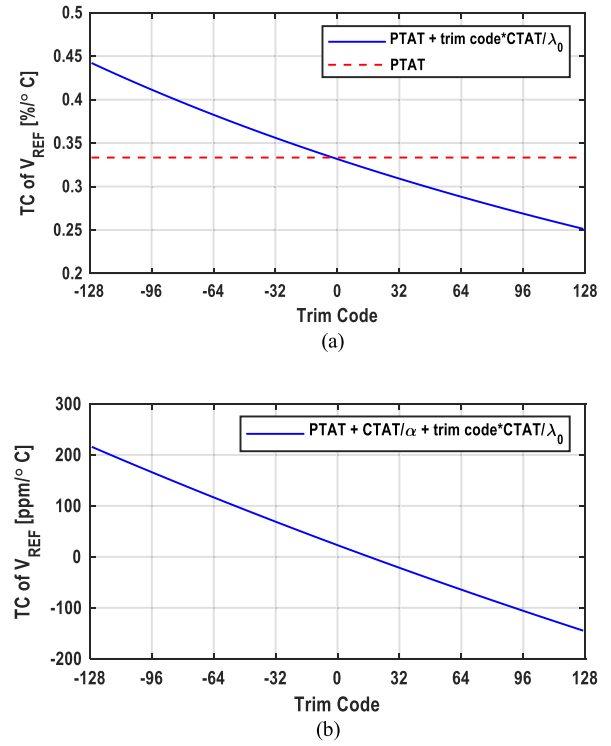


Fig. 4. (a) Simulated TC of the PTAT V_{REF} versus trim code. (b) Simulated TC of the BGR versus trim code.

amount of V_{BE} is needed to fine-tune the TC of V_{REF}. Fig. 4(a) shows the simulated TC of the tunable PTAT V_{REF} used in this work. If $1/\lambda$ is trimmed with 8-bit resolution from $-1/80$ to 1/80 (tuning step $1/\lambda_0 = 1/10240$), the TC of V_{REF} can be tuned from about 0.25%/°C to 0.44%/°C, which covers the TCs of most low-cost shunts. The maximum TC tuning step is 10 ppm/°C, which results in a trimming error of less than 0.1% over the industrial temperature range.

When the proposed sensor is used with a low-TC shunt, another attenuated CTAT path (V_{CTAT}/α) can be enabled to

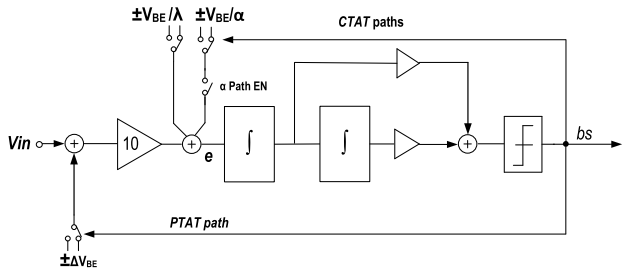


Fig. 5. Simplified block diagram of the current sensing ADC.

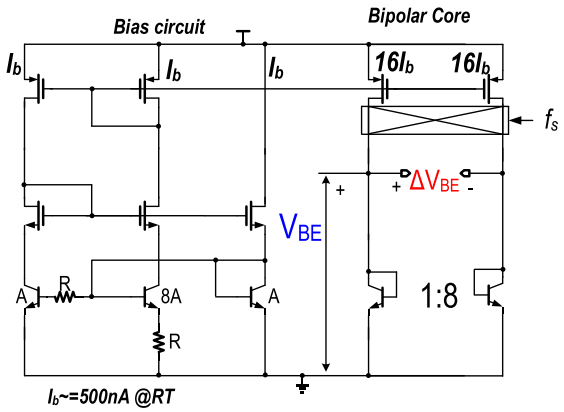


Fig. 6. Simplified circuit diagram of the reference generator.

turn V_{REF} into a reverse BGR

$$V_{REF} = V_{PTAT} + \frac{V_{CTAT}}{\alpha} \pm \frac{V_{CTAT}}{\lambda} \tag{2}$$

where α (=10) provides the attenuation needed to realize the reverse BGR and λ can be fine-tuned to match the exact TC of the shunt. As shown in Fig. 4(b), using the same tunable λ as in Fig. 4(a), the reference TC can now be trimmed from about −150 to 215 ppm/°C with a trimming step of less than 2 ppm/°C.

B. Readout Architecture

Fig. 5 shows a simplified block diagram of the proposed readout circuit. Since the input shunt voltage is quite small (<50 mV), it is boosted by a preamplifier with a gain of 10, which also serves as the summing node of a 1-bit 2nd-order feedforward switched-capacitor (SC) delta-sigma ($\Delta\Sigma$) modulator. Because the preamplifier is within the modulator's overall feedback loop, its linearity is quite relaxed [21]. To efficiently implement the large attenuation λ (>80), the 1-bit feedback $\pm V_{REF}$ is applied via two feedback paths. Its PTAT component (ΔV_{BE}) is applied via the preamplifier, while its CTAT components (V_{BE}/α and V_{BE}/λ) are applied via the 1st integrator. Thus, α and part of λ can be realized by the gain of the preamplifier. To achieve a 10-kHz bandwidth with an expected dynamic range larger than 75 dB, an oversampling ratio (OSR) of 128 is chosen to ensure that the modulator's noise floor is dominated by thermal noise. This results in a sampling frequency of 2.56 MHz.

C. Reference Generator

As shown in Fig. 6, an n-p-n-based reference generator is used to generate V_{PTAT} (ΔV_{BE}) and V_{CTAT} (V_{BE}). It consists of a current-gain (β) compensated PTAT bias circuit [22] and an n-p-n-based bipolar core. Two vertical n-p-n transistors are biased with a current density ratio of 8 to generate ΔV_{BE}(∼54 mV at room temperature). To mitigate mismatch and $1/f$ noise, the current sources in the bipolar core are chopped at the sampling frequency of the ADC f_S. To ensure that V_{PTAT} and V_{CTAT} are well settled before they are used by the ADC, the chopping clock is a delayed version of the sampling clock.

D. CCA

Fig. 7 shows the simplified circuit diagram of the ADC used in this work. The preamplifier is a low-noise capacitively coupled amplifier (CCA), whose input capacitors block the input common-mode voltage, thus allowing the same ADC to be used in high-side current sensing applications [10]. To sense the dc input and mitigate its offset and $1/f$ noise, the CCA is chopped at *fs*. Its dc operating point is set by a large resistance R_{FB}, which together with the feedback capacitance C_{FB} creates a high-pass cutoff frequency *fc* ($=1/2\pi R_{\mathrm{FB}}C_{\mathrm{FB}}$). Since the feedback capacitor C_{FB} (50 fF) is small, R_{FB} must be quite large (∼100 MΩ) to ensure that *fc* (∼30 kHz) is well below f_S (2.56 MHz). As shown in Fig. 8(a), to conserve area, R_{FB} can be implemented as a robust switched resistor [23]. Ideally, its effective resistance can be boosted by a factor T/T_{ON}, where T is the switching period and T_{ON} is the turn-on time of the switch. In this work, $T = 1/(2fs) = 195$ ns and $T_{\mathrm{ON}} \sim 2$ ns, allowing a physical resistance of 1.2 MΩ to be theoretically boosted by ∼100×.

In practice, the switched parasitic capacitor C_P of the resistor will form an SC resistor in parallel with the desired switched resistor and thus limits the maximum resistance that can be achieved [23]. Moreover, when the switch is turned off, the signal-dependent charge on C_P will be transferred to the feedback capacitance (C_{FB}) causing a signal-dependent gain error. Since the CCA input contains high-frequency quantization noise, this signal-dependent gain error will give rise to quantization noise folding.

To mitigate these issues, the switched resistor is split into N segments, as shown in Fig. 8(b). This splits C_P into N segments, which increases the impedance of the associated switched capacitors by a factor N^2. More importantly, the signal-dependent charge injected into the virtual ground is also reduced, improving gain accuracy and mitigating noise folding. As shown in Fig. 8(c), setting $N = 6$ results in a negligible gain error. It also ensures that the resulting R_{FB} is >100 MΩ.

As shown in Fig. 9, the CCA is based on a two-stage Miller-compensated amplifier, consisting of a folded-cascode input stage and a class-AB output stage. It provides >100-dB dc gain and rail-to-rail output swing. To minimize the signal attenuation at its input, the parasitic capacitance of the input PMOS pair (∼125 fF) is designed to be smaller than the input capacitance C_{IN} (500 fF). Drawing 180 μA, the CCA achieves a −3-dB bandwidth >3*fs* while driving the following SC integrator, which is based on an energy-efficient current-reuse OTA [4].

E. 1st Integrator and Tunable Reference

The output of the CCA is a square wave at the chopping frequency, whose amplitude is proportional to the difference between the input and DAC voltages. This amplitude information can be extracted by using a correlated double sampling (CDS) scheme to sample the CCA output (V_{OP} and V_{ON}) during both phases of this waveform and then take the difference [24]. In one phase, the integrator is configured in unity gain, and the CCA output V_{ON} is sampled on C_1. In the second phase, the change in the CCA output ($V_{\mathrm{OP}} - V_{\mathrm{ON}}$) is transferred to the integration capacitor C_{INT1}. This scheme rejects the CCA output offset and also mitigates the integrator's own offset and $1/f$ noise.

Since the CTAT feedback path is applied after the CCA, the large attenuations (λ and α) can be implemented by reasonable capacitor ratios: $\lambda = C_{\mathrm{REF}}/C_{\mathrm{FB}} \times C_1/C_2$ and $\alpha = C_{\mathrm{REF}}/C_{\mathrm{FB}} \times C_1/C_3$. In this work, $C_{\mathrm{IN}} = C_{\mathrm{REF}} = 10C_{\mathrm{FB}} = 500$ fF and $C_1 = C_3 = 8C_2 = 400$ fF. Their matching requirements are not too strict since the λ path is tunable.

As discussed in Section III, λ should be trimmed with 8-bit resolution. In this work, a 1-bit $\Delta\Sigma$ trimming scheme is used since the CDAC capacitor C_2 is rather small (50 fF). This involves the use of another digital $\Delta\Sigma$ modulator to precisely control the average amount of time that the CDAC is enabled. However, directly applying $\Delta\Sigma$ trimming to the CDAC will cause significant quantization noise folding. This is because the input of C_2 is the ADC bitstream output, and thus, it will be effectively multiplied by the bitstream output of the digital $\Delta\Sigma$ modulator, as shown in Fig. 10(a).

To address this issue, λ is trimmed in a bitstream-controlled (BSC) manner [26], [27], as shown in Fig. 10(b). Depending on the bitstream state, the CDAC control input is multiplexed between two digital 1st-order $\Delta\Sigma$ modulators. Similarly, the sampling clocks of the digital modulators are also generated according to the bitstream state. This scheme ensures that the shaped quantization noise of each digital modulator is always multiplied by a constant (either +1 or −1). The net effect is thus to add a small amount of properly shaped quantization noise (each with an average value of V_{BE}/λ) to the input of the ADC.

F. System-Level Chopping

As shown in Fig. 11, system-level low-frequency chopping (CHL) is applied to suppress the ADC residual offset. After the CHL transitions, however, the sudden changes in input polarity will cause large transients in the modulator's internal states. Such transients can be avoided by resetting its internal states during CHL transitions and thus operating the modulator in incremental mode. Alternatively, the polarity of the modulator's internal states can also be swapped after CHL transitions. As in [26], this involves swapping the position of the integration capacitors, thus allowing the integrator's

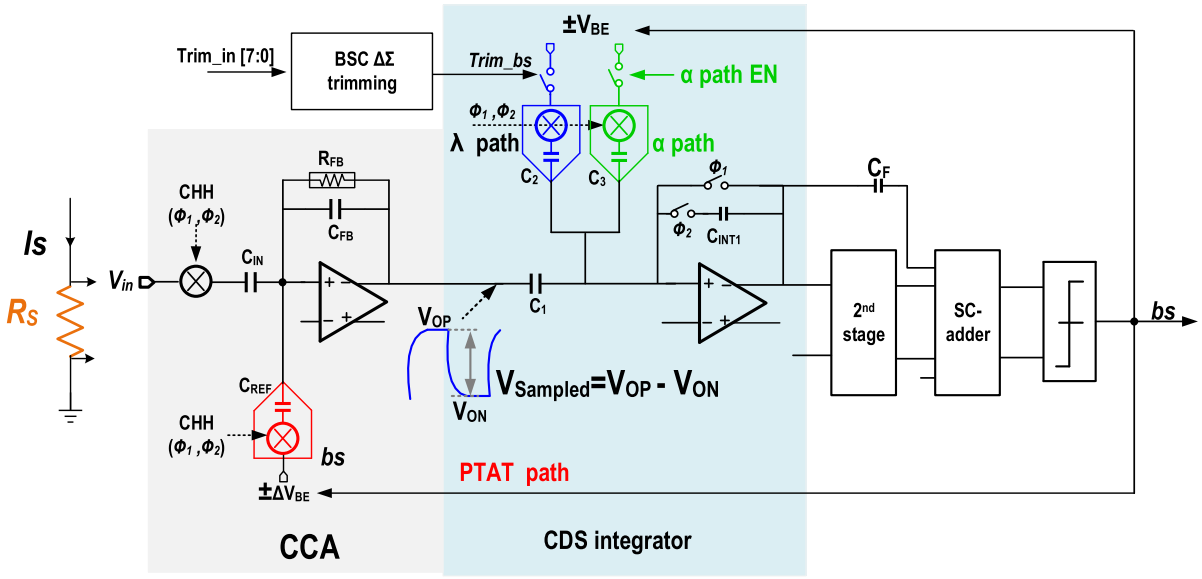


Fig. 7. Simplified circuit diagram of the current sensor.

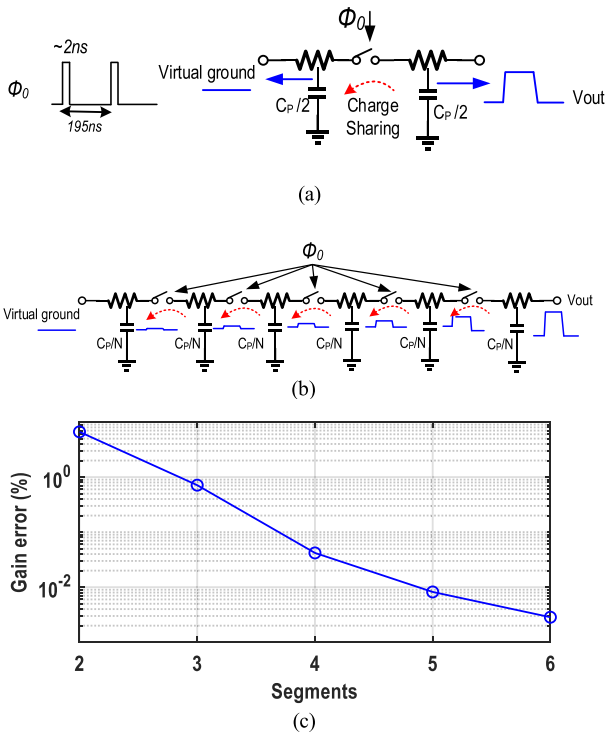


Fig. 8. (a) Conventional switched resistor [23]. (b) Proposed segmented switched resistor. (c) Simulated gain error versus segments.

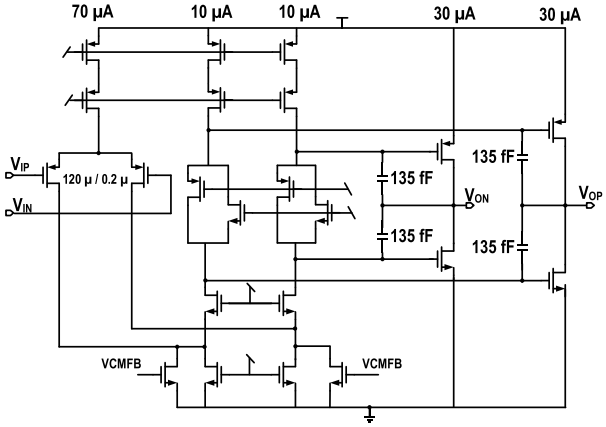


Fig. 9. Circuit implementation of the amplifier in the CCA.

G. Diagnostic Temperature Sensor

For diagnostic purposes, an on-chip temperature sensor is implemented to monitor the self-heating of the shunt. Fig. 12 shows the diagram of the temperature sensor. It consists of a separate 1st-order SC $\Delta\Sigma$ modulator that balances $11\Delta V_{\mathrm{BE}}$ against V_{BE} to generate a digital representation of temperature [26]. The required input signals (V_{BE} and ΔV_{BE}) for the diagnostic temperature sensor are generated by a separate bipolar core, thereby avoiding any intermodulation between the temperature sensor and the current sensor.

IV. Two-Current Calibration

To optimize current sensing accuracy over temperature, the TC of V_{REF} must be tuned to match the TC of the shunt. Traditionally, this involves a two-temperature calibration, which is costly and time-consuming.

In this work, a room-temperature calibration scheme is proposed to reduce the calibration cost. It exploits the fact that

output to evolve smoothly after CHL transitions. This approach allows the modulator to be operated in a free-running mode. Since the SC loop filter has a fixed one $\Delta\Sigma$ cycle delay, the clock of the output chopper is also delayed by one $\Delta\Sigma$ clock period. To avoid in-band ripple, the frequency of CHL is set to 20 kHz. The residual ripple caused by the CHL can be filtered by the notches of the following sinc^2 decimation filter.

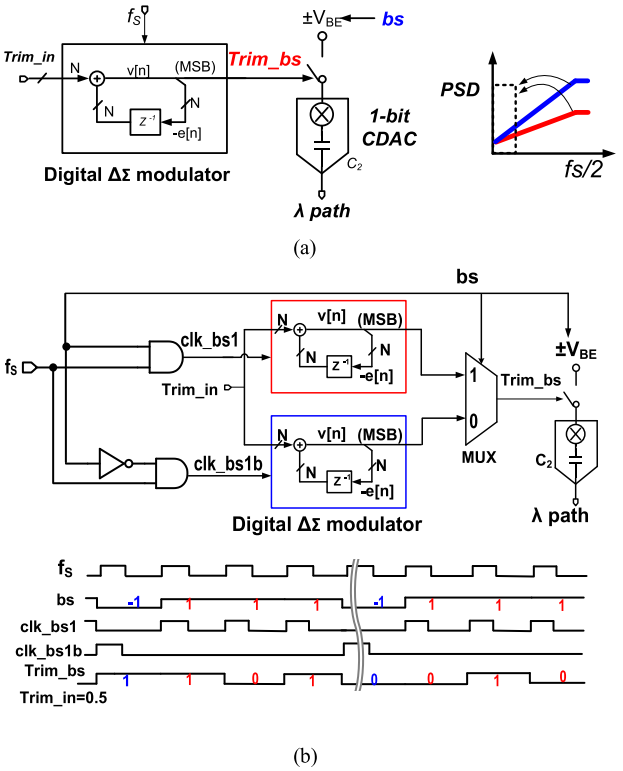


Fig. 10. (a) Simplified diagram of the direct digital ΔΣ trimming. (b) BSC ΔΣ trimming.

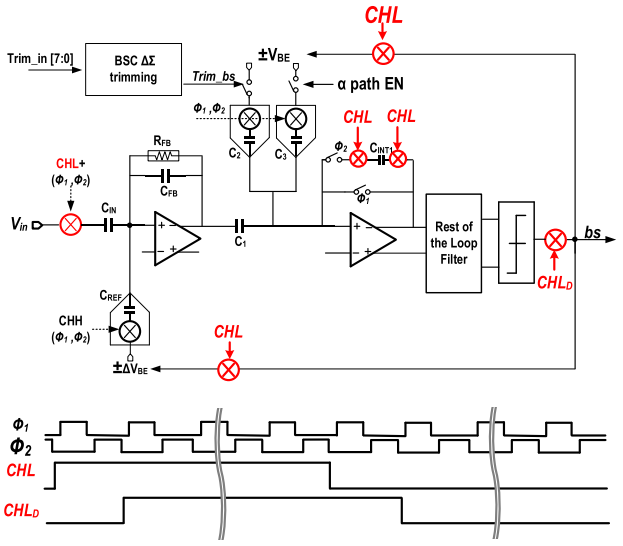


Fig. 11. Block diagram of the system-level chopping.

due to its self-heating, the shunt itself can be reused as a heater. Then, by measuring the ADC output at a low current (low self-heating) and then at a high current (high self-heating), the attenuation λ can be individually trimmed for maximum gain flatness according to their relative error. The low current (10 A in this work) is set high enough to mitigate the impact of ADC offset. As can be seen from Fig. 13, with 10- and 25-A currents, different levels of self-heating in a PCB shunt gives rise to a temperature difference of ∼20 °C, which is

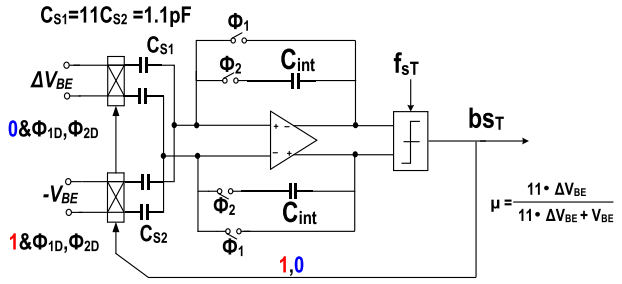


Fig. 12. Circuit diagram of the diagnostic temperature sensor.

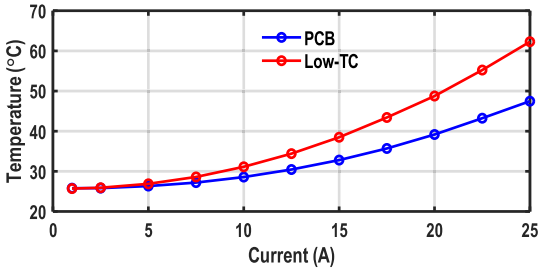


Fig. 13. Measured self-heating of the shunt resistor at large currents with a 1-min settling time.

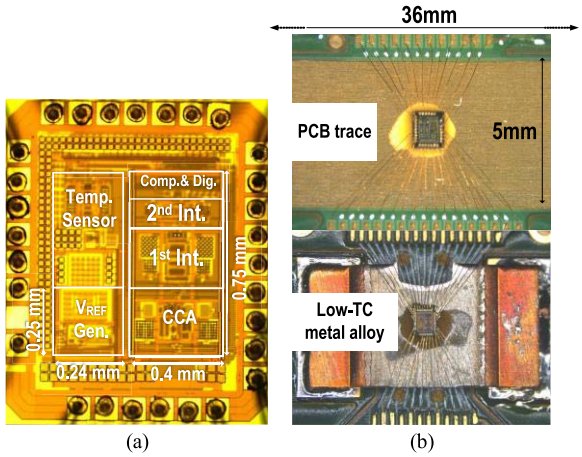


Fig. 14. (a) Die micrograph. (b) Chips on PCB trace and low-TC shunts.

enough to cause measurable gain errors. To compensate for the spread in the shunt resistance, the ADC output at 10 A is used to perform a digital gain trim.

Measurements show that the shunt has a thermal settling time of several seconds, which in turn will limit the speed of the proposed calibration scheme. However, this will still be faster, and hence cheaper, than a traditional two-temperature trim, which would involve heating and stabilizing the entire test setup. An even lower cost approach would be to use a batch-calibrated λ, at the expense of higher gain error.

V. Measurement Results

The proposed readout circuit was implemented in a standard 0.18-μm CMOS technology. Including the reference generator and current sensing ADC, it occupies 0.36 mm^2 [Fig. 14(a)]

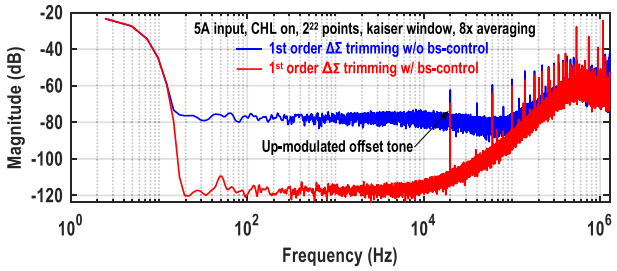


Fig. 15. Measured output spectra w/ and w/o BSC $\Delta\Sigma$ trimming.

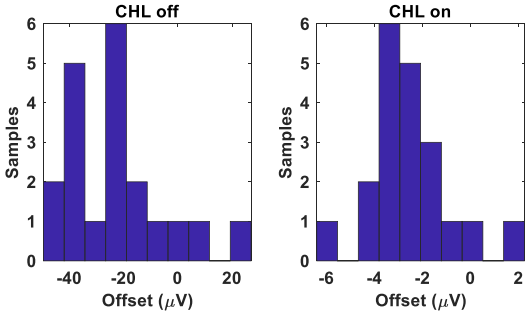


Fig. 16. Measured input offset w/ and w/o CHL.

and draws 265 μA from a 1.8-V supply at room temperature. For flexibility, the sinc^2 decimation filter and BSC $\Delta\Sigma$ trimming logic were implemented off-chip. Simulations show that implementing them on chip only consumes 15 and 10 μW. As shown in Fig. 14(b), the prototype's performance was verified with 1.6-mΩ PCB (36 $\times$ 5 mm^2) and 2-mΩ low-TC (75 ppm/°C) shunts. Good thermal coupling and galvanic isolation were achieved by directly bonding the chip to the shunt with nonconductive glue. In industrial applications, a thin isolation platelet can be used [28].

Fig. 15 shows the measured output spectra of the modulator with a 5-A dc input current through the PCB shunt. Trimming V_{REF} with a free-running digital $\Delta\Sigma$ modulator incurs significant noise folding, which is eliminated by the BSC scheme. With an OSR of 128, the modulator achieves a thermal-noise-limited resolution of 8.5 $\mu\mathrm{V_{rms}}$ in a 10-kHz bandwidth, corresponding to current resolutions of 5.3 mA (rms) with a 1.6-mΩ PCB shunt and 4.3 mA (rms) with a 2-mΩ metal-alloy shunt. The up-modulated offset at CHL and its harmonics are filtered out by the notches of the 256-tap sinc^2 decimation filter. As shown in Fig. 16, measurements on 20 samples show that the modulator's input-referred voltage offset is less than 50 μV with CHL disabled and drops below 6 μV with CHL enabled. This corresponds to input current offsets of 3.8 mA/3 mA with the PCB and low-TC shunts.

To verify the proposed TCS, a 15-A dc current is applied to the sensor and measured from -40 °C to 85 °C with different trimming codes (λ). The optimal trimming code can be found when the variation of the digital output D_{OUT} over temperature is minimized. Fig. 17 shows the sensor's D_{OUT} variations from -40 °C to 85 °C. Because of the BSC $\Delta\Sigma$ trimming scheme, the D_{OUT} variation can be trimmed with high resolution:

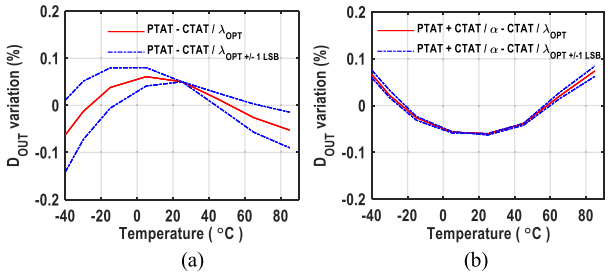


Fig. 17. (a) Measured D_{OUT} variations over temperature with a 15-A current using a PCB shunt and (b) low-TC metal-alloy shunt.

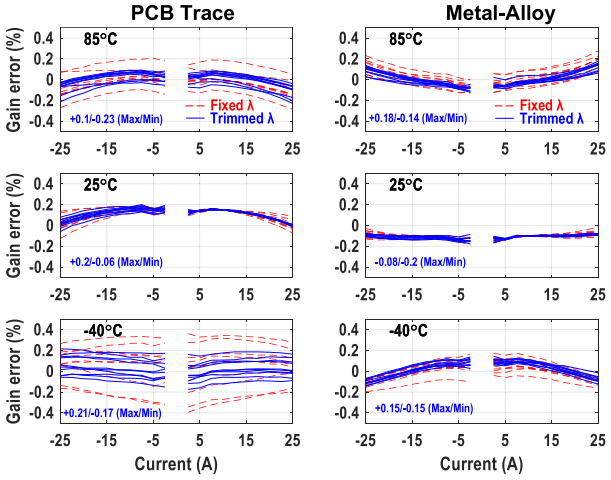


Fig. 18. Measured gain errors at different ambient temperatures for PCB (left) and low-TC metal-alloy shunts (right) w/ and w/o λ trimming.

in steps of $\sim$0.1% and $\sim$0.03% for the PCB and low-TC shunts, respectively. With the optimal λ, D_{OUT} variations can be reduced to less than $\pm$0.1% over the industrial temperature range for both shunts. The residual D_{OUT} variations are limited by the high-order TCs of the V_{REF} and the shunt.

As described in Section IV, the optimal λ for minimum D_{OUT} variation over temperature can be determined by employing the proposed two-current calibration scheme with 10- and 25-A dc currents for both PCB and low-TC shunts. For each type of shunt, ten sensors were characterized from -40 °C to 85 °C in a current range of $\pm$25 A. The input current is provided by the source meter Keithley 2260B, which can provide dc currents with 0.1% accuracy. With a single-current gain trim and a fixed value of λ ($\sim$177 for the PCB shunt and $\sim$683 for the low-TC shunt) [4], [11], [12], gain errors of $\pm$0.4% (PCB shunt) and $\pm$0.3% (low-TC shunt) were achieved. The proposed two-current calibration scheme reduces them to $\pm$0.25% (PCB shunt) and $\pm$0.2% (low-TC shunt) without further processing (Fig. 18). As shown in Fig. 17(a), the trimming resolution with the PCB shunt is lower than with the low-TC shunt, especially at low temperatures, resulting in larger errors at -40°C. The spread in the optimal λ, which reflects the combined spread in the TC of the shunt and V_{REF}, is limited to 10 and 20 LSBs for the PCB and low-TC shunts, respectively. The residual gain error over

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work		Xu SSCL'18 [11]	Zamparette VLSI'21 [12]	Vroonhoven ISSCC'20 [13]	INA 260 [16]
Technology	**0.18 µm**		0.18 µm BCD	0.18 µm	0.18 µm BCD	--
Area	**0.36 mm²**		1.4 mm²	--	0.85 mm²	--
Shunt	**1.6 mΩ (PCB)**	**2 mΩ (low-TC)**	1 mΩ (PCB)	3 mΩ (PCB)	50 mΩ (low-TC)	2 mΩ (low-TC)
Current Range	**±25 A**	**±25 A**	±12 A	±15 A	±1 A	±15 A
Gain Error	**±0.25%**	**±0.2%**	±0.35%	±0.6%	±0.5%	±0.5%
Temp. Range	**-40 to 85 °C**		-40 to 85 °C	-40 to 85 °C	-50 to 125 °C	-40 to 85 °C
ADC offset	**6 µV**		1 µV (1 mA)	0.5 µV (0.17mA)	<5 µV (0.1 mA)	10 µV (5 mA)
	3.8 mA	**3 mA**				
Bandwidth	**10kHz***		40 Hz*	32 Hz*	<2.4 Hz	3.6 kHz
Resolution	**8.5 µV**		1.1 µV (1.1 mA)	5.4 µV (1.8 mA)	--	--
	5.3 mA	**4.3 mA**				
Supply Voltage	**1.8 V**		1.8 V	1.8 V	1.7-60 V	2.7-5.5 V
Supply Current	**265 µA**		13.8 µA	1.4 µA	<5 µA	310 µA
Dynamic Range	**73.5 dB**	**75.4 dB**	80.7 dB	78.4 dB	--	--
FoM**	**147 dB**	**149 dB**	143 dB	149 dB	--	--
Polynomial Calibration	**No**		Yes	Yes	No	--

*Bandwidth for a thermal noise limited resolution
** FoM=Dynamic Range + 10 log (Bandwidth/Power)

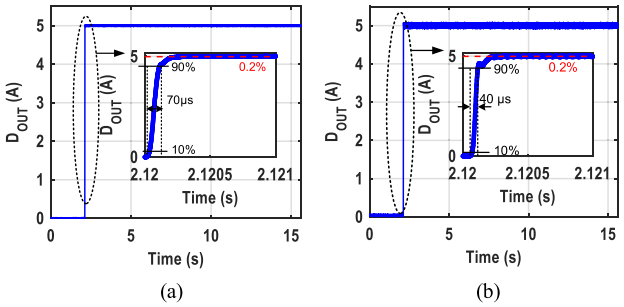


Fig. 19. Transient measurement under a 0–5-A current step input with a PCB shunt (a) using a 256-tap sinc^2 filter and (b) 128-tap sinc^2 filter.

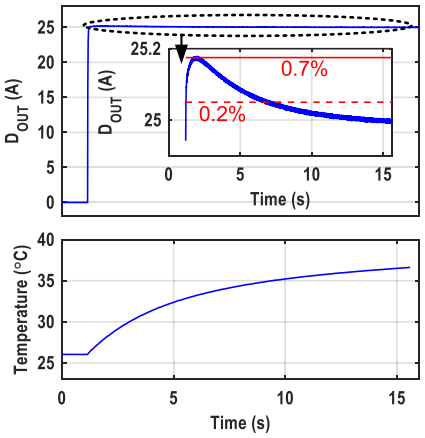


Fig. 20. Transient measurement under a 0–25-A current step input with a PCB shunt.

temperature is dominated by the high-order TC and the TC spread of the PCB shunt.

The dynamic accuracy of the sensor was evaluated with step input currents. As shown in Fig. 19(a), with a PCB shunt and a 0–5-A step, the sensor's output has a rise time of 70 μs and settles to within 0.2% in 300 μs. These times are mainly determined by the 256-tap sinc^2 filter. A faster step response can be obtained by using a shorter filter at the expense of resolution [Fig. 19(b)]. However, a 0–25-A step causes significant self-heating and slow settling. As shown in Fig. 20, a temperature rise of ~10 °C was observed over a 14-s interval. Due to the initially nonhomogenous temperature distribution in the shunt and the chip, a peak settling error of 0.7% can be seen, which drops to 0.2% within ~6 s. Due to the small TC of the metal-alloy shunt, its peak settling error for step input currents is negligible.

The sensor's performance is summarized in Table I and compared with state-of-the-art PCB and low-TC shunt-based sensors. The proposed readout achieves a compact core area of 0.36 mm^2. Compared to [11] and [12], this work has a much higher sampling frequency and bandwidth, resulting in higher power consumption. However, it has a similar figure of merit (FoM), which shows that its energy efficiency is quite competitive. Moreover, due to the low-cost two-current calibration scheme, the sensor achieves the state-of-the-art gain accuracy (±0.25%) over a wide current (±25 A) and temperature (−40 °C to 85 °C) range for both low-TC and PCB shunts.

VI. CONCLUSION

In this work, a versatile shunt-based current sensor with a tunable TCS is proposed. It can be flexibly used with both low-TC metal-alloy shunts and high-TC, but low-cost, metal shunts

while maintaining high accuracy. A bitstream controlled $\Delta\Sigma$ trimming technique is used to achieve high trimming resolution (<0.1%) without quantization noise folding. To optimize gain flatness over temperature, a low-cost room-temperature TC tuning scheme is proposed by exploiting the shunt's self-heating at large currents. Over the industrial temperature range and a ±25-A current range, it achieves the state-of-the-art gain accuracy (±0.25%) with both low-cost PCB and stable metal-alloy shunts. In future work, it would be interesting to investigate the long-term drift of the low-cost PCB shunt.

ACKNOWLEDGMENT

The authors would like to thank Zu-Yao Chang and Lukasz Pakula for chip bonding.

REFERENCES

[1] S. Ziegler, R. C. Woodward, H. H.-C. Iu, and L. J. Borle, "Current sensing techniques: A review," *IEEE Sensors J.*, vol. 9, no. 4, pp. 354–376, Apr. 2009.

[2] K. W. E. Cheng, B. P. Divakar, H. Wu, D. Kai, and H. F. Ho, "Battery-management system (BMS) and SOC development for electrical vehicles," *IEEE Trans. Veh. Technol.*, vol. 60, no. 1, pp. 76–88, Jan. 2011.

[3] S. H. Shalmany, D. Draxelmayr, and K. A. A. Makinwa, "A ±5A integrated current-sensing system with ±0.3% gain error and 16 μA offset from −55°C to +85°C," *IEEE J. Solid-State Circuits*, vol. 51, no. 4, pp. 800–808, Apr. 2016.

[4] S. Heidary Shalmany, D. Draxelmayr, and K. A. A. Makinwa, "A ±36-A integrated current-sensing system with a 0.3% gain error and a 400-μA offset from −55 °C to +85 °C," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1034–1043, Apr. 2017.

[5] A. Guha and A. Patra, "State of health estimation of lithium-ion batteries using capacity fade and internal resistance growth models," *IEEE Trans. Transp. Electrific.*, vol. 4, no. 1, pp. 135–146, Mar. 2018.

[6] P. G. Blanken and S. E. J. Menten, "A 10μV-offset 8 kHz bandwidth 4^{th}–order chopped $\Sigma\Delta$ A/D converter for battery management," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2002, pp. 388–476.

[7] L. A. Middlemiss, A. J. Rennie, R. Sayers, and A. R. West, "Characterisation of batteries by electrochemical impedance spectroscopy," *Energy Rep.*, vol. 6, pp. 232–241, May 2020.

[8] L. Xu, J. H. Huijsing, and K. A. A. Makinwa, "A 10kHz-BW 93.7 dB-SNR chopped $\Delta\Sigma$ ADC with 30V input CM range and 115 dB CMRR at 10 kHz," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2017, pp. 49–52.

[9] A. Jouyaeian, Q. Fan, M. Motz, U. Ausserlechner, and K. A. A. Makinwa, "5.6 A 25A hybrid magnetic current sensor with 64 mA resolution, 1.8 MHz bandwidth, and a gain drift compensation scheme," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 82–84.

[10] L. Xu, J. H. Huijsing, and K. A. A. Makinwa, "A ±4-A high-side current sensor with 0.9% gain error from −40 °C to 85 °C using an analog temperature compensation technique," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3368–3376, Dec. 2018.

[11] L. Xu, S. H. Shalmany, J. H. Huijsing, and K. A. A. Makinwa, "A ± 12-A high-side current sensor with 25 V input CM range and 0.35% gain error from −40 °C to 85 °C," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 4, pp. 94–97, Apr. 2018.

[12] R. Zamparette and K. Makinwa, "A ±2A/15A current sensor with 1.4 μA supply current and ±0.35%/0.6% gain error from −40 to 85°C using an analog temperature-compensation scheme," in *Proc. Symp. VLSI Circuits*, Jun. 2021, pp. 1–2.

[13] C. van Vroonhoven, "23.3 A 0-to-60V-input V_{CM} Coulomb counter with signal-dependent supply current and ±0.5% gain inaccuracy from −50°C to 125°C," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 348–350.

[14] S. H. Shalmany, D. Draxelmayr, and K. A. A. Makinwa, "A micropower battery current sensor with ±0.03% (3σ) inaccuracy from −40 to +85°C," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 386–387.

[15] S. H. Shalmany *et al.*, "A ±5A battery current sensor with ±0.04% gain error from −55°C to +125°C," in *Proc. IEEE Int. Workshop Adv. Sens. Interface (IWASI'13)*, vol. 2013, pp. 117–120.

[16] Texas Instruments. *INA 260 Data Sheet*. Accessed: Sep. 6, 2021. [Online]. Available: https://www.ti.com/lit/ds/symlink/ina260.pdf

[17] L. Spaziani, "Using copper PCB etch for low value resistance," Texas Instrum., Dallas, TX, USA, Unitrode Des. Note DN-71, 1997, pp. 1–3.

[18] S. Ziegler, R. C. Woodward, H. H.-C. Iu, and L. J. Borle, "Investigation into static and dynamic performance of the copper trace current sense method," *IEEE Sensors J.*, vol. 9, no. 7, pp. 782–792, Jul. 2009.

[19] Texas Instruments. *INA 296B Data Sheet*. Accessed: Jul. 16, 2022. [Online]. Available: https://www.ti.com/lit/ds/symlink/ina296b.pdf

[20] Z. Tang, R. Zarnparette, Y. Furuta, T. Nezuka, and K. A. A. Makinwa, "A ±25A versatile shunt-based current sensor with 10 kHz bandwidth and ±0.25% gain error from −40°C to 85°C using 2-current calibration," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2022, pp. 66–68.

[21] H. Jiang, C. Ligouras, S. Nihtianov, and K. A. A. Makinwa, "A 4.5 nV/$\sqrt{}$Hz capacitively coupled continuous-time sigma-delta modulator with an energy-efficient chopping scheme," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 1, pp. 18–21, Jan. 2018.

[22] R. K. Kumar, H. Jiang, and K. A. A. Makinwa, "An energy-efficient BJT-based temperature-to-digital converter with ±0.13°C (3σ) inaccuracy from −40 to 125°C," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2019, pp. 107–108.

[23] M. H. Perrott *et al.*, "A low area, switched-resistor based fractional-N synthesizer applied to a MEMS-based programmable oscillator," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2566–2581, Dec. 2010.

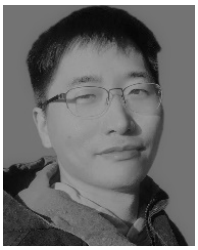
[24] M. Belloni, E. Bonizzoni, A. Fornasari, and F. Maloberti, "A micropower chopper—CDS operational amplifier," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2521–2529, Dec. 2010.

[25] Q. Fan, F. Sebastiano, J. H. Huijsing, and K. A. A. Makinwa, "A 1.8 μ W 60 nV/$\sqrt{}$ Hz capacitively-coupled chopper instrumentation amplifier in 65 nm CMOS for wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1534–1543, Jul. 2011.

[26] M. A. P. Pertijs, K. A. A. Makinwa, and J. H. Huijsing, "A CMOS smart temperature sensor with a 3σ inaccuracy of ±0.1°C from −55°C to 125°C," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2805–2815, Dec. 2005.

[27] M. A. P. Pertijs and J. H. Huijsing, "Bitstream trimming of a smart temperature sensor," in *Proc. IEEE SENSORS*, vol. 2, Oct. 2004, pp. 904–907.

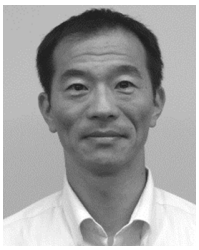
[28] M. Motz *et al.*, "A miniature digital current sensor with differential Hall probes using enhanced chopping techniques and mechanical stress compensation," in *Proc. IEEE SENSORS*, Oct. 2012, pp. 1–4.



Zhong Tang (Member, IEEE) received the B.S. and Ph.D. degrees from Zhejiang University, Hangzhou, China, in 2015 and 2020, respectively.

From 2016 to 2018, he was an Intern with Semitronix Corporation, Hangzhou, working on CMOS temperature sensor design. From 2019 to 2020, he was a Visiting Ph.D. Student with the EEIC Group, Eindhoven University of Technology, Eindhoven, The Netherlands. He is currently a Post-Doctoral Researcher with the Electronic Instrumentation Laboratory, TU Delft, Delft, The Netherlands. His current research interests include CMOS temperature sensors and other precision analog and mixed-signal integrated circuits.

Roger Zamparette (Graduate Student Member, IEEE) received the B.E. degree in electrical engineering from the State University of Santa Catarina—UDESC, Joinville, Brazil, in 2014, and the M.Sc. degree from the Federal University of Rio Grande do Sul-UFRGS, Porto Alegre, Brazil, in 2017. He is currently pursuing the Ph.D. degree with the Delft University of Technology, Delft, The Netherlands.



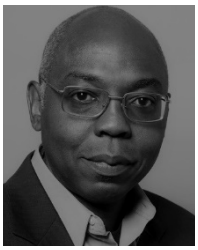
Yoshikazu Furuta (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electronic engineering from Osaka University, Osaka, Japan, in 1999, 2001, and 2003, respectively.

In 2000, he joined the Hitachi Cambridge Laboratory, Cambridge, U.K., to study carrier transport properties in poly-Si thin film for memory and display applications. After a period with Osaka University, he joined Renesas Electronics, Hyogo, Japan in 2004, where he designed WCDMA/LTE transceivers and a BLE transceiver. Since 2014, he has been with DENSO Corporation, Aichi, Japan, where he is currently loaned to MIRISE Technologies Corporation, Nisshin, where he is the Manager. His research interests include system and circuit design of sensors and data communications for automotive and industrial applications.

Tomohiro Nezuka (Member, IEEE) was born in Toyama, Japan, in 1975. He received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1997, 1999, and 2002, respectively.

From 2002 to 2011, he was with THine Electronics Inc., Tokyo, Japan, where he worked on display interfaces and ADCs. In 2011, he joined DENSO Corporation, Aichi, Japan, where he worked on AFEs for automotive sensors and ECUs. In 2020, he joined MIRISE Technologies Corporation, Nisshin, Japan, where he is currently a General Manager of the Sensor Research and Development Division. His research interests include mixed-signal circuits, high-voltage analog circuits, and sensor fusion algorithms.

Dr. Nezuka has been a member of the Technical Program Committee of the VLSI Symposium since 2018.



Kofi A. A. Makinwa (Fellow, IEEE) received the B.Sc. and M.Sc. degrees from Obafemi Awolowo University, Ife, Nigeria, in 1985 and 1988, respectively, the M.E.E. degree from the Philips International Institute, Eindhoven, The Netherlands, in 1989, and the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 2004.

From 1989 to 1999, he was a Research Scientist with the Philips Research Laboratories, Eindhoven, where he worked on interactive displays and digital recording systems. In 1999, he joined the Delft University of Technology, where he is currently an Antoni van Leeuwenhoek Professor and the Head of the Microelectronics Department. His research interests include the design of mixed-signal circuits, sensor interfaces, and smart sensors. This has led to 17 books, more than 300 technical articles, and more than 30 patents.

Dr. Makinwa is a member of the Royal Netherlands Academy of Arts and Sciences. He is an ISSCC Top-10 Contributor (with more than 60 papers). He was a co-recipient of 17 best paper awards, from the JSSC (two), the ISSCC (five), and the VLSI Circuits Symposium (two), among others. He was the Analog Subcom Chair of ISSCC and has served on the program committees for several other IEEE conferences. He has also served as a Distinguished Lecturer for the Solid-State Circuits Society and an Elected Member of its Adcom. He is currently one of the organizers of the Advances in Analog Circuit Design Workshop and the IEEE Sensor Interfaces Meeting.