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A Cryo-CMOS Oscillator With an Automatic Common-Mode Resonance Calibration for Quantum Computing Applications

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***Abstract*— This article presents a 4-to-5 GHz *LC* oscillator operating at 4.2 K for quantum computing applications. The phase noise (PN) specification of the oscillator is derived based on the control fidelity for a single-qubit operation. To reveal the substantial gap between the theoretical predictions and measurement results at cryogenic temperatures, a new PN expression for an oscillator is derived by considering the shot-noise effect. To reach the optimum performance of an *LC* oscillator, a common-mode (CM) resonance technique is implemented. Additionally, this work presents a digital calibration loop to adjust the CM frequency automatically at 4.2 K, reducing the oscillator's PN and thus improving the control fidelity. The calibration technique reduces the flicker corner of the oscillator over a wide temperature range (10 × and 8 × reduction at 300 K and 4.2 K, respectively). At 4.2 K, our 0.15-mm^2 oscillator consumes a 5-mW power and achieves a PN of −153.8 dBc/Hz at a 10 MHz offset, corresponding to a 200-dB FOM. The calibration circuits consume only a 0.4-mW power and 0.01-mm^2 area.**

***Index Terms*— Quantum computing, qubit, cryogenic, oscillator, PLL, common-mode resonance calibration, phase noise, frequency noise, flicker noise, shot noise.**

I. Introduction

QUANTUM computers have received considerable attention over the past decade, as they can potentially solve particular problems that are intractable even for today's most powerful supercomputers [1], [2], [3]. For instance, quantum computers can efficiently simulate highly-entangled many-particle quantum systems [3], [4], [5]. This could help to accelerate the design of new catalysts that improve the efficiency of nitrogen fixation into fertilizers and room-temperature superconductors that lead to more effective power transmission or improved collection of solar energy [5]. Yet, to handle the above-mentioned tasks, tens of thousands or even millions of quantum bits (qubits) would be required, which advocates scalability for the qubit-control system.

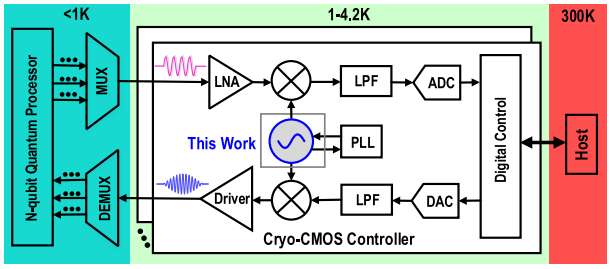

Fig. 1. Cryo-CMOS controller interfacing qubits [6].

However, current qubits operate at temperatures well below 1 K inside a dilution refrigerator, while the readout/control electronics are typically implemented with commercial instruments operating at room temperature (RT), which are hard-wired from/to qubits. Although this brute-force approach proves to be successful in few-qubits (< 100) systems, it creates scalability and performance issues due to the impractical cabling, thermal loading, and large form factor as the qubit number grows. To overcome such a bottleneck, a fully-integrated cryogenic CMOS (cryo-CMOS) control system is proposed to operate close to the qubits at 1-4.2 K [6]. This intermediate approach could support up to 1000 qubits due to a relatively high cooling power of the refrigerator at 1-4.2 K (i.e., a power consumption of ∼1 mW per qubit for the qubit controller), and hence dramatically reduces the required complex interconnections between the cryogenic refrigerator and the RT electronics. Eventually, the full integration is envisioned when the cryo-CMOS controller is co-integrated with advanced "hot" qubits operating at ∼1-4.2 K on the same die or package [7], [8], [9]. To this end, significant effort has been made in the last decade to demonstrate the feasibility of building blocks for quantum computing applications at cryogenic temperatures (CT) [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32].

For the manipulation of qubits, as shown in Fig. 1, microwave bursts of a short duration less than < 1 μs must be applied (i.e., 4–8-GHz bursts for transmons and 10-20-GHz bursts for spin qubits) [18]. A local oscillator operating at cryogenic temperatures (CT) is required to down/

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up-convert the desired amplitude and phase-modulated signals. However, designing a cryo-CMOS oscillator, as the heart of a frequency synthesizer, presents several challenges. Firstly, low phase noise (PN) is required to ensure that the oscillator does not limit the overall fidelity of a quantum computer. Secondly, the oscillator must operate at CT, where devices exhibit large temperature-induced variation of the parameters and no mature device models are available. Finally, as the cryogenic refrigerator has a limited cooling power, a low power consumption (P_{DC}) is required. Although standalone *LC* oscillators operating down to 4.2 K are presented in [15], [16], [17], [18], only the cryogenic *LC* oscillator in [18] is implemented in a standard CMOS process. Yet, the oscillator's PN at lower frequency offsets in [18] is severely compromised at 4.2 K, complicating cryo-CMOS PLL designs for quantum computing applications.

In the last few years, several flicker PN reduction techniques have been proposed at RT: 1) inserting resistances in series to the drain of oscillation sustaining devices [33]; 2) narrowing down the conduction angle of oscillation sustaining devices [34], [35]; 3) shifting the phase of the gate voltage against the drain voltage by tuning the capacitance ratio of the gate and drain capacitors in a transformer-based complementary oscillator [36]. Nevertheless, adding drain resistors degrades an oscillator's PN in the 20 dB/decade region with low supply and high current consumption. Besides, narrowing down the conduction angle needs careful consideration of the oscillation startup. Finally, the gate–drain phase shift reduces the passive voltage gain from the drain to gate, and degrades an oscillator's PN in the 20 dB/decade region.

The PN performance of an LC oscillator can be enhanced by adjusting the common-mode frequency of the circuit (F_{CM}) to be at twice the oscillation frequency (F_O). When such a technique is correctly employed, the Q-degradation due to the triode operation of the differential pair is alleviated, and the flicker noise up-conversion to PN is also ideally eliminated [37]. Initially, this condition was satisfied by a separately tuned common-mode (CM) tank [38], [39], [40]. Yet, the requirement for an extra inductor incurs an area penalty, and the need to tune it limits the frequency-tuning range. By introducing a single-end capacitor bank in the main tank, the authors of [37], [41], [42], [43], and [44] also fulfilled the CM resonance condition by accurately modeling the CM inductance and manually controlling the ratio of single-ended to differential-mode (DM) capacitance without the use of tail inductor. However, in the presence of PVT variations, the parasitic capacitance of the oscillator's core devices and the switches in the capacitor banks changes dramatically, shifting the expected F_{CM}. Consequently, even at RT, some mechanisms should be added to adjust the DM and CM capacitor banks such that the oscillator operates near its optimum performance. This issue is even more prominent at CT, since the silicon substrate becomes highly resistive due to carrier freeze-out in the substrate, reducing the parasitic capacitance to ground up to 3.6× [45]. The resulting F_{CM} is expected to change dramatically, degrading PN at 4.2 K [18].

In this article, we propose a digital calibration loop, which automatically adjusts the configuration of the DM and CM capacitor banks to ensure that the oscillator always operates near its optimum performance at 4.2 K. This article is an expanded version of [21], and is organized as follows.

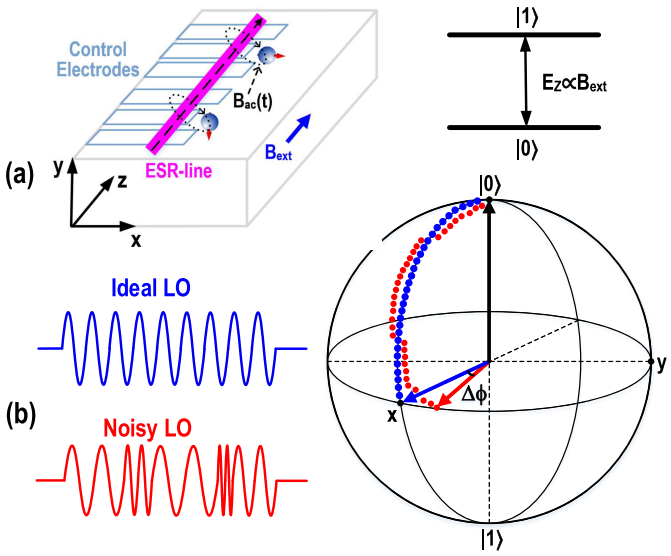

Fig. 2. (a) Generic model of a spin qubit quantum processor comprising qubits encoded in the spin of electrons trapped in quantum dots and (b) illustration of the LO's frequency-noise effect on the qubit control.

Section II derives the specifications of the oscillator based on the gate fidelity for a single-qubit operation. By considering the shot-noise effect for short channel devices in Section III, a new PN expression for an oscillator is derived. Section IV presents the proposed CM resonance calibration technique and details the circuit implementation and design considerations for the cryogenic operation. The measurement results and conclusions are presented in Section V and Section VI, respectively.

II. Oscillator Requirements

A. Manipulation of Qubit States

The cryo-CMOS controller presented in Fig. 1 shows close similarities with conventional RF wireless transceivers. The oscillator performance for wireless applications is typically determined by the error vector magnitude (EVM) and reciprocal mixing of LO phase noise with blockers. To determine the oscillator requirements for quantum computing applications, this section briefly introduces the necessary background information for quantum computing.

A quantum computer operates by processing the information stored in qubits. A qubit is a two-level quantum mechanical system whose instantaneous state can be described as a superposition of its two basis states (denoted as $|0\rangle$ and $|1\rangle$). Any single-qubit state $|\psi\rangle$ can be pictorially presented by a three-dimensional unit vector on the Bloch sphere. The temporal evolution of the qubit state can be described by a unitary propagator U(t), which transforms an initial state $|\psi(0)\rangle$ to a desired state $|\psi(t)\rangle = U(t)|\psi(0)\rangle$. The state evolution corresponds to a vector rotation on the Bloch sphere and the propagator satisfies the Schrodinger equation:

$$j\frac{dU(t)}{dt} = H(t)U(t), \tag{1}$$

where H(t) is the Hamiltonian operator.

Fig. 2 (a) shows a generic model of a spin-qubit quantum processor comprising qubits encoded in the spin of electrons trapped in quantum dots. Under a strong external static magnetic field (B_{ext}), an energy difference (E_Z) proportional to

B_{ext} between electrons with spin up and down is induced. The spin rotates around the z-axis in the Bloch sphere at a rate of the qubit resonant frequency (i.e., Larmor frequency ω_0) with the application of B_{ext} [46]. However, such a rotation is very fast and is limited to the z-axis only.

To rotate around all of the axes with a manageable speed, $|\psi\rangle$ is typically manipulated through the local application of a weak oscillating magnetic field [$B_{ac}(t)$] oriented perpendicularly to B_{ext}, produced by an on-chip electron spin resonance (ESR) line. Suppose that $B_{ac}(t)$ equals $(2\pi/\gamma_e)\omega_R\cos(\omega_{LO}(t)t + \phi)$, where γ_e is the gyromagnetic ratio of the electron, ω_R ($=2\pi f_R$) is the qubit operation speed, and $\omega_{LO}(t)$ is the LO's instantaneous frequency [47]. The resulting Hamiltonian can be estimated by [47]:

$$H_{rot}(t) \approx (\omega_{LO} - \omega_0)\frac{\sigma_z}{2} + \omega_R\left(\cos(\phi)\frac{\sigma_x}{2} - \sin(\phi)\frac{\sigma_y}{2}\right). \quad (2)$$

By substituting (2) into (1), the control propagator could be found: $U_{rot}(t) = \exp(-jH_{rot}t)$.

If ω_{LO} is precisely set to ω_0, the z-component of the Hamiltonian in (2) is eliminated, and the spin rotates around the x/y axis under the application of $B_{ac}(t)$ [see blue plots in Fig. 2 (b)]. The magnitude of $B_{ac}(t)$ determines the rotation speed (ω_R), which is typically above 0.1 MHz. And a higher ω_R is desired as the qubits are less sensitive to dephasing-induced errors, leading to a higher intrinsic qubit fidelity. The rotation axis (x/y) can be controlled by updating the phase ϕ of $B_{ac}(t)$ [i.e., 0° or 90°]. Both the amplitude and duration (τ) of $B_{ac}(t)$ can be exploited to control the rotation angle (i.e., $\theta = \omega_R\tau$).

B. Fidelity Due to LO's PN

However, if there is an instantaneous frequency mismatch between ω_{LO} and ω_0 due to LO's frequency noise (FN), the z-component of the Hamiltonian in (2) is not zero. Consequently, apart from undergoing the desired rotation around the x/y-axis, the spin also suffers from an undesired rotation around the z-axis, thus introducing control errors [see red plots in Fig. 2 (b)]. The frequency error is typically caused by both the LO's frequency inaccuracy and frequency noise. While the former is typically not a concern when a PLL is used, the latter translates to the need for an LO with extremely low noise.

To quantify the accuracy of operation introduced by LO's frequency noise, the gate fidelity F is typically used as the metric that characterizes the agreement between the intended rotation and the real rotation. For a single-qubit operation, the fidelity due to the LO's frequency noise [$\mathcal{L}_\phi(f)\cdot f^2$] can be expressed as:

$$F \approx 1 - \int_0^{+\infty} 2\cdot\frac{\mathcal{L}_\phi(f)\cdot f^2}{f_R^2}\cdot|H_{LO}(f)|^2\, df, \quad (3)$$

where $\mathcal{L}_\phi(f)$ is LO's PN and $H_{LO}(f)$ can be interpreted as a qubit filter function [48]. By considering a worst-case rotation angle of π, the squared magnitude of $H_{LO}(f)$ is [48]:

$$|H_{LO}(f)|^2 = \frac{[1+\cos(\alpha\pi)]\cdot\left(1+\alpha^2\right)}{2\left(1-\alpha^2\right)^2}, \quad (4)$$

where α is the ratio of f to f_R (i.e., $\alpha = f/f_R$). Fig. 3 (a) depicts $|H_{LO}(f)|^2$ versus the frequency offset with various qubit rotation speeds. $|H_{LO}(f)|^2$ shows a first-order low-pass response with a DC gain of 1 and a 3-dB bandwidth of $1.9f_R$, and exhibits high-frequency notches. This indicates that a qubit has a different sensitivity to VCO's PN at different frequency offsets and the choice of rotation speed has a substantial impact on the control fidelity.

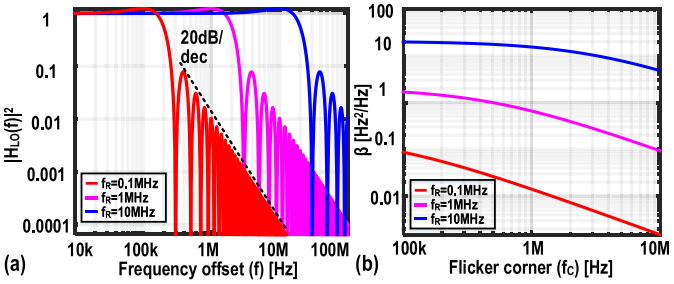

Fig. 3. (a) $|H_{LO}(f)|^2$ versus the frequency offset and (b) β versus f_C by considering a control fidelity of a 99.999% and various qubit rotation speed.

Suppose that the PN[1] of an oscillator can be expressed as

$$\mathcal{L}_\phi(f) = \frac{\beta}{f^2} + \frac{\beta\cdot f_C}{f^3}, \quad (5)$$

where β in Hz^2/Hz determines the PN in the thermal noise region and f_C represents the flicker PN corner. By substituting (4) and (5) into (3), the required β for a typical f_R and f_C higher than 0.1 MHz could be solved numerically and may be estimated by

$$\beta \approx \frac{1}{1-F}\cdot\left(\frac{\pi^2}{2f_R} + \frac{16f_C}{f_R^2}\cdot\frac{(1+0.3f_N)^4}{1.6+(1+0.3f_N)^4}\right), \quad (6)$$

where f_N is the qubit rotation speed normalized to 1 MHz (i.e., $f_N = f_R/1\text{MHz}$). Notice that a larger f_R is desired as the qubit operation is faster. Nevertheless, a larger f_R necessitates the use of microwave bursts with a larger amplitude and shorter duration for a given rotation angle. When a shorter duration is used, the control noise is only mildly averaged out, and hence the qubit is more sensitive to the high-frequency noise [see Fig. 3 (a)]. At first glance, it might conclude that a smaller f_R should be used to relax the oscillator's PN requirement. However, a larger amplitude also enhances the power of the microwave bursts to a qubit, leading to a $1/f_R^2$ factor in (3). Consequently, although a smaller f_R is beneficial for reducing the noise bandwidth, a higher f_R is desired to relax the required PN of an oscillator, as indicated by (6).

For fault-tolerant operations, a qubit fidelity larger than 99.9% is typically required. Therefore, the oscillator targets a fidelity of 99.999% to avoid limiting the inherent fidelity of a qubit. As a proof of concept, a 5-GHz oscillation frequency is targeted as both transmons and spin qubits can be addressed when a frequency doubler and triple are used. By considering those factors, Fig. 3 (b) depicts the theoretical β as a function of f_C for a 99.999% fidelity. As expected, a higher f_R relaxes the required PN. In addition, for each f_R, a higher f_C would require a smaller β and hence lower PN in the thermal-noise region. For instance, as can be gathered from Fig. 3 (b), if f_C is degraded from 1 MHz to 10 MHz for a 1-MHz f_R, the

[1]The PLL's out-of-band PN (mostly contributed by the oscillator) tends to dominate the overall fidelity as the fidelity is determined by LO's frequency noise [see (6)]. Hence, only the oscillator's PN is considered in this article.

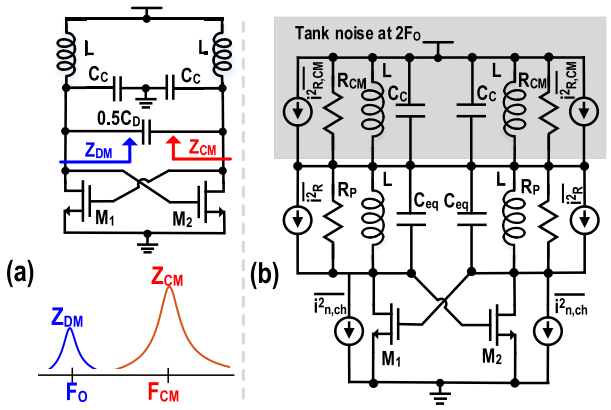

Fig. 4. (a) Class-D/F_2 oscillator's schematic and tank impedance, and (b) its corresponding noise sources.

required PN in the thermal noise region is >8 dB lower so as to maintain the same fidelity, thus increasing the oscillator's P_{DC} by >7×. Consequently, an oscillator with a low f_C is crucial to relaxing its P_{DC}. By considering a state-of-the-art f_R of 1 MHz and an f_C of 3 MHz, the resulting PN at a 10 MHz offset should be below −145.5 dBc/Hz.

III. Phase Noise Analysis

Based on the discussion in Section II, both the oscillator's PN in the thermal noise region and its flicker PN corner f_C are critical to avoid limiting the qubits' intrinsic fidelity. Fig. 4 (a) shows the schematic of a class-D/F_2 oscillator adopted in our design to satisfy these criteria simultaneously. Two sets of capacitors (C_C and C_D) are used to adjust the fundamental and second harmonic resonance of the oscillator, respectively. Due to the auxiliary CM resonance at $2F_O$, this topology reaches within 3 dB of the theoretical PN limit of an ideal cross-coupled *LC* oscillator for a given P_{DC} [37]. Meanwhile, the flicker noise up-conversion of the differential pair transistors ($M_{1,2}$) to PN is also reduced due to the symmetry of oscillation waveforms, thus lowering f_C significantly. Since the oscillator must operate at CT, it is instrumental in understanding its PN behavior at those temperatures as well. However, the conventional PN analysis is insufficient to quantify the difference between the theoretical and measured PN at CT. To this end, a new PN expression for short-channel devices is derived in this section by considering the shot-noise effect.

A. Limitation of Conventional PN Analysis

Assume that the channel current noise generated by a MOS transistor is proportional to its transconductance (g_m) according to the following equation [49]

$$\overline{i^2_{n,ch}(t)} = 4KT_{ch}\gamma\, g_m(t), \tag{7}$$

with K Boltzmann's constant, T_{ch} the channel temperature, and γ the noise coefficient. The PN expression for the oscillator can be found in previous works [49], [50], [51] and is rewritten as

$$\mathcal{L}(f) = 10\log_{10}\Big(\frac{KT_R}{2R_PC^2_{eq}V^2_{osc}}\cdot\frac{1}{(2\pi f)^2}\cdot\Big(1+\gamma\cdot\frac{T_{ch}}{T_R}\Big)\Big), \tag{8}$$

with R_P the equivalent tank parallel resistance, C_{eq} the equivalent tank parallel capacitance, V_{osc} the single-ended oscillation amplitude, and T_R the absolute temperature of the *LC* tank. By analyzing the variation of temperature-dependent terms in (8), the PN at 4.2 K could be partially understood according to the measured characteristics of devices from the target 40-nm CMOS process.

Compared with 300 K, one would expect an ∼18-dB PN reduction by assuming $T_R = T_{ch} = 4.2$ K, as predicted by (8). In addition, the measured ON-resistance of a transistor reduces by ∼2.5× due to the enhanced carrier mobility [52], [53], [54], and the measured quality factor of a spiral inductor exhibits up to a ∼2.5× increase due to both the higher substrate resistivity and metal conductivity at 4.2 K [45]. Consequently, the tank quality factor and R_P are expected to increase by ∼2.5×, thus reducing PN by ∼4 dB. Suppose that the oscillator is operating in the voltage-limited region at both 300 K and 4.2 K. Then, V_{osc} is expected to be fairly constant. Since the measured capacitance of a MOM capacitor (typically used in *LC* tank) changes only ∼5% from 300 K to 4.2 K [45], C_{eq} is not expected to vary significantly. Therefore, the estimated PN improvement of an oscillator is ∼22 dB. This contradicts with the measurement results presented in [18], [19], [20], [21], which show a maximum 12-dB PN reduction when differential pair transistors are implemented by short-channel devices. Such a performance gap between the theoretical analysis and measurement results requires an alternative method of analyzing PN at 4.2 K.

The above analysis assumes $T_R = T_{ch} = 4.2$ K. In practice, the self-heating of devices could raise T_R and T_{ch} much higher than 4.2 K. For instance, by dissipating a 2-mW P_{DC}, a transistor measuring 12 μm/40 nm could exhibit a T_{ch} of ∼44 K due to the self-heating at 4.2 K [55]. However, considering the device dimensions (i.e., 64 μm/270 nm and 135 μm/40 nm) and P_{DC} (i.e., 12 mW and 5 mW) of two published cryo-CMOS oscillators in [18] and [21] respectively, the T_{ch} in prior-art designs is estimated to be below 8 K. Besides, T_R is estimated to be ∼4.2 K due to the proper thermalization of the *LC* tank, as typically implemented by ultra-thick and wide metals to reduce the loss. Consequently, compared with 300 K, the estimated PN reduction of an oscillator is ∼19 dB even by considering the self-heating effect, which is 7 dB higher compared with measurement results [18], [19], [20], [21].

Notice that (7) assumes that the channel noise is thermal noise and proportional to T_{ch}. This is based on the assumptions that carriers in the channel undergo scattering collisions, exchange energy with the lattice, and reach thermal equilibrium with the environment. These assumptions are valid for long-channel devices as the mean-free-path of carriers (∼100 nm) is much shorter than the channel length. However, if a short-channel device is required (e.g., L<100 nm) to optimize speed and to minimize parasitic capacitance, the assumptions underlying (7) are invalid since most carriers undergo little scattering collisions, the carriers in the channel do not have sufficient time to reach thermal equilibrium, and carrier behavior tends more toward the shot noise [56], [57], [58]. Therefore, the channel's white noise is not entirely thermal noise and can be empirically modeled by [59]:

$$\overline{i^2_{n,ch}(t)} = 4KT_{ch}g_m(t)\cdot\xi\cdot(1-\nu)^2 + 2qI_D(t)\cdot\nu^2, \tag{9}$$

where ξ is the noise coefficient, and ν^2 is the Fano factor and a function of the channel length. ν reaches 0 in a long-channel device, and the resulting channel noise is dominated by the thermal noise. On the other hand, it approaches 1 in a short-channel device, and the channel noise tends to be shot noise. For a 40-nm channel-length transistor, ~25% of the total channel noise is contributed by the shot noise at 300 K [56]. Since the shot noise weakly depends on the temperature, it could set a bottleneck for the PN reduction at 4.2 K.

B. PN Analysis by Considering Shot Noise

In this section, the conversion of the circuit noise to the oscillator's PN will be investigated. According to the linear time-variant model [60], the PN of an oscillator is expressed as

$$\mathcal{L}(f) = 10\log_{10}\Big(\frac{\sum_j N_{L,j}}{2\cdot C_{eq}^2\cdot V_{osc}^2\cdot(2\pi f)^2}\Big). \tag{10}$$

$N_{L,j}$ is the effective current noise ($\overline{i_{n,j}^2}$) generated by the j-th device and is given by

$$N_{L,j} = \sum_{k=0}^{\infty}\overline{i_{n,j,k}^2}\cdot\frac{c_k^2}{2}, \tag{11}$$

where $\overline{i_{n,j,k}^2}$ is the current noise at frequencies of $kF_O \pm f$, and c_k is the k-th harmonic's amplitude of the impulse sensitivity function (ISF). $\overline{i_{n,j}^2}$ includes the noise due to resonant tank losses and the channel noise of the active devices. Note that there are two resonances (i.e., ~5/10 GHz) in the tank. The mechanism of how the two resonant peaks affect the PN will be firstly investigated. The PN contributed by the $M_{1,2}$ will be discussed later.

Fig. 4(b) illustrates the major noise sources of a class-D/F_2 oscillator, including the noise of the *LC* tank and differential pair transistors $M_{1,2}$. R_P and R_{CM} are used to model the tank losses at the fundamental and second-harmonic frequencies, respectively. In general, the ISF is related to the shape of the oscillator's waveform [60]. Due to the waveform clipping of a class-D/F_2 oscillator, it could be empirically estimated by

$$\Gamma(t) \approx \frac{1}{2}\cdot\Big(\sin(2\pi F_O t) - m\cdot\sin(4\pi F_O t)\Big), \tag{12}$$

where m is a constant ($\sim 2/\pi$) and depends slightly on the tank quality factor, based on simulations.

1) Noise of the Tank: Since the noise of R_P at frequencies far away from the fundamental is highly attenuated by the *LC* tank, based on (11), the conversion from R_P's noise to PN is then governed by c_1. Hence, the effective noise due to R_P could be found as

$$N_{L,R_P} = 2\cdot\frac{4KT_R}{R_P}\cdot\frac{1}{2\cdot 4} = \frac{KT_R}{R_P}. \tag{13}$$

The tank also largely filters the R_{CM} noise at frequencies far from the second harmonic. According to (11), the conversion from R_{CM}'s noise to PN is based on c_2. The effective noise due to R_{CM} thus could be be expressed as

$$N_{L,R_{CM}} = 2\cdot\frac{4KT_R}{R_{CM}}\cdot\frac{m^2}{2\cdot 4} = \frac{m^2KT_R}{R_{CM}}. \tag{14}$$

2) Noise of the $M_{1,2}$: Unlike the noise generated by the tank, the noise of $M_{1,2}$ is cyclostationary due to the periodic time-varying nature of the $g_m(t)$ and $I_D(t)$. Based on the Parseval's theory, (11) could be rewritten as

$$N_{L,j} = \int_0^{T_{osc}}\frac{\Gamma^2(t)}{T_{osc}}\cdot\overline{i_{n,j}^2(t)}\cdot dt. \tag{15}$$

Since the drain current $I_D(t)$ is periodic, it can be expanded in Fourier series as

$$I_D(t) = I_0\cdot\Big(1+\sum_{p=1}^{+\infty}\eta_p\cos(2\pi pF_O t+\Phi_p)\Big). \tag{16}$$

Assume that Φ_p is zero for the worst-case scenario. By substituting (12), (16), and the second term of (9) into (15), the effective noise due to the shot noise of $M_{1,2}$ could be estimated by

$$N_{L,shot} \approx \frac{q\nu^2 I_0}{2}\cdot(1+m^2-m\eta_1-\frac{\eta_2}{2}+m\eta_3-\frac{m^2\eta_4}{2}). \tag{17}$$

Similarly, the effective noise due to the thermal noise of $M_{1,2}$ can be found by substituting (12) and the first term of (9) into (15)

$$\begin{aligned} N_{L,the} &= 2\cdot\int_0^{T_{osc}}\frac{\Gamma^2(t)}{T_{osc}}\cdot 4KT_{ch}\xi g_m(t)\cdot(1-\nu)^2\cdot dt \\ &\approx \frac{KT_{ch}}{R_P}\cdot\xi\cdot(1-\nu)^2. \end{aligned} \tag{18}$$

3) PN Expression: The complete PN expression can be estimated by substituting (13), (14), (17), and (18) into (10).

$$\mathcal{L}(f) \approx 10\log_{10}\Big(\frac{N_{L,R_P}+N_{L,R_{CM}}+N_{L,shot}+N_{L,the}}{2\cdot C_{eq}^2\cdot V_{osc}^2\cdot(2\pi f)^2}\Big). \tag{19}$$

Based on transient simulations, Fig. 5(a) and (b) depict the simulated drain voltage and drain current of M_1 over one oscillation period at both 300 K and 4.2 K under a 0.5-V supply. $M_{1,2}$ are based on a look-up-table-based Verilog-A model built from the measured drain current versus gate-source and drain-source voltage.[2] In addition, based on (9), the channel white noise is also included in this model[3] to simulate the phase noise at the 20dB/decade region. The inductor is based on a lumped-element model, whose parameters are modified to account for the temperature variation [45]. Compared with 300 K, while the oscillator consumes less current due to the increase of threshold voltage of transistors at 4.2 K, it exhibits a slightly higher oscillation swing due to a 2.5× higher tank quality factor. As expected, as shown in Fig. 5(c), the simulated ISF function from the transient simulation is relatively immune to temperature variations as the oscillation waveforms show similar shapes.

Assumes that $\xi\cdot(1-\nu)^2 = 1$ and $\nu^2 = 0.5$ for a 40-nm channel length transistor. This ensures that the shot noise of $M_{1,2}$ in saturation region contributes to 25% of the total

[2]This is because the foundry PDK does not support device models at cryogenic temperatures.

[3]The "white_noise" function built-in Verilog-A is used to model the power spectrum density of both the thermal noise and shot noise of $M_{1,2}$ [i.e., (9)]. Then, conventional PSS/PNOISE simulations in Spectre RF™ are used to predict the oscillator's phase noise at 4.2 K.

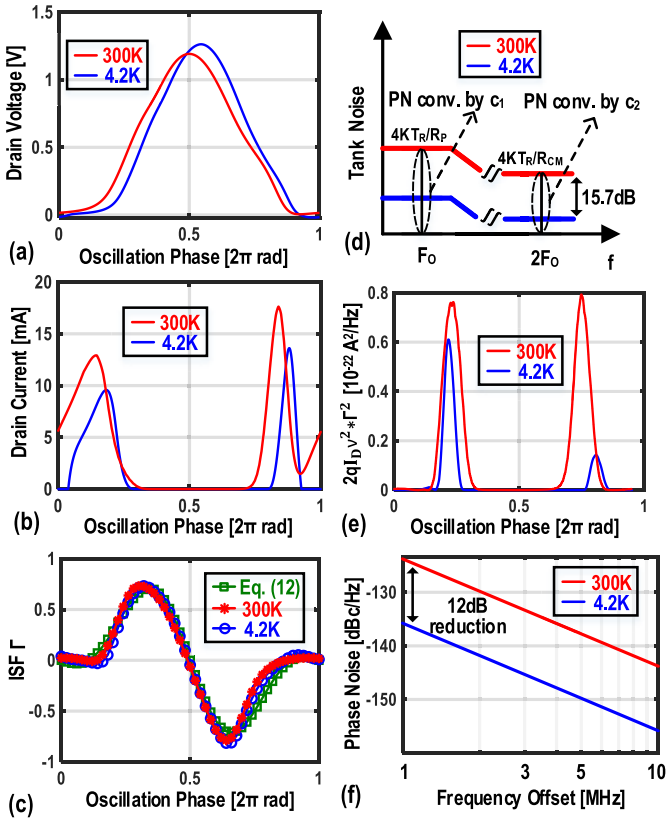

Fig. 5. Simulated (a) drain voltage and (b) drain current of M_1, and (c) ISF function, (d) illustration of the tank noise conversion to PN, (e) simulated effective current noise due to shot noise of $M_{1,2}$, and (f) simulated PN at 300 K and 4.2 K.

TABLE I

CALCULATED AND SIMULATED PN CONTRIBUTION AT 5 GHZ

PN results @ a 1MHz frequency offset	Noise Sources @ 300K				Noise Sources @ 4.2K			
	Tank	Shot	Thermal	Total	Tank	Shot	Thermal	Total
Cal. based on (15)-(24)	-127.0	-127.8	-128.5	-123.0	-147.5	-134.5	-149.1	-134.2
Cal. based on Fig. 5	-126.9	-129.5	-129.3	-123.6	-147.3	-136.5	-151.0	-136.0
Sim. in Spectre RF™	-127.1	-129.3	-129.7	-123.8	-147.6	-136.2	-151.3	-135.8

simulated channel noise, which is in line with the study in [56]. In addition, by considering the self-heating effect (i.e., $T_R = T_{ch} = 8$ K), Fig. 5 (d) illustrates the mechanism of the tank's thermal noise conversion to PN, where c_1 and c_2 determine the conversion of the noise of the R_P and R_{CM}, respectively. Thanks to the T_R reduction, the effective noise due to the tank's thermal noise is significantly reduced. However, the effective noise due to $M_{1,2}$'s shot noise is only minorly reduced [see Fig. 5 (e)]. Consequently, as shown in Fig. 5 (f), compared with 300 K, the PN at 4.2 K only improves by 12 dB, limited by the shot noise. Table I summarizes the simulated and calculated PN contributions at both 300 K and 4.2 K due to the tank's thermal noise and $M_{1,2}$'s thermal noise and shot noise. The presented theory matches well with simulation results. Notice that the shot noise and thermal noise show a similar contribution to the PN even at 300 K. By moving to 4.2 K, the shot noise contributes more than 90% of the total PN due to the substantial reduction of the thermal noise. This implies

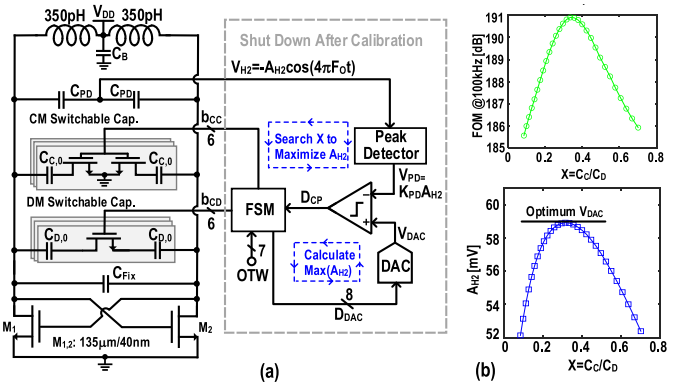

Fig. 6. (a) Block diagram of the calibration loop with the schematic of a class-D/F_2 oscillator and (b) simulated FOM and A_{H2} versus X.

that the shot noise must be carefully modeled for cryogenic designs.

C. PN Consideration in the Flicker Region

The flicker noise power spectral density of a transistor can be modeled by

$$\overline{i_{n,fl}^2(t)} = \frac{K_P}{WLC_{ox}} \cdot \frac{1}{f} \cdot g_m^2(t), \tag{20}$$

where K_P is a process-dependent constant, W and L are core transistors' width and length, respectively, and C_{ox} is an oxide capacitance per area [41]. Unlike the thermal noise, there is no indication of any temperature-dependent mechanism for flicker noise if a constant g_m is used over temperatures [61], [62]. Since the ISF is relatively immune to temperature variations [see Fig. 5 (c)], the PN of an oscillator in the flicker region is not expected to change significantly at CT. Consequently, the flicker PN corner of an oscillator f_C raises mainly due to the PN reduction in the thermal noise region at CT. Fortunately, the flicker noise up-conversion can be significantly suppressed by the selected oscillator topology.

IV. CLASS D/F_2 OSCILLATOR WITH COMMON-MODE RESONANCE CALIBRATION

The class-D/F_2 oscillator has been designed for operation at both 300 K and 4.2 K. Performance targets have been set at 4.2 K for the control electronics of a quantum computer, while the room-temperature operation has been used for convenient circuit validation and debugging. As mentioned earlier, the oscillator's parasitic single-ended capacitance (C_P) is subject to PVT variations. The resulting CM frequency F_{CM} can change dramatically and hence deviate from $2F_O$, thus degrading the PN performance. To resolve this issue, as depicted in Fig. 6, the oscillator features an automatic CM resonance calibration technique to optimize its PN over PVT variations. In this section, the implementation details of the CM resonance calibration loop and class-D/F_2 oscillator will be discussed by considering the effect of the cryogenic operation.

A. Class-D/F_2 Oscillator

As shown in Fig. 6 (a), the class-D/F_2 oscillator is implemented with a thin-oxide NMOS cross-coupled pair ($M_{1,2}$), which are sized with a minimum channel length so as to minimize C_P. To alleviate self-heating of the oscillator, the

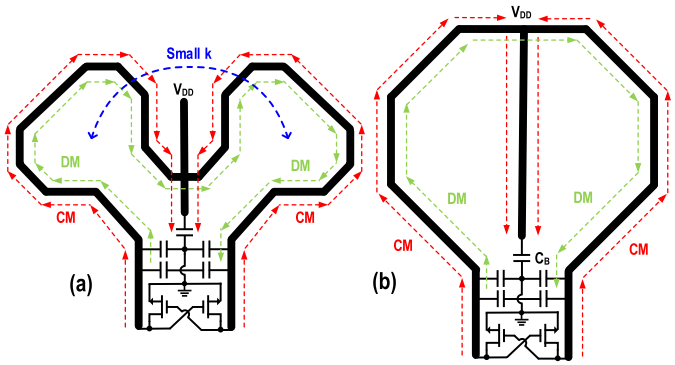

Fig. 7. Layout view of (a) optimized and (b) conventional inductor.

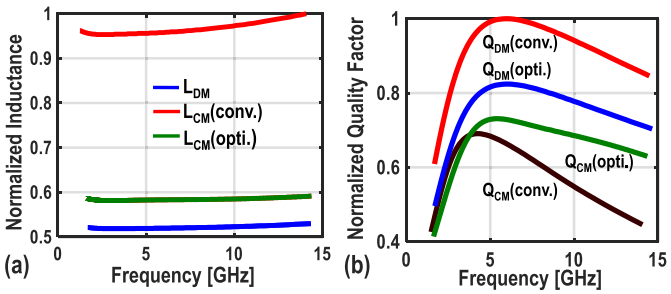

Fig. 8. (a) Inductance and (b) quality factor comparison between the optimized and conventional inductor.

thermal resistance of $M_{1,2}$'s source, drain, and gate terminals are minimized in the layout by placing redundant vias. Two sets of switched capacitor banks (C_C and C_D) are used to adjust the differential-mode and common-mode resonance of the oscillator, respectively. The implementation details of C_C and C_D can be found in [18]. The tank's quality factor degradation due to the switch loss of C_C is very small (i.e., <10%). The control bits of C_C and C_D (b_{CC} and b_{CD}) are derived from a finite-state machine (FSM). In addition, two differential capacitors (C_{PD}) extract the second harmonic of the oscillation voltage A_{H2} (used for calibration). The mismatch between C_{PD} leaks the oscillator's fundamental voltage to the output, affecting the extracted A_{H2}. To achieve the required matching, each C_{PD} is implemented with a 10-fF MOM capacitor.

To satisfy the CM resonance condition, the ratio of single-ended to differential-mode capacitance ($X = C_C/C_D$) should be adjusted to (1+k)/(3-5k) [37], where k is the coupling factor between the tank inductors. However, the supply and ground routing could introduce undesired CM inductances and losses, destroying the CM resonance condition and incurring high PN [63]. To avoid this issue, an explicit CM current return path is realized by an embedded decoupling capacitor inside a transformer in [42]. On the other hand, the authors of [37] and [41] employed coils with an even number of turns to ease the CM termination by ensuring the center tap close to core transistors. Moreover, k is larger than 0 so as to allow a large C_C in [37], [41]. However, to attain a low PN at a low supply voltage, the tank's DM impedance should be reduced, thus advocating for the use of a single-turn inductor. Since in that case, k becomes negative and the required C_C, which includes parasitics, reduces to impractically small values. This issue is even more severe when the CM return path is considered, which increases the CM inductance (L_{CM}) but has little effect on the DM inductance (L_{DM}). To minimize the unwanted magnetic coupling, as shown in Fig. 7 (a), we use two individual coils placed orthogonally to achieve $k \approx 0$. Furthermore, compared with a conventional one-turn inductor as depicted in Fig. 7 (b),[4] the center tap of the optimized inductor is now much closer to the source of the core devices, thus alleviating parasitic L_{CM} by securing the shortest return path for the CM current. As shown in Fig. 8 (a), the optimized inductor shows a 1.6× lower L_{CM}. In addition, for the same inductance, the area of the proposed inductor is also ∼30% lower compared to that of the conventional spiral one. Unfortunately, as shown in Fig. 8 (b), the optimized inductor suffers from a slightly lower DM quality factor (Q_{DM}) due to the partial magnetic-flux cancellation inside each half inductor [64]. Nevertheless, it exhibits a higher CM quality factor (Q_{CM}) and hence a higher R_{CM}, which helps to reduce the PN in the thermal noise region based on (14). Notice that, without properly terminating the oscillator's second harmonic, the flicker PN corner f_C can be easily increased to ∼10 MHz at CT [17]. This translates to a stringent PN requirement in the thermal noise region [see Fig. 3 (b)]. Consequently, even with a slightly lower Q_{DM}, our inductor is still beneficial for cryogenic operation due to a better termination of the second harmonic.

B. Calibration Loop

As mentioned earlier, the X factor should be optimized to ensure that the oscillator operates near the optimum performance. This is evidenced in Fig. 6 (b), which indicates that the simulated FOM at a 100 kHz frequency offset is severely degraded when the X factor deviates from the optimum value. Consequently, some mechanisms should be added to optimize the PN. Notice that, due to the auxiliary CM resonance at $2F_O$, the oscillator's FOM, the tank's CM impedance, and thus the A_{H2} are virtually maximized for the same X value [see Fig. 6 (b)].[5] Hence, the calibration goal is to find the optimum b_{CD} and b_{CC} codes in which A_{H2} is maximized.

As shown in Fig. 6 (a), the calibration loop is composed of a peak detector, a comparator, a voltage DAC, and a finite state machine. At the beginning of the calibration, the CM capacitor bank is kept off, while b_{CD} is set to reach the desired frequency, resulting in the lowest possible X. The second harmonic of the oscillation voltage is extracted at the common node of differential capacitors C_{PD}. A peak detector with a gain of K_{PD} then produces a DC voltage (V_{PD}) proportional to A_{H2}. V_{PD} is compared with the output of the 8-bit DAC (V_{DAC}), and the result is fed to the finite-state machine (FSM).

For now, suppose that V_{DAC} is set exactly to the maximum $V_{PD}(=K_{PD} \cdot A_{H2,max})$. Initially, X is set at its minimum, and the tank configuration is not optimum; thus $V_{PD} < V_{DAC}$ and comparator output (D_{CP}) is one. Consequently, the FSM increases X via reducing b_{CD} by 1 LSB and increasing b_{CC} by 2 LSBs. In this way, the tank's total capacitance ($C_C + C_D$) and thus F_O remain almost constant during the calibration.

[4]The inductor shows a similarity with the transformer's primary winding presented in [42].

[5]Since the higher-order even harmonics are not terminated in this design, the maximum FOM and A_{H2} occur at slightly different X.

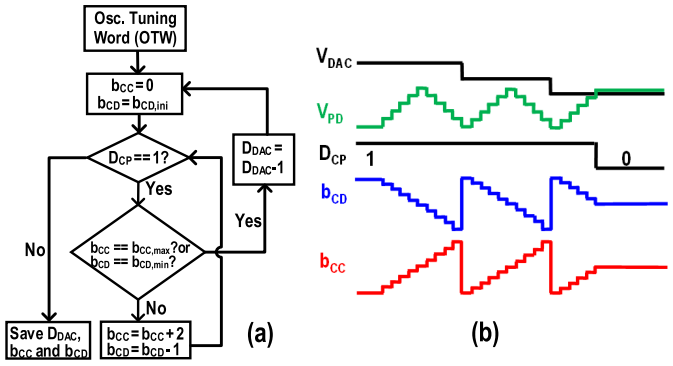

Fig. 9. (a) Calibration flowchart and (b) conceptual waveforms during calibration.

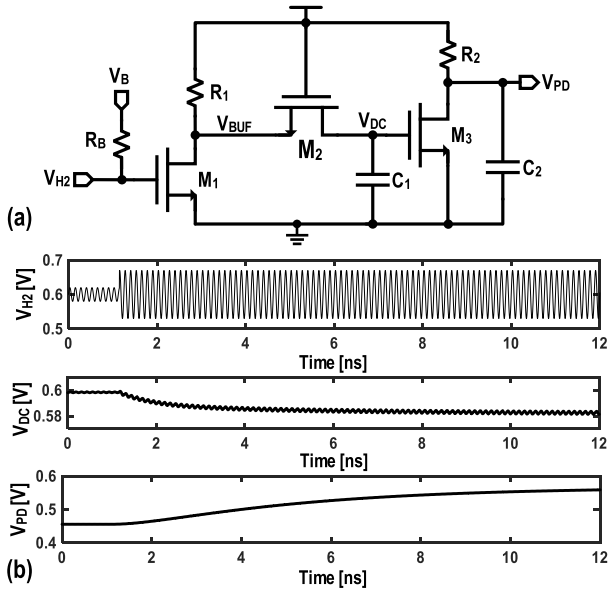

Fig. 10. (a) Peak detector schematic and (b) simulated transient response of the peak detector at 300 K.

This procedure continues until V_{PD}-V_{DAC} and D_{CP} become zero, indicating that the current b_{CD} and b_{CC} states are near the optimum.

The maximum V_{PD}, and hence the required V_{DAC}, depend on PVT, tank's CM quality factor (Q_{CM}), and F_O. Therefore, a second loop is added to adjust V_{DAC} accordingly. Initially, V_{DAC} is intentionally set to a voltage level that is safely higher than the maximum possible V_{PD}. Hence, D_{CP} is always 1, resulting in X being swept from its minimum to maximum. The FSM then lowers down V_{DAC} by 1 LSB and resets X to its minimum possible value again. This process is repeated until D_{CP} becomes zero for the first time. At this point, the DAC and b_{CD} and b_{CC} states are frozen. The calibration circuit is then shut down to save power. The flowchart and conceptual waveforms of the calibration loop are shown in Fig. 9 (a) and (b), respectively.

C. Peak Detector

The schematic of the peak detector is shown in Fig. 10 (a). A common-source buffer is used to isolate the oscillator from the detector's switching activities. The biasing resistor of the buffer (R_B) is implemented with a 10-kΩ unsilicided polysilicon[6] to minimize the tank's CM quality factor degradation. The output of the buffer (V_{BUFF}) is then connected to the detector core, consisting of an NMOS transistor (M_2) and a capacitor (C_1) [65]. The voltage drop on the buffer load resistance (R_1) is designed to be about the threshold voltage of M_2. Hence, M_2 acts as a diode and only turns on in the negative half cycle of the buffer's output (V_{BUFF}). During this phase, M_2 ON-resistance and C_1 form a low-pass filter to extract the average value of V_{BUFF} negative cycle, leading to a peak detection gain of $\sim 1/\pi$. Since the fundamental tone of V_{BUFF} is at $2F_O$ (~10 GHz), M_2 and C_1 are sized to achieve a few hundreds of MHz corner frequency to provide enough attenuation for V_{BUFF} high-frequency components and to guarantee the loop settling within ~20 ns, as shown in Fig.10 (b). Another amplifier (M_3 and R_2) further boosts the desired signal to relax the requirements on the DAC resolution and the comparator noise. K_{PD} of the entire peak detection block is ~6.

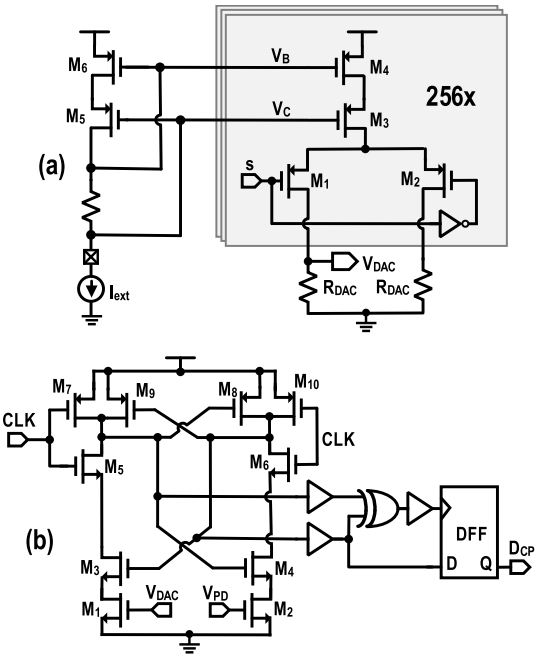

Fig. 11. Schematics of (a) DAC and (b) comparator.

D. DAC, Comparator, and VCO Buffer

Fig. 11 (a) shows the schematic of the voltage DAC, which consists of 256 unary cascode current sources with a unit current of 0.7 μA to satisfy the dynamic range, resolution, and speed requirements. The resistive components of the DAC (R_{DAC}) are implemented by unsilicided polysilicons as they are relatively immune to temperature variations. A constant-current biasing scheme is adopted to generate required bias voltages (V_B and V_C) for the cascode transistors, which circumvents the potential start-up issue at CT.[7] The linearity of the DAC is expected to become worse due to the higher

[6]The measured resistance of the unsilicided polysilicon is relatively immune to temperature.

[7]A constant-g_m biasing circuit was found to fail in start-up at 4.2 K.

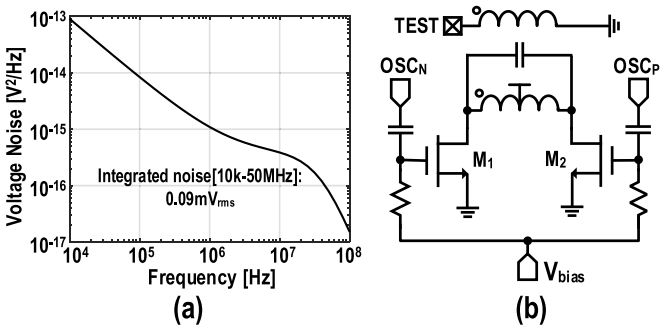

Fig. 12. (a) Simulated noise of the calibration loop referred to the input of the peak detector at 300 K and (b) schematic of the test buffer.

mismatch of transistors at 4.2 K [55]. Nevertheless, the calibration results would not be affected provided that the DAC is monotonic, which is guaranteed by the unary structure. The simulated settling time of the DAC is within 10 ns at 300 K, and is expected to decrease at 4.2 K due to the reduction of the ground capacitance. The simulated RMS voltage noise is $\sim$200 μV at 300 K, which is expected to decrease below 100 μV at CT.

Fig. 11 (b) shows the schematic of the voltage comparator, which comprises a StrongARM latch and a resampling stage. This topology is chosen to minimize the kickback noise as the input pairs ($M_{1,2}$) are clocked through the drain path rather than the source path [66]. The comparator's offset shifts the DAC control code at the optimum point, which consumes some dynamic range of the DAC. Nevertheless, it does not affect calibration results since the DAC is designed with a sufficient dynamic range. A resample stage is adopted to preserve compared results when the CLK is low, and to synchronize the comparator output with the digital clock. Fig. 12 (a) shows the simulated noise of the calibration loop referred to the input of the peak detector at 300 K. The integrated voltage noise is $\sim$90 μV, ensuring that the calibrated PN is within 1 dB of the optimum, as can be gathered from Fig. 6 (a).

Fig. 12 (b) shows the schematic of the VCO buffer, which is an AC-coupled common-source amplifier with a transformer load. The buffer is designed with a sufficiently large swing to drive the long cable of the cryogenic measurement setup and the instrument. The biasing resistor is implemented with unsilicided polysilicon ($\sim$30 kΩ) to avoid the reduction of the VCO's tank quality factor. Since the buffer consumes a high P_{DC}, it can increase the temperature of the VCO core, degrading PN. For example, at an ambient temperature of 4.2 K, the substrate heating was observed to be more than 50 K and 7 K, when respectively measured at distance of 0 μm and 15 μm from a heater dissipating 6.5 mW [55]. To mitigate this issue, the buffer is placed physically far away ($\sim$ 100 μm) from the VCO in the layout.

V. Measurement Results

The oscillator with the proposed CM resonance calibration technique is implemented in a standard 40-nm bulk CMOS process. Fig. 13 (a) and (b) respectively show the chip micrograph and measured power breakdown at 4.2 K. The core area of the chip is 0.15 mm^2, in which the calibration circuits occupy $\sim$0.01 mm^2. The oscillator has been wire-bonded on

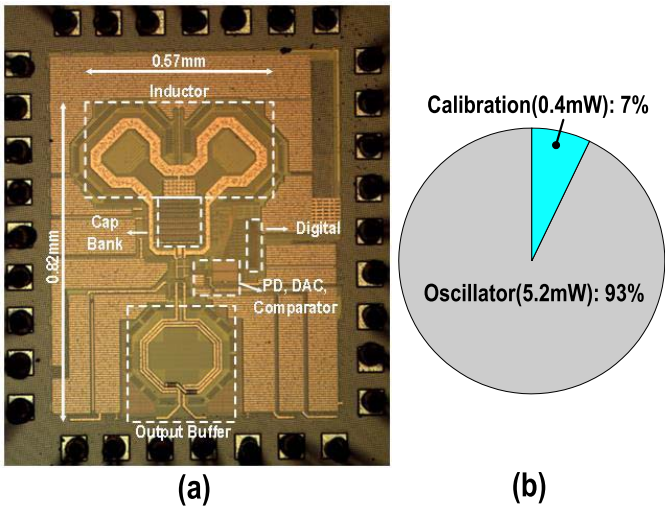

Fig. 13. (a) Chip micrograph and (b) measured power breakdown at 4.2 K.

a printed circuit board (PCB) for room temperature and cryogenic measurements. To characterize its performance at 4.2 K, the PCB was mounted at one end of a dipstick, which immersed the oscillator sample into the liquid helium [18]. The oscillator's PN has been measured from an R&S FSWP8 phase noise measurement setup. A signal generator with a nominal frequency of 50-MHz is used to provide the clock for calibration. At 300 K, the oscillator consumes 4.3 mW from a 0.5-V supply. By cooling the chip to 4.2 K, it consumes 5.2 mW (excluding 0.4 mW of the calibration loop) from a 0.6-V supply. The oscillator can cover an output frequency range of 4.1–5 GHz and 4.4–5.3 GHz at 300 K and 4.2 K, respectively. The increased output frequency at 4.2 K is mainly due to the reduction of the parasitic ground capacitance to the substrate. The oscillator's frequency change is not a concern as the output frequency can be precisely set by a PLL.

The oscillator's PN is measured over all possible b_{CC} and b_{CD} states while disabling the calibration to find the best and worst PN profiles over the tuning range at 300 K. The calibration loop is then activated to investigate the effectiveness of the proposed technique. Fig. 14 (a) shows the measured PN profiles before and after automatic calibration at 4.56 GHz. The calibration loop successfully finds the optimum b_{CC} and b_{CD} codes, suppressing the oscillator's PN from $-$87.9 dBc/Hz to $-$98.6 dBc/Hz at a 100 kHz offset. It also reduces the flicker PN corner from 1 MHz to 130 kHz at 300 K. Fig. 14 (b) and (c) respectively depict the measured flicker PN corner and PN at a 100 kHz offset of the oscillator over the tuning range. The calibrated results follow the optimum ones in most cases.

The oscillator's PN has been measured at 4.2 K as well. Fig. 15 (a) depicts the measured PN profiles before and after automatic calibration at 4.65 GHz. The calibration is capable of reducing the oscillator's PN from $-$90.7 dBc/Hz to $-$102.9 dBc/Hz at a 100 kHz offset. Moreover, Fig. 15 (b) and (c) respectively depict the measured flicker PN corner and PN at a 100 kHz offset of the oscillator over the tuning range, indicating the robustness of the calibration at 4.2 K. After the automatic CM resonance calibration, a PN of $-$153.8 dBc/Hz at a 10 MHz offset (i.e., $\beta = 0.041$ Hz^2/Hz) and a flicker PN corner f_C of 1.3 MHz are achieved. This translates to an estimated fidelity of 99.999% for an f_R higher

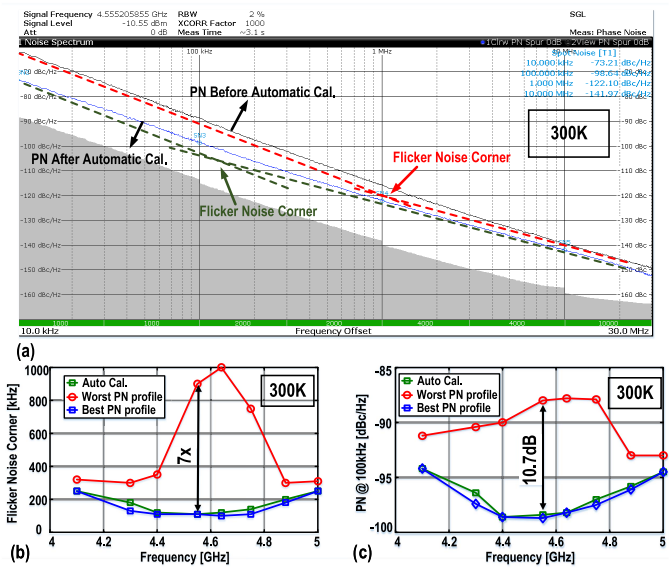

Fig. 14. (a) Measured PN profiles before and after automatic calibration at 4.56 GHz; measured (b) flicker noise corner and (c) PN at a 100 kHz offset over its tuning range for the worst, best, and calibrated at 300 K when a 50-MHz calibration clock is used.

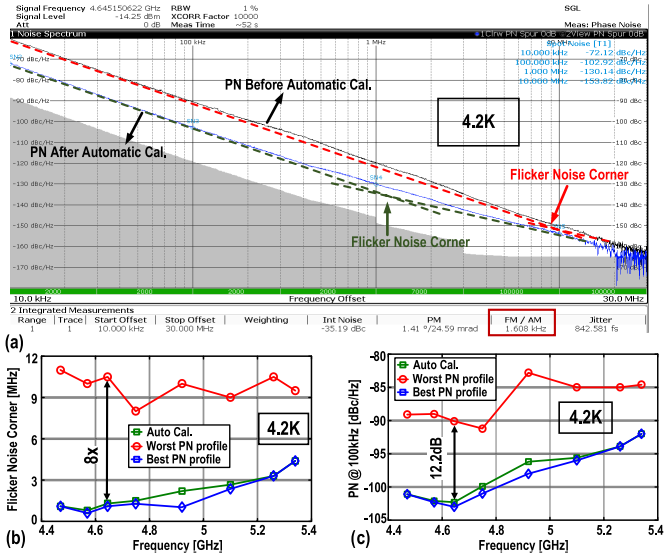

Fig. 15. (a) Measured PN profiles before and after automatic calibration at 4.56 GHz; measured (b) flicker noise corner and (c) PN at a 100 kHz offset over its tuning range for the worst, best, and calibrated at 4.2 K when a 50-MHz calibration clock is used.

than 0.25 MHz, thus satisfying the requirements of LO generation for quantum computing applications. Compared with 300 K, the normalized PN reduction at a 100 kHz offset is ∼2 dB (∼3.7 dB) before (after) the automatic calibration. Those results suggest that the absolute flicker noise of transistors is not a strong function of temperature. Moreover, the normalized PN reduction at a 10 MHz offset is ∼11 dB, which is in line with our analysis presented in Section III.

Fig. 16 shows the measured settling of the calibration loop. For this measurement, instead of using the regular 50 MHz clock frequency, a very low-speed clock (0.5 kHz) is used for the calibration loop to allow monitoring of the comparator output D_{CP}, DAC code D_{DAC}, and b_{CC} and b_{CD} states during

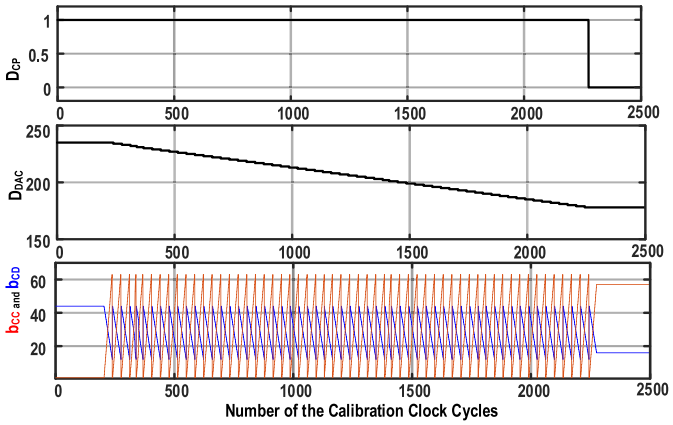

Fig. 16. Measured settling behavior of the calibration loop at 4.2 K when a 500-Hz calibration clock is used.

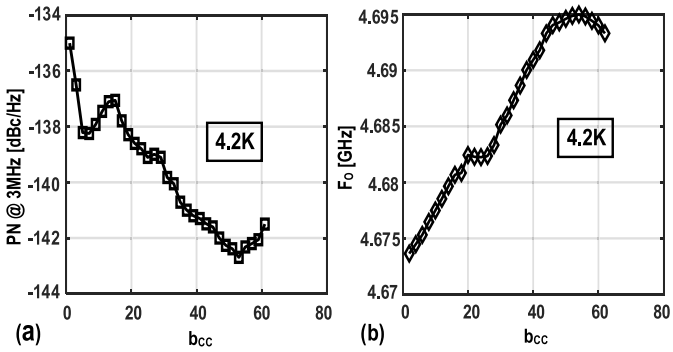

Fig. 17. Measured (a) PN at a 3 MHz offset and (b) oscillator frequency by increasing b_{CC} by 2 LSBs and reducing b_{CD} by 1 LSB at 4.2 K.

the calibration via an SPI link.[8] Initially, the DAC code voltage is too high and D_{CP} is 1. This results in b_{CC} being swept from its minimum to maximum and b_{CD} being swept from its maximum to minimum. Then, the DAC output code is gradually reduced by 1 LSB to search the maximum peak detector voltage V_{PD}. Once D_{CP} becomes 0 for the first time, the D_{DAC}, b_{CC}, and b_{CD} are frozen. The calibration loop successfully settles from an initial setting ($b_{CC} = 1, b_{CD} = 44$) to the optimized b_{CC} and b_{CD} states within 2500 clock cycles. Consequently, the estimated calibration time is less than 50 μs during the nominal operation. Fig. 17 shows the measured oscillation frequency (F_O) and PN versus b_{CC} while sweeping $X = C_C/C_D$ at 4.2 K. At each sweep step, b_{CC} is increased by 2 LSBs and b_{CD} is reduced by 1 LSB. In this way, F_O remains almost constant during the calibration. When this technique is employed in a PLL, F_O is first roughly adjusted by the coarse frequency selector, this calibration is then run to find the optimum X, and finally, the PLL locks to the desired frequency by using a tracking bank.

Table II compares the performance of the presented oscillator with the state-of-the-art. The achieved FOM of this work at RT is limited by the low supply voltage and by the lower tank's quality factor, due to the use of a smaller single-turn inductor and a larger capacitor bank [see Fig. 13]. However, our work

[8]In this chip, due to the speed limitation of the SPI link and long cables, we cannot directly monitor D_{CP}, D_{DAC}, b_{CC} and b_{CD} states during the calibration if the regular 50 MHz clock frequency is used.

TABLE II
TABLE OF COMPARISON WITH PRIOR ART

	This Work		ISSCC'2021 [19]	ISSCC'2022 [17]		CICC'2021 [20]	JSSC'2018 [18]	ISSCC'2015 [41]	ISSCC'2015 [37]	JSSC'2015 [40]	ISSCC'2018 [44]
Osc. Topology	NMOS CM Resonance Class-D/F_2		CMOS Push-Pull LC-Tank VCO	Hybrid Class B/C Mode-Switching VCO		CMOS Class-B VCO	NMOS CM Resonance Class-$F_{2,3}$	NMOS CM Resonance Class-$F_{2,3}$	NMOS Implicit CM Resonance	NMOS $2f_{LO}$ Tail Tuning	CMOS DM Resonance Inverse Class-F
Temperature [K]	300	4.2	4.2	295	3.5	4.2	4.2	300	300	300	300
Frequency [GHz]	4.73	4.65	12.7	15.3	15.9*	10.8	6.3	7	3.3	8.4	4.51
Supply Voltage [V]	0.5	0.6	NA	1.35	1.4	1.1	1	1	0.9	1.5	0.6
Tuning Range	4.1-5 (19.8%)	4.4-5.3 (18.6%)	NA	13.4~17.0 (23.7%)	13.9~18.1 (25.5%)	9.4-11.6 (21%)	5.8-7.3 (25%)	5.4-7 (25%)	2.85-3.37 (27.2%)	7.4-8.4 (12.7%)	3.49-4.51 (25.5%)
Power [mW]	4.3	5.3	4.38	3.55	3.08	1.7	12	10	6.8	20	1.14
PN [dBc/Hz] @100kHz/1MHz/10MHz	-99.0/ -122.4/ -143.0	-102.9/ -130.2/ -153.8	-87.4 -114.5 -136.2	-88.5*/ -112*/ -132.6*	-93.1*/ -119.9*/ -141.7*	-83 -113 -138	-94/ -120/ -149	-102.1/ -124.5/ -144.5	-106*/ -129.5*/ -150.2*	-88*/ -118*/ -146.8	-98.5/ -123.7*/ -143.7
FOM** [dB] @100kHz/1MHz/10MHz	186.2/ 189.6/ 190.2	189/ 196.3/ 200	183.1/ 190.2/ 191.2	186.1/ 189.9/ 190.3	191.3/ 198.7/ 201.1	183.7 193.7 196.4	179.2/ 185/ 194	188.9/ 191.4/ 191.4	188/ 191.5/ 192.2	173.5/ 183.5/ 192.3	191/ 196.2/ 196.2
Flicker Corner [kHz]	180	1300	800	55-145	165-497	4000	5700	130	200	600	300
Technology	40nm CMOS		40nm CMOS	130nm SiGe HBT		40nm CMOS	40nm CMOS	40nm CMOS	28nm CMOS	55nm CMOS	65nm CMOS
Oscillator Area [mm^2]	0.14		NA	0.05		0.1*	0.13	0.13	0.19	0.17	0.14
Calibration Area [mm^2]	0.01		NA	NA		NA	NA	NA	NA	NA	NA
Inductor	One Turn		2 Inductors	2 Inductors		One Turn	1:2 XFMR	1:2 XFMR	Two Turns	One turn+tail Ind.	2:4 XFMR
CM Resonance Calibration	Auto		NA	NA		NA	Manual	Manual	Manual	NA	Manual

*Estimated from the measured phase noise plot of the oscillator **FOM=|PN(f)|+20log10(F_0/f)-10log10(P_{DC}/1mW)

is the only one offering automatic CM resonance calibration, while requiring a negligible area overhead ($\sim$0.01 mm^2). Thanks to the calibration loop and the optimization of the inductor layout, this work achieves a 200-dB FOM in the thermal noise region at 4.2 K and meets the PN specification required for the control electronics of a scalable quantum computer. In addition, our cryo-CMOS oscillator reaches the performance of a recent SiGe HBT design in [17]. Moreover, it also shows more than 5-dB FOM improvement in the flicker noise region, compared with the cryogenic oscillator in [18], [19], and [20]. The proposed technique will potentially enable the realization of cryogenic low-power, low-jitter frequency synthesizers required for the control of quantum computers.

VI. CONCLUSION

A cryo-CMOS LC oscillator for the qubit control is presented. The impact of the oscillator's PN on the qubit fidelity is analyzed in depth. Based on the required fidelity for a single-qubit operation, the oscillator's PN specification is firstly derived. In addition, a new PN expression is derived by considering the shot-noise effect to explain the difference between the theoretical predictions and measurement results at CT. The implemented oscillator features an automatic CM resonance calibration technique to reduce its PN. At 4.2 K, the oscillator achieves -153.8-dBc/Hz PN at a 10 MHz offset and 1.3-MHz flicker PN corner, while consuming only 5.2 mW at 4.2 K. Such a performance is sufficient to achieve a fidelity of 99.999% for an f_R higher than 0.25 MHz, thus meeting the stringent requirements of a qubit controller.

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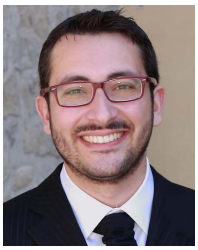

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