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DOI
10.1016/j.applthermaleng.2022.119503

Publication date
2023

Document Version
Final published version

Published in
Applied Thermal Engineering

Citation (APA)
Sattari, R., Hu, D., Liu, X., Zeijl, H. V., Vollebregt, S., & Zhang, G. (2023). Transient thermal measurement on nano-metallic sintered die-attach joints using a thermal test chip. *Applied Thermal Engineering*, *221*, Article 119503. https://doi.org/10.1016/j.applthermaleng.2022.119503

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Applied Thermal Engineering 221 (2023) 119503

Contents lists available at ScienceDirect

Applied Thermal Engineering

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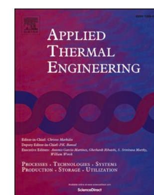

Research Paper

Transient thermal measurement on nano-metallic sintered die-attach joints using a thermal test chip

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ARTICLE INFO

Keywords:
Power electronics
Sintered die-attach joints
Transient dual interface method
Thermal test chip
Junction-to-case thermal resistance
Infrared thermography

ABSTRACT

The rapid development of power electronics has challenged the thermal integrity of semiconductor packaging. Further developments in this domain can be supported significantly by utilizing fast and flexible thermal characteristic evaluation. This study employs the transient dual interface method (TDIM) to characterize and compare the thermal resistance of Ag- and Cu-sintered die-attach joints using an in-house developed thermal test chip (TTC). The proposed TTC with 82.5% active area achieves a temperature sensitivity of 12 Ω/K and maximum power of 360 W per cell, which are 50% and 44% higher than the state-of-the-art, respectively. The uniformity of the temperature distribution (1 °C at 68 W) is verified by infrared thermography. The cost-effective manufacturing process allows the design to be applied to any substrate, such as SiC or GaN. Ag and Cu sintering is performed to bond the TTC on a Cu substrate, and the junction-to-case thermal resistance of the sintered structures is extracted. The lowest junction-to-case thermal resistance of 0.144 K/W is measured for the device sintered using Ag paste. Meanwhile, the Cu sintered structure exhibits a comparable value of 0.158 K/W. The proposed TTC in combination with TDIM accelerates the introduction of novel and cost-effective materials such as Cu.

1. Introduction

Thermal management is one of the major issues in microelectronic packaging, especially for high-power-density devices in advanced computing and power electronics. Driven by energy transitions, the demand for reliable power electronics is increasing [1]. Wide-bandgap (WBG) semiconductor devices can operate at considerably higher temperatures, that is, 400 °C and above, whereas the practical operating temperature of silicon electronics is limited to 150 °C [2]. This unique feature of the WBG technology presents a significant breakthrough in the next generation of power modules [3,4]. However, the increased power densities, together with the emergence of WBG semiconductors, raise new challenges for the thermal management of electronic packages, impeding the practical development of high-temperature and high-power electronics [5,6]. To address these challenges, novel materials and semiconductor packages are being investigated to overcome thermal-mechanical reliability issues [7–12]. Most research focus on the die-attach layer between the device and its substrate, as this interface substantially affects the efficiency of package heat removal. Furthermore, the die-attach layer is one of the most critical interfaces determining the reliability of a power electronic package.

Recently, nano-metallic sintering, such as that of Ag and Cu, has received extensive attention in die-attach technology [13–16]. Nano-metallic materials are tuned to have process temperatures comparable to those of conventional solders. However, in contrast to soldering, nano-metallic sintering is an irreversible process, yielding a material with a higher melting point and excellent electrical and thermal conductivity [17–19]. The evaluation of the thermal performance of nano-metallic materials as a die-attach layer is crucial for developing and applying these materials in corresponding processes and packages.

Conventionally, to determine the junction-to-case thermal resistance θ_{JC}, the junction temperature T_j, case temperature T_c, and power dissipation of the device under test (DUT) must be measured. This widely used method applies a thermocouple to a case to measure the case temperature. However, the thermocouple can only estimate the temperature of a single contact point under the DUT, whereas the temperature distribution over the heatsink may not be uniform. Consequently, the accuracy and reproducibility of the conventional thermocouple

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https://doi.org/10.1016/j.applthermaleng.2022.119503
Received 14 May 2022; Received in revised form 29 September 2022; Accepted 17 October 2022
Available online 21 October 2022
1359-4311/© 2022 Published by Elsevier Ltd.

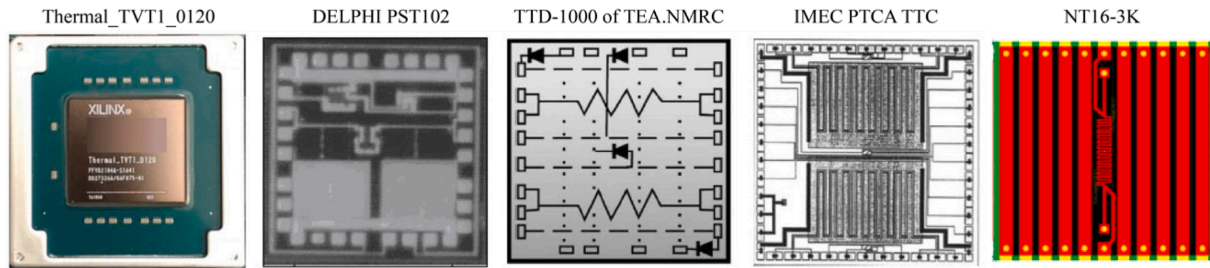

Fig. 1. Conventional TTC designs [27,29,35–37].

method are low [20]. In 2010, the JEDEC51-14 standard specified the transient dual interface method (TDIM) without thermocouples to improve the reproducibility of $\theta_{th\text{-}JC}$ measurement with a 1D dominant heat flow path [20,21].

For a systematic approach to apply the TDIM method and measure the junction-to-case thermal resistance, it is preferable to use a chip that provides power delivery and temperature measurements in the test package [22]. Transient thermal measurements of sintered metallic materials have been reported by utilizing device characteristics, such as the gate-emitter voltage [13,23,24] and forward voltage [25,26]. Further developments in this domain can be supported significantly through fast and flexible thermal characteristic evaluation for power electronic packaging. Therefore, a universal solution is urgently required to enable fast material selection in different user cases.

Such a thermal test chip (TTC) includes microheaters to mimic the device power mapping and sensors for tracking the junction temperature. Recently, TTCs have been presented to conduct reliability assessments, thermal characterizations, and qualifications of materials and semiconductor packages [22,27–38]. A few of the previously proposed TTCs are shown in Fig. 1. Microheaters can be developed using insulated-gate bipolar transistors (IGBT) as unit power cells [39] or CMOS transistors [40,41]. They can provide precise control over the power owing to their small size; however, they provide less uniformity in power distribution, which is critical for many applications. Moreover, front-end TTCs, developed by semiconductors, can only be realized in specific process technologies, while back-end TTCs, powered by resistive Joule heating, can be applied to any kind of semiconductor substrate, such as SiC or GaN, in thin film technology. Previous studies have also used silicon diodes as temperature sensors [29]. However, resistive temperature detectors (RTD) exhibit a four-fold higher sensitivity than Si diodes during calibration [27].

In this study, a fast and flexible thermal evaluation approach for nano-metallic die-attach joints is presented. An in-house developed TTC [42] is applied as a tool in TDIM to compare the thermal conductivities of different nano-metallic sinter pastes. Our TTC contains Ti thin-film resistive microheaters and resistive temperature detectors. The TTC, with an active heating area of 82.5%, reaches a temperature sensitivity of 12 Ω/K, and maximum power of 360 W per cell, which are 50% and 44% higher than the state-of-the-art, respectively [28]. The TTC was bonded on a Cu substrate (further referred to as the case) with different metallic sinter pastes (Ag and Cu). The thermal performance of different die-attach sinter pastes was evaluated and compared using the TDIM method following the JEDEC51-14 standard. The details of the experimental method, including the design and fabrication of the proposed thermal test chip, sintering experiment, and measurement setup, are discussed in Section 2. Section 3 addresses the calibration and thermal uniformity of TTC, followed by junction-to-case thermal resistance analysis of the four samples using TDIM. In addition, scanning acoustic microscopy (SAM) is applied to detect the microstructure evolution. Finally, the thermal characterization results are compared, and the potential capability of Cu nanoparticle sintering in die attach technology is discussed in Section 4.

2. Experimental method

The conventional junction-to-case thermal resistance measurement method directly measures the temperature difference using thermocouples combined with on-chip temperature sensors [20]. However, this method is susceptible to errors. First, the temperature distribution over the package case may not be uniform, while the thermocouple measures the temperature only at its contact point. Second, the thermocouple is not entirely embedded in the cooling plate, and therefore does not provide an accurate temperature reading. Third, a trench or hole is needed at the backside of the heatsink plate to place the thermocouple, which adversely affects the accuracy of the measurement and influences the thermal resistivity of the heat removal path. Moreover, the clamping pressure applied in this method might close any potential delamination at the interfaces that must be detected in reliability experiments.

The TDIM mitigates the errors in the thermocouple measurements, allowing for higher reproducibility and consistency without a case temperature measurement [43]. To evaluate the thermal impedance or $Z_{\Theta JC}$ (t), the following equation is defined:

$$Z_{\theta JC}(t) = \frac{T_J(t) - T_J(t=0)}{P_H}, \quad (1)$$

where P_H is the constant power dissipated by the DUT at t = 0 and $T_J(t)$ is the time-dependent junction temperature measured by a dedicated RTD when the case surface is sufficiently heat sunk by a cooling setup.

This method requires two measurements under different cooling conditions on the case surface. Accordingly, the thermal impedance does not change until the heat reaches the heatsink contact, where the temperature starts to rise. At this point, the impedance curves begin to separate, and the external thermal resistance contributes to heat removal. The cumulative thermal resistance at the separation point of these two measurements is denoted as $R_{\theta JC}$.

A constant current is applied to the on-chip microheaters to generate a certain P_H to heat the DUT. To measure $T_J(t)$, on-chip high-precision RTDs with a sensitivity of 12 Ω/K are used. After the heating power is switched off, the data acquisition system records the RTD transient resistance. The online RTD data provides a cooling curve that is not disturbed by heating power. Using the RTD calibration data of the TTC (discussed in Section 3.1), its resistance is converted to the DUT junction temperature.

2.1. TTC design and fabrication

TTCs have been widely used in various thermal reliability experiments as the primary tool for applying heat distribution and measuring the junction temperature. The TTC employed in this experiment can generate programmable power mappings, for example, uniform and non-uniform power densities, while monitoring the in situ junction temperature by three RTDs. The chip comprises heating and sensing units combined in 4 × 4 mm^2 modules. Modules can be combined monolithically or by post-processing to support larger die sizes, which provides the freedom to adjust the number of active cells in the rows and columns to precisely mimic the behavior of correspondingly larger

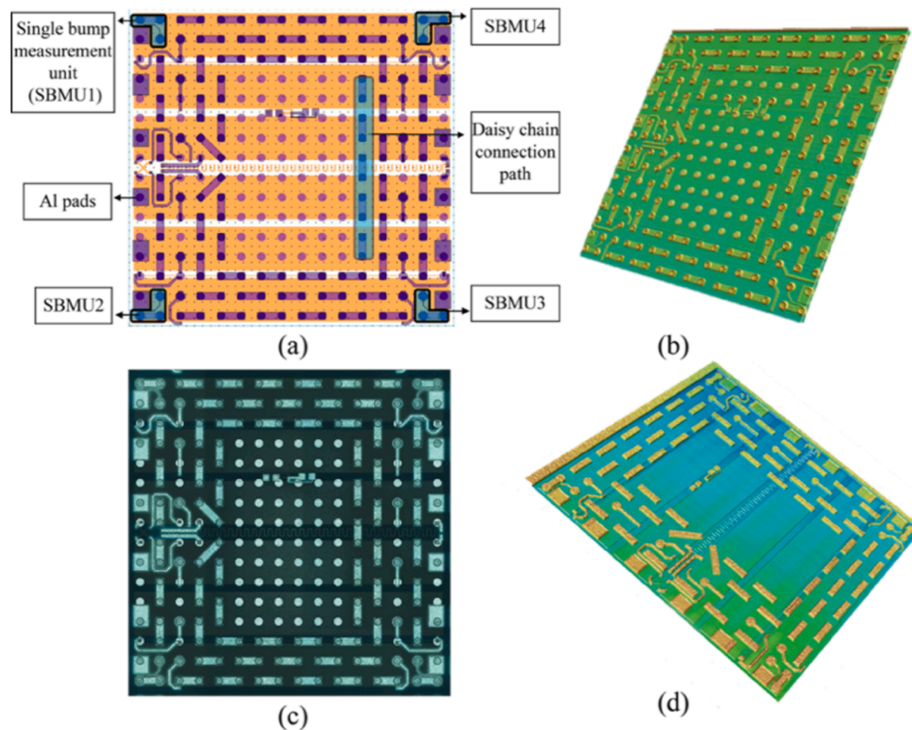

Fig. 2. (a) Second metallization layer including single bump measurement units (SBMU) and daisy chain connections, (b) 2D optical microscopy of a unit cell, (c) 3D optical imaging of the complete process fab-out, and (d) 3D optical imaging after the second metallization layer.

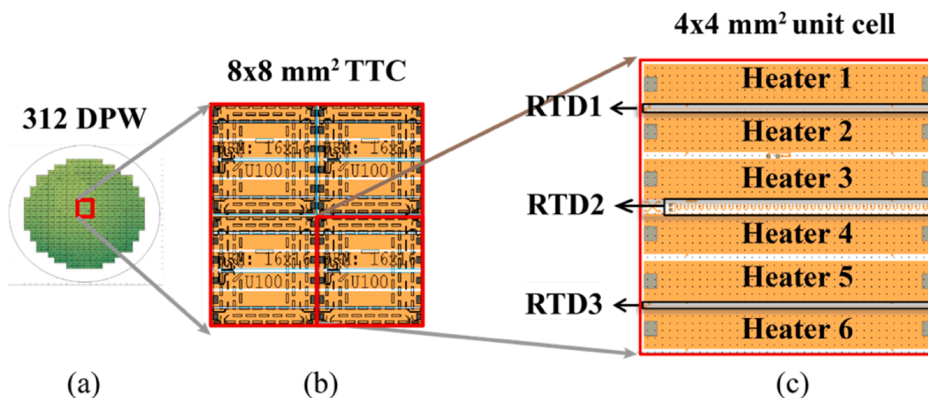

Fig. 3. (a) Wafer layout design including 312 4 × 4 mm^2 cells, (b) an array of 2 × 2 as the DUT in TDIM, and (c) a unit cell.

power modules. Compared to state-of-the-art devices [27,28], the thin-film test chip used improves the cell power, power homogeneity, RTD sensitivity, and sensing spatial resolution [42]. The enhanced uniformity of the temperature distribution was verified using finite element method (FEM) simulation and infrared (IR) thermography.

The thin film test chip contains three metal layers. The first metallization layer is Ti, which is a CMOS-compatible material. Moreover, the temperature coefficient of resistance (TCR) of Ti is 8.5 × 10^{-6}/°C, making it a suitable option for RTD materials. The second metal layer is Al, which creates interconnects and daisy chain connections. The top metal layer contains Al having 100 μm octagonal bonding pads with a pitch size of 250 μm that can be used for both wire-bonding and, with appropriate under-bump metallization (UBM) added, for flip-chip bumping. Compatibility with flip-chip assembly technology allows for the reliability investigation of solder bumps and solder joints. To this end, the second metallization layer of the TTC unit cell, shown in Fig. 2, contains blocks of daisy chain connections and single bump measurement units in the four corners that are mainly susceptible to failure.

There are 312 dies per 100 mm wafer (DPW), as shown in Fig. 3(a). The smallest heating cell is 4 × 4 mm^2, including six electrically isolated microheaters and three RTDs, as depicted in Fig. 3(c). Microheaters can be activated individually using separate input/output connections. Apart from the modularity in size, the chip supports adjustable power mappings and power densities, which allows it to be compatible with the desired (non)uniform active power distributions or hotspot profiles for reliability experiments. To monitor the dissipated power, 4-point Kelvin connections are provided. The TTC unit cell dedicates 82.5% of the area to active heating elements, which allows the chip to meet the JEDEC standards regarding power homogeneity [44]. The 3D model of a unit cell was designed in SolidWorks®, and its power distribution was simulated in COMSOL® Multiphysics, as shown in Fig. 4. The unit cell dissipates 16 W of power, while each microheater is driven by a 200 mA current.

Three RTDs are located such that two microheaters are between each of the two RTDs, which is independent of the cell configuration. Therefore, RTD data provides temperature mapping with uniform and

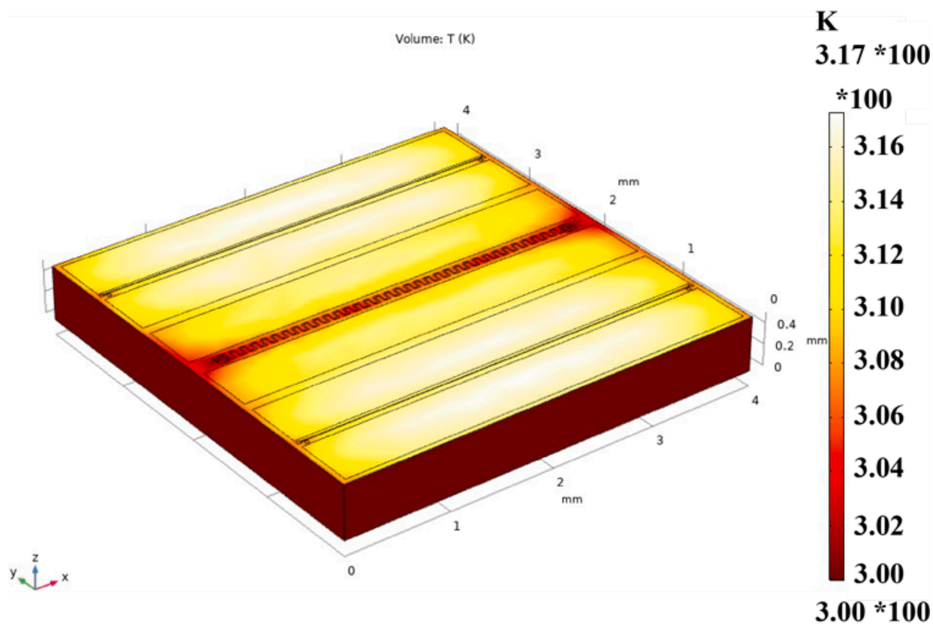

Fig. 4. Unit cell designed in SolidWorks and simulated in COMSOL Multiphysics.

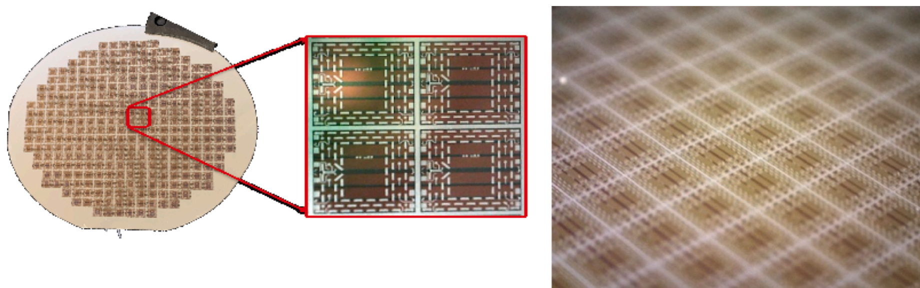

Fig. 5. 100 mm processed silicon wafer containing arrays of 2 × 2 TTC unit cells (zoomed in).

sufficient spatial resolution. Similar to the microheaters, 4-point Kelvin connections are included in the RTD design for accurate temperature measurements.

Two types of RTDs are designed with two different geometries to meet different application requirements. The RTD in the center has a spiral or meandering shape with a Ti line width of 15 μm, whereas the top and bottom RTDs are designed in a linear shape with a Ti line width of 5 μm. The spiral RTD (SRTD) has a wider line width and, therefore, better fabrication reproducibility than the linear RTD (LRTD). Consequently, this results in a higher batch-to-batch uniformity in the resistance. A higher process uniformity allows for more straightforward calibration to meet the required RTD accuracy. However, the drawback

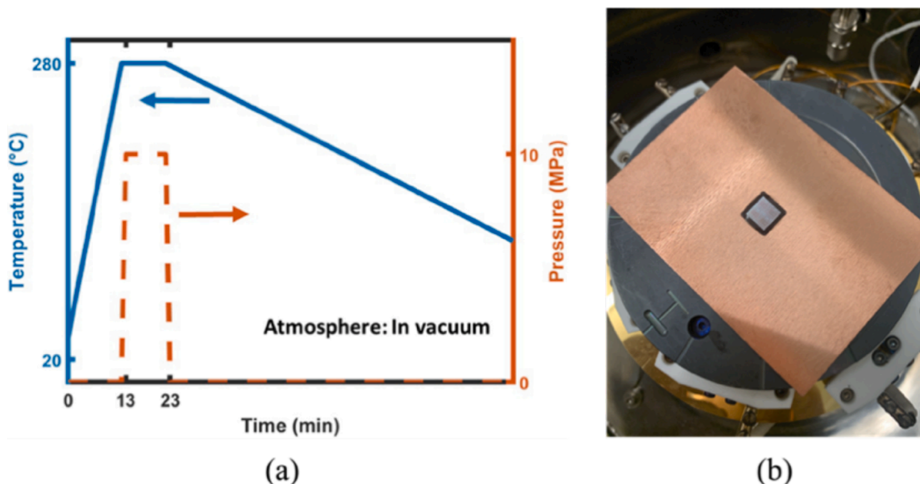

Fig. 6. (a) Sintering profile for TTC die-attach and (b) the sample in the vacuum bonder.

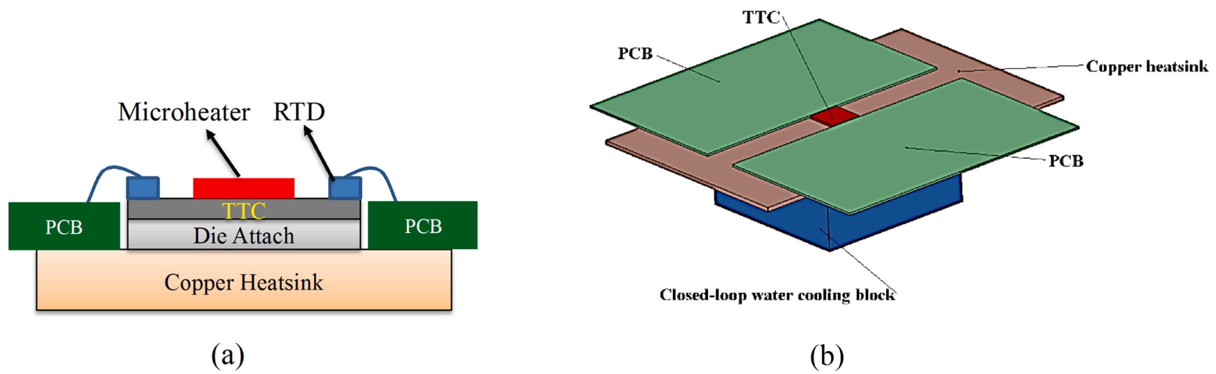

Fig. 7. (a) Cross-section of the prepared sample and (b) 3D test setup modeled in SolidWorks.

lies in the lower initial resistance value, which leads to lower RTD sensitivity. One or both RTD types can be utilized based on the application requirements.

TTC was fabricated on 100 mm p-type silicon wafers with a thickness of 525 μm as shown in Fig. 5. A 300 nm thick SiO_2 film was used for surface insulation. The first metal layer having a thickness of 137 nm was deposited by Ti sputtering. The Ti film was patterned using photolithography and RIE to form microheaters and RTDs. After Ti patterning, a PECVD SiO_2 film with a thickness of 300 nm was deposited. The PECVD process reduced the active Ti film thickness by approximately 37 nm, yielding a Ti film with a sheet resistance of 6.17 Ω/sq. The PECVD SiO_2 film was patterned with vias, followed by the sputter deposition of 2 μm Al with 1% Si. Photolithography and RIE were applied to form metal interconnects as redistribution layers (RDL) and bump reliability measurement units. Next, a passivation layer of PECVD SiO_2 was deposited, followed by opening the contacts and top-level Al bonding pad metallization. The backside of the wafer was then coated with a stack of Ti and Au metals using electron beam evaporation with thicknesses of 50 nm and 500 nm, respectively. Finally, the wafer was diced into chips with different numbers of 4 × 4 mm^2 elements.

Considering the electromigration limits, the critical current density of Ti is 10×10^6 A/cm^2. The TTC pads were designed to be large enough to support the heating current needed for uniform power density of 100 W/cm^2 and above. Considering the proposed design, 16 W can be achieved per cell at 12 V. Therefore, a 20 × 20 mm^2 die, including 25 cells, can yield 400 W. The current density required to obtain this power is 0.4×10^6 A/cm^2, which is considerably lower than the critical value. Appropriate cooling conditions allow the unit cell power to reach 360 W in high-power applications.

2.2. Sintering experiments

This study applied four metal nanoparticle pastes (Ag paste A, Cu paste A, B, and C) from different vendors. First, the metallic sinter paste was dispensed by stencil printing on the top surface of pure Cu plates, which were pretreated with isopropanol (IPA). The thickness of the printed layer was 100 μm. Subsequently, a drying step was performed in the air at 110 °C for 20 min. Subsequently, TTC was mounted on the dried paste, and pressure-assisted sintering was conducted in a vacuum bonder (AWB-04, Applied Microengineering Ltd, UK). The adopted sintering profile is illustrated in Fig. 6(a), and the sample in the vacuum bonder is shown in Fig. 6(b). The sample was then heated to 280 °C with a 20 °C /min ramp. Subsequently, a uniaxial force of 10 MPa was applied for 10 min. Finally, the pressure was released, and the sample was cooled down in the bonder to 80 °C to prevent oxidation.

2.3. Test setup

A cross-sectional image of the sample is shown in Fig. 7(a). The Si TTC is located on the top, followed by the sintered die-attach layer, and finally the Cu plate as the heatsink. A schematic representation of the DUT is shown in Fig. 7(b). The available die-attach printing stencil allows an 8 × 8 mm^2 TTC size; hence, the sample includes an array of 2 × 2 cells or four unit cells, which contain 24 microheaters and 12 RTDs. In our case study, we opted for the LRTD as a temperature sensor because of its higher sensitivity, and the LRTDs recorded the thermal responses during the TDIM cooling curves. In our experiment, each sample contained an array of 2 × 2 cells (8 × 8 mm^2), as shown in Fig. 2(b).

To alleviate the difficulty in accessing the inner bond pads, two microheaters and RTDs in the same row were wire-bonded in series and tested simultaneously. The sintered sample was wire-bonded to a PCB

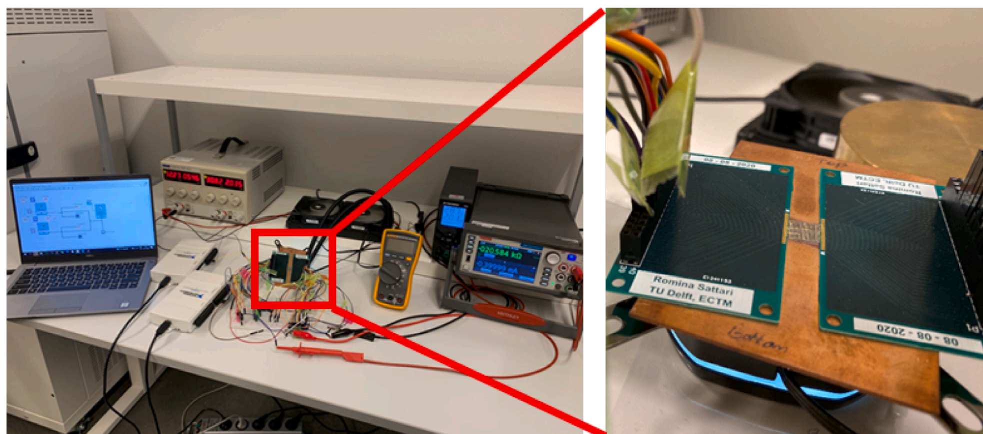

Fig. 8. TDIM measurement setup and the wire-bonded sample.

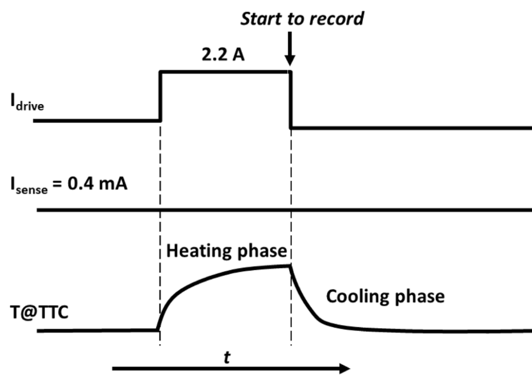

Fig. 9. Thermal transient test sequence.

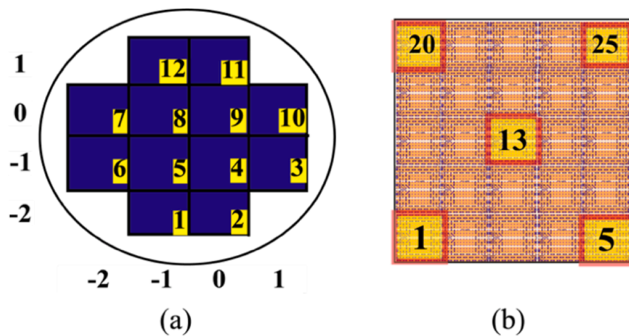

Fig. 10. (a) Numbered measurement sections and (b) measured RTD cells on a 20 × 20 mm^2 die.

for electrical connection using 25 μm thick Au wires, and the entire assembly was connected to a closed-loop water-cooling element. According to the TDIM method, the heatsink-cooling plate is in contact with the Cu case, with or without thermal grease. For thermal grease, MX-4 from Arctic GmbH with a thermal conductivity of 8.5 W/m•K was used in this study.

The entire measurement setup is shown in Fig. 8. The test sequence is illustrated in Fig. 9. The RTD sensing current used to determine the chip temperature was set as 0.4 mA to exclude self-heating errors. Meanwhile, the heaters were driven by a current of 2.2 A from a BK Precision 1550 DC power supply (36 V, 3 A). The driving current was chosen to maximize the output power within the limitations of the power supply. To record sufficient data points and guarantee synchronization, two data acquisition systems (sampling rate: 250 kS/s) from National Instruments were used to read out the voltage of the heater and the temperature sensor, respectively.

3. Results and discussion

3.1. Thermal test chip calibration

To use the TDIM method for thermal resistance characterization, the TTC must first be calibrated. This section reports the characterization of TTC by evaluating the power uniformity and RTD sensitivity. Fourteen wafers were used to assess the reproducibility of the design and process. The I–V measurement results include the characterization of the microheaters and RTDs. Measurements were performed using a semi-automatic wafer-probe station. Twelve 20 × 20 mm^2 dies on each wafer were analyzed, and are shown in Fig. 10(a). The captured data were averaged and the mean values were exported using a data visualization tool (DVT) in MATLAB.

The resistance distribution of the microheaters at room temperature (RT) of approximately 25 °C is shown in Fig. 11. The uniformity of the process is indicated by the standard deviation of 0.8 Ω in this fabrication run. The dashed lines show the minimum and maximum resistances,

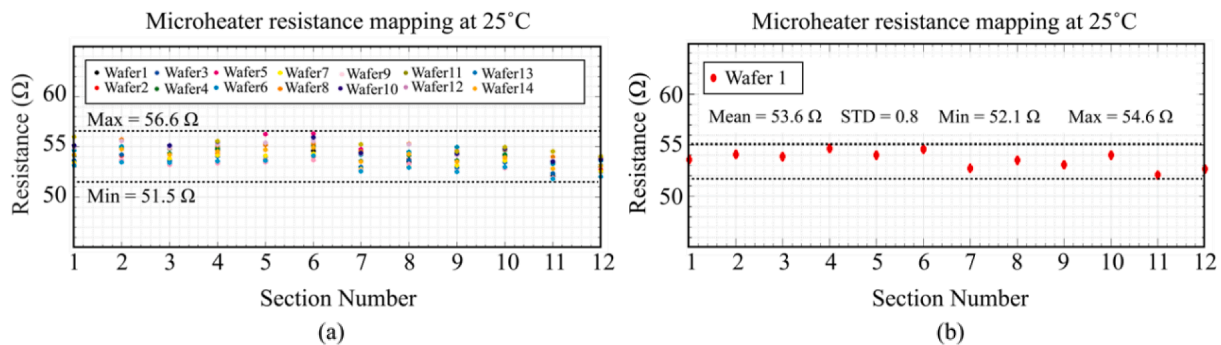

Fig. 11. (a) Heater resistance distribution over 14 wafers at 25 °C and (b) resistance distribution in a single wafer.

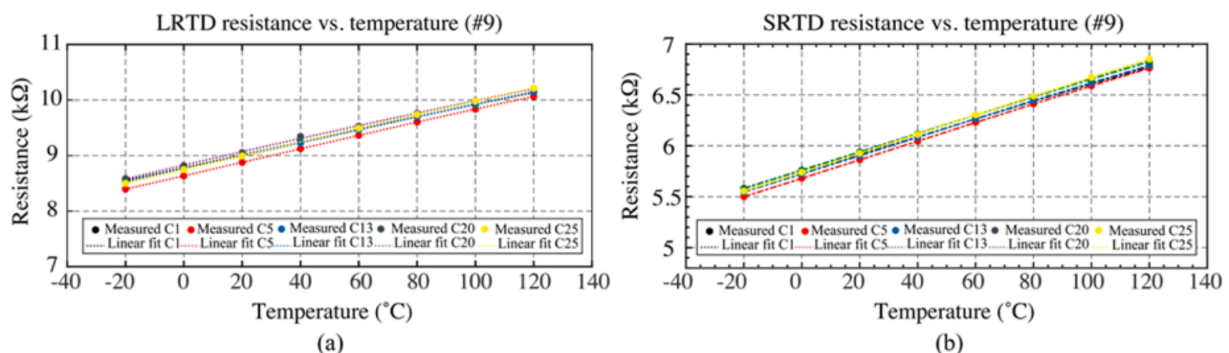

Fig. 12. (a) LRTD resistance at different temperatures and (b) SRTD resistance at different temperatures.

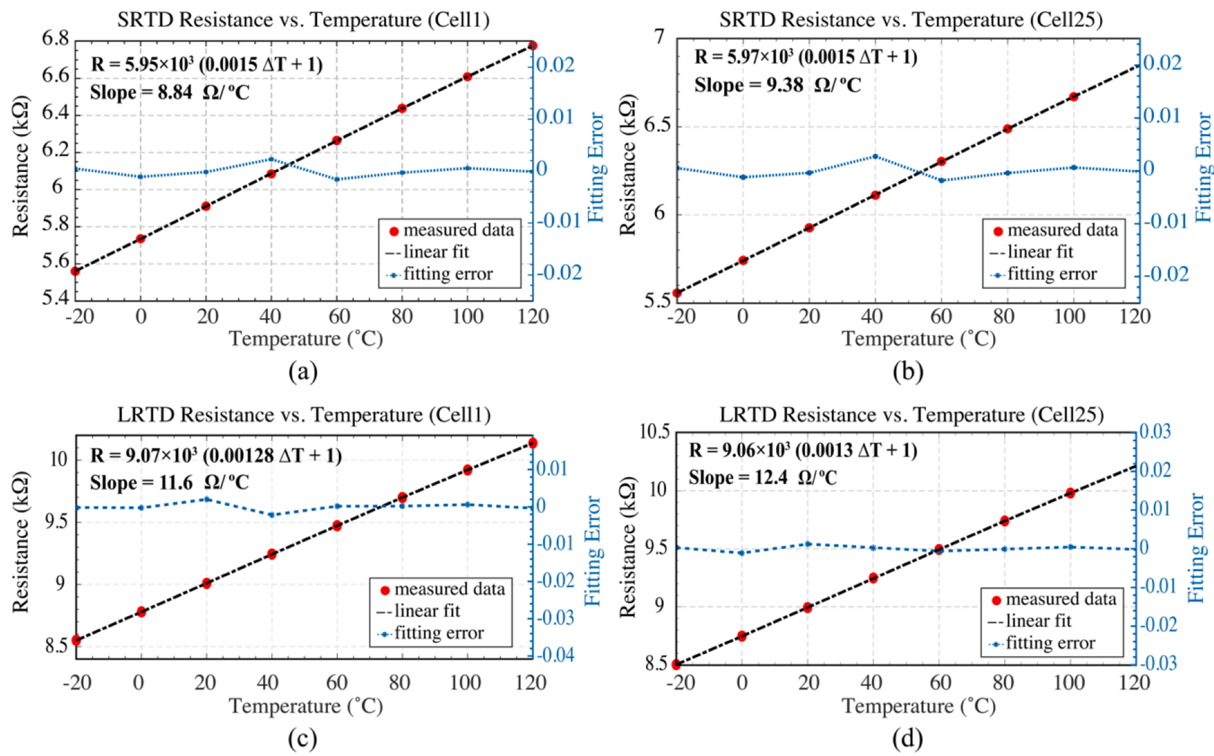

Fig. 13. Thermal characterization of (a) SRTD in cell 1 (b) SRTD in cell 25 (c) LRTD in cell 1 (d) LRTD in cell 25.

Table 1
TTC Performance Comparison.

TTC	This work (TUD22) [42]	NT16-3 K [27]	NT20-3 K [28]	Siegal & Galloway [29]
Sensor Type	RTD	RTD	RTD	Diode
Heater Type	Resistor	Resistor	Resistor	Resistor
Cell Size (mm^2)	4 × 4	3.2 × 3.2	2.5 × 2.5	2.5 × 2.5
Sensitivity (Ω/K)	12	8	8	2
Cell Power at 12 V (W)	16	9	17	26 [a.]
Max Power per Cell (W)	360[b.]	250[b.]	70	22
Resistance per Heater (Ω)	54	160	17	11
Heaters per Cell	6	10	2	2
Sensors per Cell	3	1	1	4
Active Heater Area	82.5%	62%	82%	85%

[a.] Exceeds the maximum current handling of the heater. [b.] Can be achieved only by applying proper cooling.

which were 52 Ω and 54 Ω, respectively, in a single wafer measurement. A ± 1 Ω resistance variation over the wafer leads to less than 2% nonuniformity in power density.

The RTD was calibrated by measuring five cells per die, as shown in Fig. 10(b), in the temperature range of −20 °C to 120 °C. The wafer was vacuum-clamped to the chuck in the probe station chamber, and the chuck was adjusted to the desired temperature. An extra settling time was considered at each step to ensure that the chuck temperature stabilized.

The calibration results are shown in Fig. 12. As expected, the SRTD calibration indicates 1.3% non-uniformity and 9 Ω/K sensitivity, whereas the LRTD shows an increased non-uniformity of 2.2% and an improved sensitivity of 12 Ω/K. The reason lies in the larger variation in the LRTD initial resistance (ranging from 8.93 kΩ to 9.13 kΩ) compared to that of SRTD (ranging from 5.90 kΩ to 5.98 kΩ). Two single-cell calibration graphs are plotted separately in Fig. 13, where the fitting lines and corresponding linear equations are provided using MATLAB. The results verify the improvement in RTD sensitivity compared to the state-of-the-art TTC. Table 1 summarizes the TTC specifications and compares their performance with those of other studies.

3.2. Thermal test chip characterization and IR thermography

The homogeneity of the heat profile generated by the TTC directly affects the accuracy of the thermal reliability experiments. To analyze this parameter, the heat flux distribution and temperature gradient of a TTC of 20 × 20 mm^2, including 25 cells, were measured using IR thermography as a noncontact thermal measurement method. A Vario CAM 800 thermal camera (InfraTec GmbH, DE, USA) equipped with a close-up lens was employed while the chip surface was exposed to air. Five microheaters per row were connected in series by wire-bonding to heat all the microheaters simultaneously. Serial connections created 30 rows in parallel. Owing to the voltage limitation of the power supply, the maximum driven current was 1.8 A.

The temperature distributions at the different current levels are shown in Fig. 14. The steady-state measurements by IR thermography in Fig. 15 show the uniformity of the temperature distribution, which is evaluated with the largest temperature difference over the 20 × 20 mm^2 die. Owing to the sizable active area, the TTC showed a temperature variation of less than 1 °C at 68 W power excitation, while all microheaters were driven by the same current. The sharp successive spikes in the temperature profile chart are related to the top metal bonding pad locations, where more thermal conductivity is expected through the metal. At higher driving currents, the temperature gradient in the central parts of the chip increased and exhibited a stronger heat profile concentration. This could be partly related to the chip being directly exposed to air and the corners experiencing higher convective heat

Fig. 14. TTC steady-state IR thermography measurement results and temperature profile charts.

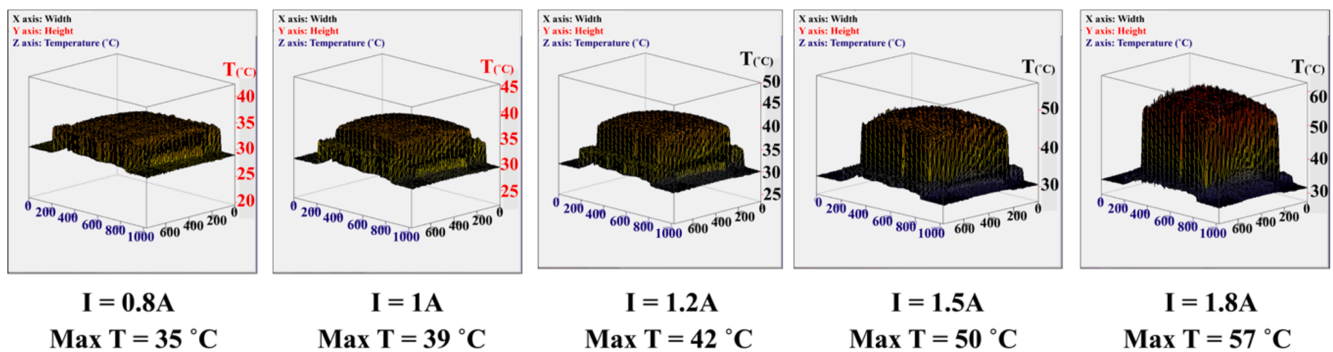

Fig. 15. 3D temperature distribution of TTC at different current levels.

removal. Furthermore, the heat loss from the chip to the substrate was higher at the edges.

3.3. Evaluation of junction-to-case thermal resistance $\theta_{th\text{-}JC}$

Prior to the measurement, the setup with an 8 × 8 mm^2 chip on the Cu substrate was set to equilibrium with a driving current of 2.2 A. The corresponding chip temperature and power consumption at equilibrium are shown in Fig. 16. All samples consumed approximately 68 W of power. The minor difference in the power consumption, that is, less than 0.2 W, can be attributed to the variations in the temperature-dependent heater resistance. As for the chip temperature, the Ag paste sample had

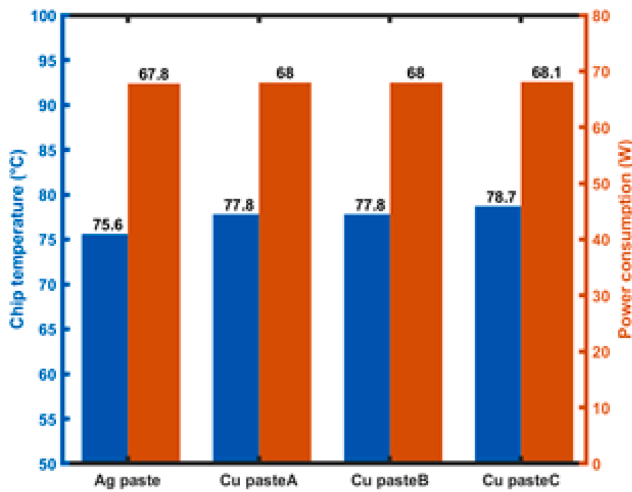

Fig. 16. Chip temperature and power consumption at equilibrium.

the lowest value at 75.6 °C, while that of the samples of Cu pastes A and B were 77.8 °C, and Cu paste C performed slightly worse, at 78.7 °C.

Subsequently, the driving current was switched off and the signal on the temperature sensor was recorded simultaneously for 120 s. A digital low-pass filter was first applied to denoise the oversampled signals during the signal process. The sparse signals were then smoothed using a Gaussian-weighted moving average filter. Fig. 17 show the curves of the temperature change and thermal impedance of the sample. Fig. 17(a) shows the smoothed results of the temperature change of the Cu paste A sample with and without TIM. In addition, owing to the inevitable electrical disturbance, an offset time of 1000 μs was subtracted according to the standard [20]. After the offset correction, the temperature change for the sample with and without TIM was 48.38 °C and 28.12 °C, respectively.

It can be seen in Fig. 17(a) that the sample reaches steady-state at 100 s and the difference in thermal impedance Δθ is 0.2848 K/W. It can be noticed that the two curves present a separation point when the heat flux reaches the top surface of the cooling block. Therefore, the thermal impedance of the separation points indicates $\theta_{th\text{-}JC,}$ as marked in Fig. 17 (b).

To precisely determine the point of separation, the variable transformation t to z = ln(t) was applied, where a(z) was derived to obtain the θ_{JC} value as a function of z, as shown in Eq. (2):

$$a(z) = Z_{\theta JC}(t = \exp(z)\,)\,for z = \ln(t) \tag{2}$$

Therefore, piecewise linear interpolation can be performed at the measurement points $\{(z_i, Z_{\theta JC})\}$ to compute the derivatives of da/dz. The number of interpolations chosen was 200, which meets the requirements of the standard [20]. Subsequently, to minimize the impact of the steady-state difference, the derivative of a was normalized by Δθ, as shown in Eq. (3):

$$\delta Z_{\theta JC}(\mathrm{t}) = \frac{\Delta(da/dz)(t)}{\Delta\theta}. \tag{3}$$

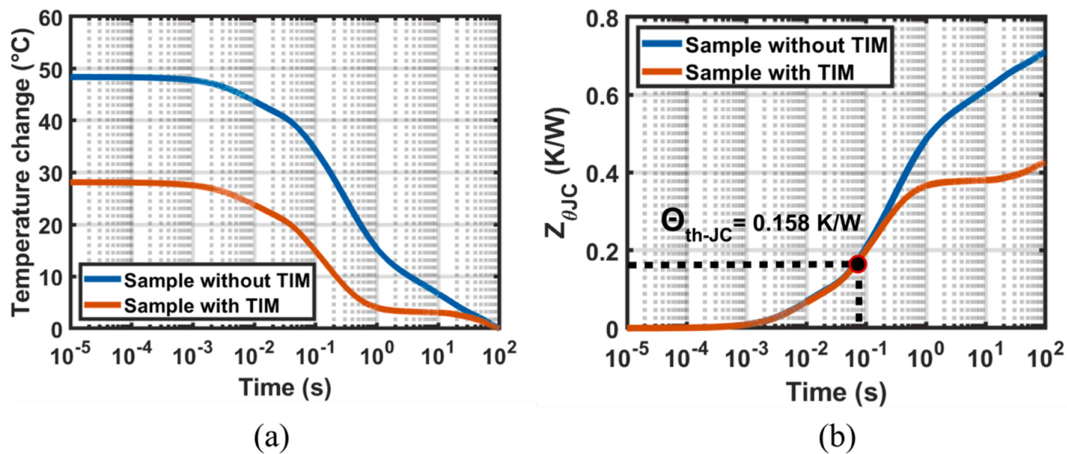

Fig. 17. (a) Junction temperature change and (b) Zth curve during the thermal transient for the sample with and without TIM.

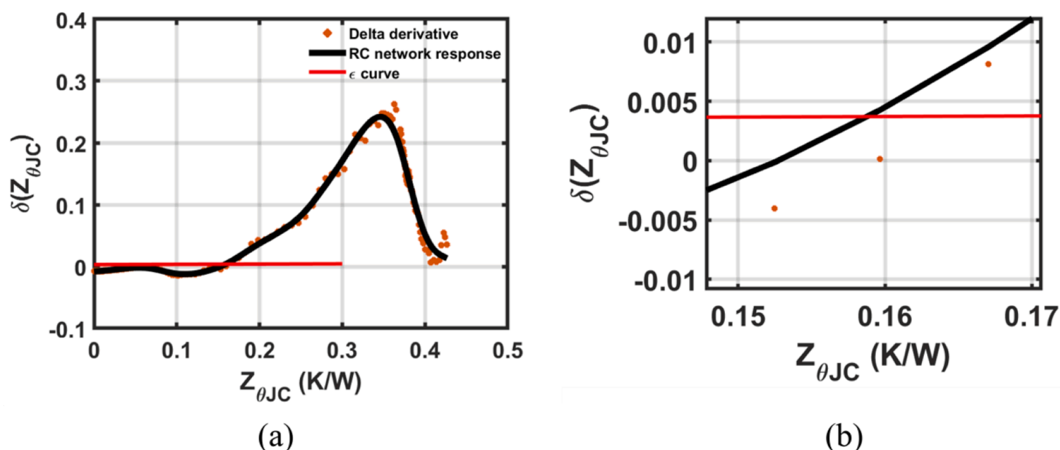

Fig. 18. (a) θ_{JC} is the abscissa of the intersection of the RC response network and ε curve. (b) Zoomed-in curve.

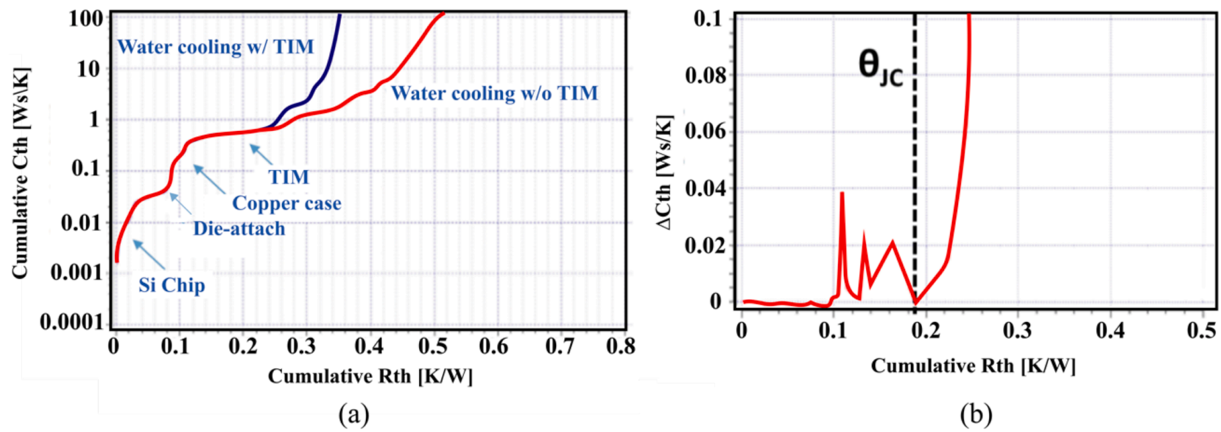

Fig. 19. Cumulative structure function for Cu paste A sample.

To prevent the result from being influenced by random fluctuations of the $\delta(Z_{\theta JC})$ curve, the difference between the two $Z_{\theta JC}$ curves was fitted with the RC network response. Then, a trend line $\varepsilon = 0.0045$ W/K $\times \theta_{JC} + 0.003$ was applied, and the abscissa of the intersection point of the δ and ε curves, as shown in Fig. 18, is the θ_{JC} of the sample. Thus, the junction-to-case thermal resistance θ_{JC} of Cu paste A sample is found to be 0.158 K/W.

The evaluation of θ_{JC} was also performed by utilizing the separation of the cumulative structure functions $C_{\theta\Sigma}$ ($R_{\theta\Sigma}$) calculated from the sample with or without TIM. The cumulative structure function (SF) of a heat flow path is defined as the cumulative thermal capacitance $C_{\theta\Sigma}$ as a function of the cumulative thermal resistance $R_{\theta\Sigma}$ along the heat flow path. In the case of a 1-D heat-flow path, the cumulative SF can separate the thermal properties of the individual layers in the package. Similar to the Z_{th} curves, the cumulative SFs of the two Z_{th} curves were expected to separate because the heat flux flowed into an interface with different thermal conductivities. Thus, the separation point of the cumulative structural functions indicates the value of θ_{JC}.

In this study, $Z_{\theta JC}$ curves were transformed into cumulative structure functions using the TDIM-Master software [45]. First, as recommended by the JEDEC51-14 standard [20], the time-constant spectrum is computed by numerical deconvolution with bandwidth Φ and edge steepness σ of 0.45 and 0.05, respectively. The time-constant spectrum was related to the FOSTER RC model for the distributed thermal networks. The lumped-element *FOSTER* model can then be generated from the discredited time-constant spectrum function. However, the FOSTER model cannot be utilized to characterize the thermal structure because it contains only the node-to-node capacitance. Thus, the FOSTER RC network was transformed into the CAUER RC network to obtain an accurate physical description of the heat flow path [46]. The cumulative structure extends the CAUER ladder description to the continuous case. In other words, the discretization of the cumulative SF results in a CAUER RC network.

Fig. 19(a), presents an example of the cumulative SF for Cu paste A sample after numerical transformation. The red and blue lines represent the samples with and without TIM, respectively. The horizontal axis denotes the sum of the thermal resistance along the thermal path. The different portions of the curve are identified as the Si TTC chip, die-attach layer, Cu case, TIM, and closed-loop water cooling element. It can be seen that the SFs initially match well until the cumulative Rth reaches a value where the TIM is included. As shown in Fig. 19(b), the separation point of the SFs can be extracted by plotting the deviation between the two curves. The figures below show the data analysis of Cu paste sample A, yielding a junction-to-case thermal resistance value of 0.191 K/W.

Thus, the θ_{JC} of all the samples was extracted based on the point of separation of $Z_{\theta JC}$ curves, as well as the cumulative structure functions.

Table 2
θ_{JC} of die-attach sintered using different metal nanoparticle pastes.

Die-attach materials	θ_{JC} (K/W) from $Z_{\theta JC}$ curves separation	θ_{JC} (K/W) from SF separation
Ag paste	0.144	0.149
Cu paste A	0.158	0.191
Cu paste B	0.162	0.205
Cu paste C	0.168	0.214

The results are presented in Table 2. The θ_{JC} value obtained from the SF separation is slightly larger than that obtained from $Z_{\theta JC}$ curve separation, which was reported in another study as well [21]. Table 2 shows that the Ag paste sample has the lowest θ_{JC} for both methods, followed by Cu pastes A, B, and C. This trend is consistent with the above-mentioned difference in the chip temperatures.

To elaborate on the θ_{JC} difference between different materials, Fig. 20 displays scanning acoustic microscopy (SAM) images of the sintered samples after measurement. The scanning process resulted in horizontal shadows. It can be seen that a homogeneous sintered layer was observed in the sintered Ag paste and Cu paste A samples. However, sintered Cu paste B showed several black spots, which can be attributed to the drying channels of the organic compound. The sintered Cu paste C sample exhibited dense spots, indicating that worse drying channels occurred during the sintering process. In addition, the evident cracks in Fig. 20(c) and (d) may have been caused by external forces during transportation and operation. Therefore, it was found that the adhesion in the different sintered samples corresponded to their thermal performance. The seamless adhesion of Ag resulted in it outperforming the others. Similarly, Cu paste A outperformed the other two Cu paste samples owing to its better adhesion.

4. Conclusion

This study presents the design and fabrication of a configurable TTC as a flexible and cost-effective solution for fast thermal evaluation of nano-metallic die-attach materials. The fabricated TTC was used to evaluate the thermal performance of Ag and Cu nano-metallic die-attach joints in TDIM measurements. The TTC layout was designed with a large active area of 82.5% while accommodating three RTDs per cell. The TTC reached a high temperature sensitivity of 12 Ω/K and maximum power of 360 W per cell, which are 50% and 44% higher than the state-of-the-art, respectively [27,28]. Improved uniformity of temperature distribution was demonstrated using FEM simulations and infrared thermography at multiple power levels. Temperature mapping showed an absolute variation of less than 1 °C at 68 W excitation. Furthermore, the cost-effective manufacturing process of the proposed TTC can be applied

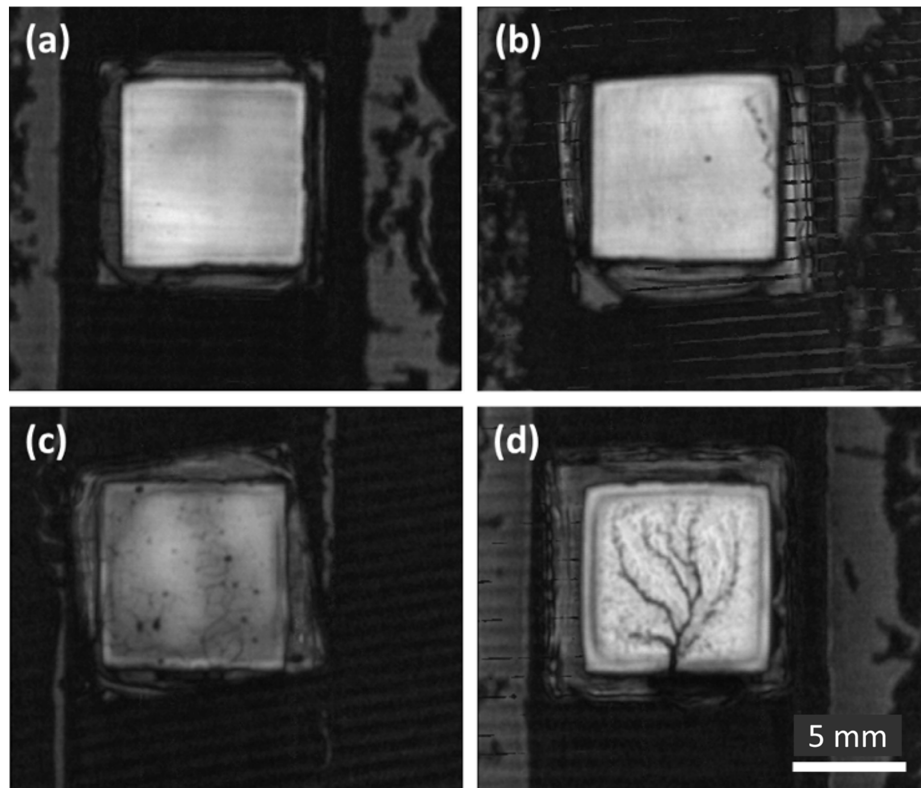

Fig. 20. SAM images of sintered (a) Ag paste, (b) Cu paste A, (c) Cu paste B, and (d) Cu paste C.

to any substrate such as SiC or GaN.

The results verified the successful application of the in-house developed TTC as a valid concept for flexible and accelerated evaluation of thermal characteristics in power electronic packaging. The junction-to-case thermal resistance of four different nano-metallic sintered packages were extracted from the separation point of $Z_{\theta JC}$ curves, as well as the SFs. The device sintered using the Ag paste outperformed the devices sintered using Cu pastes A, B, and C. The Ag sinter paste exhibited the lowest θ_{JC} values of 0.144 K/W, and Cu sinter paste A exhibited θ_{JC} value of 0.158 K/W, as determined by $Z_{\theta JC}$ curves. The Scanning acoustic microscopy was carried out to confirm the consistency of the analysis.

This approach enables a flexible design of experiments to screen the optimal thermal resistance of die-attach materials and subject them to further reliability tests. According to the same sintering conditions, the TTC can be employed not only to compare the zero hour thermal properties, but also to evaluate the reliability of nano-metallic sinter materials in extensive reliability programs in relation to the final application. Thus, the proposed TTC can provide an opportunity for promising material selection by TDIM and online health monitoring for power electronic packaging. This potentially accelerates the introduction of novel and cost-effective materials, such as Cu.

Declaration of Competing Interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Romina Sattari reports financial support was provided by Delft University of Technology. Romina Sattari reports a relationship with Delft University of Technology that includes: employment and funding grants.

Data availability

The data that has been used is confidential.

Acknowledgment

This work was supported by the ECSEL Joint Undertaking (JU) under grant agreement No 826417, National Key R&D Program of China (2018YFE0204600), and HiPer project, which concentrates on the development of high-performance vehicle computer and communication system for autonomous driving. The research is funded within the framework of Penta (project number: 17006), the JU, and the Dutch authority. The JU receives support from the European Union's Horizon 2020 research and innovation program and Germany, Austria, Spain, Finland, Hungary, Slovakia, Netherlands, and Switzerland. The authors would like to thank Zu-Yao Chang for his significant contribution to wire-bonding the TTC, Boschman B.V. for the SAM service, and Arvind Babu from the faculty of Mechanical, Maritime and Material (3 mE) of Delft University of Technology for the support in IR thermography setup.

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