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A Millimeter-Wave Front-End for FD/FDD Transceivers Featuring an Embedded PA and an N-Path Filter Based Circulator Receiver

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***Abstract*— This work presents an ultra-compact single-antenna FD/FDD transceivers front-end. It comprises a nonreciprocal circulator, RX, and an integrated power amplifier (PA). In the proposed circulator, we devise a ring quarter-wave transmission line topology with adjusted characteristic impedances to improve TX-to-antenna insertion loss and TX-to-RX isolation. Besides, an AND-gate switching-based N-path filter is proposed to realize the circulator's nonreciprocal gyrator while acting as a mixer-first RX. Owing to the ultra-compact N-path filter structure, the circulator occupies only 0.38mm^2 core area. Over a 27.1-to-31.1GHz band, the realized front-end offers >20dB TX-to-RX isolation while its measured TX-to-antenna insertion loss is 1.7∼2.2dB. The RX path tolerates the PA's blocker signal, achieving 5dBm in-band and 13dBm out-of-band B_{1dB}. Moreover, the PA delivers 15.15dBm peak output power with 33% drain efficiency. Our front-end prototype occupies only 0.7mm^2, including circulator, PA, quadrature hybrid coupler LO generators, and baseband circuits.**

***Keywords*— Blocker-tolerant receiver, CMOS circulator, FDD, full-duplex, mm-wave, N-path filter, power amplifiers.**

I. Introduction

The millimeter-wave (mm-wave) point-to-point backhaul 5G communication systems utilize TDD beamforming to cover a large range. In this regard, the maximum transmitter (TX) power and minimum receiver (RX) noise figure are critical to fulfill the strict requirement of the communication link budget. On the other hand, high spectral efficiency, low network latency, and robust connection links are necessary for high-capacity mm-wave wireless access applications (e.g., indoor access, repeaters, and wireless relay switches). Nevertheless, the half-duplex TDD operation of these systems compromises the network latency and capacity to avoid leaking a local transmit signal into its own RX when using a single antenna. Therefore, a simultaneous transmit and receive (STAR) beamforming, e.g., in-band (IB) full-duplex (FD) and FDD, can improve the network latency and capacity. Nonetheless, the FD demands strict IB blocker rejection conditions at its transceiver (TRX) front-end [1]. Conversely, FDD entails stringent out-of-band (OOB) blocker rejection [2], [3], [4], [5] and TX-to-RX isolation at its antenna interface front-end [6]. In [7], a mm-wave FD/FDD TRX is presented, conceiving separate antennas to provide TX-to-RX isolation.

A feasible integrated single-antenna FD/FDD TRX front-end is to employ a nonreciprocal circulator [8] to address the above challenges. As depicted in Fig. 1(a), it comprises a circle of three quarter-wave transmission lines (QTLs) and an active gyrator, e.g., two back-to-back N-path filters, supporting

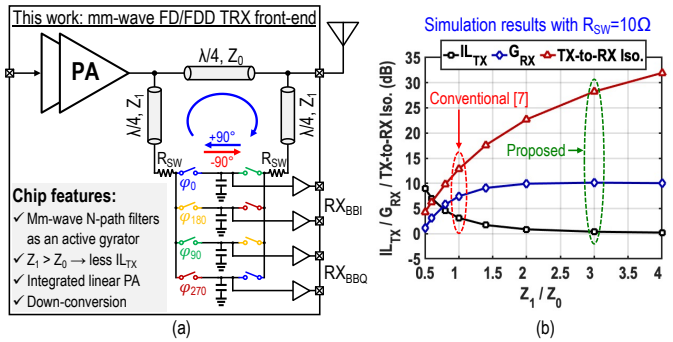

Fig. 1. (a) The proposed mm-wave FD/FDD TRX front-end architecture and (b) simulation results of TX insertion loss, RX gain, and TX-to-RX isolation versus characteristic impedance of gyrator's QTLs.

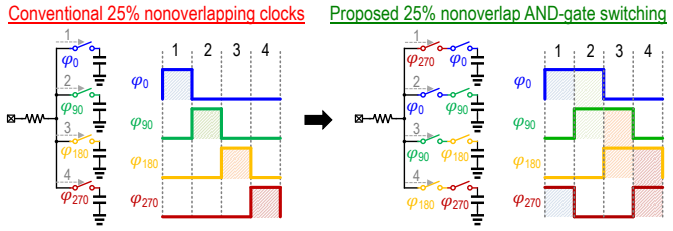

Fig. 2. The AND-gate switching N-path filter's principles.

only clockwise wave propagation. However, providing the nonoverlapping LO clocks required for such an N-path filter at mm-wave is challenging. Although the nonoverlapping 25% clocks are implemented at mm-wave [5], they only can support small-sized switches in advanced CMOS technologies with optimized parasitic capacitors.

In [9], a nonreciprocal delay technique is proposed to realize a mm-wave CMOS circulator at the cost of occupying a relatively large chip area and high TX-to-antenna insertion loss (IL_{TX}). Therefore, considering the strict size constraint of 5G phased-array systems, implementing a compact mm-wave single-antenna FD/FDD TRX front-end with high IB/OOB blocker tolerance and reasonable IL_{TX} (e.g., 1-2dB) is still an open challenge to solve.

This work presents an ultra-compact FD/FDD TRX front-end based on a nonreciprocal circulator featuring: 1) a mm-wave N-path filter as a nonreciprocal gyrator that simultaneously functions as a blocker tolerant RX, 2) a compact differential ring QTL topology with adjusted characteristic impedances to improve the IL_{TX}, RX gain (G_{RX}), and TX-to-RX isolation, and 3) an integrated push-pull power amplifier (PA) directly connected to the proposed front-end.

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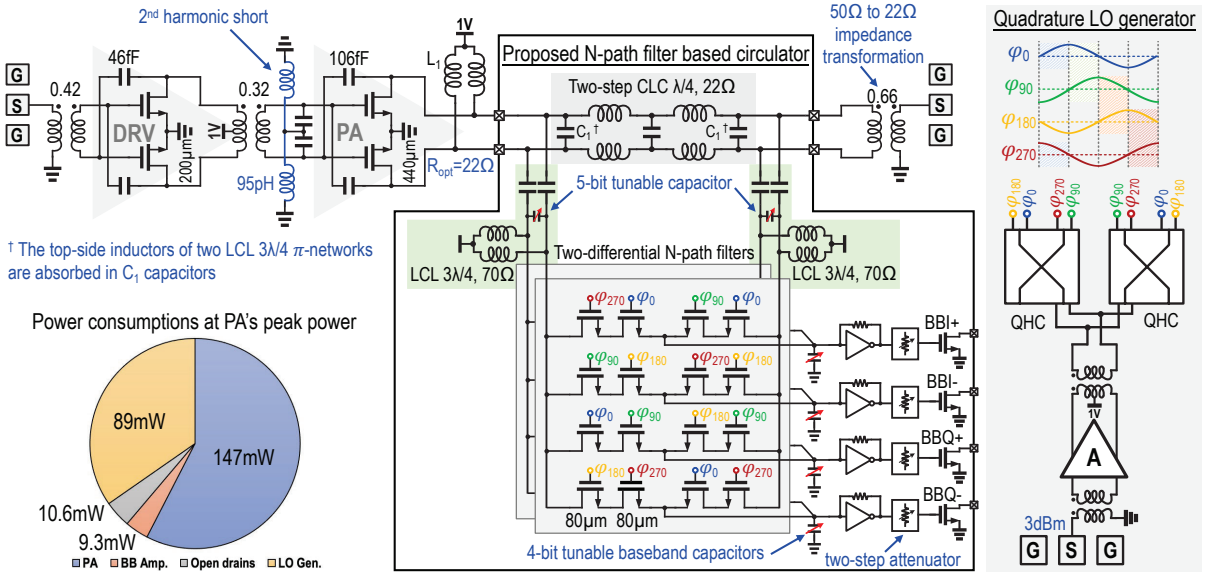

Fig. 3. The top-level view of the mm-wave FD/FDD TRX front-end and its power consumption at PA's peak power.

II. Mm-wave CMOS FD/FDD TRXs Front-End

As depicted in Fig. 1(a), in the proposed circulator, the QTL impedance of the direct path is Z_0, equal to the impedance of the circulator. The characteristic impedance of two other QTLs (Z_1) is chosen higher than Z_0 to minimize the TX-induced power waves entering these lines yielding less IL_{TX}. Since the N-path filter down-converts the RX signal, the actual RX port of the circulator is left open [8]. Therefore, using a relatively higher impedance value for Z_1 compared to Z_0, the desired RX signal arrives with a higher voltage amplitude at the baseband, benefiting the conversion gain. The simulation results with ideal components demonstrated in Fig. 1(b) confirm the substantial improvement of IL_{TX}, G_{RX}, and TX-to-RX isolation. Moreover, in this structure, the RX signal passes through the nonreciprocal N-path filter and is eventually absorbed in the TX ports termination [8]. Therefore, the input impedance of the antenna port is determined by TX termination.

As exhibited in Fig. 2, in a conventional N-path filter, e.g., four-path filter, nonoverlapping 25% LO clocks are required to diminish the charge sharing of switches, providing high-Q filtering. To achieve the nonoverlapping operation at the mm-wave frequencies, we proposed an N-path filter structure with pass-transistor-based AND-gate switches driven by quadrature 50% LO clocks. In this context, each path's capacitor is connected to the shared RF node when both switches are ON, replicating bitwise AND-gate operation and resembling 25% nonoverlap switching. It is worth mentioning that a similar approach was presented in [2] for SAW-less GPS applications.

III. Circuit Implementation

Fig. 3 demonstrates a detailed schematic of the mm-wave FD/FDD TRX front-end based on the proposed circulator featuring two back-to-back AND-gate switching N-path filters

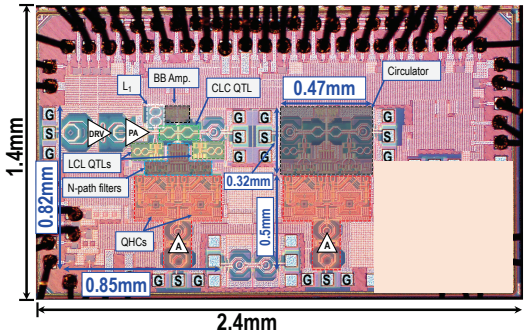

Fig. 4. Die micrograph of the proposed FD/FDD TRX front-end.

and an integrated PA. The circulator is also realized separately by replacing the PA with a balun. A two-step lumped-element CLC π-network is employed to realize the circulator's PA-to-antenna QTL. Its equivalent impedance Z_0 is set to 22Ω to match the PA's required optimum load (R_{opt}). Two 70Ω LCL π-networks are utilized to form the circulator's remaining QTLs. They connect the TX and antenna ports to the gyrator and perform DC blocking. Here, the LCL's top side inductors are absorbed in C_1. Accordingly, the proposed gyrator is implemented by two-differential N-path filters (Fig.2), whose switches are realized by NMOS transistors with relatively large channel width (80μm) to minimize their impedance (R_{SW}). The parasitic capacitors of the switches are resonated out by two differential inductors, which are combined with LCL's bottom side inductors. Additionally, two 5-bit tunable capacitors are employed to adjust the resonance frequency.

The down-converted baseband signals are amplified by self-bias inverter-based transconductance amplifiers and their subsequent open-drain NMOS transistors. A two-step attenuator is implemented in each baseband path, providing possible attenuations of 8-dB and 16-dB. Besides, 4-bit tunable capacitors are utilized in the baseband to control the RX bandwidth slightly. Furthermore, a designated input amplifier

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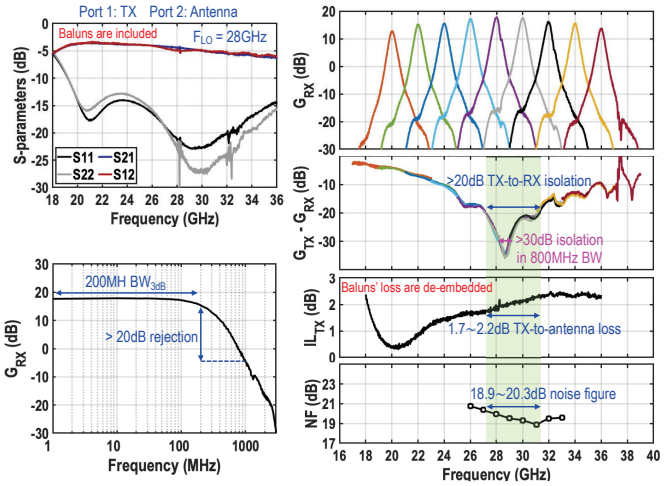

Fig. 5. Small-signal s-parameter, RX gain, TX-to-RX isolation, noise figure, and TX-to-antenna insertion loss over the 20-to-36GHz band.

provides the required LO power level of two quadrature hybrid couplers (QHCs) to generate mm-wave sinusoidal quadrature LO clocks. As depicted in Fig. 3, the proposed circulator, located between the PA and the output balun, is realized differentially to improve its power handling capability by 6-dB. A neutralized common-source push-pull PA is designed with input second harmonic short condition to boost its linearity. Besides, an 8-shape symmetrical inductor (L_1) resonates out the parasitic capacitors of the PA and provides its DC feed. Finally, a neutralized common-source pre-driver is implemented to drive its following PA.

IV. Measurement Results

The chip is fabricated in 40nm bulk CMOS technology (Fig. 4). The core area occupied by the proposed circulator and FD/FDD TRX front-end, including their LO generators and baluns, are 0.38mm^2 and 0.7mm^2, respectively.

A. Circulator Performance

The s-parameter measurement results of the circulator are presented in Fig. 5, including its baluns' loss. The RX achieves 400MHz 3dB bandwidth (BW_{3dB}) with 18dB gain and 20dB rejection at 1GHz spacing away from the carrier frequency. Moreover, the circulator is widely tunable over a 22-to-36GHz band, achieving more than 30dB TX-to-RX isolation in an 800MHz bandwidth. It also offers >20dB isolation within the 27.1-to-31.1GHz band. The measured IL_{TX} is 1.7∼2.2dB, and the noise figure (NF) is 18.9∼20.3dB in the same band. Note that the measured NF includes the insertion-loss/NF of the circulator and the mixer-first down conversion path. Nonetheless, its NF is limited mainly by the impedance transformation ratio of the balun (50Ω → 22Ω) and the passive down-conversion mixer's topology. Therefore, there is a trade-off between PA power handling and RX's NF. Nevertheless, employing more advanced technology nodes that offer lower switching impedance with much lower parasitic capacitors can relatively improve RX performance, thus increasing TRX's link budget.

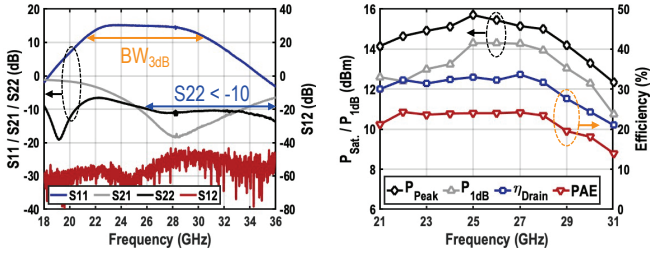

Fig. 6. Small-signal s-parameter and large-signal CW measurement results of the TX path.

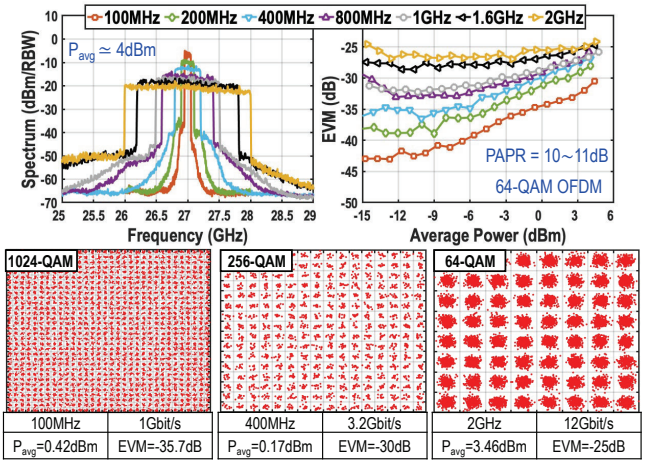

Fig. 7. The OFDM signal measurement results of the TX path.

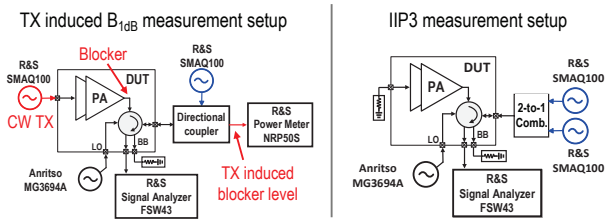

Fig. 8. The measurement setups of the TX induced B_{1dB} and IIP_3.

B. TX Path

Fig. 6 demonstrates the small-signal and large-signal performance of the TX path. According to the s-parameter measurement results, the integrated PA offers almost 10GHz BW_{3dB} with 15.4dB small-signal gain. Owing to the relatively low measured IL_{TX}, the PA achieves 15.15dBm peak power at the antenna port with 33%/24.2% drain-efficiency/PAE. Its P_{1dB} also exceeds 14dBm. The spectrum and EVM of the modulated 64-QAM OFDM signals with various modulation bandwidth are depicted in Fig. 7. Additionally, the measured constellations of 1024-QAM, 256-QAM, and 64-QAM OFDM signals are shown, achieving up to 12Gbit/s data rate that is limited by measurement instruments.

C. RX Path

As depicted in Fig. 8 (left), the RX gain compression under a large blocker is measured when the CW blocker signal is applied to the PA, and its power is measured and reported at the antenna port. The measured TX induced B_{1dB} at various carrier frequencies are demonstrated in Fig. 9, where the front-end

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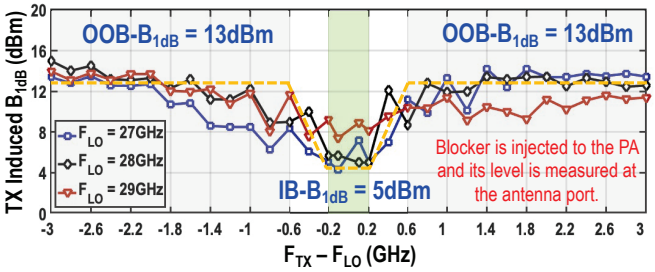

Fig. 9. The measured TX induced B_{1dB} at various carrier frequencies.

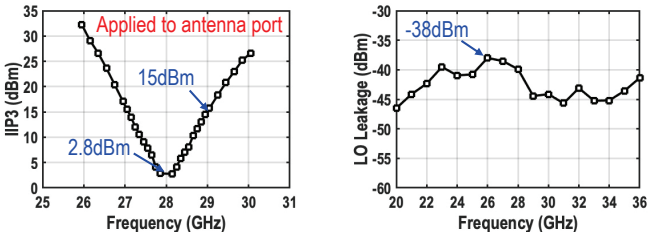

Fig. 10. The measured IIP_3 and LO leakage.

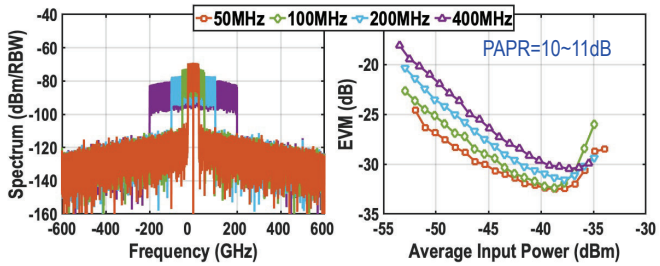

Fig. 11. The OFDM signal measurement results of the RX path.

achieves better than 5dBm IB TX induced B_{1dB} while its OOB TX induced B_{1dB} is 13dBm, confirming its capability to support FD and FDD TRX operations. Additionally, the input third-order intercept points (IIP3) are measured using the measurement setups shown in Fig. 8 (right). As shown in Fig. 10, the measured IB IIP3 is 2.8dBm while the related OOB IIP3 at 600MHz offset is 15dBm. Besides, its LO leakage power is always lower than -38dBm. Moreover, Fig. 11 exhibits the spectrum and EVM of a 64-QAM OFDM signal with various modulation bandwidths up to 400MHz. Lastly, the RX EVM degradation under the OOB CW TX blocker is measured. In this case, the level of CW TX blocker causing 1dB degradation in EVM of a 400MHz OFDM is measured as shown in Fig. 12. As a result, the proposed front-end can support FDD. However, for FD applications, an additional self-interference cancellation is required.

V. Conclusion

This work aims to address the large area and high IL_{TX} of mm-wave CMOS circulators by proposing an ultra-compact adjusted characteristic impedance ring QTLs and AND-gate switching N-path filter. Thanks to the mixer-first RX path, the front-end brings high OOB blocker tolerance, making it suitable for an mm-wave single-antenna FDD link. Therefore, considering the ultra-compact die area and performance, the proposed front-end is suitable for a STAR short-range

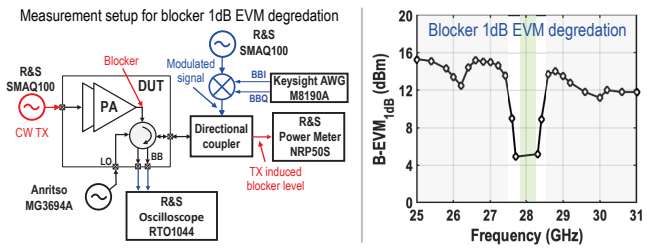

Fig. 12. The RX EVM degradation under the OOB CW TX blocker measurement setup and results.

Table 1. Performance summary and comparison to prior works.

		Nonreciprocal Circulators / RXs			Blocker Tolerant RXs / Filters		
Parameter	This Work	Reiskarimian ISSCC 2017	Dinc ISSCC 2017	Garg ISSCC 2021	Boynton RFIC 2020	Song RFIC 2020	Hari RFIC 2021
Architecture	AND-gate switching N-path filter based circulator RX with embedded PA	N-path filter based circulator RX	Circulator with nonreciprocal delay	FD circulator RX with SIC	Series mixer-first RX	Mixer-first RX with passive Elliptic LPF	Reflection-mode N-path filter
Technology	40nm CMOS	65nm CMOS	45nm SOI	45nm SOI	65nm CMOS	65nm CMOS	45nm SOI
Core Area (mm²)	0.7 (FD/FDD front-end), 0.38 (Circulator RX)	0.94	2.16	4.54	NR	0.63	2.25 (Die size)
Supply (V)	1 (PA + LO), 1.4 (BB)	2.4	NR	NR	NR	1.2	1→1.3
Frequency (GHz)	TX: 21-31, RX: 22-36	0.61-0.975	22.7-27.3	25.5-27.75	9-31	21-29	6-31
G_{RX} (dB)	18	28	-3.2 (Ant. to RX)	16.1	40	3-6	-4.5~-6.6
RX BW_{3dB} (MHz)	400	20	NA	800	NR	500	1-1.22GHz
NF (dB)	18.9~20.4	6.3	3.3~4.4 (without RX)	5.8	12.5~17	12~14.5	5~20 (18.5 @28GHz*)
IB IIP3 (dBm)	2.8	-18.4	NA	NR	NR	NR	1.4~6.3
OOB IIP3 (dBm)	15 (ΔF/BW=1.5)	15.4 (ΔF=500MHz)	NA	NR	21*	NR	14~20 (ΔF/BW=1)
IB B_{1dB} (dBm)	5†	NR	NA	11.5 (with SIC)	-45*	-6	-8 @20GHz*
OOB B_{1dB} (dBm)	13† (ΔF/BW=1.5)	NR	NA	NR	-6→+4	3.4 (ΔF/BW=2)	4.4 (ΔF/BW=1)
TX-to-antenna insertion loss (dB)	1.8 @ 28GHz	1.8	3.3	3.1	NA	NA	NA
TX-to-RX isolation (dB)	>30dB (28.3-29.1GHz) >20dB (27.1-31.1GHz)	26* / 40 (with Bal. Network)	>18.5	53 (with SIC)	NA	NA	NA
P_{DC} (mW)	LO buffer: 89 Baseband: 19.9	108	78.4	RX: 88 SIC: 23.5	72→162	22.8	146-384

*Graphically estimated †Blocker signal is applied to the PA, and its level is measured at the antenna port.

high-capacity wireless access where the network latency and capacity are more critical than its link budget.

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