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Antenna-in-Package (AiP) Using Through-Polymer Vias (TPVs) for a 122-GHz Radar Chip

Hengqian Yi, Efe Öztürk, Marco Koelink, Jana Krimmling, Andrei A. Damian, Wojciech Debski, *Member, IEEE*, H. W. van Zeijl, *Member, IEEE*, Guoqi Zhang, *Fellow, IEEE*, and René H. Poelma, *Member, IEEE*

***Abstract*— High-performance IC-to-antenna interconnection is one of the key enablers for the mass production of high-end millimeter wave (mmW) radar systems above 100 GHz. In this work, a radar system with an on-package antenna array working at 122 GHz is presented. The antenna is placed on top of the molded package and the antenna-to-chip interconnection is realized by through-polymer via (TPV) technology. The detailed fabrication process of the radar antenna-in-package (AiP) with TPV is discussed. The results from the functional tests of the radar AiP are presented and benchmarked to a commercial quad-flat no-leads (QFN) package with an open antenna cavity. The detection margin between the echo signal and the constant false alarm rate (CFAR) threshold is approximately 10 dB higher for the TPV radar AiP compared with the benchmarked commercial QFN package.**

***Index Terms*— 0.13-μm silicon germanium bipolar complementary metal-oxide semiconductor (SiGe BiCMOS), film-assisted molding, metalized polymer, monostatic frequency-modulated continuous-wave (FMCW) radar, patch antennas, radar antenna-in-package (AiP), SU-8, system-in-package (SiP), through-polymer via (TPV).**

I. Introduction

THE development of silicon germanium bipolar complementary metal-oxide semiconductor (SiGe BiCMOS) technology has enabled the monolithic integration of state-of-the-art system-on-chip transceivers in the G-band frequency range (110–300 GHz). All RF signals are kept inside the chip except the signals from the chip to its antennas. Due to the increasing application frequencies, the influence of undesired parasitic electromagnetic interference introduced by the manufacturing limitations of the interconnects is becoming more pronounced [1], [2].

Due to the size reduction of the antennas with increasing frequency, the integration of antennas into the IC package is becoming possible and beneficial at frequencies above 100 GHz. Many antenna-in-package (AiP) concepts are developed recently using different packaging technologies, including quad-flat no-leads (QFN) with wire bonding, embedded wafer-level ball grid array (eWLB), and low temperature co-fired ceramics (LTCC).

For the QFN packaging solutions, wire bonding is used for the IC-to-antenna interconnection. Since the mm wavelength becomes comparable to the wire bond length, the wire bond introduces uncontrollable parasitic effects with its corresponding manufacturing tolerances [3]–[5]. To meet the RF requirement, the wire bonding process becomes costly, time-consuming, and yields limited performance improvement. eWLB technology allows antennas to be connected to the IC by the redistribution layer (RDL) [6]–[11]. However, the antennas are placed on the side of the IC which limits the area that can be used for the antenna fabrication. Furthermore, the chip is not placed in direct contact with any thermally conductive plane which is a disadvantage for high-power monolithic microwave integrated circuit (MMIC) applications. LTCC packages are advantageous for their low loss tangent, high thermal conductivity, and low thermal expansion coefficient (CTE) [12]–[14]. However, the co-fire temperature is much higher than the temperature that the Si circuit can withstand. Thus, the antenna substrate is fabricated separately and assembled afterward adding extra steps in the package fabrication. In addition, metal patterns made in the LTCC process have relatively large surface roughness which is not desired in mm-wave applications.

New package solutions for mm-wave frequency radar systems are needed. One promising package solution is to create a radar package with its antennas placed on top of the molded QFN package and connected vertically to the radar IC. In this case, additional fabrication, assembly, and wire-bonding of an external antenna substrate are avoided. Moreover, the length of electrical interconnection can be reduced to the thickness of the epoxy molding compound (EMC) layer. The antennas are patterned on top of the EMC; hence, the package can be further

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miniaturized when compared to other packaging solutions. Additionally, the IC can be bonded directly to a metal plate for improved heat dissipation. Therefore, the advantages of such radar AiPs are shorter electrical interconnection, a simpler fabrication process, finer antenna features, smaller footprints, and compatibility with high-power MMICs.

Conventionally, a vertical interconnection can be made through a molded package by laser drilling followed by Cu plating or solder filling of the drilled hole. This technology is called through mold via (TMV) [15]–[17]. The disadvantages of TMV include the damage of the substrate by laser, contamination of burned epoxy, thermal damage, limited aspect ratio and density, and poor sidewall control. As a novel technology for through package vertical interconnection, through-polymer via (TPV) takes an unconventional approach [18]. Instead of a laser drilling process, metalized polymer pillars are produced on the substrate, such as a wafer, before the epoxy molding process which is a bottom-up approach. The pillars are high-aspect-ratio extensions of the top layer interconnects on the chip. Next, the substrate with pillars is molded using film-assisted transfer molding (FAM) technology [19]–[22]. In a FAM process, the mold parts are covered by plastic films fixed by vacuum. When the mold parts are closed prior to the injection of the molding compound, the top side of a metalized polymer pillar is in contact with the top mold and is slightly pressed into the soft plastic film. When the molding compound is injected into the mold, the top side of the pillars is then sealed by the film. Hence the FAM process keeps the top side of the metalized polymer pillars clean of the molding compound and enables further processing of the antennas. Compared with TMV, TPV is a lower-cost and cleaner process. It does no damage to the substrate and is suitable for scale-down and high-density fan-out. Furthermore, the TPVs are made by a lithographic process, which enables high precision, free form factor, and high-volume wafer-level production capabilities.

In this research, we demonstrated an AiP solution for a 122-GHz radar system with an on-package antenna array using TPVs as the IC-to-antenna interconnections. In Section II, the radar IC and the AiP solution are introduced. Then the antenna design and the simulation results are discussed in Section III. Furthermore, the fabrication process is explained and the results are shown in Section IV. Finally, the functional test results of the radar AiP are presented in Section V. The performance of a commercial radar AiP using open cavity and wire bonding with the same IC and same antenna array is compared with our work.

II. Radar IC and Packaging Design

A. Radar IC and Its Layout

The radar IC is manufactured by SiGe technology with the 0.13-μm BiCMOS process [23]–[27]. The radar IC operates at 122-GHz industrial, scientific, medical (ISM) band and is designed for highly accurate short-distance measurement. It consists of a push-push type voltage-controlled oscillator (VCO), a power amplifier, an in-phase-quadrature receiver chain, a 1/32 frequency divider, an external phase-locked loop

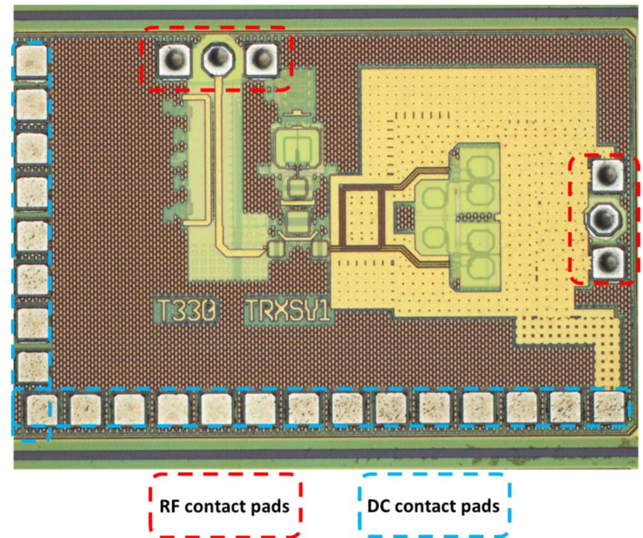

Fig. 1. Optical microscopy image of the radar IC (top-view). The red boxes indicate the RF contact pads and the blue boxes indicate the dc contact pads.

(PLL), several temperature sensors, and power detectors. The VCO can tune the signal frequency from 120.6 to 124.3 GHz.

Before reaching the antenna array, the signal is boosted by a power amplifier and around 0 dBm of output power could be achieved. The radar IC occupies a total chip area of 940 $\times$ 1450 μm with 22 contact pads for interconnection with the QFN package and six RF contact pads for the interconnection with its antennas. A top view of the radar IC is shown in Fig. 1. The three contact pads on the top side of the IC are connected to the transmitter antennas and the other three contact pads on the right side of the IC are connected to the receiver antennas as indicated by the annotations in Fig. 1. The total power consumption of the radar IC is around 450 mW which is supplied with a single 3.3-V source [23].

B. Packaging Design Using TPVs

In our proposed packaging solution, the electrical interconnections between the radar IC and the antenna array are realized with TPVs instead of wire bonds. The main process steps of the TPV technology are shown in Fig. 2. First, a substrate is coated with a layer of polymer material, such as a photoresist. Then, the polymer layer is patterned into the desired high aspect ratio polymer pillars. The polymer pillars are coated with a metal layer for electrical conductivity. A FAM molding process is carried out afterward to encapsulate the substrate with the top side of the metalized pillars exposed. Finally, a metal layer can be added to the top of the encapsulated package.

The polymer material used in the process is SU-8 negative resist [28]–[30]. SU-8 is epoxy-based and therefore suitable for permanent use and compatible with the thermal budget requirements for transfer molding and soldering [30]. Furthermore, the SU-8 photoresist enables the fabrication of high aspect ratio structures [28].

The 3-D schematic of the radar AiP using TPVs for chip-to-antenna interconnections is shown in Fig. 3. The EMC is shown transparent in Fig. 3(b) and (c) to view the embedded

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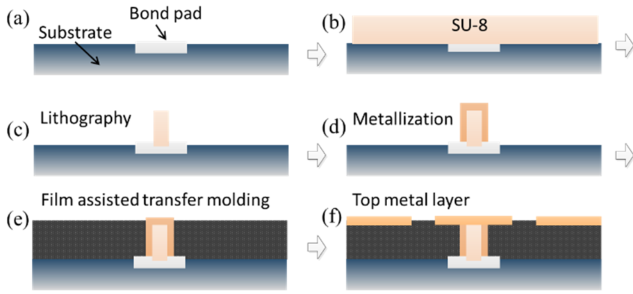

Fig. 2. Illustration of the main process steps of TPV fabrication. (a) Substrate with contact pads. (b) Coating of SU-8 layer on the substrate. (c) Patterning SU-8 via lithography. (d) Metallization of SU-8 pillars. (e) Molding process. (f) Top metal layer deposition.

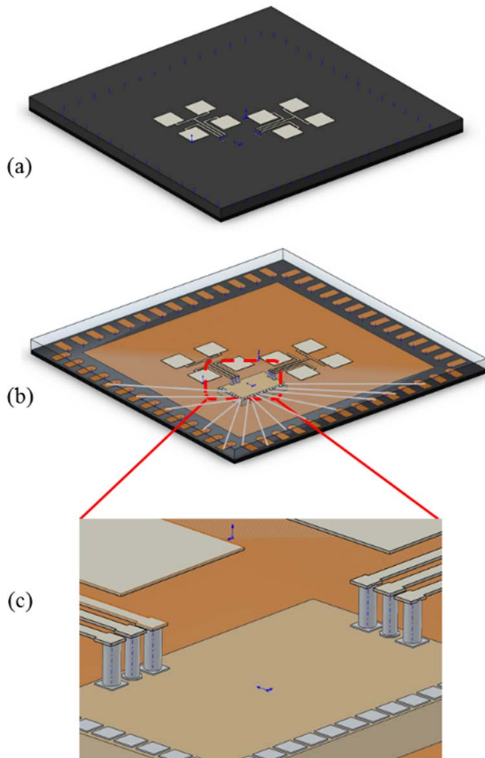

Fig. 3. Schematic of the proposed package design. (a) QFN package with antennas on top. (b) Mold compound is made transparent to view the TPVs. (c) Zoomed-in view on the TPVs.

IC, wire bonds, and TPVs. Wire bonds are still in use for interconnecting the non-RF I/Os on the Radar IC to the QFN package lead frame. The minimum thickness of the molded EMC layer is in this particular design limited by the loop height of the wire bonds. The thickness of EMC above the radar IC requires a minimum of 150 μm to keep the wire bonds sufficiently shielded. Hence the TPVs are designed to be 150 μm in height. According to the position and dimension of the contact pads, the diameter and the pitch size of the SU-8 pillars are determined to be 40 and 100 μm, respectively. The SU-8 pillars are conformably coated with Al (1%Si) alloy by sputtering to match the metallization of the contact pads of the die. A thickness of 2.5 μm is chosen for sufficient electrical conductance and step coverage. The skin effect depth of Al at the working frequency of 122 GHz is 0.23 μm. Thus, the

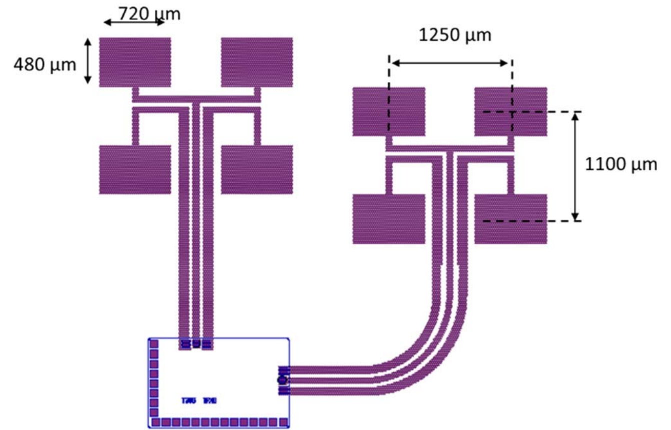

Fig. 4. Patch array antenna design using a GCPW feeding network and the dimensions of the patch elements.

electrical conductance of the TPVs, in this case, is limited by the skin effect rather than the metal coating thickness. The metalized SU-8 pillars have a diameter of 45 μm, and an aspect ratio of 10:3. For the package housing, an 8 $\times$ 8 mm QFN is used, the same as the benchmarked commercially AiP [31].

III. Antenna Design

Patch array antenna structures are designed for the first fabricated radar packages. The antenna design uses a grounded coplanar waveguide (GCPW) as the feeding network [32], as shown in Fig. 4. The GCPW feeding lines are chosen instead of microstrip (MS) lines because they match with the on-chip GCPW networks, and no transition from the ground-signal-ground (GSG) pads to MS lines is required. Additionally, by using GCPW lines, the complete feeding network is realized in between the antenna elements which optimizes the space usage. The GCPW-fed antenna uses three vias for the GSG interconnection. The patch element has a height of 480 μm and a width of 720 μm. The pitches between the patch elements are 1250 μm in the horizontal direction and 1100 μm in the vertical direction. The vias and the feeding lines are designed for an optimized impedance matching. The die-attachment pad of the QFN which is about 300 μm away from the antenna is used as the antenna reflector. The ε' and tanδ of the EMC material used in this work are 3.6 and 0.01 measured at 100 GHz according to the material manufacturer. The 2 $\times$ 2 patches could reach around 13 dBi of directivity. With the additional matching network and efficiency drop due to the substrate, the gain would eventually reduce.

The simulations are completed using a full 3-D EM model of the package with EMPIRE 3-D software. The full 3-D EM model includes the antenna array, the TPVs, the GCPW lines, the radar chip, and the QFN package. The results of the radiation pattern and the realized gain in the E-/H-plane are shown in Fig. 5. The impedance matching design in the simulation is more straightforward when using TPVs when compared to wire bonds which reduce the cost of computation time and design effort. According to the results, the antenna

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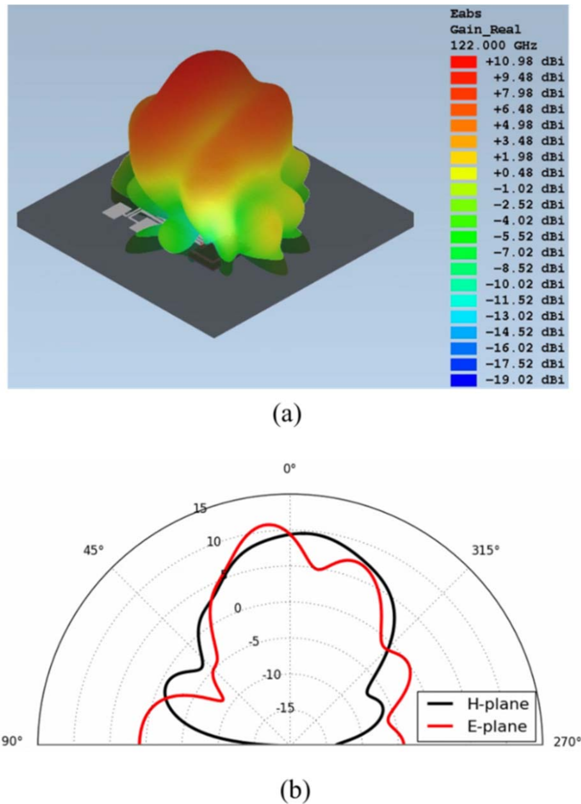

Fig. 5. Simulation results of the antenna utilizing GPCW matching network showing (a) 3-D radiation pattern and (b) more than 10-dBi gain in E-/H-plane at 122 GHz of operation frequency.

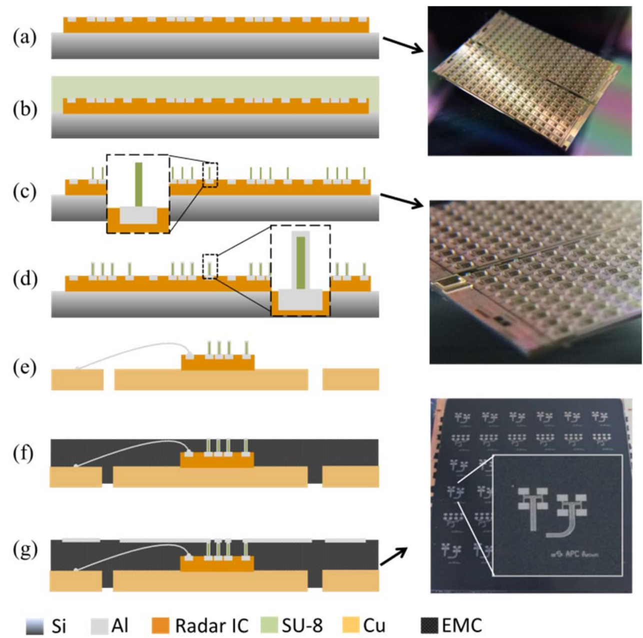

Fig. 6. (Left) Schematic of the fabrication process flow of the proposed radar package. (Right) Images showing the intermediate fabrication results. (a) Assembly of the radar IC tile onto a silicon carrier wafer. (b) Spin coating of SU-8 resist. (c) Exposure and development of the SU-8 layer to obtain polymer pillars. (d) Metallization of polymer pillars and patterning of the metal layer. (e) Assembly of the singulated radar ICs onto a QFN substrate, including pick & place and wire-bonding steps. Each QFN panel was assembled with 36 radar ICs. (f) Film-assisted molding of the QFN substrate. (g) Metallization on top of the molded QFN and patterning of antenna structures. The schematic shown is not to scale. Following (g), the dicing of the QFN panel is performed to obtain individual radar AiPs.

could provide more than 10 dBi of realized gain through the whole IC operation band. The beam tilt could be eliminated by correcting the antenna position on the package in future work. The antenna simulation has shown similar results compared to the design used in the commercial package with wire bonds [32].

IV. Package Fabrication

A. Fabrication Process

The TPV process can be a wafer or panel-level process. The 200-mm radar wafers are diced in tiles of 24 × 19 mm. Each tile contains 270 radar ICs. The tile is mounted on a 4-in silicon carrier wafer using a temporary bonding layer. This allows the samples to be handled in the Else Kooi Lab (EKL), TUDelft cleanroom facilities. After the fabrication of TPVs, the wafer tile is removed from the carrier wafer by a thermal releasing process. Compared to the commercial package, the length of the RF interconnection is reduced from a wire bond length of 350 μm to a TPV height of 150 μm. The shorter electrical length reduces the inductive parasitic effect which is critical in millimeter-wave radar systems.

A detailed process flow is presented in Fig. 6. First, the wafer tile is bonded onto a silicon carrier wafer. The temporary bonding material used is poly (propylene carbonate) [33], [34]. Since the wafer tile is 150-μm thick, a 300-μm thick SU-8 layer is spin-coated at a spin speed of 500 r/min for 60 s so that the thickness of the SU-8 above the radar IC is around 150 μm. After the spin coating, a soft baking step is applied to evaporate the solvent and solidify the SU-8 film. The exposure of SU-8 is carried out on an EVG 420 mask aligner with an exposure dose of 885 mJ/cm^2 followed by a post-exposure bake (PEB) step. The PEB process was carried out on a hotplate and consists of two stages. The first stage of PEB is a low-temperature bake at 65 °C for 5 min. The second stage of PEB is a higher temperature bake at 110 °C for 10 min. The SU-8 layer is developed in propylene glycol methyl ether acetate (PGMEA). During development, the wafer is placed in a wafer carrier facing down in the PGMEA solution. Gentle agitation is provided by a magnetic rotor. A low-power plasma flash is applied to remove the remaining residue of SU-8 after the development process. A hard baking step in a vacuum oven is carried out before metallization which helps the SU-8 to further cross-link and degas thoroughly. A hard baking temperature of 180 °C which is higher than the molding temperature is used to ensure the thermal stability of the polymer core during the molding process.

After hard baking, sputtering of 2.5-μm thick Al with 1% Si layer is performed. During the sputtering process, the wafer holder is kept at 25 °C, however, the temperature at the surface of the wafer can rise above the glass transition temperature with continuous deposition. Hence, a cooling step is inserted after every 156-nm-thick deposition. In this way, the sputtering process induces no damage to the SU-8 pillars.

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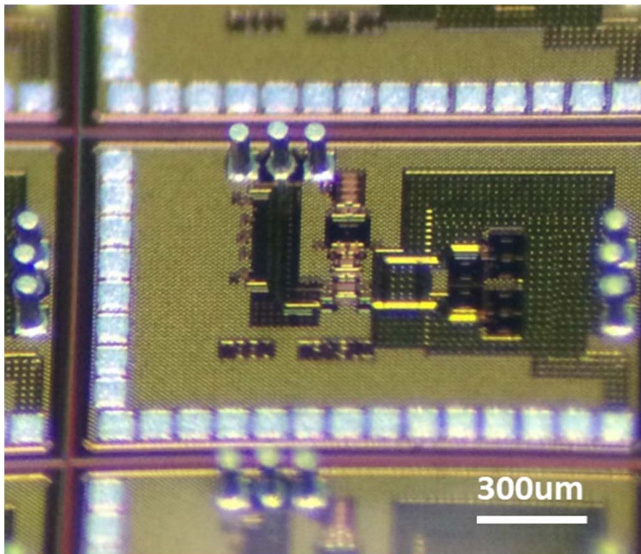

Fig. 7. View of metalized SU-8 pillars fabricated on the radar IC under an optical microscope.

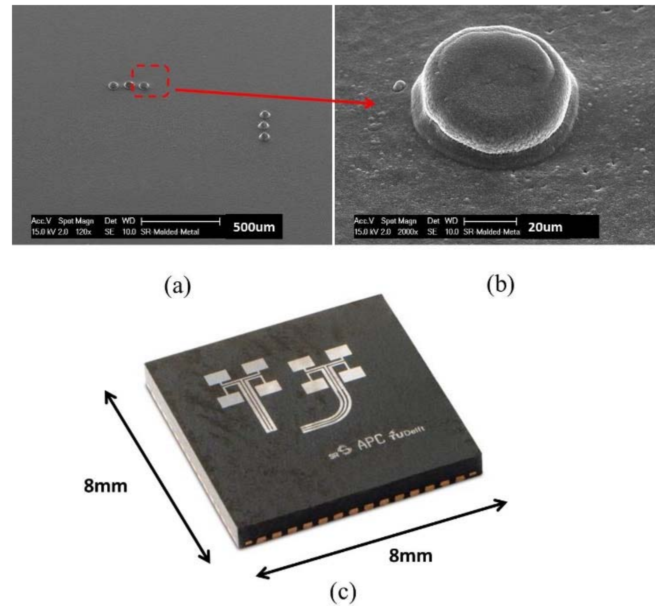

Fig. 8. (a) Protruding top surface of a TPV after FAM. (b) Close-up view. (c) Picture of the fabricated radar AiP with on-package antenna array using TPVs as the antenna-to-IC interconnection after package singulation.

The fabrication results of metalized SU-8 pillars on the radar IC are shown in Fig. 7. The wafer tile containing the radar ICs is removed from the carrier wafer and diced into single chips. The removal of the IC is achieved by heating the wafer up to 180 °C to soften the PPC layer and then sliding the IC off the carrier wafer. The singulated radar chips with metalized pillars are then picked up and placed onto a QFN panel in a 6 × 6 array. An automated wire bonder connects the remaining radar IC contact pads to the QFN panel using Al wire bonds. The entire panel is then molded using film-assisted molding which keeps the top surface of the metalized pillars clean of EMC which subsequentially results in the realization of TPVs.

The last step is to fabricate the antenna arrays and the feeding networks on top of the encapsulated QFN panel. The antennas are created using front-end semiconductor manufacturing technology combined with film-assisted molding. Using FAM, the radar IC is encapsulated inside the EMC while keeping the top surface of the TPVs clean, as shown in Fig. 8(a) and (b). Before the metallization, a cleaning process is applied to the surface of the EMC molded QFN panel to remove any contamination and improve adhesion. Next, metallization of the entire QFN panel is carried out to form the antenna layer using sputtered Al (1%Si) to match the metallization of the TPV coating. The Al layer is masked and patterned using lithography and etching techniques. A photoresist layer is spin-coated on the surface of the metalized QFN panel. The antenna patterns are exposed on the photoresist layer and developed, followed by Al wet etching. After the resist removal by acetone, the antenna structures are completed and connected to the IC through the TPVs. An example of the fabricated radar AiP is shown in Fig. 8(c).

A miniaturized package could be achieved since the antennas are placed directly above the IC. For radar systems working at even higher frequencies, the dimension of the antenna will reduce further to be comparable to or even smaller than the size of the chip. This enables chip-scale or wafer-level packaging of radar systems with the antenna arrays on top.

B. TPV Profile Optimization

Good adhesion of the TPV pillars on the substrate is critical. For instance, during the dicing process of the wafer tiles, the TPVs are subjected to a high-pressure water jet from the dicing tool. The profile of the interface between the TPVs and the substrate has a decisive influence on the adhesion of the metalized pillars toward the contact pad material, and the step coverage of the metal coating. We improved the interface profiles of SU-8 pillars from an undercut profile to a foot profile, as shown in Fig. 9. SU-8 pillars with an undercut profile have smaller footprints while SU-8 pillars with a foot profile have larger footprints and no undercut. Because the resist material is exposed from the top, the lower parts of the film receive less exposure energy and are therefore less crosslinked. Under nominal process conditions (95 °C PEB and then development), an undercut profile at the interface is obtained. The adhesion of TPVs with the undercut profile is proven not sufficiently strong to survive the water jet from the dicing tool.

To obtain a foot profile, the exposure energy is kept the same, however, the PEB temperature was increased from 95 °C to 110 °C. Because the PEB step was carried out on a hotplate, the resist material at the interface receives more thermal energy. Consequently, in this area the thermally induced crosslinking is more effective which leads to the desired foot profile. The high-resolution SEM images of the resulting undercut and foot profiles of TPVs are shown in Fig. 10.

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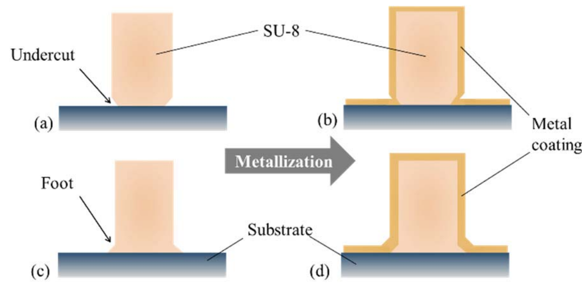

Fig. 9. Schematic illustration of the two different interface profiles between TPVs and substrate. (a) Undercut profile after SU-8 development. (b) Undercut profile after metalization. (c) Foot profile after SU-8 development. (d) Foot profile after metalization.

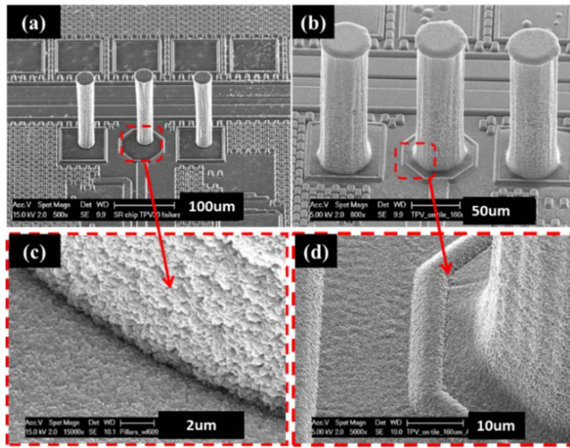

Fig. 10. SEM images of metalized SU-8 pillars on the radar IC bond pads. Shows foot profile (a) A and (b) B.

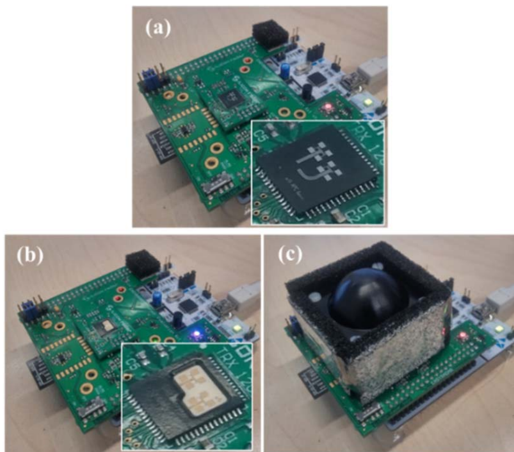

Fig. 11. Images of the fabricated radar package with TPVs and the commercial package assembled on the same test kit. The test kit loaded with the QFN AiP using TPVs with GCPW-fed patch array antenna is shown in (a). Test kit loaded with the open cavity QFN AiP is shown in (b). (c) Shows the test kit assembled with an RF lens.

V. Radar Functional Test

To characterize the functional performance, the fabricated radar AiPs using TPV technology were assembled on a test kit at Silicon Radar GmbH, Frankfurt (Oder), Germany. The radar AiPs using TPVs under test is shown in Fig. 11(a). A commercially available radar AiP with open cavity and wire bonding was also measured to provide a reference for the performance, shown in Fig. 11(b). In this commercial package, antennas were fabricated on a substrate called Rogers ULTRALAM 3850 which has low permittivity and low losses up to the millimeter-wave range [32]. In the commercial package, the antennas are connected to the radar IC by 3 Al bond wires with a wedge-to-wedge technique. The test kit consists of three main parts, the radar package frontend under test, a baseband PCB assembly, and an additional plastic lens with lateral shielding. The additional lens and lateral shielding are used to enhance the signal and reduce side lobes. The test kit was fixed by glue on the table to make sure the position of the tested packages and RF lens could not change between measurements.

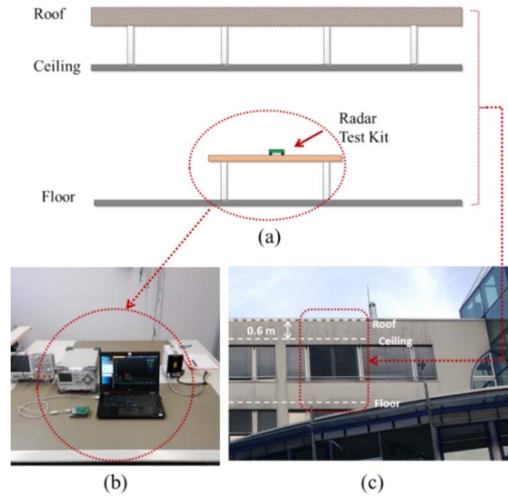

Fig. 12. Schematic of the test environment. Both the ceiling and the roof of the building were used as targets. (a) Schematic illustration of the test setup. (b) Measurement setup. (c) Photograph of the detected building features.

The radar test kit operates with a frequency modulated continuous wave (FMCW) principle using the constant false alarm rate (CFAR) mechanism for determining the detection threshold. An adaptive threshold can be calculated by keeping the probability of false alarms constant while the noise background is continuously changing [35]. The frequency of the signal is centered at 122 GHz. A bandwidth of 4500 MHz and 1024 fast Fourier transform (FFT) data acquisition were used to obtain an optimized detection accuracy of 19.4 mm with a maximum measurement range of 10 m. The radar signal was beamed toward the ceiling. A schematic illustration of the measurement environment is shown in Fig. 12.

The echo signal strength and the CFAR threshold curve are plotted over the measurement range for both radar AiPs, as shown in Fig. 13(a) and (b). The measurements were carried out with a refresh rate of around 10 Hz, which generated ten sets of echo signal strength and CFAR threshold values in one second. The plotted curves are the average of the ten measured datasets. An object is considered detected when a peak is observed in the echo signal strength above the CFAR threshold curve.

According to the measurement results, objects at distances of 2.1 and 2.7 m are detected. The object detected at 2.1 m away corresponds to the ceiling, while at 2.7 m away it

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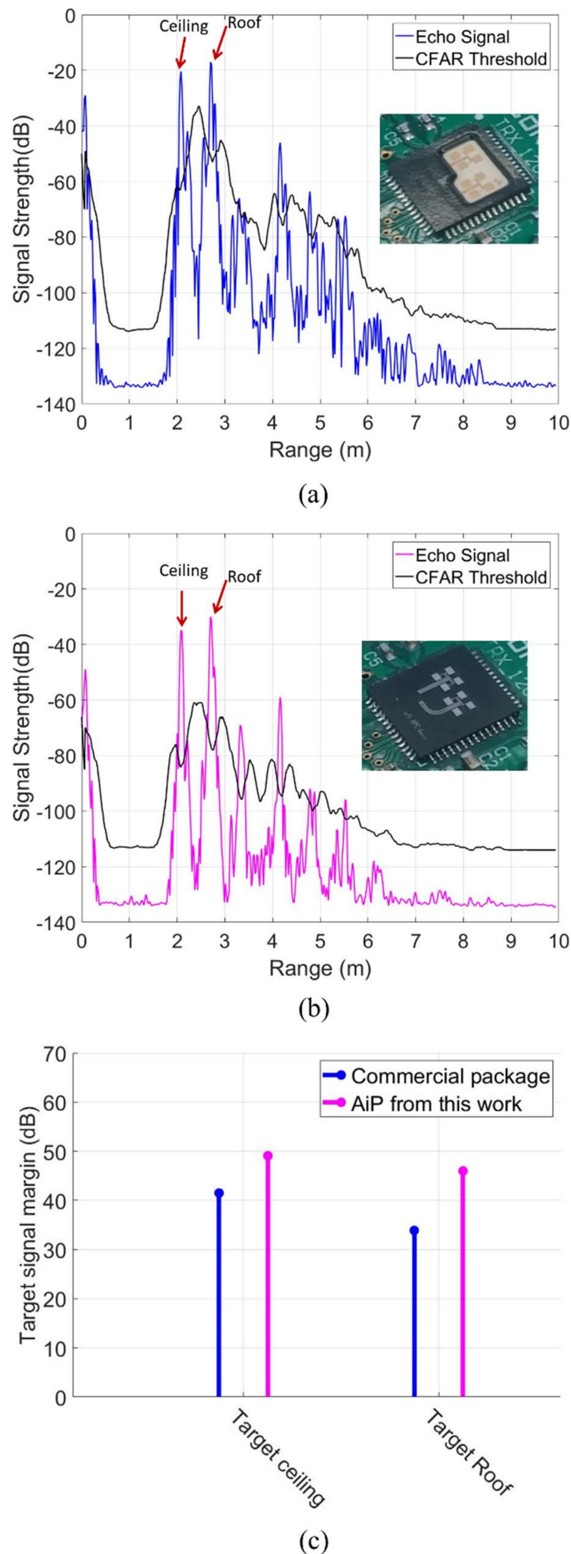

Fig. 13. (a) Echo signal and CFAR threshold measured from the open cavity QFN AiP plotted over the detection range. (b) Echo signal and CFAR threshold of the QFN AiP using TPVs with GCPW-fed antenna plotted against distance. (c) Comparison of the detected target signal margin of the first two targets, the ceiling and the roof, measured by both AiPs.

corresponds to the roof of the building. Both radar AiPs under test captured the objects with a clear echo signal. The conventional AiP using wire-bonding and open cavity receives echo signals with strengths of −21 and −17 dB at 2.1 and 2.7 m, respectively. The AiP using TPVs with a GCPW-fed antenna receives an echo signal with a strength of −35 and −30 dB.

However, comparing the measured echo signal strength with the CFAR threshold, the target signal margins obtained by the conventional AiP are around 41.51 and 33.89 dB at the two targets. The target signal margins obtained by the AiP using TPVs are around 49.09 and 46 dB which are 7.5 and 12.1 dB higher than the conventional AiP, as shown in Fig. 13(c). This indicates the AiP using TPVs distinguishes the echo signals better from the background noise. The TPV interconnection which is shorter in length and lower in parasitic effect compared to the wire bonds contributes to the low noise performance.

The functional RF performance of the radar systems using the TPV packaging solution is superior to the conventional package. The prototype packages detect targets at similar accuracy with a lower noise level compared to the commercial package. The relatively higher loss observed in echo signals can be improved by optimizing both the impedance matching and the substrate material properties.

VI. Conclusion

In this work, we have presented a 122-GHz radar system with an on-package antenna array using TPVs as the IC-to-antenna interconnections. The length of the electrical connection of the IC-to-antenna interconnection is reduced to an average of 150 μm. The antenna array is placed on top of the IC which enables the miniaturization of the footprint of mm-wave radar AiPs. The antenna layer is fabricated directly on the EMC as the substrate which saves the cost of extra antenna substrates. By tuning process temperatures, the robustness of the TPVs in the following dicing and molding process was optimized. The final packages are tested with FMCW measurements. The performance of the radar AiP using TPVs is benchmarked with the radar AiP using wire bonds. The TPV interconnection shows a better noise performance compared to the wire bonds. The margin between the echo signal and the CFAR threshold curve at the detection peak of an object is 10 dB higher on average measured by the radar AiP using TPVs.

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