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A 39 W Fully Digital Wideband Inverted Doherty Transmitter

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***Abstract* — A high-power fully-digital Doherty transmitter (DDTX) is proposed. It features two segmented LDMOS output switch banks implemented in a custom V_T-down-shifted LDMOS technology. A 40 nm CMOS controller digitally activates the individual LDMOS gate segments of the output stage at RF speed. An inverted Doherty power combiner is proposed that features non-short circuited 2nd harmonic conditions for the main and peak switch banks to boost the RF bandwidth. To guarantee smooth output power and efficiency vs. frequency, a 2nd harmonic trap is introduced in the power combiner, yielding an RF bandwidth of $>$ 400 MHz . The realized demonstrator can achieve over 39 W peak output power. Its highest drain and system efficiencies, respectively 60 % and 57 %, were found at 34.2 W of output power, while in power back-off its peak drain and system efficiencies are 52 % and 48 % respectively. Over a 25 dB output range, the system efficiency is within 4 percent points of the drain efficiency.**

***Keywords* — digital transmitters, LDMOS, CMOS, inverted Doherty, wideband.**

I. Introduction

Digital transmitters (DTXs) offer promising benefits over traditional analog transmitters (TXs): namely, they do not require any input impedance matching or quiescent currents for their output stages. Furthermore, they completely eliminate stability issues and are flexible in their activation profile and output matching [1, 2]. Consequently, the DTX concept can offer very high system efficiencies, especially at power back-off (PBO), while its RF bandwidth (BW) is only limited by the design of the applied output matching network.

In the work of [2] and [3], focus was placed on achieving high DTX RF output power and peak efficiency; however, neither works offer enhanced efficiency in PBO, nor high RF BW. With this work, we present world's first fully-digital high-power Doherty transmitter ($P_{\text{out}} > 39$ W). Smooth wideband RF operation is achieved using a modified inverted Doherty topology (BW > 400 MHz). The measured peak drain/system efficiency is 60 % and 57 % respectively. The overall system efficiency is within 4 % points of the drain-efficiency over a 25 dB PBO range. These initial results pave the way for high-power, highly integrated, and energy-efficient DTX line-ups that will enable future "green" fifth-generation (5G) massive multiple-input and multiple-output (mMIMO) systems.

II. Design of the Harmonic Output Match

The core of this digital Doherty transmitter (DDTX) design is a high-power dual polar DTX line-up [Fig. 1(a)]. It consists of a 40 nm CMOS controller chip, which drives two segmented RF-output stages implemented in a custom V_T-down-shifted LDMOS die [1]. The CMOS controller/driver is bondwire connected to the gates of the LDMOS segments, which can be individually switched on/off by the controller in a digital fashion at the speed of the RF operating frequency. The total gate width ($W_{G,\text{tot}}$) of the segments in each of the two switch banks is 20.7 mm, yielding a C_{DS} of 7.9 pF per bank including bondbar.

Digital class-C operation [3, 4] was selected as operating class in this work for the DTX output stages; its capability to handle a relatively large output capacitance, its linear operation,

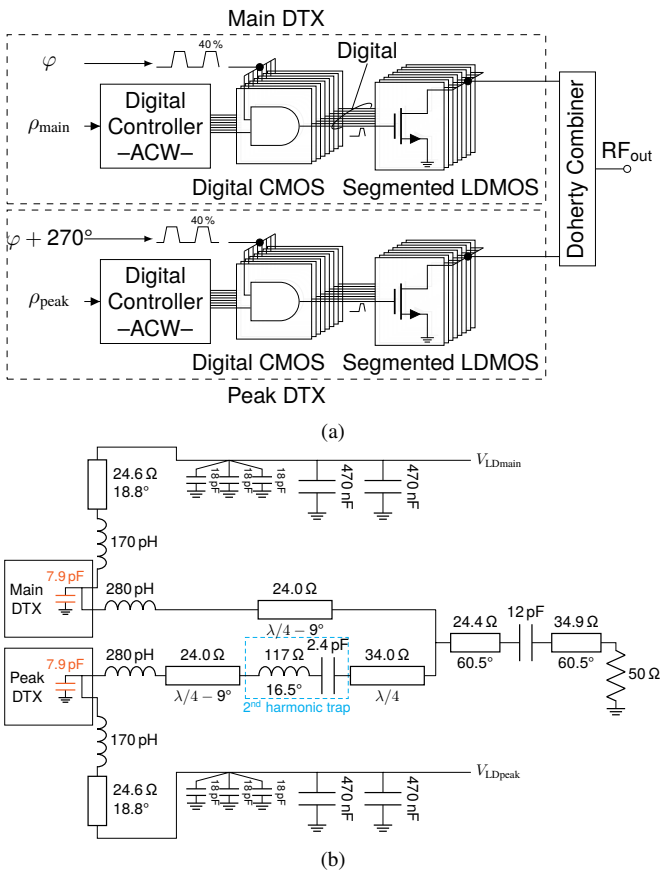

Fig. 1. (a) Principle schematic of the high-power dual polar DTX line-up. (b) Schematic of the proposed inverted Doherty power combiner featuring a low-Q 2nd harmonic trap in the peak path to guarantee smooth output power and efficiency vs. frequency. The second harmonic trap is implemented by a high ohmic impedance transmission line section and an SMD capacitor.

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limited voltage swing and excellent efficiency-output power relation motivated this choice [3]. Lowering the duty-cycle in digital class-C operation increases the efficiency at the cost of RF output power. For the DTX hardware used, the minimum achievable duty-cycle is 40 % at the targeted RF operating frequency of 2.0 GHz by using on-chip duty-cycle adjustment. This sets the maximum theoretical achievable efficiency for these conditions to 75.7 %, while providing 21 % higher output power compared to analog class-B, assuming an ideal device and lossless output matching network [3]. Similar to the analog transconductance classes, digital class-C operation demands close to short-circuited conditions for its higher harmonics. For an activation duty-cycle of 40 %, the resulting internal LDMOS current waveform will be dominated for its higher harmonics by the 2nd and, to a lesser extent, the 3rd harmonic [5]. However, realizing wideband short-circuited conditions for the 2nd harmonic without reducing the bandwidth of the fundamental matching is challenging. Therefore, in this design the use of explicit 2nd harmonic shorts at the drains of the active devices has been omitted. To achieve wideband operation, shunt inductors have been used at the drains of the switch banks to resonate out their (7.9 pF) output capacitance around the center frequency of 2 GHz. The relative high C_{DS} of the switch bank capacitances tend to approximate AC short-circuited conditions for the higher harmonics.

A. *Inverted Doherty*

The inverted Doherty topology has been selected for its improved power and efficiency bandwidths in power back-off operation over the classical Doherty topology [5]. Since both switch banks have the same total $W_{G,\mathrm{tot}}$, a symmetric inverted Doherty is designed. The DTX switch banks have a nominal load impedance of $R_L = 17\,\Omega$ with a supply of $V_{\mathrm{LD}} = 28\,\mathrm{V}$. The schematic used for the inverted Doherty power combiner is shown in Fig. 1(b). A part of the output inductance of the bondwires is absorbed in the connecting $\lambda/4$-lines lines by slightly shortening the lines. The PCB also provides the bondwire connected stubs that are used to feed the DC bias. The $\lambda/2$-line is split into two $\lambda/4$-lines with different impedances to further enhance the RF bandwidth [5, 6]. Finally, the output of the inverted Doherty combiner is matched to 50 Ω using a two-section impedance transformer, including a DC blocking capacitor.

B. *Harmonic Trap*

The main and peak DTXs are driven by signals that are delayed 90° from each other at the center frequency. The total electrical length between the main and peak DTXs is $3\lambda/4$ for the fundamental at the center frequency, fulfilling the requirement for the Doherty load modulation. In Figs. 2(b) and 2(c), the fundamental impedance seen by the main switch bank is shown at full and back-off powers. However, since there is no explicit 2nd harmonic short applied, the C_{DS} susceptance of the peak DTX at the 2nd harmonic is transferred by the $3\lambda/4$ network and directly seen by the main DTX. For frequencies slightly higher than the center frequency of the design, the

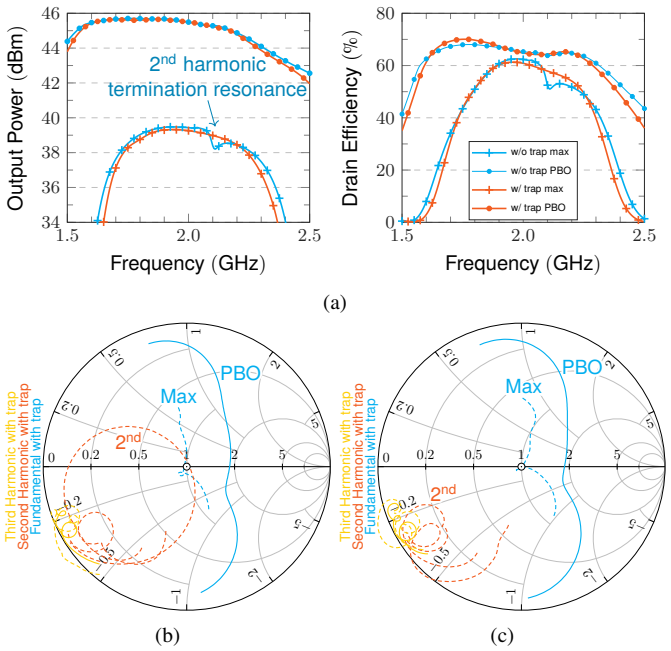

Fig. 2. Simulated performance of the DDTX on a schematic level, showing the impact of the harmonic trap: (a) comparing the output power and efficiency vs. frequency, showing the dip for power back-off (PBO); (b) the impedance seen by the main DTX without the harmonic trap, for the fundamental, and second and third harmonics. The second harmonic impedance shows a resonance, causing the dip in power and efficiency. (c) the impedances with harmonic trap, showing that the harmonics now see a lower impedance.

transformed C_{DS} susceptance of the peak DTX yields a large inductive susceptance, which is in parallel with the output capacitance of the main DTX. At this frequency, it results in an undesired parallel resonance in the 2nd harmonic termination of the main DTX [see Fig. 2(b)]. This leads to a sharp increase in the 2nd harmonic termination of the main, causing a sharp dip in output power and efficiency [see Fig. 2(a)]. To prevent this phenomenon and avoid degradation of the usable bandwidth of the DDTX, a 2nd harmonic trap was added by placing a series LC resonator in the peak path. This resonator is designed to have a low Q-factor at the fundamental to not degrade the bandwidth of the DDTX. By placing it after the first $\lambda/4$-line, the undesired 2nd harmonic parallel resonance for the main path no longer occurs [see Fig. 2(c)], while it has the added benefit of also providing a short for the 3rd harmonic for the peak DTX.

III. Measurement Results

The realized DDTX design (see Fig. 3) was measured using external signal generators capable of changing the mutual phase relations for the digital sampling clock, and the RF activation clocks for the main and peak DTXs. The amplitude information programmed in the DTX controllers' memory has a time duty-cycle of 10 % to prevent excessive thermal heating. The resulting output powers have been measured using a Keysight U8488A power meter, with the losses of a 30 dB high-power attenuator de-embedded.

First, the performance in terms of output power and efficiency for full power and power back-off operations are

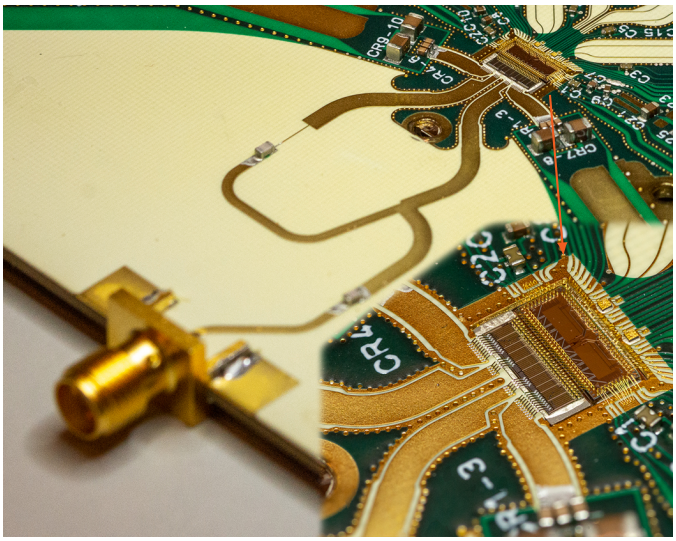

Fig. 3. Photograph of the realized Doherty combiner on PCB.

evaluated in Fig. 4(a). Comparing these measurements with a 3D EM simulated version of the output network show that there has been some significant downshift due to some deviations in its actual assembly, impacting the realized efficiencies. Nonetheless, at 1.66 GHz, a peak drain efficiency of 60 % was measured with a simultaneous output power of 34.2 W. With only the main DTX activated, optimum operation was achieved at 1.77 GHz. The performance over the output power range for this frequency [Fig. 4(b)] shows a peak drain efficiency of 57 % with an output power of 39.1 W. At 6.6 dB power back-off this is 52 %, an 25 % point improvement over the case without efficiency enhancement. Relative to these levels, −1 dB-power bandwidths of 430 MHz and 440 MHz for respectively peak power and power back-off are achieved.

Similarly, for the −10 %-drain efficiency bandwidths these are 590 MHz and 370 MHz. System efficiencies are close to the drain efficiencies, as the controllers' dynamic power consumptions scale with the output stages' activation (between 0 W and 3.47 W), and the static power consumption is only 191 mW (such as SRAMs and the clock tree). In Fig. 4(b), the system efficiencies are 55 % and 48 % for respectively peak power and power back-off. In fact, over the entire measured operating range, the system efficiency remains within 4 percentage points of the drain efficiency.

The capability of the DDTX to handle modulated signals is demonstrated using digital pre-distortion (DPD) with a 7 MHz 256-QAM signal around 1.77 GHz with a PAPR of 5.5 dB. This achieved an ACLR of < -52.0 dBc and an EVM of 0.4 %. In this operation, average drain and system efficiencies of respectively 49 % and 46 % were measured.

IV. Conclusion

A wideband high-power fully-digital Doherty transmitter (DDTX) is presented, achieving 60 % drain efficiency at 34.2 W peak output power. In power back-off, 52 % drain efficiency is achieved. To the best of the author's knowledge, this is at least a 10× improvement in RF output power over all fully-digital

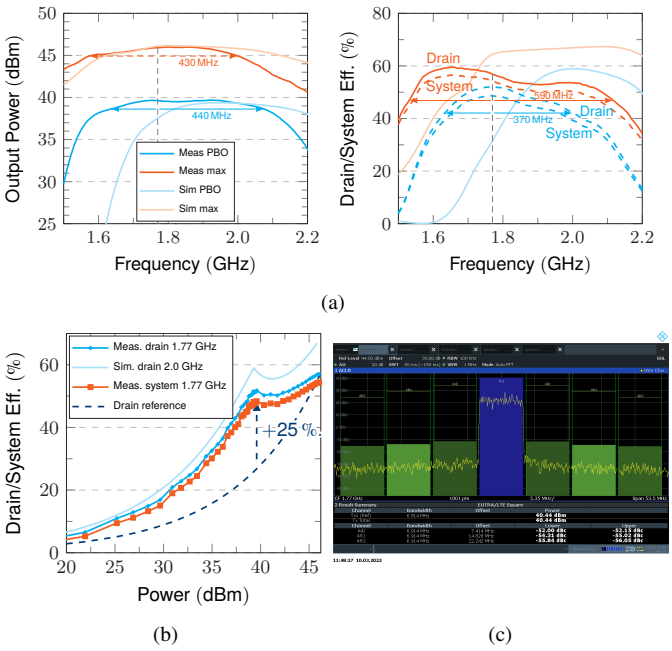

Fig. 4. Measurement results of the DDTX compared with the 3D EM simulated design. (a) The bandwidth at peak power and power back-off of the DTX. Compared to the EM simulated design, it is clear that the realized design has shifted down in frequency. (b) The efficiency vs. output power at $f_c = 1.77$ GHz, showing efficiency improvement in power back-off with respect to a situation without efficiency enhancement by 25 percentage points. (c) Modulated 256-QAM signal showing an ACLR < -52.0 dBc after DPD.

Doherty transmitters reported up to date. This output power level is compatible with the requirements of mMIMO base stations. The efficiency and high output power of the DDTX are obtained by using digital class-C operation with a 40 % RF duty cycle, providing 21 % higher output power compared to analog class-B operation. The realized DDTX reaches > 430 MHz for the −1 dB-power bandwidths, and 590 MHz and 370 MHz for the −10 %-efficiency bandwidths at respectively peak power and PBO operation. These bandwidths have been achieved by omitting the use of explicit second harmonic shorts as normally present for trans-conductance classes. A harmonic trap was introduced to guarantee smooth output power and efficiency vs. frequency. The system efficiency of the realized DDTX is within 4 efficiency points of the drain efficiency over more than 25 dB output power range, while its static power consumption is less than 191 mW (including SRAMs). These latter properties are of great interest to (future) mMIMO system implementations where power consumption in low-traffic situations is a serious concern.

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