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***Abstract*—In this paper, a novel bubble-shift super junction (SJ) MOSFET structure is proposed, and its main static electrical parameters and reverse recovery characteristics are simulated by TCAD software tool. By designing the P-pillar ion implantation windows with a certain offset, the bubble-shift SJ-MOSFET contains a curved pillar region in the upper half of the P-pillar. In the reverse recovery test of the proposed bubble-shift SJ-MOSFET, the peak reverse recovery current (I_{rrm}) is reduced from 16.04 A to 15.21 A, and the current drop rate (di/dt) is reduced from 1587 A/μs to 815 A/μs. Correspondingly, the proposed device achieves a better reverse recovery characteristic while sacrificing a small fraction of the drain-source breakdown voltage (BV) and drain-source special on-resistance ($R_{on,sp}$). Compared with the BV of 700 V and the $R_{on,sp}$ of 9 mΩ·cm^2 of the benchmark SJ-MOSFET. The proposed device has a BV of 650 V and a $R_{on,sp}$ of 12.4 mΩ·cm^2. Mechanistically, the non-uniform depletion of the curved P-pillar reduces the carrier extraction rate, thereby prolonging the reverse current drop time (t_f) and increasing the softness factor (S) of the bubble-shift SJ-MOSFET.**

Keywords—super junction, reverse recovery, P-pillar, bubble-shift, TCAD

I. Introduction

The super junction (SJ) power MOSFET is widely applied in white goods in the voltage range of 500-900 V because it breaks the silicon-limit between the drain-source breakdown voltage (BV) and drain-source specific on-resistance ($R_{on,sp}$) [1]. Compared with the conventional power VDMOS, the SJ-MOSFET has a heavier doped drift region, which brings a lower on-resistance (R_{on}) under the same breakdown voltage requirements. However, due to the particularity of the structure, the SJ-MOSFET is not only complicated to fabricate, but also possesses a large junction surface parasitic body diode consisting of the P/N-pillar regions. The intrinsic P-N junction body diode in the SJ-MOSFET exhibits a poor reverse recovery capability after freewheeling, especially giving rise to a large number of non-equilibrium carriers stored charge (Q_{rr}) and a snappy reverse recovery current change rate (di/dt), which limits its application in high-frequency circuits [2]. The drift region of the SJ-MOSFET is usually fabricated by using deep trench filling (DTF) and multilayer epitaxial deposition (MED) [3]. In contrast to the MED process, the DTF process built a more uniform N/P-pillar distribution, which gives it a better tradeoff relationship between BV and $R_{on,sp}$. However, the structural design capability and process adjustment capability of the MED process are more powerful.

In this paper, a novel structure of SJ-MOSFET with a curved P-pillar is constructed by MED process and investigated its reverse recovery capability by TCAD simulation software. The proposed device adopts the MED process, which implants Boron ions after each N-type epitaxial layer growth, and drives the Boron bubbles through the annealing process for overall connection, and finally forms the complete P-type pillar. Therefore, the MED process can design different Boron bubble distributions to build the P-pillar with different shapes, and this method is called bubble-shift method. In Section II, the device structure design parameters and bubble-shift scheme are presented. Meanwhile, the bubble-shift SJ-MOSFET is modeled by TCAD simulation software according MED process. Then, the device electrical performance simulation results and mechanism analysis are presented in Section III. Finally, the conclusions of the paper are summarized in Section IV.

II. Device Structure and Mechanism

A. Design of Device Structure

Fig. 1(a) and Fig. 1(b) show the cell cross sections of the benchmark SJ-MOSFET and the proposed bubble-shift SJ-MOSFET with a curved P-pillar, respectively. Table I lists the important structure parameters of the device cell used for simulation. The maximum offset of bubbles are limited to 0.7 μm because the cell-pitch is only 5.5 μm. For objective comparison, the two SJ-MOSFETs have the same 12 Boron bubbles. In Fig. 1(a), the ion implantation windows of each Boron bubble are in a straight line, so the P-pillar shape of the benchmark SJ-MOSFET is relatively straight after annealing. However, in Fig. 1(b), the ion implantation windows of the upper six-bubbles are shifted to both sides by 0.7 μm. Therefore, the upper half of the P-pillar is S-shaped in the proposed bubble-shift SJ-MOSFET, while the bottom half of the P-pillar is the same as the benchmark SJ-MOSFET. Apart from the shape of the P-pillar, other physical parameters are in same conditions. The main physics models used for process simulation of the TCAD include carrier mobility models (High Field Saturation and Doping Dependence), carrier recombination models (Auger and Shockley-Read-Hall) and effective intrinsic density model (OldSlotboom).

B. Reverse Recovery Mechanism

In the inductive load circuit applications, the intrinsic body diode consisting of the P-body and N-substrate in the SJ-MOSFET often serves as a freewheeling diode. When the

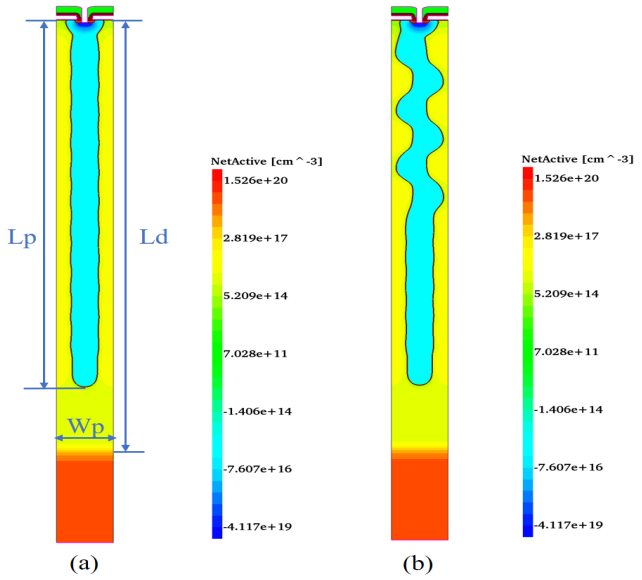

Fig. 1. The cell cross sections of (a) the benchmark SJ-MOSFFET and (b) bubble-shift SJ-MOSFET with 0.7 μm offset.

TABLE I. KEY PHYSICAL PARAMETERS USED FOR SIMULATION

Symbol	*Parameters*	*Values*
W_p	Cell pitch	5.5 μm
L_d	Length of the drift region	50.5 μm
L_p	Length of the P-pillar	42 μm
N_D	Phosphorus doping concentration	1×10^{16} cm^{-3}
N_A	Boron doping concentration	1×10^{16} cm^{-3}
P_{window}	Width of ion implantation window	0.55 μm

large junction surface PN body diode is in the conductive stage under the forward bias, a large number of non-equilibrium minority carriers are injected into each other between P/N-pillar. These carriers will be stored in the drift region and need to be extracted when the body diode transitions to the withstand voltage stage [4]. In the carrier extraction stage, the carrier exhaust rate influences the reverse current change rate di/dt and softness factor S [5], which depicts as

$$S=t_f/t_s \qquad (1)$$

where t_f is the reverse current drop time, and t_s is the carrier storage time. In the reverse current drop stage, a high di/dt will result in a high dv/dt, which will cause the circuit oscillation and damage the device.

III. SIMULATION RESULTS AND ANALYSIS

A. Static Electrical Characteristics

The Fig. 2 presents the tradeoff relationship between BV and $R_{on,sp}$ varies with the bubble offset increase. Firstly, the BV and $R_{on,sp}$ of the benchmark SJ-MOSFET are calibrated to 700 V and 9 mΩ • cm^2, respectively. Then, the offset of bubbles is increased in step of 0.1 μm, and the maximum offset is 0.7 μm in this experimental design. As shown in the BV change curve in Fig. 2, the BV decreases with the bubble offset increase in an acceptable range and remains stable above 650 V. Moreover, the $R_{on,sp}$ shows a clear increasing trend with the bubble offset increase. In detail, the SJ-MOSFET is a majority carrier device, which conducts by the

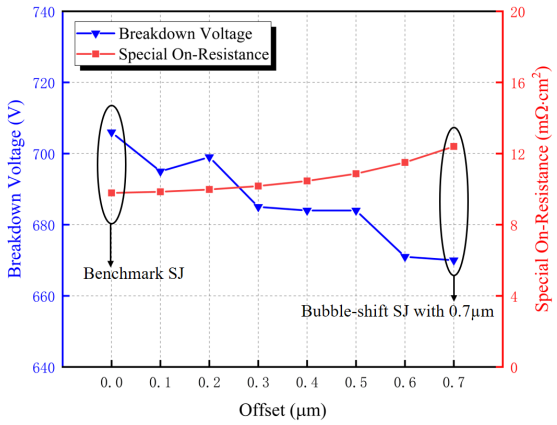

Fig. 2. Influence of bubble offset increase from 0~0.7 μm on BV and $R_{on,sp}$ for the SJ-MOSFET.

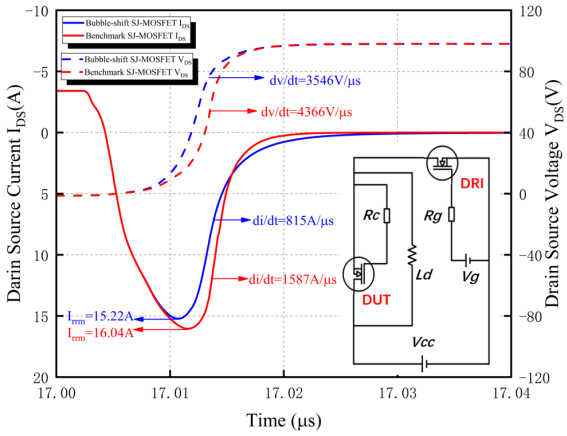

Fig. 3. The reverse recovery simulation circuit, reverse recovery current and voltage waveforms of the bubble-shift SJ-MOSFET and benchmark SJ-MOSFET.

electrons in the N-pillar region. At the same doping concentration, the curved P-pillar will compresses the current conduction path and increase resistance eventually.

B. Reverse Recovery Characteristics

The Fig. 3 presents the reverse recovery simulation circuit with V_{cc} = 100 V and R_g = R_c = 10 Ω. The gate voltage and load inductance are set to 10 V and 2 mH, respectively. DUT is the device under test, and DRI is the drive switch that controls the transition process of the SJ-MOSFET body diode from the forward conduction to withstand voltage stage [6]. In Fig. 3, it can be observed that the peak reverse recovery current (I_{rrm}) is 15.21 A of the bubble-shift SJ-MOSFET with 0.7 μm offset. Compared with the I_{rrm} (16.04 A) of the benchmark SJ-MOSFET, the I_{rrm} is effectively reduced by 5%. As for the reverse recovery current drop rate di/dt, the bubble-shift SJ-MOSFET presents a lower value of 815 A/μs compared with the benchmark SJ-MOSFET (1587 A/μs), and there is an optimization of 48%. At the same time, the dv/dt of the bubble-shift SJ-MOSFET is 3546 V/μs and is 18.7% lower than the benchmark SJ-MOSFET (4366 V/μs). These curve tendencies indicate that the proposed bubble-shift SJ-MOSFET is softer than the benchmark SJ-MOSFET device in the carrier sweep out

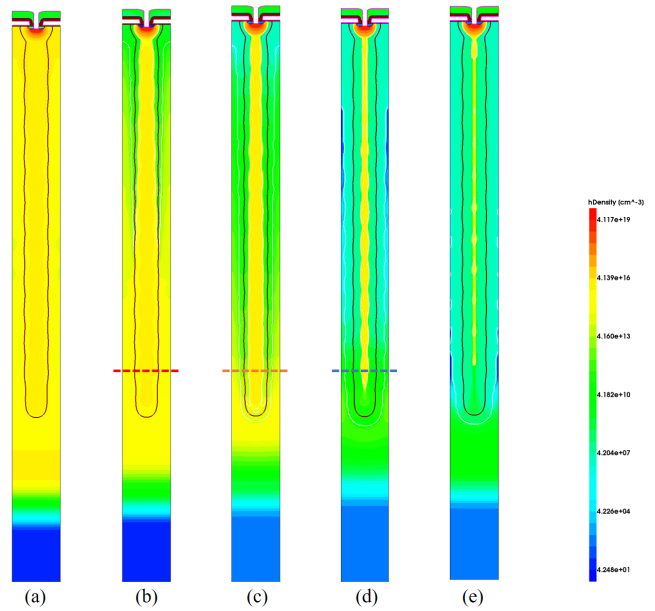

Fig. 4. Evolution of the hole density distribution in the benchmark SJ-MOSFET during the reverse recovery.

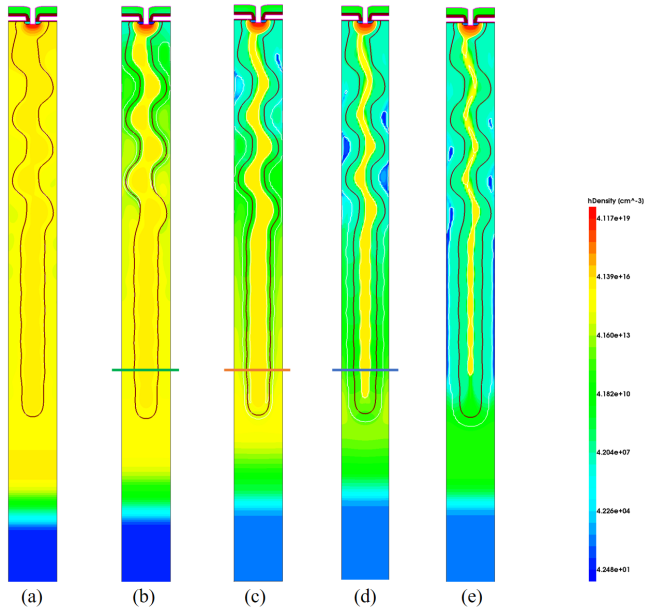

Fig. 5. Evolution of the hole density distribution in the bubble-shift SJ-MOSFET during the reverse recovery.

stage during the reverse recovery, which will reduce the device failure probability due to the current and voltage oscillations. Moreover, we calculate the softness factor S for the both devices. Compared with the benchmark SJ-MOSFET (S = 1.39), the bubble-shift SJ-MOSFET performs a better soft factor (S = 2.94) where has a 111% addition.

In order to further explore the optimization mechanism of reverse recovery, the Fig. 4 and Fig. 5 show the hole density distribution in the same time stage during the reverse recovery of the benchmark SJ-MOSFET and bubble-shift SJ-MOSFET, respectively. In Fig. 4(a) and Fig. 5(a), the body diode is in the forward conduction state, and a large number of hole carriers inject into the N-pillar region. In Fig. 4(b) and Fig. 5(b), the depletion region begins to construct and broaden, and the hole carriers are continuously sweep out from the N-drift region, and the SJ-MOSFET body diode

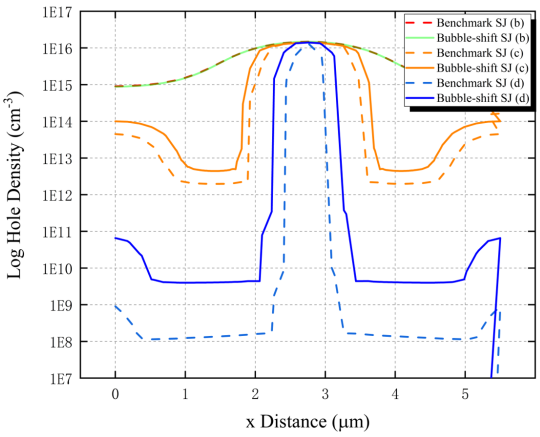

Fig. 6. Hole density variation in the x-direction of the benchmark SJ-MOSFET and bubble-shift SJ-MOSFET during the reverse recovery.

begin to withstand voltage. Furthermore, the hole carriers are also continuously depleted from the P-pillar, but there is a distinct difference of depletion rate of the two devices, as shown in the stage (c), (d), (e) of Fig. 4 and Fig. 5, respectively. Compared with the uniform and rapid depletion between the P and N pillar in the benchmark SJ-MOSFET, the carriers depletion rate is obviously slower in the bubble-shift SJ-MOSFET, especially some undepleted electron regions appear at the curved part of the P-pillar. These undepleted regions will be further depleted with the increase of the withstand voltage.

The Fig. 6 further shows the hole density variation in the x-direction in the stage (b), (c) and (d) of the benchmark SJ-MOSFET and bubble-shift SJ-MOSFET, respectively. In order to avoid the difference of non-uniform hole concentration distribution caused by the bubble-shift of the P pillar, we select the second bubble place where has the same straight P-pillar and hole density in the both devices to compare the hole density variation tendency. In stage (b), the hole density curves of the two devices almost overlap, indicating that the broadening of depletion region has not affected the carrier sweep out in this region. At this time, both the P-pillar and the N-pillar are filled with a large number of hole carriers. In stage (c), the depletion effect begins to sweep out hole carriers in this region, but it is obvious that the hole carrier density in the bubble-shift SJ-MOSFET is significantly higher than the benchmark SJ-MOSFET. In stage (d), most of the hole carriers are sweep out in the N-pillar of the both devices, but there are still a large number of undepleted hole carriers in the P-pillar, and the number of remaining holes in the bubble-shift SJ-MOSFET is significantly higher. According to the above phenomenon, there is a clear difference of extraction speed with hole carriers in the two devices during the withstand voltage stage, and the bubble-shift SJ -MOSFET has a lower carrier extraction rate. The curved P-pillar slows down the hole carriers sweep out rate and smooths the current change rate di/dt during the recovery current drop stage.

IV. Conclusions

In the design principle of the conventional SJ-MOSFET, although the drift region with the alternating P/N-pillar optimizes the internal electric field distribution of the device, constructs a parasitic body diode with a large junction

surface at the same time, resulting in a poor reverse recovery performance. To reduce the impact of this problem on devices performance, the bubble-shift SJ-MOSFET with a curved P-pillar fabricated by multilayer epitaxial deposition (MED) process is proposed and simulated. Its drain-source breakdown voltage (BV) and drain-source special on-resistance ($R_{on,sp}$) losses are within an acceptable range, but the reverse recovery indicators di/dt, dv/dt and softness factor (S) are enhanced with 48%, 18.7% and 111%, respectively. Furthermore, the optimization mechanism is discussed and explained through the hole carriers evolution distribution in different stages during the reverse recovery, which illustrates that the curved P-pillar slows down the carrier sweep out rate and smooths the di/dt during the reverse recovery current drop stage. Moreover, compared with the cell pitch of 5 μm in this paper, our works have a higher guiding significance in the optimization of device design with a wider cell pitch. In conclusion, the bubble-shift method achieved by changing the ion implantation windows can effectively optimize the reverse recovery capability of the SJ-MOSFET body diode.

V. Acknowledgment

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