Integrated Circuits for 3D High-Frame-Rate Intracardiac Echocardiography Probes

Hopf, Y.M.

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Dissertation

for the purpose of obtaining the degree of doctor
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chair of the Board for Doctorates
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by

Yannick Matthias HOPF

Master of Science in Electrical Engineering and Information Technology,
Technische Universität Darmstadt, Germany
born in Seligenstadt, Germany.

This dissertation has been approved by the promotors.

Composition of the doctoral committee:

Rector Magnificus,	chairperson
Dr. ir. M.A.P. Pertijs,	Delft University of Technology, promotor
Prof. dr. ir. N. de Jong,	Delft University of Technology, promotor

Independent Members:

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Dr. ir. P.J.A. Harpe,	Eindhoven University of Technology

Other Members:

Dr. ir. J.G. Bosch,	Erasmus University Medical Center

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To Lea and my Family

Contents

1

Introduction

1.1. Motivation & Background

1.1.1. Cardiovascular Conditions

In 2019, the World Health Organization (WHO) evaluated that cardiovascular diseases (CVDs) are the leading cause of death in the world, with a rising share as numbers further increased while deaths due to communicable diseases have been decreasing over the last two decades [1]. Cardiovascular diseases include a wide range of conditions in the vascular system and heart but the cause of death commonly is the acute event of a stroke or heart attack. These are usually caused by restricted blood flow to the brain or heart, e.g. due to cerebrovascular or coronary heart disease [2].

Next to lifestyle changes and medicinal treatment, cardiovascular interventions are an important tool in dealing with cardiovascular diseases [3]. These include heavily invasive procedures like heart transplantation, artificial heart operations, or coronary bypass surgery that require a complex open-chest intervention.

However, there are also less intrusive, minimally-invasive procedures that are applied to target specific conditions in the heart and vascular system. Balloon angioplasty uses a catheter to move through an artery and inflate a balloon at the place where a blockage has been identified. This can open the artery to increase the blood flow and a stent can be placed to prolong the effect [4]. Other examples

of the treatment of structural heart conditions include the transcatheter closure of a patent foramen ovale, atrial septal defect [5], or ventricular septal defect [6] and pulmonary [7] or mitral [8] valvuloplasty. Additionally, minimally invasive procedures can also be applied to target electrical heart defects that cause atrial fibrillation, the most common heart arrhythmia with a 33% increase over the last 20 years and a risk factor for having a stroke [9]. During this so-called electrophysiology with catheter ablation, an electrical map of the heart is obtained and afterwards faulty tissue is ablated to restore a regular heartbeat [10].

While not all cardiac interventions can be performed with minimally-invasive procedures, they have shown a reduced risk, can typically work on local anesthesia, and will see a rising share compared to traditional surgery [11].

1.1.2. Impact of Ultrasound Imaging

The use of minimally-invasive interventions in the heart requires that procedure guidance can move from direct vision, as predominantly used in open-chest surgery, to imaging tools. In the following, several medical imaging tools are discussed.

In 1895, x-rays were first discovered by Wilhelm Conrad Röntgen and used to observe the structure and function of the heart [12]. X-rays are a form of electromagnetic radiation with wavelengths between 0.01 to 10 nm and can generally pass through human tissue. An image is formed by recording the remaining radiation after passing through the body and thus displays the local density variation in the medium on a capturing screen [13]. Due to their high energy, x-rays belong to the class of ionizing radiation, meaning that they can harm human tissue, being able to cause cancer for prolonged exposure [14]. In current minimally-invasive procedures, x-rays are still frequently used during fluoroscopy to image the process inside the body [15]. Fluoroscopy generally works with the continuous application of radiation and its capturing on a fluorescing screen to provide real-time investigation and procedure guidance. Fig. 1.1(a) shows a typical setup with a table for the patient to lie on and the scanner above. While plain x-ray imaging and fluoroscopy generally suffer from superimposition in the depth of the image, x-rays can also be used in a computed tomography (CT) procedure to generate high-quality cross-sections of the body. During CT imaging, with a scanner as shown in Fig. 1.1(b), several acquisitions are obtained at different angles and combined to reconstruct the data of each voxel in the chosen plane [13].

Magnetic resonance imaging (MRI) is another popular tool in medical imaging

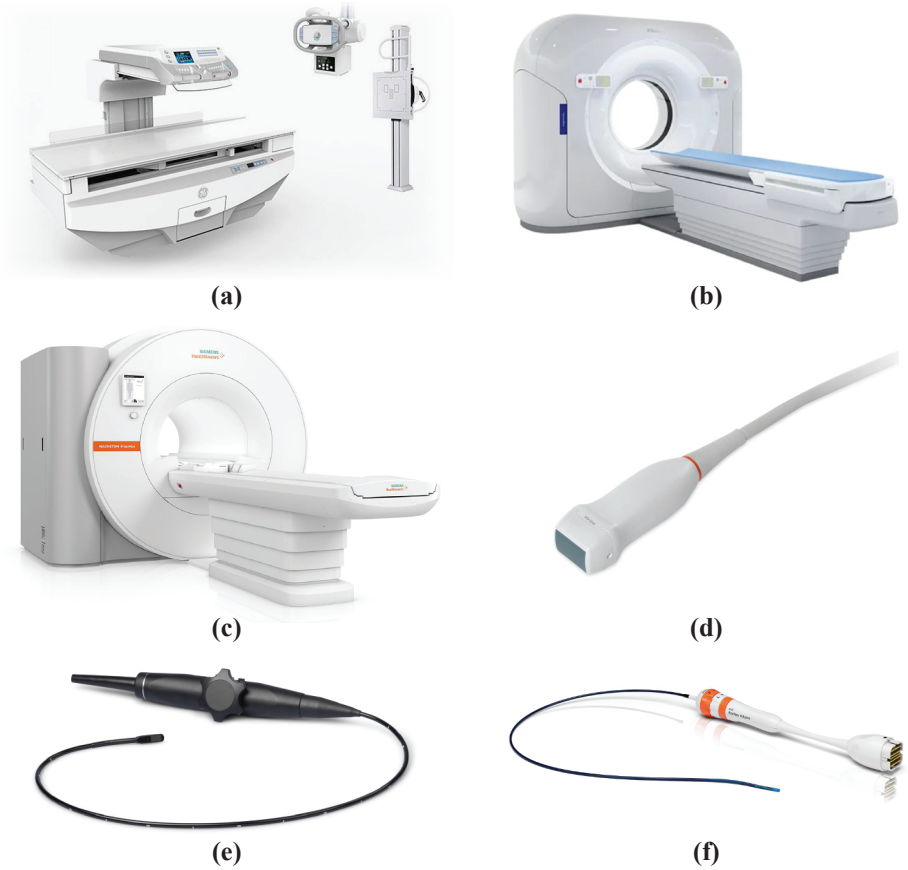

Figure 1.1: (a) Classical patient-side fluoroscopy system (Precision 600, GE Healthcare, USA); (b) CT scanner (CT 5000 Ingenuity, Philips, The Netherlands); (c) MRI scanner (MAGNETOM Free.Max, Siemens Healthineers, Germany); (d) Hand-held ultrasound probe (PM1-6A, Samsung, Seoul); (e) TEE probe (Adult 4D TEE Probe Premium, Oldefit Ultrasound, The Netherlands); (f) ICE catheter (ACUSON AcuNav Volume ICE Catheter, Siemens Healthineers, Germany)

and can produce high-resolution images without the application of ionizing radiation. An MRI scanner, such as displayed in Fig. 1.1(c), instead applies a strong magnetic field in a pulsed fashion to force the alignment of the hydrogen atoms in the body to it. Subsequently, it measures the radiofrequency waves emitted from the body when the atoms break alignment again. However, a major limitation to the application in minimally-invasive procedures is that the strong magnetic fields prevent imaging in the presence of implants, such as cardiac pacemakers, and restrict the use of tools with metallic components [13], [16].

Ultrasound imaging can in many cases present an alternative without this limitation and a low usage threshold. While ultrasound was already used for medical therapeutic purposes in the 1930s, it wasn't until 1947 that Karl Theo Dussik was able to create the first ultrasonically generated images. Since then, it has risen to be a common medical imaging tool [17]. Medical ultrasonic imaging is based on sound waves ranging from several MHz to several tens of MHz. A transducer transmits pressure waves and subsequently captures the returning echoes from the medium. No need for harmful ionizing radiation and the ability to generate high-resolution 3D images are clear advantages over fluoroscopy. Compared to CT and MRI, ultrasonic imaging requires less hardware and acquisition time, translating into a lower cost and better compatibility for active procedure guidance [18].

One of the most common applications of ultrasound for imaging the heart is in a transthoracic echocardiography (TTE) procedure with a cardiac probe similar to Fig. 1.1(d). During the investigation, the hand-held probe is positioned on the chest of the patient and acquisitions are obtained through the rib cage [19]. However, as the pressure wave attenuation is proportional to the traveled distance as well as, for heart tissue, approximately the ultrasound frequency, only relatively low frequencies can be applied [20]. This limits the obtained resolution and, combined with the limited acoustic window through the ribs and the need for a dedicated operator, makes TTE less favorable for the guidance of minimally-invasive interventions [21].

To enable higher image quality, special probes for use in transesophageal echocardiography (TEE) or intracardiac echocardiography (ICE) procedures were first developed in the 1960s [17]. TEE probes have a transducer array at the tip of a gastroscopic tube as shown in Fig. 1.1(e) and can get close to the heart by moving through the esophagus. This enables them to obtain high-resolution cardiac images while still providing substantial space for the integration at its tip and inside the tube for connection with an imaging system outside the body [22]. However, the application can lead to substantial discomfort and conscious sedation is frequently applied to diminish pain and anxiety at the cost of an increased number of potential complications [23]. This is avoided in the use of ICE probes, as displayed in Fig. 1.1(f), that can be introduced into the vascular system via a small incision in the groin area and then image from within the heart [24], [25]. Additionally, even higher spatial resolution can potentially be reached as the distance to the area of interest decreases further [26]. As the transducer is integrated at the tip of a catheter with a diameter of only around 3 mm diameter, integration

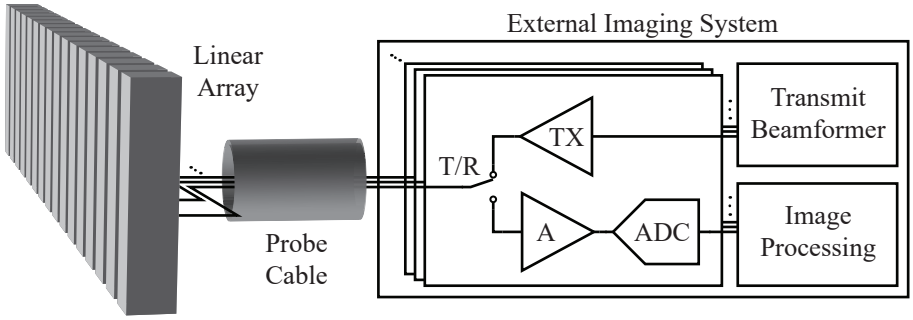

Figure 1.2: Conceptual drawing of a typical ultrasound imaging setup.

becomes more challenging though [27].

In this work, the possibilities for ultrasonic imaging with intracardiac echocardiography procedures and the design of probes are therefore further investigated.

1.1.3. Conventional Ultrasound Probes

Traditional ultrasound imaging setups include a passive transducer connected with a cable to an imaging system as conceptually shown in Fig. 1.2 [28]. The transducer is conventionally made from lead zirconate titanate (PZT) but transducer designs based on microelectromechanical systems (MEMS), such as capacitive micromachined ultrasonic transducers (CMUTs) [29] and piezoelectric micromachined ultrasonic transducers (PMUTs) [30], are also entering the field. While these can achieve comparable performance, are compatible with wafer-level volume production, and can be monolithically integrated with CMOS technologies, they do come with their own challenges. These include the requirement of a high-voltage transducer bias for CMUTs and high process variation for PMUTs [31], [32].

The transducer elements are then connected with individual micro-coaxial cables within the probe cable. In the imaging system, a transmit/receive (T/R) switch is connecting the element either to the transmit (TX) path for the excitation of ultrasound waves or to the receive (RX) path to capture the resulting echoes from the imaged medium. During TX, the imaging system applies electrical transmit patterns with voltage amplitudes in the order of 10s to 100s of volts to enable a sufficient signal-to-noise ratio (SNR) for image reconstruction. The transmission is controlled by a TX beamformer that applies delays to the signals of the individual elements in order to determine the direction and divergence of

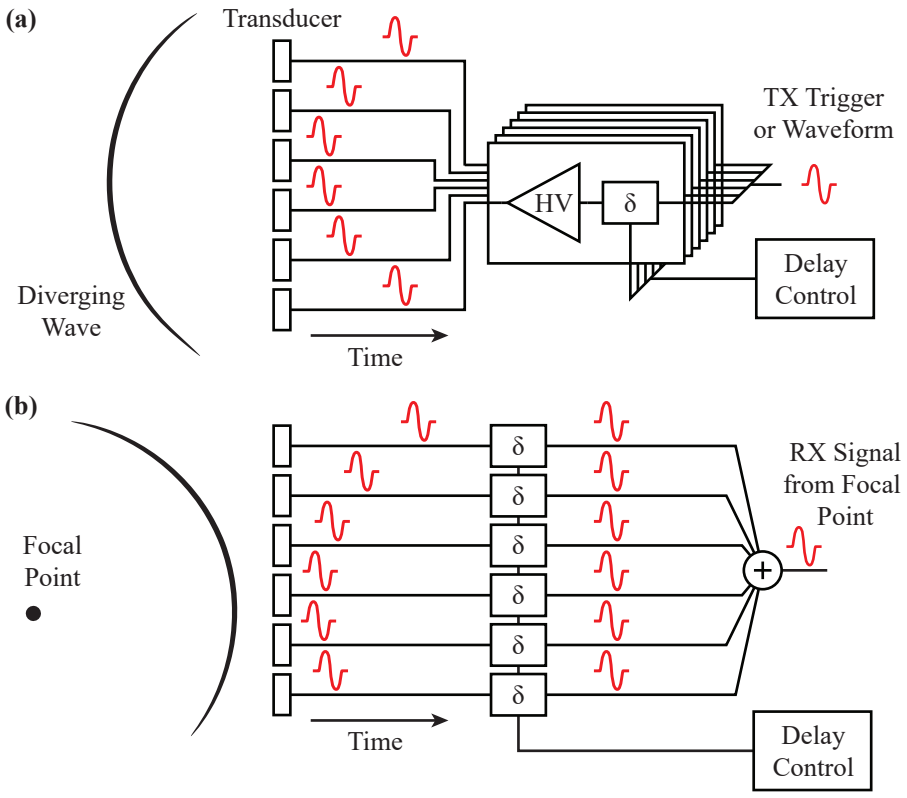

Figure 1.3: (a) Illustration of transmit beamforming of a diverging wave with six transducer elements; (b) Conceptual drawing of delay-and-sum beamforming.

the ultrasound beam as shown in Fig. 1.3(a).

During RX, on the other hand, returned signals down to the level of µVs have to be amplified before further processing is possible. Since the attenuation of the ultrasound waves is dependent on the distance traveled and thus the time passed after TX, the gain is commonly adjusted with time in a so-called time gain compensation (TGC). This can reduce the total dynamic range (DR) requirement, which can go beyond 100 dB, for the following system to the instantaneous DR of interest as shown in Fig. 1.4. The received signals are subsequently digitized at ideally 4 to 10 times the transducer center frequency [33] and fed to an image processing block. Fig. 1.3(b) conceptually illustrates how the information from each voxel is, in the simplest case, reconstructed by delay-and-sum (DAS) beamforming [28].

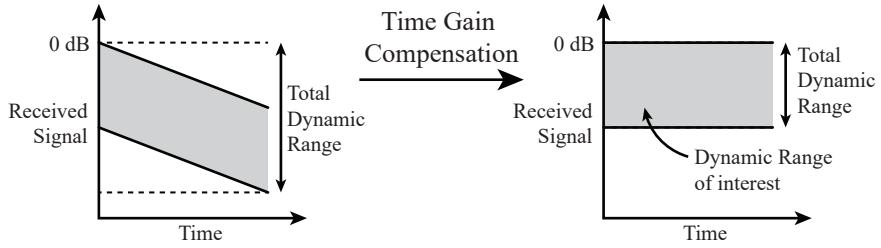

Figure 1.4: Illustration of how time gain compensation can reduce the total dynamic range of the received signal to only the range of interest.

A major drawback of the traditional probe configuration is that each transducer element requires an individual micro-coaxial cable for connection. This leads to a significant cost and complexity factor in the assembly but also adds substantial loading to the transducer, resulting in signal attenuation [34]. This is particularly concerning for CMUTs as they have a relatively high impedance [35] but also generally an issue when going to 3D imaging. While 2D plane imaging requires only a 1D array of transducer elements (the second dimension being the recorded time of arrival of the echoes) 3D imaging generally requires a 2D matrix of elements. As both azimuth and elevation direction have a pitch limitation to stay below an acceptable level of unwanted effects such as grating lobes, the elements of the 2D matrix are quite small and have a higher impedance [36].

The interconnect to the imaging system also becomes a bottleneck simply because of the limited diameter of the probe shaft. Hand-held devices shouldn't become too stiff to operate and catheter-based probes are fundamentally limited by the dimensions of the human body. Thinner cables can sometimes be applied but generally introduce stronger loading and more attenuation [37], [38]. The consequence is that there is a limit to the number of elements of any probe if implemented in the traditional way.

1.1.4. Integrated Circuits in Ultrasound Probes

Application-specific integrated circuits (ASICs) can be employed to alleviate the challenges of conventional ultrasound imagers and enable 3D imaging even with catheter-based probes. Fig. 1.5 gives an overview of a possible ultrasound system design with an ASIC at the tip of the probe [27], [39]. The loading of the transducer element is reduced by moving part of the electronics in front of the cable [40].

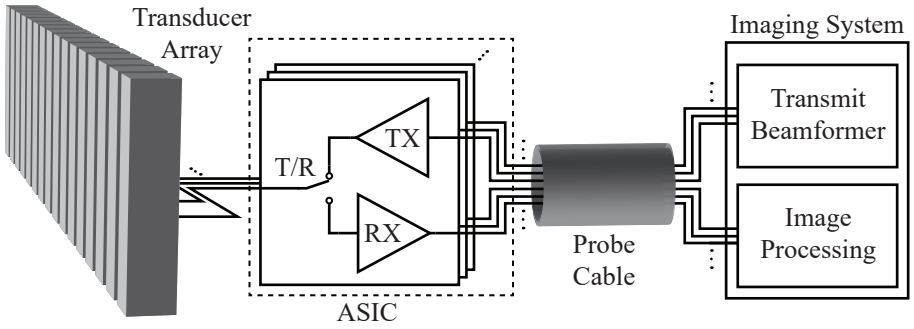

Figure 1.5: Example of an ultrasound system with ASIC inside the imaging probe.

This usually includes the T/R switch as well as TX- and RX-related circuitry. The transmitter can be implemented as high-voltage (HV) pulsers [41], [42] or also just as switches gating a high-voltage signal from the external system [43], [44]. The receiver typically at least features a low-noise amplifier (LNA) that can be tailored to the applied transducer [45]. A variable gain stage is often also applied to enable time gain compensation [32], [46]. Digitization with analog-to-digital converters (ADCs) can moreover be added to make the sensitive received signals more robust, allow digital data transmission, and facilitate upcoming signal processing techniques such as machine-learned data reduction [47], [48].

Another major opportunity provided by in-probe ASICs is cable-count reduction. It can enable 2D transducer arrays with a high element count for 3D imaging but also be applied to just reduce the cost of a cable assembly or reduce the stiffness of the probe [49], [50]. However, the cable count is actually higher to start with as each element in Fig. 1.5 theoretically requires a separate connection for TX and RX while this was shared for the probe without an ASIC. This can be more than compensated by the use of circuit design techniques though.

In TX, it has been shown that, despite a large number of elements, beamforming is possible with only a few cables with the implementation of an on-chip beamformer. This can be configured with an efficient serial link into local registers [51], [52] or a compact shift register [39], [53]. Another possibility to reduce the hardware, albeit with restricted TX beamforming capabilities, is the use of a row/column approach to generate transmit patterns [43], [54], [55].

In RX, the channel-count reduction can't be as efficient due to the larger output bandwidth but significant factors have still been achieved with multiplexing

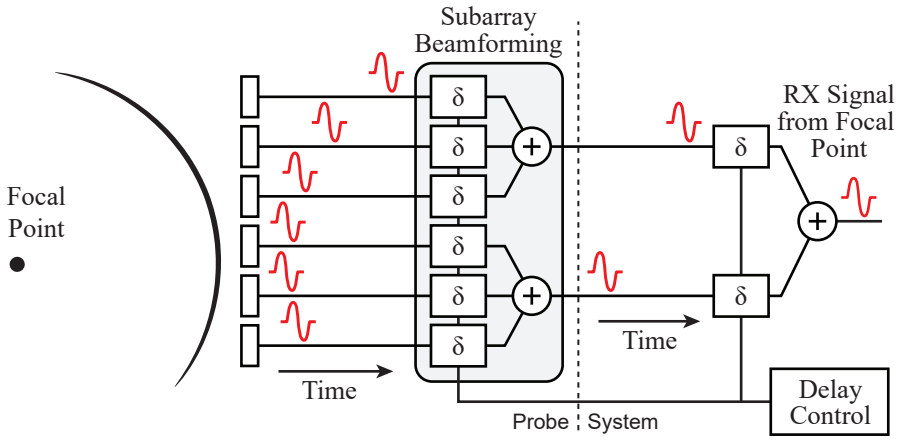

Figure 1.6: Conceptual overview of subarray beamforming operation in the image reconstruction.

and subarray beamforming[1]. Analog output signal multiplexing has been shown in the time [56], [57] and frequency domain [58]. Reduction rates in the order of 10x could be achieved but the sensitive analog signals suffer from bandwidth limitation and channel-to-channel crosstalk on the small cables [59]. This can be addressed by moving to digital time-division multiplexing (TDM) with better tolerance to cross-talk, interference, and noise [60]. Another beneficial feature of multiplexing is that it is generally compatible with subarray beamforming. Subarray beamforming does receive beamforming of subarrays of the transducer matrix already in the probe instead of completely in the external imaging system as shown in Fig. 1.6 [61]. The process is also based on DAS operations with delay configurations to pre-steer the receive beam and can reduce the number of channels by only transmitting the combined signal. The combination between TDM and μBF has been shown in digital beamforming of element-level signals [62]–[64] and analog beamforming followed by digitization and TDM [65]–[67]. This has shown channel-count reductions of up to 36x and is thus of particular interest for the following discussion on the design of ICE probes with cable diameters in the order of 3 mm [27].

[1]Also known as micro-beamforming (μBF) subaperture beamforming, or subaperture processing (SAP).

1

1.2. Intracardiac Echocardiography Probes

1.2.1. Developments

The first recorded intracardiac ultrasound experiments go back to 1956, not even ten years after the first general ultrasound imaging [17], [68]. The early study already applied catheters with a single-element ultrasound tip and saw the development of rotating and multi-element probes shortly after, in the mid-1960s [69]. This was followed by the first 32-element, 9-Fr catheter which could obtain real-time, two-dimensional cross-sections from within the heart in 1971 [70]. However, the transducer elements were still assembled around the catheter tip and it took until 1996 before the first 128-element, side-looking phased-array ICE catheter was reported [71]. Since then, several phased-array transducers for intracardiac imaging, such as the AcuNav catheter from Siemens/Biosense Webster, ViewFlex from St. Jude Medical, and SOUNDSTAR from Biosense Webster, have become commercially available and are being used in clinical procedures [34], [72]. All of these are 64-element, side-looking probes ranging from 8 to 10 Fr in size but are also all still limiting the field of view to 2D cross-sections of the heart.

As 3D visualization is quite interesting in the guidance of minimally-invasive procedures [15], it was initially explored in research how 3D images could be obtained from manual rotation of a 1D array [73]. The method was able to successfully reconstruct 3D images of the heart but not in real-time, given a mapping period in the order of 20 minutes. This could be alleviated with a probe that replaced the manual rotation with a rotating 1D transducer array at the tip [74]. The design achieved real-time volume acquisition but was still limited by a frame rate of 7 volumes/s at an opening angle of 40°. In the device described in [75], another approach was taken by applying a twisted 1D array instead of device rotation. While this can only provide a limited opening angle of 22°, there is no inherent limitation to the frame rate associated with it.

To enable 3D intracardiac ultrasound imaging without the deficiencies of 1D transducer arrays, 2D matrices have been investigated in parallel[2]. The first reported design goes back to 2001 and featured 64 active channels individually wired through the catheter [77]. More designs with up to 512 elements followed but saw a rising complexity in the interconnect with only limited image quality [37], [38].

[2]In the class of forward-looking probes [42], [76], 3D imaging has also been shown but is not further discussed as they typically serve in close conjunction with therapy catheters and have limited imaging capabilities.

It wasn't until the co-integration with electronics at the tip of the catheter to reduce the cable count and buffer the received signals that the first real-time 3D ICE probe was shown by Wildes *et al.* in 2016 [27]. It featured a transducer matrix of 60×14 elements in a 10-Fr catheter, could cover a field of view of 90°×90°×8 cm, and could image at a rate of up to 50 volumes/s. Since then, several commercial parties, such as Oldelft Ultrasound with its 4D ICE Transducer, Siemens Healthineers with its ACUSON AcuNav Volume ICE Catheter, and Philips with its VeriSight Pro, have announced their new 3D ICE probes.

The following section gives an overview of the different challenges in the design of these 3D probes and also presents opportunities for future ICE catheters.

1.2.2. Challenges & Opportunities

Something to generally take into account is the acceptable probe temperature and thus power consumption. While conventional, passive probes typically only face the heating from thermal losses in the transduction process, the new generation of probes with co-integrated ASICs also have to deal with the additional power consumption of the electronics. There is no clearly defined limit to the power an intracardiac catheter may dissipate in order to gain clearance but requirements for a maximum surface temperature of 43°C have been formulated by the US Food and Drug Administration (FDA) [78], [79]. This absolute value poses a tighter requirement on the power consumption per element for 3D probes with 2D transducers compared to phased array catheters for 2D imaging. While the implications aren't as severe at the frontend as the smaller elements also reduce the power per element in TX and ease the noise requirement per channel in RX, circuit overhead and especially the possibly higher output data bandwidth need to be considered [46], [65]. Ultimately, it is quite complicated to derive a power consumption limit from the temperature regulation as the translation depends heavily on the applied environment, thermal design of the probe, and imaging conditions. Even a small blood flow can for example already lead to a significant temperature distribution and short burst acquisitions at high power consumption can only result in a minor temperature increase due to the low-pass characteristic of the mechanical structure [80]. The general approach in this thesis is therefore to minimize power consumption as much as possible.

Similar to the power overhead when progressing from 2D to 3D imaging catheters, there is also a relative increase in the need for circuit area in the transition which

can result in a significant challenge. The circuitry of each channel or unit cell should ideally be matched to the pitch of the transducer elements to ease the system design and enable scalability to larger apertures [81]. The pitch is typically determined by the transmission frequency in order to minimize the effect of grating lobes that are at angles

$$\Theta_g = \pm arcsin\Big(\frac{m\lambda}{p}\Big) \tag{1.1}$$

where Θ_g is the angle of the grating lobe for m $\neq$ 0, p is the pitch and λ is the wavelength of the ultrasound wave. The maximum pitch, in order to not have grating lobes in the image, thus is half of the wavelength and commonly in the order of 100 µm to 200 µm for ICE probes [20]. This forms a tough requirement for the circuitry and has led to many designs that either couldn't match the electronics to the transducer pitch [63], [67], sized the elements substantially larger than half of the wavelength [32], [62] or didn't implement all of the desirable features [65], [82]. Particularly the transmit-related circuits are very area-intense as the application of high voltages to excite sufficiently strong pressure waves requires the use of transistors with large isolation structures [39]. As a consequence, one of the main goals of this work is to explore architectures with a high area efficiency and optimize blocks accordingly.

Next to the limited area, the interconnect to the imaging system becomes a major concern with the larger number of elements in 2D transducer matrices and the small intracardiac catheters in the order of 10 Fr [37], [38]. Other than with power and area, there is no inherent scaling factor with the element size but a linear increase of necessary connection bandwidth with the number of elements if the signal is to be used for image reconstruction in the external unit unharmed. As designs are often implemented in mature technologies to make use of their HV transistor options and apply thin micro-coaxial cables, both imposing severe bandwidth limitations, an unfeasible number of cables would be required to transfer all the generated data in real-time [43], [46].

To cope with the discussed power, area, and interconnect requirements, two main methods have previously been shown. The first is to not implement all circuitry at the element level and allocate a fixed channel in the probe cable to each element. Instead, the elements are multiplexed over the course of multiple pulse-echo cycles [39], [50]. This is a direct relief to all discussed aspects but trades with a reduced frame rate. The second is subarray beamforming as described in section 1.1.4 and also applied in imaging catheters such as the first full 3D ICE

probe from Wildes *et al.* [27]. While compared to multiplexing there is more overhead in the delay and summation of element-level signals, this is also very effective in the reduction of output data bandwidth, can still reduce the required circuitry significantly, and theoretically reads out all the elements in real-time [81]. However, it does not provide the raw data of the full array and introduces focusing errors that result in increased grating and side lobe levels as well as broadening of the main beam. Narrower transmit beams can be used to mitigate these effects but require more acquisitions per volume, again limiting the frame rate [83].

These inherent trade-offs with frame rate are why one aspect that has not yet been reported in conjunction with high-image-quality 3D intracardiac probes as introduced in section 1.2.1 is high frame rate. A high frame rate is interesting to record phenomena with very short time windows, such as electromechanical or shear waves, in the heart. Their investigation can lead to additional diagnostic potential by e.g. being able to detect abnormal electrical activation patterns or create a stiffness map of the heart. However, they travel at speeds in the order of 1 m/s along the heart tissue and require a frame rate of at least 1000 volumes/s to be captured [84], [85].

Consequently, techniques to address the identified main challenges of power consumption, circuit area, and cable-count reduction without excessively limiting the frame rate are being investigated.

1.3. Thesis Organization

The aim of this work is to explore opportunities in intracardiac ultrasound probes and arrive at a concept for a next-generation imaging catheter. This starts with the discussion of a desired transducer array design as well as an imaging scheme to enable the targeted acquisition modes. The focus is thereafter laid on innovations in the ASIC architecture and its circuit-level building blocks to address current challenges in the field. The thesis is organized in six chapters to present different aspects in logical units from the idea to the evaluation. The division of the chapters is as follows.

Chapter 2 discusses the value of a high-frame-rate 3D ICE probe design and proposes an imaging scheme to enable it. The scheme employs 1D subarray beamforming with seven steps in the elevation direction to achieve a high frame rate while reducing the channel count sufficiently for realization in a 10-Fr catheter. It

is presented how the transmit beam divergence and center frequency are optimized based on the required image quality for electromechanical wave imaging (EWI). Numerical simulation results show that a set of 7 fan-shaped transmission beams can provide a frame rate of 1000 volumes/s and a sufficient spatial resolution to visualize the electromechanical wave propagation on a large 3D surface.

Chapter 3 introduces a compact HV transmit circuit for dense 2D transducer arrays used in 3D ultrasonic imaging systems. The chapter shows how stringent area requirements can be addressed by a unipolar pulser with an embedded transmit/receive switch. Combined with a capacitive HV level shifter, the circuit forms the ultrasonic HV transmitter with the lowest reported HV transistor count and area. It is shown how the novel level shifter can reduce sensitivity to transients on the HV supply caused by pulsing and how hardware sharing can further reduce the active circuit area. The description of a prototype of 8×9 elements and its characterization is included to demonstrate the functionality and performance.

Chapter 4 presents an ASIC for 3D, high-frame-rate ultrasound imaging probes. The design is the first to combine element-level, high-voltage transmitters and analog frontends, subarray beamforming, and in-probe digitization in a scalable fashion for catheter-based probes. The integration challenge is met by a hybrid analog-to-digital converter, combining an efficient charge-sharing successive-approximation-register (SAR) first stage and a compact single-slope (SS) second stage. Merging with the subarray beamformer and additional hardware-sharing between neighboring channels ultimately leads to the lowest reported area and power consumption across miniature ultrasound probe ADCs. Electrical, acoustic, and imaging experiments are shown to verify the design's functionality at up to 1000 volumes/s.

Chapter 5 discusses a second-generation ASIC for catheter-based high-frame-rate 3D ultrasound imaging probes. It presents a method to reduce the number of cables in the catheter while maintaining a small footprint per element by realizing transmit beamforming on the chip with a combination of a shift register (SR) and a row/column (R/C) approach. To explore an additional cable-count reduction in the receiver part of the design, a channel with a combination of time-division multiplexing, subarray beamforming, and 4-level pulse amplitude modulation (PAM-4) data transmission is also included. This achieves an 18-fold total cable-count reduction and minimizes the power consumption in the catheter by a load modulation (LM) cable driver. The functionality and performance are evaluated in the characterization of a prototype of 16×18 transducer elements.

Chapter 6 concludes the thesis by summarizing the main findings and presenting suggestions for future research.

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2

Imaging scheme for 3D high-frame-rate ICE

This chapter is based on the publication "Imaging Scheme for 3-D High Frame Rate Intracardiac Echography: A Simulation Study" in IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, vol. 69, no. 10, pp. 2862-2874, Oct. 2022.

2.1. Introduction

2.1.1. Clinical Background

The heart pumps blood with a rhythm determined by a group of pacemaking cells in the sinoatrial node. These cells generate an action potential that depolarizes cardiomyocytes. This action potential triggers the adjacent cells and propagates along the cardiac wall to generate global contraction. The conduction properties of cardiomyocytes and electrical pathways can be changed by normal aging or certain diseases which lead to various types of arrhythmias. Atrial fibrillation (AF) is the most common cardiac arrhythmia and is the major cardiac precursor of stroke [1]. AF can be treated by RF ablation. A high-resolution 3D anatomical mapping of electrical activity is required for localizing sources generating AF to

plan the ablation procedure [2], [3]. A key feature of atrial fibrillation is its irregularity in time and space. Because the patterns of atrial activation change on a beat-to-beat basis, a series of consecutive activation maps are needed to cover the spatiotemporal variation in activation [4]. Intracardiac electro-anatomical mapping is widely exploited to generate a 3D surface map of atrial electrical activity [5].

2.1.2. Electromechanical Wave Imaging

Electrical excitation of cardiomyocytes is followed by a transient contraction after about 20-40 ms [6]. The electrical excitation is passed to neighboring cells and propagates along the atrial wall as a reaction-diffusion wave with a velocity of 0.5-2 m/s [7]. A high correlation between electrical and resulting mechanical activations has been reported in several studies [8]–[11] and this activation propagates as a wave-like phenomenon over the atrial wall: the electromechanical wave (EW). Electromechanical wave imaging (EWI) was introduced and has been developed by the group of Konofagou [7], [12]–[19] as a non-invasive ultrasound-based imaging method to map the electro-mechanical activations in the heart. Recent studies demonstrated a high correlation between the cardiac electrical activity and its consequent electromechanical wave for healthy and arrhythmic cases in a simulation study [16], in the left ventricular wall [17], [18], atrial wall [15], and also in the walls of all four chambers [20].

Electromechanical wave imaging is accomplished in a two-stage process on ultrasound data [12]–[15]. In the first stage, tissue strain is estimated, commonly by a cross-correlation technique, along the axial direction on consecutive RF signals which are acquired at a motion-estimation rate (500 - 2000 Hz) [19]. In the second stage, electromechanical wave onset is estimated by measuring the time at which the axial incremental strain departs from or crosses zero at a given pixel. We intend to image the propagation of the EW wavefront with a spatiotemporal resolution suitable for the identification of local electrophysiological phenomena. Since the EW velocities are in the order of 0.5 - 2 m/s and the desired spatial resolution is in the order of millimeters, we aim at a volume rate of 1,000 Hz and a lateral resolution of 2 to 5 mm.

Current electromechanical wave imaging can provide single-beat 2D maps of the electromechanical wavefront (i.e. a cross-sectional image with activation times) with a lateral resolution of < 5 mm. Since the electromechanical waves propagate

throughout the entire heart, volumetric imaging is desirable to fully visualize their patterns. In previous studies, several 2D images were acquired and processed separately. Then, a pseudo-3D map was generated by combining these 2D maps through electrocardiogram (ECG) gating [20] and spatial interpolation. Recently, Grondin *et al.* used a transthoracic matrix transducer to achieve 3D EWI of the entire heart from the apical view [21]. The narrow intercostal space and channel count limitations restricted their transducer size to 9.6 mm × 9.6 mm. In consequence, the lateral resolution was limited, to 5.8 mm at 40 mm. For the atria which are located much deeper ($>$ 10 cm) the lateral resolution will be lower. It would be interesting to see if a higher resolution can improve strain mapping and reduce local inaccuracies in the electromechanical wave patterns in the atria.

2.1.3. High-Frame-Rate 3D Intracardiac Echocardiography

Using an intracardiac echocardiography (ICE) transducer can drastically reduce the required imaging depth for atrial EWI compared to the transthoracic apical view. Moreover, the possibility of using a higher central frequency compared to transthoracic transducers allows a higher spatial resolution in the atrial regions. Nowadays, ICE is widely exploited for RF ablation procedures to guide electrophysiologists in septal puncture and to navigate the ablation catheter. However, this is limited to low-frame-rate 2D-ICE. Several 3D-ICE designs have been proposed [22]–[24], but these are not capable of imaging at high frame rates. A high-frame-rate 3D ICE probe, in addition to delivering at least the functionality of conventional 2D ICE, could provide a single-beat 3D electromechanical wave map. However, high-frame-rate 3D ultrasound imaging introduces several challenges, including handling a high data rate generated by a large number of elements. Moreover, a high volume rate allows just a few transmissions to illuminate the total volume, so a diverging wave transmission scheme is required. Possibilities for compounding are limited, and thus SNR will be relatively low [25]. Furthermore, an intracardiac catheter imposes additional constraints on the transducer size, cable count, and power dissipation. ICE catheters typically have diameters in the order of 3 mm [22] and need to accommodate the entire imaging matrix as well as associated electronics at the tip as well as all interconnect in the shaft. Therefore, data reduction and an educated choice of design tradeoffs are crucial for high-frame-rate 3D ICE.

2.1.4. Data Rate Reduction by Micro-Beamforming

Micro-beamforming is a well-established method to reduce the channel count while preserving the image quality and SNR for volumetric imaging [26], [27]. In this method, element signals in a sub-aperture are mutually delayed and summed to form a single micro-beamformed signal from a predefined –steered– direction. The entire region of interest can thus be imaged by steering the sub-apertures to a sequence of different directions in, potentially, both azimuth and elevation, and implementing a parallel beamforming technique at the back-end system [28]–[30]. Since the final beamforming is based on the received data from sub-apertures with a relatively large effective pitch, grating lobes can occur. Using relatively narrow transmit beams that are steered to the pre-steering directions can reduce the grating lobe artifacts. Hence, a significant number of such narrow beams should be utilized to preserve the image quality [26]. Thus, increasing the number of elements per sub-aperture reduces the channel count but also reduces the achievable volume rate or field of view.

Wildes *et al.* developed a 2D transducer consisting of 60 × 14 elements with application-specific integrated electronics for volumetric intracardiac echocardiography based on a 10-Fr (3.3 mm) catheter [22]. A 2D micro-beamforming approach was used to reduce the total receive channel count to 48 (along with power, transmit, and auxiliary signals leading to a total of 88 connections). Their method provided an imaging sector of 90° × 60° × 8 cm with a spatial resolution of 1.7 mm × 4.9 mm (azimuth × elevation) at a depth of 50 mm. They concluded that the achieved spatial resolution was sufficient for atrial imaging. To suppress the grating lobes formed by micro-beamforming, narrow beams were used in transmission, which limited the frame rate to 30 vol/s [22].

Implementing a 1D (i.e. a 1xN sub-aperture) rather than a 2D micro-beamformer introduces the grating lobes only in the direction in which the micro-beamforming is implemented. Therefore, the transmit beams need to be narrow only in the corresponding direction. Consequently, 1D micro-beamforming could provide a relatively high volume rate 3D imaging by employing a set of fan-shaped diverging transmit beams that are narrow in the micro-beamforming direction and wide in the perpendicular direction, see Fig. 2.1. These asymmetric fan-shaped beams can cover a large volume of interest with a limited number of transmissions. These fan-shaped beams can be generated by a dual virtual source similar to the method proposed by Chen *et al.* [31] or a single virtual source behind a rectangular transducer as illustrated in Fig. 2.1(b). Since a dual virtual source approach generates

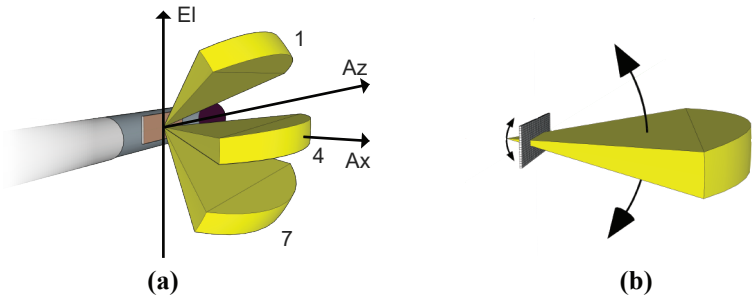

Figure 2.1: (a) A schematic representation of the proposed side-looking transducer mounted in an intracardiac catheter. Azimuth (Az), elevation (El), and axial (Ax) directions are indicated on the corresponding axes. A set of 3 out of 7 fan-shaped beams steered to different directions in elevation is shown to illustrate the transmit scheme. (b) A fan-shaped transmit beam is generated from a virtual source behind the transducer.

a curved transmit fan beam, it is less appropriate to be combined with a micro-beamforming approach. Therefore, we use a single virtual source approach in this study.

The size of the 1D micro-beamformer should be chosen such that the needed reduction in channel count is achieved while grating lobe levels are kept sufficiently low. In the design of the high-frame-rate 3D ICE, many trade-offs need to be made to realize an imaging scheme that satisfies the requirements for EWI while remaining within the constraints on transducer size and cable count, resulting from the small catheter size. Furthermore, the elements will be mounted on a pitch-matched application-specific integrated circuit (ASIC) containing all the required electronics, including high-voltage pulsers, low-noise amplifiers, time-gain compensation circuits, analog-to-digital converters (ADCs), and micro-beamformers, which are necessary to realize the proposed method [27], [32], [33]. The minimum pitch of the transducer elements is limited to 160 µm × 160 µm by the area required for the designed electronics.

In this study, we did not consider electronic noise and ultrasonic attenuation in the simulations, since we are assuming they are not limiting factors on the clutter and PSF image quality parameters we are studying here. They have been considered in the electronics design procedure [33] to achieve the desired imaging depth. Although these circuit design choices put some limits on the transducer layout and the imaging scheme as mentioned in the introduction and methods section, fully describing these choices is out of the scope of this manuscript.

2.1.5. 3D ICE Imaging Scheme Design

In this study, we develop a novel imaging scheme for high-frame-rate 3D ultrasound imaging with a matrix intracardiac catheter as sketched in Section 2.1.4, and gear the transducer design and imaging scheme towards intracardiac electromechanical wave imaging. The main goal is to enable volumetric imaging with a sufficient frame rate and image quality for electromechanical wave imaging while reducing the data rate to realistic values. The proposed method consists of implementing 1D micro-beamforming in the elevation direction to reduce the data rate. By combining this with the transmission of fan-shaped beams, a high frame rate is enabled while grating lobes in the elevation direction are suppressed. The proposed method achieves a further reduction of the grating lobe artifacts and improved CNR by implementing angular-weighted coherent compounding. We will discuss the decision on critical imaging scheme parameters (transmit frequency, micro-beamformer size, and transmit beam divergence) to achieve the desired channel count reduction while providing a sufficient frame rate and image quality for EWI. Finally, we evaluate the proposed imaging scheme in a series of simulations. The novelty of this work lies in an imaging scheme designed for dedicated integrated circuitry to realize high-frame-rate 3D ICE suitable for EWI.

2.2. Materials and Methods

2.2.1. Imaging Scheme Design: Parameters

We strive for a 3D ICE design with a frame rate of 1000 Hz, imaging depth of 10 cm, opening angle of 70° by 70°, and lateral resolution of 5 mm to be able to realize 3D EWI of the left atrium from the right atrium.

For a depth of 10 cm, the pulse repetition frequency (PRF) is limited to 7.7 kHz by the round-trip travel time of the ultrasound waves assuming a speed of sound of 1540 m/s. Therefore, a maximum number of 7 transmissions is available to acquire the entire region of interest, and we will always use this number of transmissions in our scheme.

We base the design of the matrix transducer on a 10-Fr intracardiac catheter, which limits the transducer size to 3 mm in elevation direction (Fig. 2.1(a) and the number of cables to a maximum of 100 [22], [34]. The aperture of the matrix array is rectangular, with the shortest axis perpendicular to the ICE probe shaft.

We consider square elements with a pitch of 160 µm, imposed by the area needed for the pitch-matched application-specific electronics [32]. Choosing such a large pitch (50% to 80% of the wavelength for the assumed frequency range of 5 to 8 MHz) introduces grating lobes in image reconstruction and also secondary waves in diverging wave transmission. To counteract these, we optimize the central frequency in the given range to suppress the secondary waves. In addition, an angular weighting function is applied to a conventional delay-and-sum to reduce the grating lobes. Based on the chosen pitch and catheter size constraints we consider a matrix array of 18×64 elements.

The imaging scheme consisting of steered fan-shaped diverging transmit beams will be used with 1D micro-beamforming in elevation direction and acquisition of all element-level signals in the azimuthal direction. Furthermore, angular weighted coherent compounding will be used to reduce grating lobe levels. Transducer size, pitch, number of transmissions, and imaging depth are fixed in this study, whereas the other features are optimized in a simulation study.

2.2.2. Steerable Fan-Shaped Transmit Beam

A single virtual source was used to generate the desired fan-shaped beam. In this approach, the beam divergence in azimuth and elevation are not independent. First, we determined the virtual source location based on the transducer size and desired beam divergence in the elevational direction, and then the effective transducer size in azimuth was determined to achieve the required beam divergence in that direction (see appendix I).

2.2.3. Angular Weighted Averaging

A voxel-based delay-and-sum is proposed to reconstruct an intermediate full volumetric image corresponding to each transmission. Since only a narrow region is insonified in elevation direction for each transmission, reconstructing regions far from this transmission direction only adds noise to intermediate images. In addition, the receive beam profile contains strong grating lobes at directions corresponding to the large effective pitch associated with the micro-beamformer size [26]. Hence, the final volumetric image is obtained by applying angular weighting functions to the intermediate images in order to suppress the noise and grating

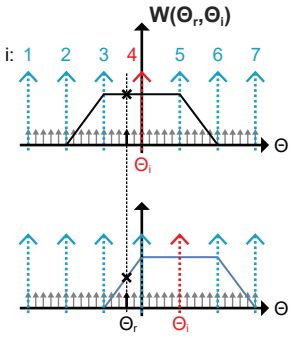

Figure 2.2: Applied weights $W(\Theta_r,\Theta_i)$ as a function of the reconstruction elevation direction Θ_r for different transmit beams. Blue arrows show all transmission directions and the red arrow shows the current transmission direction with its corresponding angular weighting function. Black arrows show the reconstruction directions and the bold black arrow shows an example of receive line with its corresponding weights (black cross) when the transmit direction is Θ_i.

lobes in non-insonified regions and also improve the image quality by coherent compounding of overlapping regions using

$$I(R,\Theta_r,\varphi)=\sum_{i=1}^{7}W(\Theta_r,\Theta_i)\sum_{m=1}^{N_{\mu BF}}\sum_{n=1}^{N_{AZ}}S_{m,n}(t-\sigma_i-\sigma_{m,n}) \tag{2.1}$$

where $I(R, \Theta_r, \varphi)$ is a reconstructed RF sample in a spherical coordinate system, $W(\Theta_r,\Theta_i)$ is the weighting function (as illustrated in Fig. 2.2) corresponding to the transmit direction Θ_i, $S_{m,n}$ is the micro-beamformed signal of a subgroup at elevation position m and azimuthal position n in the transducer array, $\sigma_i(R, \Theta_r, \varphi)$ is transmit delay, $\sigma_{m,n}(R, \Theta_r, \varphi)$ is receive delay and Θ_i is transmit/pre-steering direction.

Fig. 2.2 shows the angular weights as a function of the reconstruction line direction for different transmission directions. To avoid abrupt changes in image intensity, the angular weights have some overlap with their neighboring transmissions [33].

2.2.4. Simulation Setup

The simulation study consists of three steps. First, the azimuthal beam divergence and central frequency in a range of 20° - 45° and 5 - 8 MHz respectively are mutually optimized to provide an acceptable trade-off among the imaging opening angle,

Table 2.1: Imaging parameters

Parameters	Value
Transducer size	2.88 mm x 10.24 mm
Pitch	160 µm x 160 µm
Kerf	20 µm
Number of elements	18 x 64
Micro-beamformer size	1 - 4 elements *
Imaging depth	10 cm
Frame rate	> 1000 Hz
Transmit beam	Steerable Fan beam
Number of transmissions	7
Transmission beam (azimuth)	Direction: 0° Divergence: 20° - 45° *
Transmission beam (elevation)	Direction: -30° to 30°; step 10° Divergence: 10.7°, 12.5° - 20° *; step: 2.5°
Central frequency	5 - 8 MHz *
Sampling frequency	4 x central frequency
Transmit apodization	2D Tukey window with cosine fraction 0.2

* These parameters are evaluated within the given ranges to optimize the imaging scheme.

transmit beam quality, and spatial resolution. Transmit beam quality in diverging wave imaging is known to be susceptible to the occurrence of so-called axial lobes or secondary pulses [35], [36], related to imperfect signal cancellation of late-arriving element signals from arrays with pitch larger than half a wavelength. Since the quality of the transmitted wave is very important for our image quality, we will first investigate and optimize the temporal profile of the transmitted diverging wave in our simulations.

Second, transmit beam divergence in elevation will be determined based on grating lobe artifacts, and the intensity uniformity between transmissions. Finally, the image quality will be evaluated for a micro-beamformer size ranging between 1 (no micro-beamforming) and 4 to achieve an acceptable trade-off between the desired image quality and data rate reduction. The imaging parameters are summarized in Table 2.1. All simulations are performed in Field II [37].

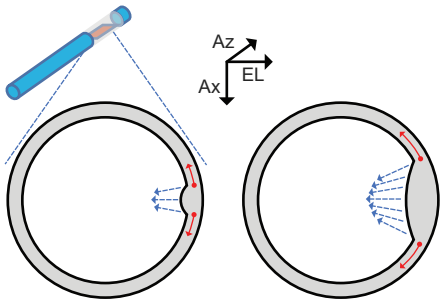

Figure 2.3: Schematic cross-sections of the 3D left atrium numerical phantom (radius 50 mm, thickness 3 mm). Left: a wave is introduced as a radial wall thickening (blue arrows). Red arrows show the circumferential electromechanical wavefront propagation direction. Right: wavefront propagation after 10ms (thickness/excursions not to scale).

2.2.5. Numerical Phantoms

Static phantom: A 3D numerical phantom, a cube with an edge length of 100 mm containing hyperechoic and hypoechoic spherical regions with diameters of 2, 4, 6, and 10 mm, highly reflective points, and background point scatterers with an average density of $0.2/\lambda$ has been used in Field II simulations. The relatively low point scatterer density is chosen to limit simulation time for this large-size cubic phantom and the high number of transducer elements. In addition, a single point scatterer at a depth of 50 mm is simulated to determine the Point Spread Function (PSF).

Beating left atrium: To evaluate the proposed high-frame-rate imaging scheme in a dynamic environment, a spherical shell with an outer diameter of 50 mm and a thickness of 3 mm has been simulated to mimic a left atrium. The center of the sphere is at an axial distance of 50 mm, equivalent to imaging the left atrium from the center of the right atrium. A circumferentially propagating wave has been introduced to this phantom by applying a radial thickening with an amplitude of 10 mm/s (10 µm/frame). The atrial thickening initiates from a single point and propagates omnidirectionally along the atrial wall with a velocity of 2 m/s [7]. A cross-section of the beating left atrium numerical phantom is illustrated in Fig. 2.3.

We use 1D axial cross-correlation to estimate the frame-to-frame tissue displacement. Since simulating a 3D numerical phantom with a matrix array in Field II is very time-consuming, we limit our simulations to only 3 pairs of consecutive volumetric data sets acquired at an interval of 1 ms within each pair (i.e., mimicking a frame rate of 1000 Hz). The consecutive pairs of data sets have been

simulated for 3 time-points, t = 0 ms, 10 ms, and 20 ms, to show the concept of electromechanical wave imaging. The final map of tissue displacement (actually displacement over 1ms in the direction of the ultrasound beam, so the axial tissue velocity component) has been generated by applying an image intensity-based mask to the displacement data to only visualize the atrial wall. In addition, another mask based on tissue displacement has been applied to the displacement map to exclude non-moving tissue.

2.2.6. Evaluation Criteria

The performance of various combinations of transmission and micro-beamforming schemes has been evaluated, as assessed by the widths of PSF at -6 dB (azimuthal and elevational resolutions), the side lobe level, the grating lobe level, and the contrast-to-noise ratio (CNR). The side lobe level is defined as the peak level of the highest side lobe compared to the main lobe in dB, and the grating lobe level is defined as the peak level at the theoretically-expected grating lobe direction. These two were measured by imaging only one scatterer in the field of view. The CNR is calculated using [38]

$$CNR = \frac{\mu_s - \mu_c}{\sqrt{\frac{\sigma_s^2 + \sigma_c^2}{2}}} \tag{2.2}$$

where μ_s and μ_c are the mean amplitudes and σ_s and σ_c are the standard deviation of the gray levels in the speckle and anechoic cyst regions, respectively, of the 3D numerical phantom.

Imaging with a limited number of diverging beams and micro-beamforming may result in angle-dependent changes in image characteristics. To evaluate these effects, a lateral shift-variance plot (LSV-plot) [35] is used. An LSV-plot is constructed for a given imaging system by imaging a point scatterer shifting laterally. For each lateral position, a PSF is calculated and stacked to the other PSFs to form a 2D image. The entire image is normalized to its maximum value and plotted in dB scale. If there is little position dependence, the plot will be invariant along the diagonal. Otherwise, deviating structures will be visible revealing the nature of the position dependence. In this study, a point scatterer at a distance of 50 mm from the center of the transducer is shifted along the elevation direction from -45° to 45° with a step of 1° to create the LSV-plot.

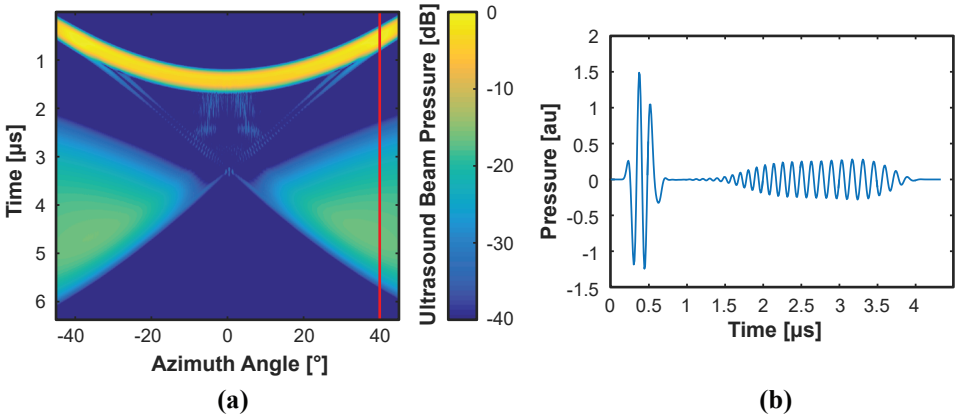

Figure 2.4: Transmitted pressure profile of a diverging wave as a function of time and azimuth angle at typical imaging depth of 50 mm, f= 7.5 MHz, divergence= 45°, (a) envelope of the pressure from -45° to 45° (red line indicates the position of the point used to acquire the 1D signal in (b). (b) time-domain pressure signal at 40° azimuth. The secondary pulse is observed as a longer pulse with lower amplitude compared to the main pulse.

2.3. Results

2.3.1. Imaging Scheme Optimization

Transmit Central Frequency and Azimuthal Divergence Angle

When evaluating the transmitted diverging waves, we found significant secondary pulse levels in the transmitted time signals. In Fig 2.4(a), where the envelope of the transmit pulse is shown for all azimuth angles, it can be seen that the secondary pulse is present over a large range of the opening angle and gets longer for larger angles, following the primary short pulse after a few microseconds. Fig. 2.4(b) shows the transmit pulse generated by a transducer with a 45° divergence and 7.5-MHz center frequency at a point 50 mm from the transducer, at an angle of 40°.

We evaluated how the pulse shape depended on the beam divergence and transmit central frequency. The level of the secondary pulse has been measured at points located on a spherical surface with a radius of 50 mm ranging from -45° to 45° in both azimuth and elevation direction. The maximum of the secondary pulses measured in different directions is shown in Fig. 2.5(a) as a function of central frequency and beam divergence. The function has a triangular local minimum

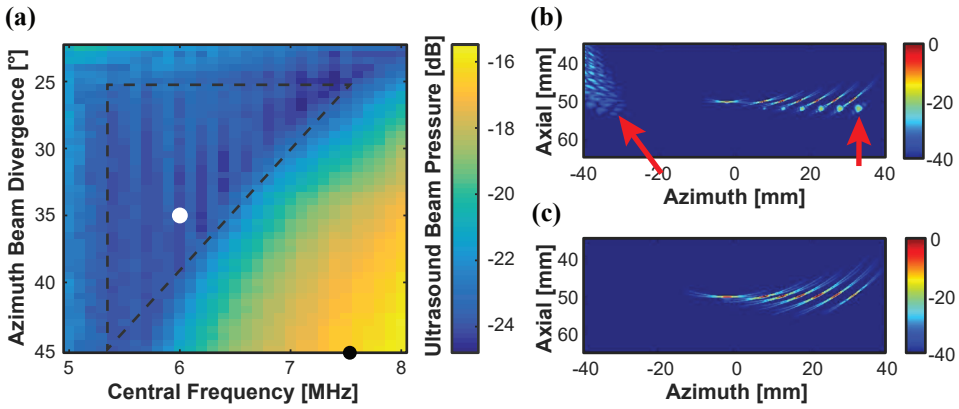

Figure 2.5: (a) Maximum secondary pressure peaks as a function of central frequency and azimuthal beam divergence. Reconstructed images based on a fully sampled array for a central frequency and azimuthal beam divergence of (b). f = 7.5 MHz and $\varphi_{az} = 45°$ (black point in (a)); and (c). f = 6 MHz and $\varphi_{az} = 35°$ (white point in (a)). Red arrows show the secondary reflection and grating lobe caused by poor destructive interference of waves transmitted from each individual element.

region in the frequency band of 5.3 - 7.5 MHz and the azimuthal beam divergence of 25° - 45°. Any local minimum close to the triangle hypotenuse will achieve low secondary pressure levels for a relatively high central frequency and opening angle. To show the effect of these secondary pulses, images of point scatterers made with transmit beams with different secondary pressure levels are reconstructed. Fig. 2.5(b) shows that the larger secondary pulse (corresponding to the black dot in Fig. 2.5(a) will interact with the scatterers to show prominent secondary echoes of scatterers (arrows) whereas in Fig. 2.5(c), where the transmit beam has a lower secondary-pulse pressure level (corresponding to the white dot in Fig. 2.5(a), the secondary echoes are almost invisible. We choose a central frequency of 6 MHz and an azimuthal beam divergence of 35° and these values will be used as bases for the rest of the simulations.

Elevational Beam Divergence and Intensity Ripple

With the proposed transducer size and the chosen azimuthal beam divergence of 35°, the single virtual source technique can provide an elevational beam of 10.7°. The transmit beam profile for this elevational beam divergence is illustrated in Fig. 2.6 which shows an intensity ripple over an elevational angle of -3.6 dB. To reduce this ripple, we would need to increase elevational beam divergence. To

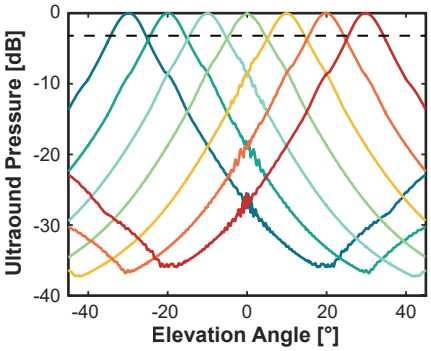

Figure 2.6: Transmit beam profile in elevation direction for an elevational beam divergence of 10.7°. The horizontal dash line shows an intensity ripple level of -3.6 dB.

Table 2.2: Transmit beam profile non-uniformity measured by the intensity ripple between two consecutive transmissions

Elevational beam divergence	Intensity ripple (dB)
10.7° (possible minimum)	-3.6
12.5°	-3.3
15°	-2.4
17.5°	-1
20°	-0.4

achieve the wider elevational beam divergences of 12.5°, 15°, 17.5°, and 20°, the effective number of elements in azimuth was reduced from 64 to 56, 47, 41, and 36 elements respectively. This azimuthal apodization was needed to maintain the 70° azimuth opening angle when bringing the virtual focus closer to the probe for more elevational divergence. The intensity ripples between two adjacent transmissions are listed in Table 2.2 for different elevational beam divergences as a measure of non-uniformity. The results show a lower intensity ripple for a broader beam which indicates a more uniform image intensity along the elevation direction.

Elevational Beam Divergence and Grating Lobes

In the next step, the effect of elevational beam divergence on the grating lobe level has been evaluated. The grating lobe directions for a micro-beamformer size of 2, 3, and 4 are 53°, 32°, and 24° respectively, at the chosen frequency of

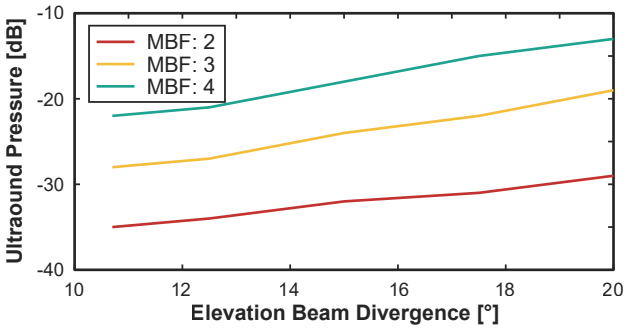

Figure 2.7: Transmit pressure at grating lobe directions, normalized to transmit pressure at main lobe for different beam divergences.

6 MHz. The acoustic pressure at grating lobe directions has been compared for elevational beam divergence of 10.7°, 12.5°, 15°, 17.5°, and 20°. Fig. 2.7. shows that increasing the transmission elevational beam divergence intensifies the grating lobe levels. An elevational beam divergence of 10.7°, which is the narrowest possible divergence, with a beam separation of 10°, provides the lowest grating lobe level and highest SNR at the cost of some non-uniformity in image intensity. We chose the elevational beam divergence of 10.7° and used this value in the remainder of the simulations. With this elevational divergence, the set of steerable fan-shaped beams provides an imaging field of view of 70° (width of insonified region at -3 dB) in the elevation direction.

2.3.2. Imaging Performance Evaluation

The angular weighted coherent compounding approach is evaluated for a micro-beamformer of 2 - 4 elements by reconstructing images of a single point-scatterer. Applying the proposed angular weighting function reduces the grating lobe level to a value that we will refer to as the grating lobe residual (GLR). Fig. 2.8(a) illustrates the effect of using angular-weighted coherent compounding compared to uniform coherent compounding for a micro-beamformer size of 3 elements. This angular weighted coherent compounding reduces the grating lobe levels by 28, 16, and 13 dB for micro-beamformer sizes of 2, 3, and 4, respectively. Elevational point spread functions for angular-weighted compounding for different micro-beamformer sizes are illustrated in Fig. 2.8(b). The width of the point spread function at -6 dB is illustrated in Fig. 2.9 for different imaging depths in both azimuthal and elevational directions.

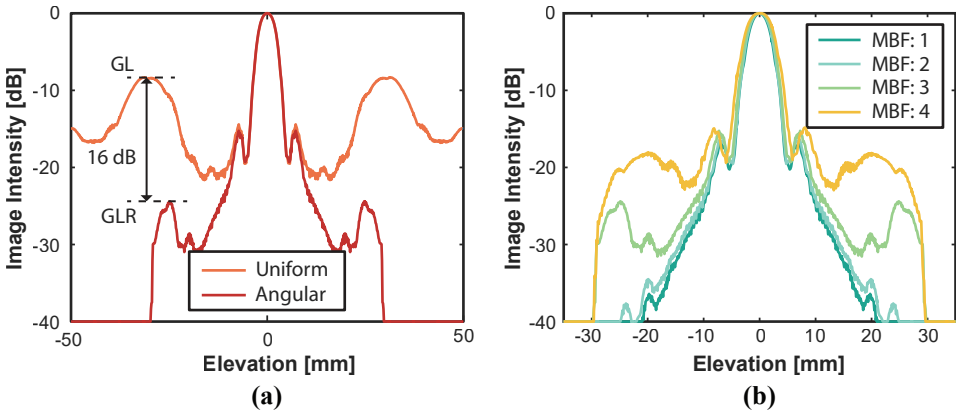

Figure 2.8: (a) Point spread function (PSF) in the elevational direction, for a single point scatterer at 50 mm depth which is reconstructed by uniform coherent compounding and reconstructed by angular-weighted coherent compounding. Grating lobe (GL) level and grating lobe residual level are shown for uniform coherent compounding and angular-weighted compounding respectively. (b) Point spread function for angular-weighted compounding for different micro-beamformer sizes and elevational beam divergence of 10.7°.

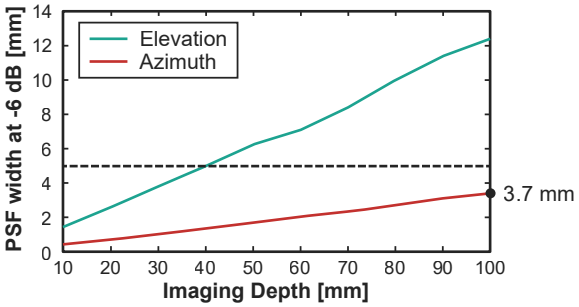

Figure 2.9: Lateral resolution as a function of depth in azimuth and elevation directions for a micro-beamformer size of 3 elements. The horizontal dash line indicates the desired lateral resolution for EWI.

The spatial variance of the proposed imaging scheme in elevation direction is evaluated by a lateral shift variance plot. Fig. 2.10(a) depicts the lateral shift variance plot for micro-beamforming size 3. Although the effect of the 7 transmit beams is visible as non-uniform image intensity in this plot, the lateral resolution, side lobe level, and grating lobe levels are fairly diagonally uniform. In addition to lateral shift variability, LSV-plot was used to compare the proposed angular weighting function with the conventional triangular weighting function [35]. Since the proposed method compounds a high number of transmissions to reconstruct a single receive line, the LSV-plot is more diagonally uniform and has a narrower

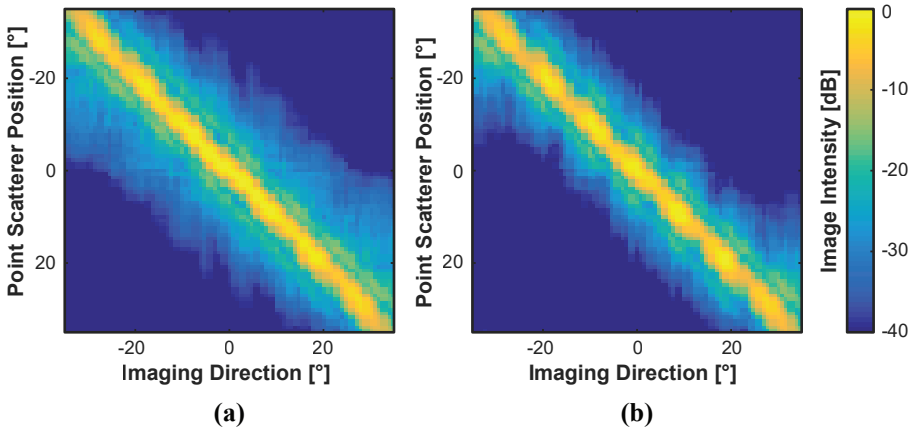

Figure 2.10: Lateral shift-variance plot of a single point scatterer at different positions ranging from -35° to 35° in elevation direction which is reconstructed by (a) the proposed weighting function and (b) the triangular weighting function.

main lobe. However, it produces higher clutter around the main lobe as illustrated in Fig. 2.10.

The numerical tissue-mimicking phantom has been imaged to evaluate the image quality in terms of CNR for the various micro-beamformer sizes. The clutter level is increased in hypoechoic regions by increasing the micro-beamformer size (Fig. 2.11.(a-d)), which reduces the CNR in both elevation and azimuth planes as illustrated in Fig. 2.11(e). Narrow transmission beams with a large separation angle cause non-uniform image intensity along elevation direction, as expected from Fig. 2.6. Fig. 2.11(a) and (b) show that the axial resolution (estimated at 0.8 mm) is not affected by the micro-beamforming, as expected, and seems sufficient with respect to the atrial wall thickness.

2.3.3. Imaging of a Beating Atrium Phantom

A rendered volumetric image of the beating left atrial numerical phantom has been generated with a micro-beamformer size of 3 elements and is shown in Fig. 2.12. A quarter of the top hemisphere has been removed to show the wall thickness in the azimuthal, elevational, and c-plane. We can clearly see the spherical object mimicking the left atrium. The atrial wall appeared thicker in the elevational direction which is caused by the lower elevational resolution. A combination of fan-shaped transmit beams and the proposed weighting function successfully suppressed the

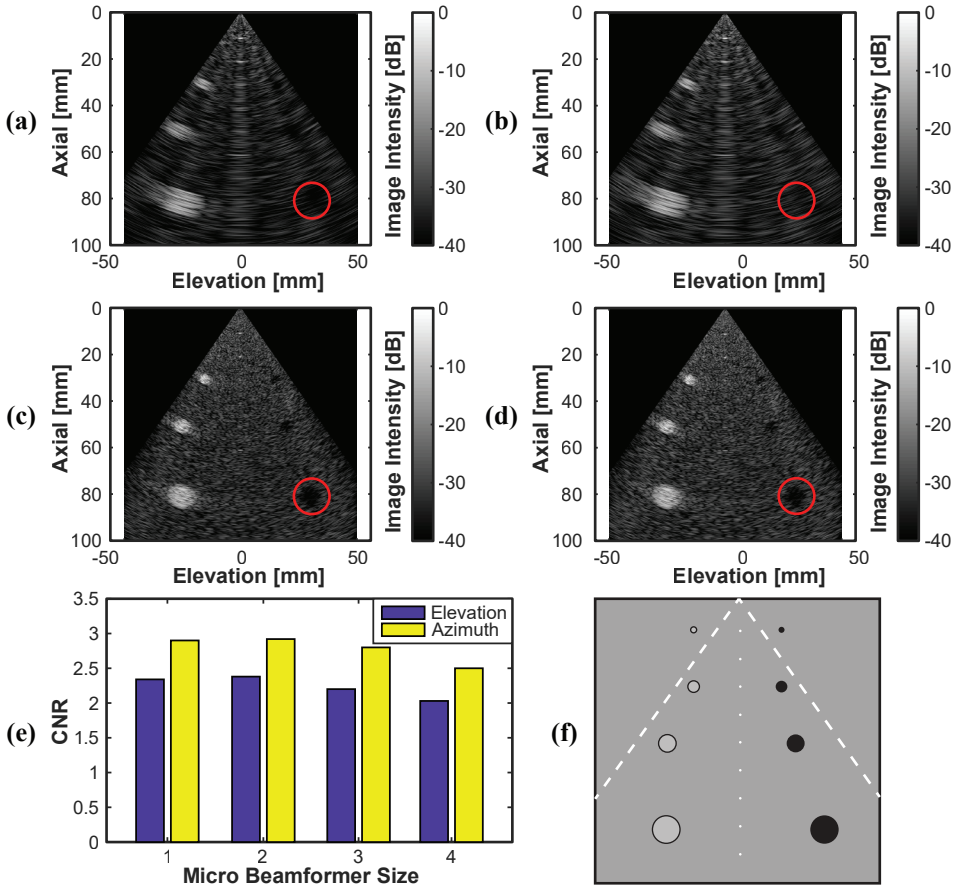

Figure 2.11: Reconstructed images of a tissue-mimicking phantom in (a) elevation direction for a fully sampled array; (b) in elevation direction for a micro-beamformer size of 3 elements; (c) in azimuth direction for a fully sampled array, and (d) in azimuth direction for a micro-beamformer size of 3 elements. Red circles show hypoechoic regions where the CNRs were calculated. (e) Contrast to noise ratio in azimuth and elevation for different micro-beamformer sizes. (f) Schematic representation of tissue-mimicking phantom, rotated to the elevation (a,b) or azimuth plane (c,d).

grating lobes and no obvious grating lobe is visible. However, non-uniform image intensity is rather visible in the elevation direction.

Fig. 2.12(a)-(c) illustrates the tissue displacement maps on 3 orthogonal planes, namely azimuthal, elevational, and c-plane, which were calculated at t = 1, 11, and 21 ms. The electromechanical wave has initiated from a point shown by the blue arrow in Fig. 2.12(a) and propagated omnidirectionally on the atrial surface.

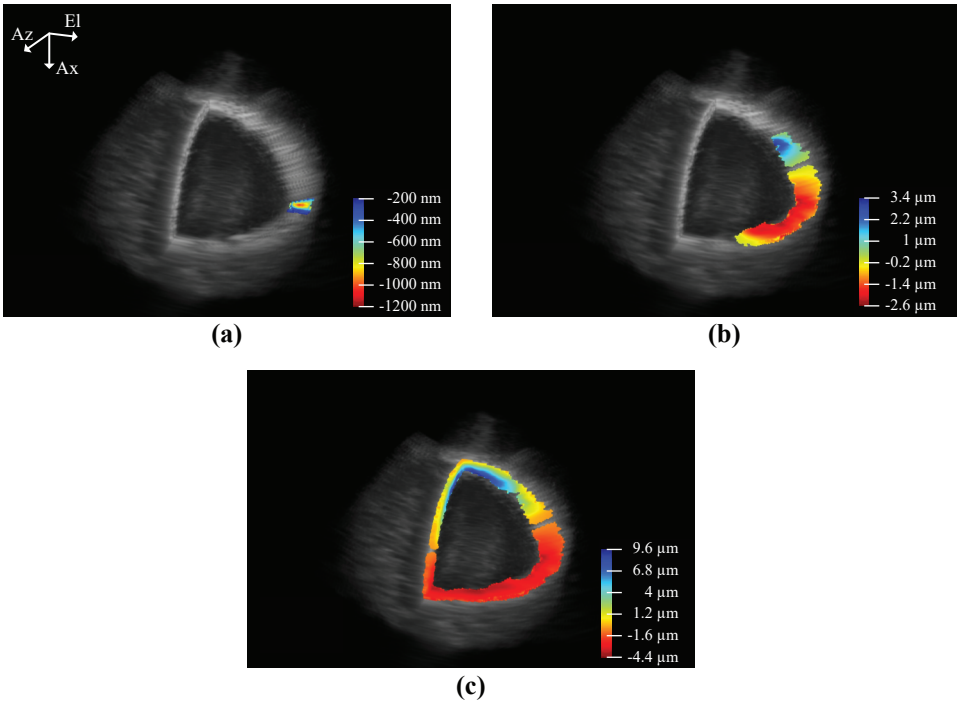

Figure 2.12: Tissue frame-to-frame axial displacement map corresponding to electromechanical wave propagation at (a) t = 1 ms, (b) t = 11 ms, and (c) t = 21 ms plotted on orthogonal planes. The blue arrow on (a) shows the initial point of EW and the red arrow on (c) shows the location at which the displacement is perpendicular to the ultrasound axial direction and cannot be estimated. The probe is located left side of the atrium at a 50-mm distance. Please note that the color scale represents axial displacement over 1ms, so a displacement of 10 µm is equivalent to an axial velocity component of 10 mm/s.

Fig. 2.12(b) and (c) show the propagation of the electromechanical wave at 11 and 21 ms after the wave generation. The electromechanical wavefront is clearly visible and the color gradient indicates the radial strains. The electromechanical wave map was masked by an intensity-based mask derived from the B-mode images. There is no unwanted motion detection on other parts of the region of interest. The red arrow in Fig. 2.12(c) shows a region where the radial motion is purely perpendicular to the ultrasound wave axial direction. Therefore, the 1D axial cross-correlation technique could not detect this displacement.

2.4. Discussion and Conclusion

In this study, we have proposed a novel imaging scheme for high-frame-rate 3D ultrasound imaging with a matrix intracardiac catheter. The main goal is to enable volumetric imaging with a sufficient frame rate and image quality for electromechanical wave imaging while reducing the data rate to realistic values. The proposed method consists of three main parts: 1) implementing 1D micro-beamforming in the elevation direction to reduce the data rate, 2) transmitting fan-shaped beams to suppress grating lobes in the elevation direction while providing a high frame rate, and 3) angular-weighted coherent compounding to further reduce the grating lobe artifacts and improve CNR.

The transducer consists of 64×18 elements with a pitch of 160 µm, which is larger than half of the wavelength at 5 - 8 MHz, giving rise to spatial aliasing. Generating a diverging wave from an array with such pitch can lead to a secondary, trailing, pulse as a result of poor destructive interference of the signals from the adjacent elements – see Fig. 2.4. This secondary pulse will also interact with scatterers, leading to secondary reflections in the reconstructed images and thus increased axial clutter levels [36] as illustrated in Fig. 2.5(b). Such axial lobes were previously reported by Rodriguez-Molares *et al.* [39] for coherent plane-wave compounding. They theoretically analyzed secondary pulse formation and proved that late-arriving transmit waves lead to delayed echoes which render as axial lobes. They showed that in a densely sampled array (pitch $< \lambda/2$), late-arriving signals will cancel each other out which reduces the axial lobe level. In this work, we reduce the secondary pulse level by carefully choosing the central frequency and azimuthal beam divergence for the given array configuration (Fig. 2.5(a)).

We intend to image the EW wavefront propagation in 3D with a sufficient spatial resolution by employing a high volume rate of 1 kHz. This is sufficient for local motion estimation over the whole volume, but previous research on EWI [19] suggests that while a local motion detection rate of 0.5 - 2 kHz is required, a slower rate might be sufficient for the motion sampling (the generation of the strain maps), leaving room for more lenient interleaved spatial interrogation. Konofagou and Provost [19] report that a mapping rate of 120 Hz would suffice since the highest frequency content of the electromechanical wave would be around 50 Hz. However, since we operate at a higher spatial resolution and the EW is a complex reaction-diffusion wave, we are not sure that this bound is valid in our situation. Therefore, we preferred to pursue the full 1 kHz volume rate. Furthermore, this also opens the way to other high-frame-rate applications such as shear wave elastography,

ultrafast Doppler, etc.

A high ultrasound frequency was preferred to achieve a sufficient lateral resolution for EWI. On the other hand, a large opening angle was needed to capture the entire left atrium. As shown in Fig. 2.5, a central frequency of 6 MHz and azimuth opening angle of 35° will result in a low secondary-pulse pressure level. Furthermore, at these values, small variations in the fabrication process and delay-quantization frequency will not have large effects on the secondary pressure level.

The elevational beam divergence is subject to a trade-off between the image-intensity uniformity, SNR, and grating lobe levels. A wider transmission reduces image intensity non-uniformity, but also generates a higher acoustic pressure in the grating lobe direction. Since we use a single virtual source method, the effective aperture size in the azimuthal direction must be reduced to generate divergences larger than the smallest realizable divergence of 10.7°. Consequently, wider elevational divergence reduces SNR.

To achieve a high SNR and low grating lobe levels we selected a divergence of 10.7° in the elevation direction. This leads to a non-uniform image intensity in the elevation direction. This non-uniformity is not expected to influence the performance of the proposed method for EWI, since the tissue displacement is measured in the axial direction. Non-uniformity of the transmitted power in B-mode can be compensated for by applying a weighting function to the reconstructed images. However, this corrects the non-uniform image intensity at the cost of producing a non-uniform SNR.

By using a dual virtual source technique similar to that proposed by Chen *et al.* [31], the dependence between the azimuthal and elevational beam divergence can be avoided, such that all aperture sizes can be used. However, we found that using a dual source was an unsuitable solution for our design since beams appeared to curve in elevation direction when steering to large angles, which decreases the overlap between the transmit beam directions and the micro-beamforming pre-steering direction.

The proposed set of steerable fan-shaped beams can insonify a region of 70° × 70° which is sufficient to cover the entire left atrium from the center of the right atrium, as illustrated in Fig. 2.12.

Fig. 2.12 illustrates a rendered volumetric image of the left atrium. Since the lateral resolution is lower in elevation, the atrial wall seems to be thicker in this direction in comparison to the azimuthal direction. The image intensity non-uniformity caused by narrow transmit beams in elevation is visible as darker

traces. In addition, there are some artifacts at lower depths that are caused by the high clutter level of the proposed method as shown in Fig. 2.10(a). The high clutter levels are mainly caused by implementing 1D micro-beamforming in elevation as illustrated in Fig. 2.8(b). This can reduce the tissue displacement estimation accuracy. Hence, more advanced beamforming techniques such as minimum variance and clutter suppression techniques might be further used to improve motion estimation and electromechanical wave tracking.

In this study, we evaluated the imaging performance of the proposed method in a series of simulations in which we tried to mimic the in-vivo situation. However, there are more practical challenges that could not be investigated in these simulations. For instance, signal-to-noise ratio or detecting EWI onset in the presence of noise, motion, and anisotropic tissue scattering are important in-vivo challenges that should be evaluated extensively in in-vitro, ex-vivo, and/or in-vivo studies.

The tissue motion has been estimated by 1D cross-correlation and illustrated in Fig. 2.12(a)-(c). The atrial wall thickening has been successfully shown as a radial gradient in the frame-to-frame displacement map. However, this is only a limited and highly simplified proof of principle of the electromechanical wave onset detectability. The electromechanical wave onset is usually tracked by finding a zero crossing on strain rate data. Since only three pairs of high-frame-rate volumes have been simulated in this study, a full map of an electromechanical wave is not generated. Nevertheless, the electromechanical wave onset is clearly visible on the tissue displacement maps. The electromechanical wave approximately propagated one-eighth of the sphere circumference at 10 ms which equals a velocity of 2 m/s. These intermediate results show the general imaging performance of the proposed method and its potential for EWI, although this remains to be confirmed by more realistic simulations and shown in experiments.

The proposed method provides an azimuthal lateral resolution smaller than 3.7 mm on the entire imaging depth (10 cm), which is likely sufficient for EWI [7]. The diameter of the targeted 10-Fr catheter limits the transducer size to 3 mm in the elevation direction, leading to a poorer lateral resolution in this direction. Therefore, at depths beyond 40 mm, the resolution in elevation direction exceeds 5 mm. The results show that the proposed method outperforms the state of the art on 3D ICE in terms of frame rate [22]. Moreover, previous works on pseudo-3D EWI showed that 2 to 4 planes already provided additional information for EWI of the atrium [14], [20] to reconstruct a volume by spatial interpolation. Our proposed method provides a volume consisting of 12 planes in elevation direction (natural

divergence of the transducer at 6 MHz is 6[9]) which can thus provide even more 3D details. In addition, the proposed method acquires the 3D electro-mechanical wave at a single heartbeat which is more suitable than ECG-gated 3D EWI for mapping cardiac arrhythmia. With this increase in 3D detail, the proposed design has the potential to improve the accuracy of electromechanical activation mapping and detect smaller and non-periodic arrhythmogenic sources.

In this study, we have focused on EWI for mapping atrial fibrillation. However, recent studies showed that EWI can be useful for mapping other cardiac conduction system abnormalities and arrhythmias such as atrial flutters [18] or accessory pathways in patients with the Wolf-Parkinson-White syndrome [13].

Many aspects are still unclear regarding EWI. The relation between electrical activation and mechanical contraction is determined by a combination of biochemical and mechanical interactions of partially unknown properties. Especially in cases of nonuniformities or pathology, this relation will be very complex. Whether the mechanical response alone can be used for patient-specific diagnosis remains to be shown. Nevertheless, measuring the mechanical response with a high spatiotemporal resolution is important to gain insight here.

A practical probe implementation requires channel-count reduction since the number of elements far exceeds the number of cables that can be accommodated. A 1D micro-beamforming scheme reduces the data rate by a factor equal to the number of elements per sub-aperture. We have shown that a data rate reduction by a factor of 2 results in negligible image quality loss. A micro-beamformer size of 3 or 4 introduces some imaging artifacts. PSF analysis has shown that the elevational resolution changes negligibly by increasing the micro-beamformer size to 3, but increases from 6.1 mm to 7 mm by utilizing a micro-beamformer of 4 elements at 50 mm imaging depth. Fig. 2.8(b) shows an increase of 16 and 22 dB in residual grating lobe level for a micro-beamformer of 3 and 4 elements respectively.

The channel count is reduced from 1152 (the number of elements) by a factor corresponding to the micro-beamformer size. Since a 10-Fr intracardiac catheter with a diameter of 3.3 mm limits the number of data transferring channels to around 100 micro-coaxial cables [34], the total reduction factor should be at least 12 to account for additional control signals and power supplies. A further on-chip reduction by at least a factor of 4 is thus required to reduce the channel count sufficiently. This can be achieved by methods such as analog time division multiplexing [40], in-probe digitization combined with digital multiplexing [30], [32] or coding of the digitized signal [41].

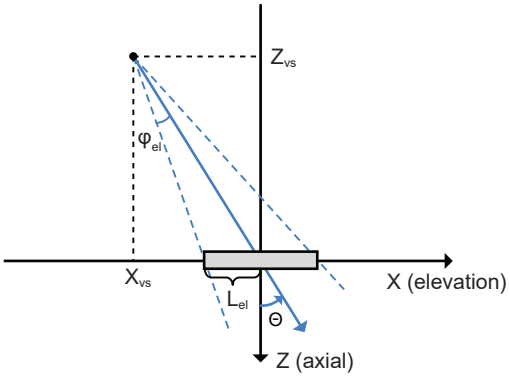

Figure 2.13: Generating a fan-shape transmitting beam with a divergence of φ_{el} in elevation and steered to Θ using a virtual source behind the transducer.

In conclusion, the results show a feasible solution for intracardiac 3D EWI. The 1D micro-beamforming approach, in combination with on-chip channel-count reduction, can sufficiently reduce the data rate for transfer over a 10-Fr intracardiac catheter, while the proposed fan-shaped transmit beams and weighted averaging function preserve the image quality. The proposed method has the potential to offer single-beat 3D EWI of the left atrium.

Appendix I

Fan-Shaped Transmit Beam Generation

To calculate a set of delays required for generating the desired beam, first, a virtual source location was determined based on beam divergence, transducer size, and steering direction in elevation, then the transducer effective size in azimuth was determined based on the virtual source location and azimuthal beam divergence (Fig. 2.13). The virtual source location was calculated by

$$X_{vs} = \begin{cases} -sign(\Theta)\frac{L_{el}\,tan|\Theta|}{tan|\Theta|-tan(|\Theta|-\varphi_{el})} & ,\Theta \neq 0 \\ 0 & ,\Theta = 0 \end{cases} \tag{2.3}$$

$$Z_{vs} = \begin{cases} \frac{X_{vs}}{tan(\Theta)} & ,\Theta \neq 0 \\ \frac{L_{el}}{tan(\varphi_{el})} & ,\Theta = 0 \end{cases} \tag{2.4}$$

where Θ is the steering angle with a counter-clockwise direction from the axial direction, φ_{el} is the beam divergence in elevation from a center line to a -6 dB contour and $\mathrm{L_{el}}$ is half of the transducer size in elevation. The Y-coordinate value of the virtual source was always zero because there was no transmit beam steering in the azimuth dimension. Having the virtual source location, the effective transducer size in azimuth was calculated by

$$L_{az} = R_{vs}\, tan(\varphi_{az}) \tag{2.5}$$

$$R_{vs} = \sqrt{X_{vs}^2 + Z_{vs}^2} \tag{2.6}$$

where $\mathrm{L_{az}}$ is half of the effective aperture size in azimuth and φ_{az} is the beam divergence in azimuth from a center line to a -6 dB contour.

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3

A compact high-voltage pulser for miniature ultrasound probes

This chapter is based on the publication "A Compact Integrated High-Voltage Pulser Insensitive to Supply Transients for 3D Miniature Ultrasound Probes" in IEEE Journal of Solid-State Circuits Letters, vol. 5, pp. 166-169, June 2022.

3.1. Introduction

Ultrasonic imaging is widely used in medicine for its versatile and nondestructive nature. In recent years, integrated circuit research is working on enabling further applications and, at the example of catheter-based devices for intracardiac echocardiography (ICE), moving from 2D to 3D visualization [1]. A major challenge in this transition is posed by the necessity of 2D transducer arrays with around 1000 elements and small pitches in the order of 100 to 200 µm to achieve sufficient image quality. To maximize the imaging aperture within probe tips with around 3 mm diameter, circuitry to transmit pressure waves and receive echoes on the same transducer need to be matched to the element area.

For transducer actuation, small circuits have been achieved through the use of

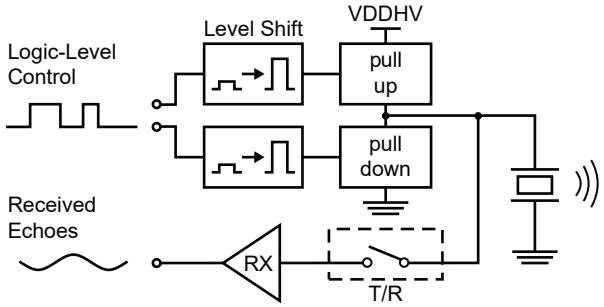

Figure 3.1: Common ultrasound system with level shifters, a pulser and transmit/receive (T/R) switch to receive electronics (RX).

standard CMOS devices [2], [3]. These, however, can not provide sufficient signal-to-noise ratio (SNR) at relevant imaging depths due to limited output pressure and the attenuation of ultrasound in the medium. Therefore, high-voltage (HV) transistors are typically applied despite their large size, and transmit/receive (T/R) switches are used to protect the receive path from high potential differences [4]–[6]. A common topology is shown in Fig. 3.1. While a class-A pulser topology as in [7] is area saving, the associated large static power consumption and tissue heating are undesirable and push-pull architectures are more common. These can be unipolar [8], [9] or bipolar [4]–[6], leading to a trade-off between less out-of-band energy for bipolar pulses at the expense of several more HV transistors.

The pull-up path is typically implemented with an HV PMOS and an HV level shifter is required to drive from logic supply levels. The voltage gap can be bridged by HV devices such as transistors [4], [8] or capacitors [10], the latter being preferable in terms of area but more sensitive to HV supply transients preventing regular operation, their cause being high transient pulsing currents and inductive loops, especially in catheter-based probes with limited local supply decoupling.

This work presents a unipolar pulser with an embedded T/R switch and a capacitive HV level shifter. The architecture is designed for beneficial scaling with large arrays and employs a latch-based high-side topology that enables pulsing in the presence of significant HV supply transients. The system is designed for driving a 160-µm×160-µm PZT transducer element with a central frequency of 6 MHz but the presented techniques are also applicable to other transducers once scaled.

This chapter is organized as follows. Section 3.2 presents the implementation of the transmit circuit, including the pulser, the HV level shifter, and an on-chip

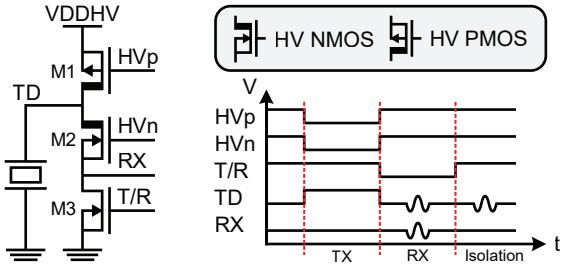

Figure 3.2: Structure and timing of the proposed unipolar pulser.

regulator. Section 3.3 details the fabricated prototype and discusses electrical and acoustical measurements. The chapter ends with a comparison to the prior art and a conclusion.

3.2. Circuit Implementation

3.2.1. High-Voltage Pulser

The proposed HV pulser design is shown in Fig. 3.2. The pull-up and pull-down paths are realized with a single HV transistor, M1 and M2, each, enabling compact unipolar pulsing. Similar to the bipolar design in [4], a T/R switch M3 is integrated with the pulser. This can be implemented as a smaller 5-V transistor given that the HV NMOS shields the RX node from rising above its breakdown voltage.

The transducer array is on one side directly bonded to the ASIC on nodes TD while on the other side an aluminum foil provides a common low impedance path to ground. A transmit event is initiated by closing M1 and keeping M2 open, pulling the transducer to the HV supply. To end the pulse, the transducer is then pulled to ground by closing M2 and opening M1. During this repeatable transmission phase, M3 remains closed to prevent any damage to it. In the receive phase, M3 and M1 are open while M2 conducts incoming signals to the receive electronics.

3.2.2. High-Voltage Level Shifter

While HV transistors can sustain large source-to-drain potential differences, their gates typically still have a limited breakdown voltage. To enable logic-level control,

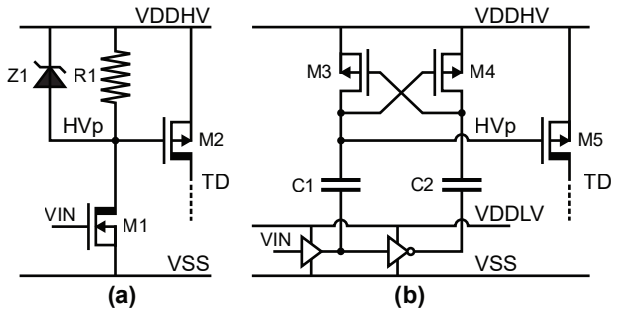

Figure 3.3: Level shifter architectures based on (a) HV transistors and (b) capacitors.

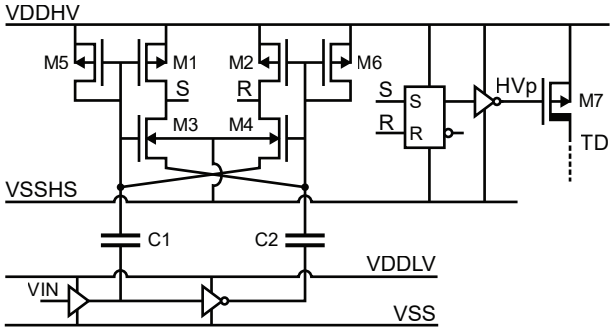

Figure 3.4: Proposed supply transient insensitive, capacitor-based HV level shifter.

the HV PMOS of the pulser, therefore, has to be driven with a level shifter. Fig. 3.3 shows two common ways to bridge such potential gaps with HV devices [4], [10].

The implementation with an HV transistor and a pull-up resistor provides a reliable and simple solution at the expense of using large HV devices. In addition, the pull-up resistor has to provide sufficient current to pull up the large pulser transistor with a sufficient slew rate, leading to static power consumption. These issues can be addressed with a capacitor-based design given that the bridging components are smaller and can be implemented in metal layers. This however has issues with transients on the HV supply. The transistors can be kept within their safe operating range with additional diodes but the capacitors will maintain their charge and cause an undefined overdrive on the HV PMOS of the pulser or in the worst case flipping of the high-side latch formed between M3 and M4. In area-limited catheter-based probes with substantial inductive supply loops, this can be particularly problematic as the highest current transients on the HV supply occur during pulsing, and dedicated transient-reduction techniques are difficult to integrate without area penalty or compromising the pulse shape.

Fig. 3.4 shows the proposed HV level shifter designed to enable a small footprint in large arrays without introducing supply transient sensitivity on the control of the high-side HV transistor. The HV gap is still bridged with capacitors C1 and C2 but as the high-side circuitry poses a much smaller capacitive load than the large HV PMOS, their size can be reduced while maintaining the same attenuation towards the top plates. The capture circuit accepts differential signals from the low side while rejecting common mode inputs. A differential input signal causes transistors M1/M3 and M2/M4 to act like inverters towards the attached reset-set (RS) NAND latch. If the capacitor top plate potentials however get close to each other, as could happen in the event of ripple on the HV supply VDDHV, potentials at nodes R and S will remain high, leading the RS latch to maintain its output state. For a low common mode, transistors M1 and M2 directly connect the output of the capture circuit to VDDHV and a high common mode leads M3 and M4 to connect the common mode to the output. The high-side capture circuit serves the additional purpose of shielding the mismatch-sensitive latch with a less vulnerable structure, making the system more reliable than a direct high-side latch implementation. An output inverter is driving the HV PMOS transistor to present a small load to the latch and enable it to switch quickly.

Unlike its conventional counterpart, this capacitive level shifter maintains the overdrive on the pull-up device of the HV pulser through a driver in a separate supply domain provided by an on-chip regulator generating VSSHS. Capacitive coupling maintains the potential difference even in the event of HV supply transients and the HV PMOS conductivity, therefore, remains stable. The high-side transistors of the level shifter can be small low voltage devices as they are shielded from the substrate potential with an isolation pocket. This pocket can be shared among multiple level shifters, making the device beneficial for arrayed architectures. Should HV supply transients cause potential differences between the capacitor top plates and gate regions of the low voltage transistors to become close to their breakdown limit, parasitic diodes of transistors M3 to M6 will dissipate any excess charge.

3.2.3. High-Side Regulator

To provide the low voltage pocket for driving the HV PMOS of the pulser, VSSHS, a supply 5 V lower than the HV supply, is generated on the periphery of the chip. The circuit is shared by the whole array and implemented as a basic HV PMOS

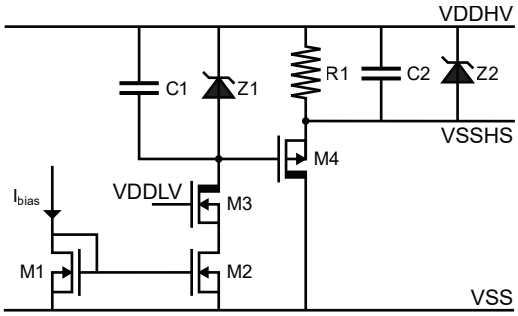

Figure 3.5: Regulator for high-side low supply.

source follower as shown in Fig. 3.5. The Zener diode Z1 provides an input 5.6 V lower than the HV supply and is biased with a low current from a current mirror. The HV NMOS M3 shields the current mirror transistor M2 by preventing its drain to pass the low voltage supply, VDDLV, enabling a small footprint with a defined mirror ratio. VSSHS is therefore regulated to VDDHV − 5.6 V + $V_{th,p}$, $V_{th,p}$ being the HV PMOS threshold voltage.

The additional capacitor C1 provides a high-frequency path to protect the gate of HV PMOS M4 in the event of HV supply transients. The decoupling capacitor C2 is sized to accommodate transient currents from driving the HV PMOS pulser transistors and can be as low as 100 pF for at least 20 consecutive pulses of all elements in this design. While the source follower can provide sufficient sinking capabilities for the application even with a low quiescent current, an additional Zener diode Z2 is added for sourcing capabilities in case of an unexpected drop in the regulated output. The power consumption of the regulator is negligible compared to the level shifter and pulser operation.

3.3. Measurement Results

A prototype chip has been fabricated in TSMC 180 nm HV BCD technology. It features an array of 8 by 9 elements and contains a pulser as well as an analog frontend per element. The element pitch is 160 µm by 160 µm of which 27 % is occupied by transmit-related structures, leading to an area per element of 0.008 mm^2. The HV level shifters of 6 elements are laid out together to share their isolation ring for the high-side circuitry. Next to a 65-V high-voltage supply, a 5-V

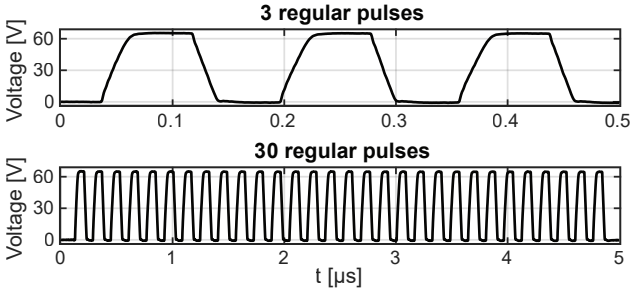

Figure 3.6: Electrical measurement of 3 and 30 pulses from the proposed pulser.

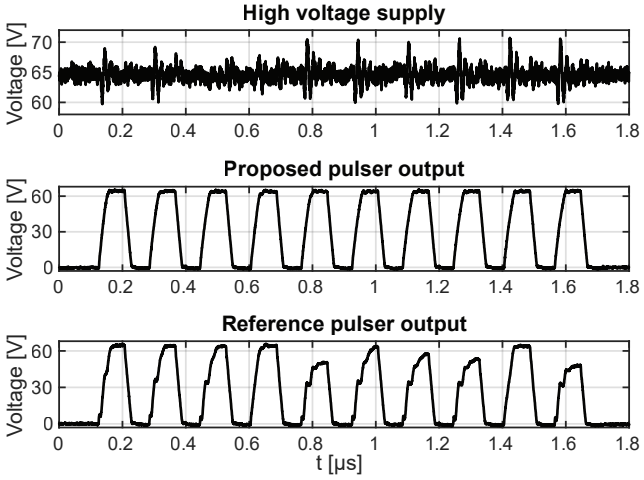

Figure 3.7: Comparison of pulsing with the proposed and reference HV level shifter in the presence of supply ripple with 27 nH added supply inductance.

and a 1.8-V supply are used in the transmit circuitry to provide level shifting and logic-level control options. The consumed power largely depends on the imaging mode and is dominated by the dynamic power consumption of driving the transducer. On-chip 160-pF VDDHV decoupling is added according to an estimation of how much could be integrated with a full device.

Electrical characterization has been performed with a 2-pF capacitive load emulating the transducer capacitance. Different pulse sequences are evaluated and shown in Fig. 3.6. Next to the regular array with transducers, two separate pulsers are installed at the periphery of the chip. One performs HV level shifting with the proposed design as the rest of the array while the other implements a capacitive level shifting scheme as shown in Fig. 3.3 with added Zener diodes to protect the high-side transistors against breakdown during measurement. This

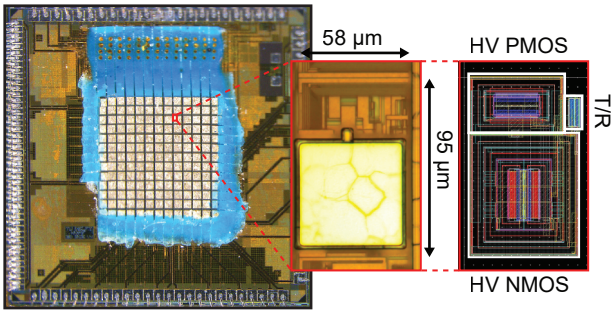

Figure 3.8: Die micrograph with PZT transducer array and pulser inset as microscope image and layout view.

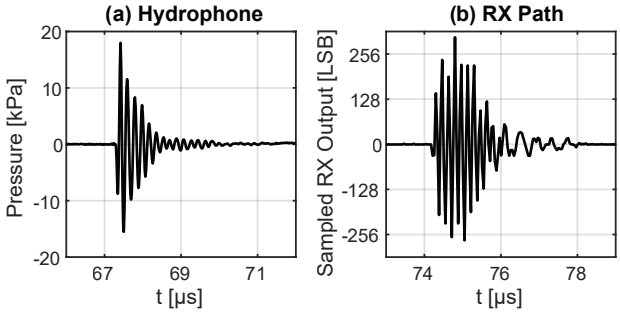

Figure 3.9: One transmitted pulse measured by a hydrophone at about 10 cm distance in (a) and reflected at about 5.5 cm from plate-reflector, received by the on-chip analog frontend and sampled at 24 MHz in (b).

additional setup is used to study the behavior of the two circuits when subjected to the same HV supply transients. Since this prototype, however, is more than ten times smaller than an actual imaging device and therefore also has a much lower transient pulsing current, a series inductor is inserted in the HV supply connection. Fig. 3.7 shows the supply variation caused by the 72-element array with an additional inductance of just 27 nH, implementing a low estimate of the supply ripple a full device could experience. The reference structure already shows a variation of the pull-up path conductivity up to complete opening, resulting in an irregular pulse shape and imaging artifacts. The proposed circuit in contrast shows little variation from the regular pulse shape even at the highest tested inductance of 220 nH.

Acoustic verification of the chip is performed with a PZT transducer matrix with a central frequency of 6 MHz. Fig. 3.8 shows a die photo with the array manufactured on top of the chip. Pulses with a peak amplitude of 65 V are

Table 3.1: Comparison with the Prior Art

	Integrated HV Transmitter			
	This Work	JSSC'20 [4]	JSSC'19 [6]	ESSCIRC'14 [9]
Technology	**180nm HV BCD**	180nm HV BCD	180nm HV SOI	180nm HV BCD-SOI
Max output	**65 Vpp**	60 Vpp	138 Vpp	100 Vpp
Pulse freq.	**6 MHz**	9 MHz	2 MHz	10 MHz
Load	**2 pF**	18 pF	Not Stated	23 pF
Area	**0.008 mm²**	0.167 mm²	0.04 mm² [a]	0.12 mm² [a]
# DMOS	**2**	10	10	3
# HV Diodes [b]	**0**	4	2	0
T/R embedded	**yes**	yes	no	no
Level shifter	**capacitive**	HV MOS	HV MOS	HV MOS
Pulser	**unipolar**	bipolar	bipolar	unipolar

[a] Not Including T/R. [b] Including zener diodes.

driven from the on-chip pulsers to the bottom plate of the transducer elements posing a 2-pF capacitive load. The top plate of the transducer stack is in a final step connected to an aluminum ground foil that is shared by the whole array and connected to the transmit ground potential of the chip. Fig. 3.9(a) shows the pressure measurement obtained with a hydrophone in water, 10 cm in front of the surface of the assembly. A single pulse was fired from a row of nine elements and the waveform as well as a peak-to-peak pressure level of 34 kPa are in good agreement with our expectations. Verification of the ability to perform pulse-echo measurements is obtained in a second experiment in which a plate reflector is installed in front of the array. After transducer actuation, the embedded T/R switch is opened, and received echoes are channeled to the included analog frontend [11]. The obtained results are subsequently sampled at 24 MHz and displayed in Fig. 3.9(b).

Table 3.1 compares the presented transmit circuitry to the prior art. It is expected that the HV level shifter can similarly be applied to bipolar pulsers and that realization of the transmit circuitry in an SOI technology as in [6] would lead to further area reduction due to smaller lateral HV device dimensions and enable higher driving voltages.

3.4. Conclusion

An HV transmit circuit for catheter-based ultrasound probes is presented. A compact pulser with an integrated T/R switch is driven with a novel HV level shifter that is insensitive to HV supply transients. The level shifter does not require any HV transistors, has no static power consumption, and benefits from application in large 2D arrays as used for 3D ultrasonic imaging. Electrical and acoustical measurement results that verify the functionality and performance of the presented techniques have been presented.

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4

An asic with shared hybrid beamforming adc for high-frame-rate 3d ice

This chapter is based on the publication "A Pitch-Matched Transceiver ASIC with Shared Hybrid Beamforming ADC for High-Frame-Rate 3D Intracardiac Echocardiography" in IEEE Journal of Solid-State Circuits, vol. 57, no. 11, pp. 3228 - 3242, Nov. 2022.

4.1. Introduction

Several cardiovascular conditions can be addressed using minimally invasive interventions, including the treatment of cardiac arrhythmia through electrophysiology and catheter ablation, trans-catheter valve replacement, closure of atrial septal defects and occlusion of the left atrial appendage [1], [2]. Real-time guidance of these interventions is traditionally achieved through fluoroscopy. However, this is associated with a low resolution of soft tissue and exposure of the patient and the physician to harmful ionizing radiation [3].

Ultrasound imaging can alleviate these disadvantages. But simply obtaining images of the heart from outside the body with a hand-held probe, in a so-

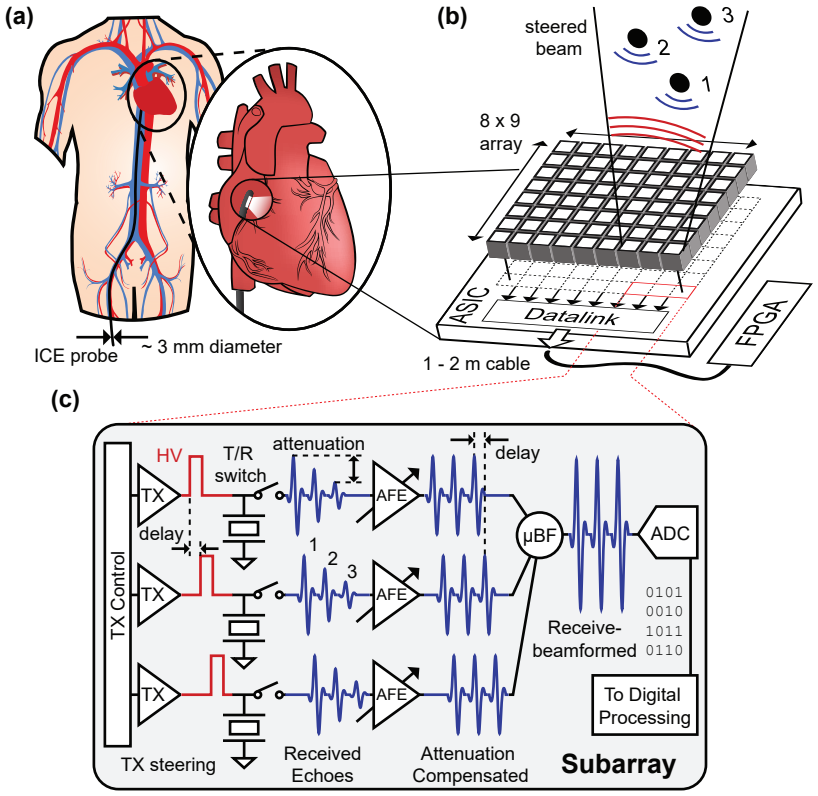

Figure 4.1: (a) Example of an intracardiac echocardiography (ICE) procedure with catheter entry from the inferior vena cava and imaging of the left ventricle from the right atrium. (b) Transducer matrix array integration overview. (c) Schematic of a 1×3-element subarray including transmit (TX) and receive circuitry.

called transthoracic echocardiogram (TTE), suffers from a limited acoustic window through the chest and requires a dedicated operator [4]. It is possible to obtain unobstructed, high-resolution ultrasound images from within the body by imaging from the esophagus in a transesophageal echocardiography (TEE) procedure or from within the heart in an intracardiac echocardiography (ICE) procedure [5]. The latter can often work on the same local anesthesia as the actual intervention as opposed to the, more risky, general anesthesia required for working from the esophagus. This has made ICE one of the most commonly applied ultrasound tools for minimally invasive cardiac interventions [4].

Until recently, a drawback of ICE probes was their limitation to 2D images. This was mostly due to the integration and wiring challenge posed by the larger

transducer matrix that is generally required for 3D imaging [6]. The probes are limited to a diameter of around 3 mm to enable accessing the heart through the vascular system, as shown in an example with entry from the inferior vena cava in Fig. 4.1(a). Within this space, the transducer array has to be accommodated at the tip and all external connections in the shaft. To enhance the visualization for the physician, 3D images were initially created from either manual [7] or motorized [8] rotation of 1D transducer arrays, sacrificing real-time imaging capability or resulting in very low frame rates. In [9], a helical 1D array was applied instead, enabling 3D imaging at higher frame rates at the cost of a limited elevation opening angle of just 22°. The class of forward-looking, ring-shaped probes [10], [11] showed a similar issue in being able to provide 3D images but only for a small volume ahead of the device and therefore not being applicable for the full range of procedures. A way to achieve a sufficient field of view and imaging rate is provided with the advanced integration of 2D transducer arrays in the catheter tip. However, the problem is that for individual connection from each transducer element to an imaging system outside the body, the interconnect becomes limiting to the array size, resulting in insufficient image quality [12]–[14].

Subarray beamforming has recently been investigated as an approach to interface large arrays, such as the approximately 1000 elements of a typical 3D ICE device [6], [15]. The method shifts part of the receive beamforming, usually applied in the imaging system, into the catheter in the form of delay-and-sum operations on the received signals of a subarray [16]. This effectively reduces the number of connections needed inside the catheter shaft as only the combined signal is transmitted. However, it does not provide the raw data of the full array and introduces focusing errors [17]. These result in increased grating and side lobe levels as well as broadening of the main beam, all negatively impacting image quality. Narrower transmit beams can be used to mitigate these effects but require more acquisitions per volume, ultimately leading to a trade-off between subarray size, with related channel-count reduction, and achievable frame rate [18].

A reduction in frame rate leads to worse motion tracking and can prevent the use of upcoming imaging modes like high-frame-rate blood flow or electromechanical wave imaging [19], which offer more diagnostic potential to physicians but require about 1000 volumes/s. A method to manage the impact on frame rate while still offering cable-count reduction is provided by multiplexing multiple channels onto one cable in analog or digital form. Analog multiplexing has been demonstrated in the time [20], [21] and frequency [22] domain but is constrained

by the limited bandwidth across the commonly applied micro-coaxial cables and suffers from channel-to-channel crosstalk [23]. Digital time-domain multiplexing (TDM), on the other hand, has been shown to benefit from better tolerance to cross-talk, interference and noise [15]. The availability of digital receive signals in the catheter moreover opens the possibility for future co-integration with emerging image processing such as data reduction with machine-learned compression [24], [25] or adaptive beamforming [26]. A major benefit of multiplexing lies in the compatibility with subarray beamforming, as has been shown in digital beamforming of element-level signals [27]–[29] and analog beamforming with subsequent digitization and TDM [15], [30], [31]. While the former requires an analog-to-digital converter (ADC) per element, the subarray area available for the latter makes the scheme more feasible for large arrays.

Both ways, current digital ICE probe designs still suffer from large ADCs. This expresses itself in the reported designs not being able to match the element-level circuitry to the transducer pitch [28], [31], a requirement for a scalable system, or the associated silicon area requirement making co-integration with adequate transmit circuitry impossible [15], [32], [33]. These transmitters need to excite the transducer elements with high-voltage (HV) pulses to obtain sufficient signal-to-noise ratio (SNR) for around 10 cm imaging depth, requiring the use of HV transistors with large isolation rings [6].

In this chapter, a scalable ASIC with a co-integrated 160-µm×160-µm transducer array is presented [34]. While [15] has already shown a large channel-count reduction through the combination of subarray beamforming and digital TDM with a beamforming ADC, the presented converter was too big to be able to include transmitters. Moreover, its associated subarray size of 3×3 elements precludes frame rates on the order of 1000 volumes/s. To address these issues, this chapter presents a novel hybrid beamforming ADC, consisting of an efficient charge-sharing successive-approximation-register (SAR) first stage and a compact single-slope (SS) second stage. The ADC architecture achieves the smallest reported power consumption and area among miniature ultrasound probe ADCs, enabling a subarray size of only 1×3 elements and thereby pushing the maximum frame rate to the targeted 1000 volumes/s. Moreover, it allows for the integration of per-element 65-V transmitters [35] and frontends, analog subarray beamformers and digitization in a pitch-matched fashion. The system has a 12-fold data-channel-count reduction, resulting in 96 data channels for the envisioned full system [17]. In a trade-off between the available circuit area and the achievable

image quality, the transducer pitch was chosen just above the half-wavelength margin. The resulting grating lobe artifacts stay below an acceptable level [17] and can be further reduced through coherent compounding of sub-volume acquisitions [36] and potentially further mitigated through recently shown machine-learning-based image processing techniques [37], [38].

This chapter is organized as follows. Section 4.2 presents the system architecture, with the circuit implementation of the ADC being further detailed in Section 4.3. Section 4.4 covers the fabricated prototype and discusses electrical, acoustic and imaging experiments. The chapter ends with a comparison to the prior art and a conclusion.

4.2. System Design

4.2.1. Overview

An overview of the conceptual system, showing common techniques in ultrasound imaging applied in this design, is given in Fig. 4.1(c). Each transducer element is used for the transmission (TX) of pressure waves as well as the subsequent reception (RX) of echoes, generated by reflectors in the imaged medium, in a pulse-echo (PE) cycle. The shared element usage between TX and RX maximizes the achievable aperture in size-constrained probes, as displayed in Fig. 4.1(b).

During the TX phase, HV pulsers are driving the transducer elements based on inputs from a TX controller. The controller applies delays to achieve TX beam steering, forming diverging waves to scan the whole volume with a small number of transmissions. In order to protect the low-voltage RX circuits from the HV operation of the transmitter, a transmit/receive (T/R) switch is placed between the two sections of the design.

Once the transmission is completed, the switch closes and a readout circuit can access the transducer. A common issue in ultrasound imaging systems is the large dynamic range (DR) accumulated by propagation in an exponentially attenuating medium. The attenuation A, in dB, is proportional to the distance z, the attenuation coefficient α and, for heart tissue, approximately the frequency f [39]:

$$A = 2 \cdot z \cdot f \cdot \alpha \tag{4.1}$$

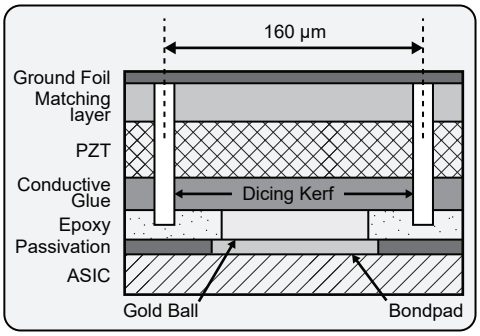

Figure 4.2: Conceptual sketch of the transducer stack directly manufactured on the surface of the ASIC.

The imaging frequency has to be determined based on a trade-off between axial resolution and imaging depth and is in this design set to 6 MHz with a depth of 10 cm [17]. Combined with an attenuation coefficient of about 0.5 dB/MHz/cm for heart tissue [39], the attenuation could reach 60 dB. Considering an instantaneous DR of 40 dB, the total DR can therefore reach 100 dB. As not all of that range is of interest throughout an RX period and the attenuation is time-dependent, the DR to be handled by the RX circuits can however be reduced by a procedure called time gain compensation (TGC). This is achieved by giving the analog frontend a variable gain that can be adjusted during one PE cycle, giving equally strong reflectors at different distances from the transmitter a similar output and easing the design requirements for the following circuitry [40].

The received signals from each channel in the device are combined in a beamforming operation to reconstruct the information of each voxel in the imaged volume. An SNR gain of $\sqrt{N}$ for N elements in the beamformer is possible if the system SNR is limited by uncorrelated noise and can aid in the design for a large DR. To reduce the number of connections from the probe to a beamforming system, part of the reconstruction can already be performed in the probe per subarray. This subarray beamforming, also referred to as micro-beamforming (µBF), applies delay-and-sum operations to individual signals of a subarray, effectively steering the RX beam to target the previously insonified area [16]. The combined signals can then be digitized for further local processing and sent to an imaging system.

An overview of the co-integration of the ASIC and a bulk-piezoelectric PZT transducer matrix array is given in Fig. 4.1(b). The 160-µm-pitch stack is an optimized version of what has been presented in [41] and gets manufactured directly

on the surface of the ASIC. It connects to exposed top metal pads on one side and a shared aluminum ground foil on the other side, as shown in Fig. 4.2. The 8×9-element assembly serves as a prototype with an architecture and layout design suitable for scaling to a full array of 64×18 elements [17]. While the prototype has a reduced aperture, it is already tailored towards the intended imaging scheme of acquiring a 70°×70°×10 cm volume in front of the transducer matrix at a frame rate of 1000 volumes/s. Given an imaging depth z of 10 cm and the speed of sound c of 1540 m/s in tissue, a maximum pulse-repetition-frequency (PRF) = $c/(2z)$ of 7.7 kHz can be reached. This provides 7 PE cycles for the formation of each volumetric image at a rate of 1000 volumes/s. To optimize their usage towards the best image quality, the beam profile and subarray receive beamformer size are determined in a trade-off with the required channel-count reduction and necessary circuit area. This work applies seven transmit beams of 70° divergence in the azimuth direction and 10.7° divergence in the elevation direction in a sweep of the elevation steering angle to cover the full 70°×70°×10 cm volume. In receive, subarrays of 3 elements along the elevation direction are applied which pre-steer the received signal in the same direction as the transmit beams [17].

4.2.2. Architecture

The implemented system architecture of the prototype is shown in Fig. 4.3. Each transducer element's bottom plate is connected to an individual pulser and a variable-gain analog front-end (AFE), implementing TGC. The TX part is realized as a unipolar, 65-V design with a pull-up and a pull-down path provided by DMOS transistors. To facilitate test modes and reduce the complexity, the TX control signals are provided externally per row, with an area reserved for an integrated TX controller in a future version. A single low-voltage (LV) transistor, protected against voltage breakdown by the HV NMOS of the pulser, enables T/R switching to the input of a low-noise amplifier (LNA)[42] in the receive phase [35]. The LNA is configurable to a voltage gain between -12 dB and 24 dB at a step size of 18 dB and, together with the second-stage programmable gain amplifier (PGA) that provides 6 dB to 24 dB at a step size of 6 dB, achieves a total variable gain between -6 dB and 48 dB at a step size of 6 dB [15]. In each PE cycle, the gain is gradually switched from the lowest to the highest gain setting to first grant sufficient linearity for the initially received strong echoes and later enough gain to detect strongly attenuated echoes out of the noise floor. The PGA is a voltage

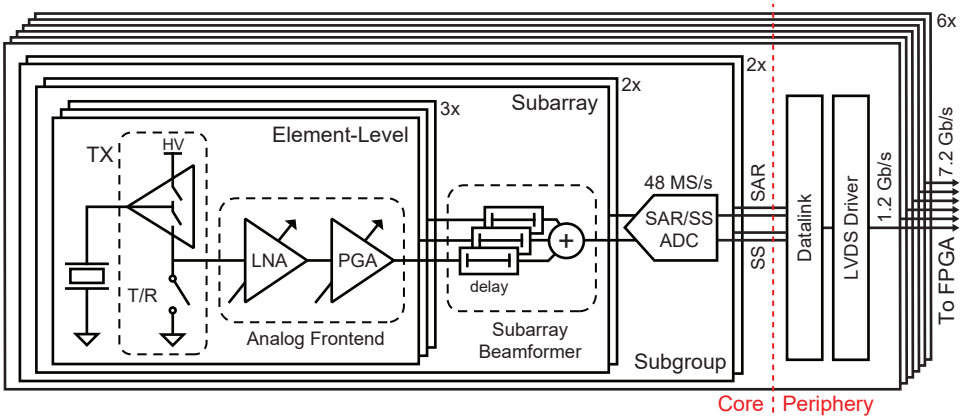

Figure 4.3: System architecture including element-level pulsers and analog frontends, subarray beamformers, and a shared hybrid ADC structure per subgroup. On the periphery, each channel is connected to an FPGA via a datalink and an LVDS driver.

amplifier with a compact T-type capacitive feedback network [43], configured for quick settling after switching the gain during active operation. To provide rejection of common interference in the following signal chain, it converts the single-ended signal to a differential output.

The outputs of three element-level circuits are merged in a 1×3-element subarray beamformer, of which two are combined in a 2×3-element subgroup. Each subgroup shares a hybrid SAR/SS ADC structure that separately digitizes the two channels at 24 MS/s with a resolution of 10 bits each. The outputs of two subgroups are received by a periphery-level block, providing a datalink to process the received data and applying TDM onto a low-voltage differential signal (LVDS) driver to transfer the data to an off-chip field-programmable gate array (FPGA). Each periphery block serves a 4×3 matrix of elements and 6 of these are arranged to form the prototype of 8×9 elements. A total channel-count reduction of 12 is implemented by the subarray beamformer size of 3 and TDM of the digital outputs of 4 subarrays onto one channel.

4.2.3. Hybrid ADC

To cover the discussed dynamic range of up to 100 dB, a 10-bit resolution is chosen to complement the 54-dB TGC and √N beamforming gain. The sampling

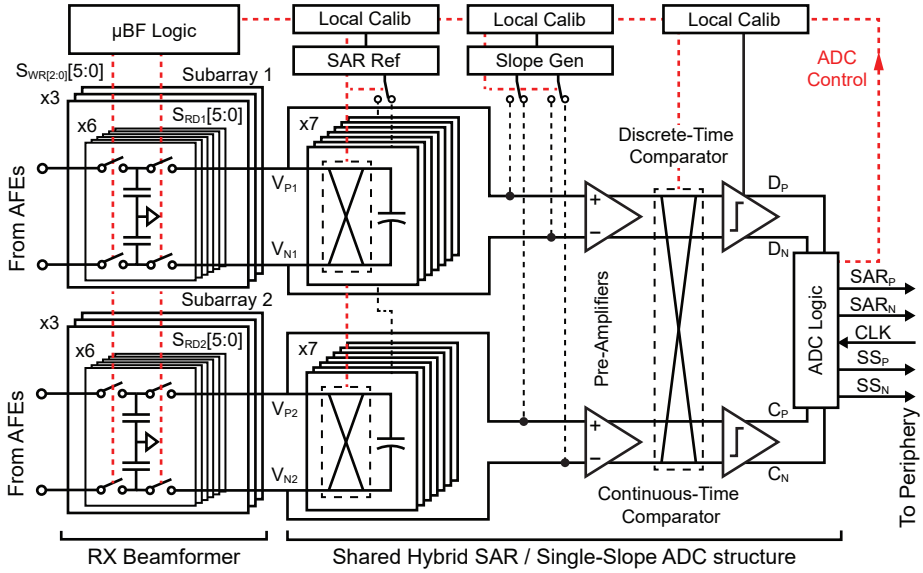

Figure 4.4: Architecture of the proposed hybrid analog-to-digital (ADC) converter formed between a successive-approximation-register (SAR) first stage and a single-slope (SS) second stage.

frequency should be at least 4 times higher than the frequency of the transducer to maintain an acceptable side lobe level[44], leading to a 24-MHz sampling rate for the 6-MHz device. For similar specifications, SAR ADCs have been shown to be an effective solution due to their high efficiency and Nyquist-rate sampling [45]. Similar to [15], the SAR conversion is performed in the charge domain to benefit from direct integration with a subarray beamformer into a beamforming ADC. However, this design employs a capacitive digital-to-analog converter (CDAC) with metal-oxid-semiconductor capacitors (MOSCAPs). While their voltage-dependent capacitance excludes them from use in charge-redistribution ADCs, in charge-sharing topologies MOSCAPs reduce area through high integration density and improve comparator offset as well as noise tolerance [46].

One drawback of SAR ADCs in general is the exponential increase of the CDAC size per added bit of resolution in the binary search algorithm. This can be alleviated by means of combination with a slope ADC that digitizes the residual of a SAR first stage in a hybrid converter [33], [47]. A slope ADC can be compact but suffers in efficiency when converting with a high resolution and sampling rate. In the following, the architecture of a hybrid SAR/SS beamforming ADC operating in the charge domain is presented. An optimal split between the two stages

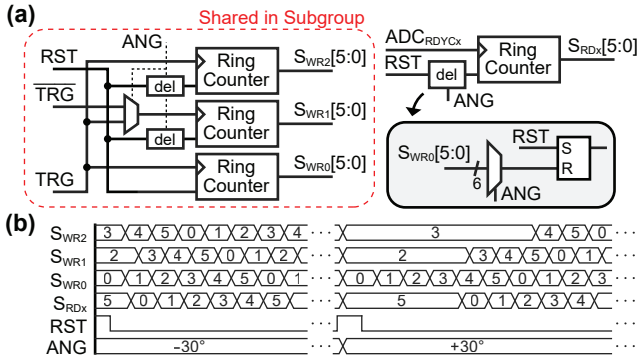

Figure 4.5: (a) Schematic overview of subarray beamformer. (b) Conceptual S/H-cell timing diagram with maximum positive and negative angles.

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is found in a 6-bit SAR and a 5-bit SS conversion with one bit of redundancy between them. This considers the required size reduction of the SAR stage and added complexity to the slope stage of the design. In order to benefit from the reduction of the CDAC size, the gained area must outweigh that of the added SS blocks. As the unit capacitor of the CDAC is still sized for 10-bit linearity, this is mainly achieved by enabling a CDAC size that is actually linearity-limited, good MOSCAP matching and the overhead reduction due to a reduced number of unit capacitors.

The ADC is interfacing with the subarray beamformer as shown in Fig. 4.4, avoiding the need for an additional high-bandwidth buffer compared to converters with conventional sampling [33], [47]. The delaying of the received signals is implemented by means of capacitive sample-and-hold (S/H) cells, similar to [48]. The summation of the delayed signals can then be achieved passively by switching the right cells together at the input of the ADC, as in [15]. In contrast with [15], the control-logic of the subarray beamformer, shown in Fig. 4.5(a), can also provide delay quantization independent of the sampling frequency. This is enabled by separate read- and write-pointers, S_{RDx} and S_{WRx}. The former is advancing based on completed ADC conversion cycles, ADC_{RDYC}, while the latter advances based on an adjustable input trigger, in this case a locally generated 24-MHz signal and its 180°-phase-shifted version, TRG and $\overline{\text{TRG}}$. While each ADC requires its own read-pointer, the write-pointers can be shared between multiple channels. The pointers are realized as ring-counters, and different steering angles, determined by ANG, can be realized by delaying the reset signal between the pointers. An

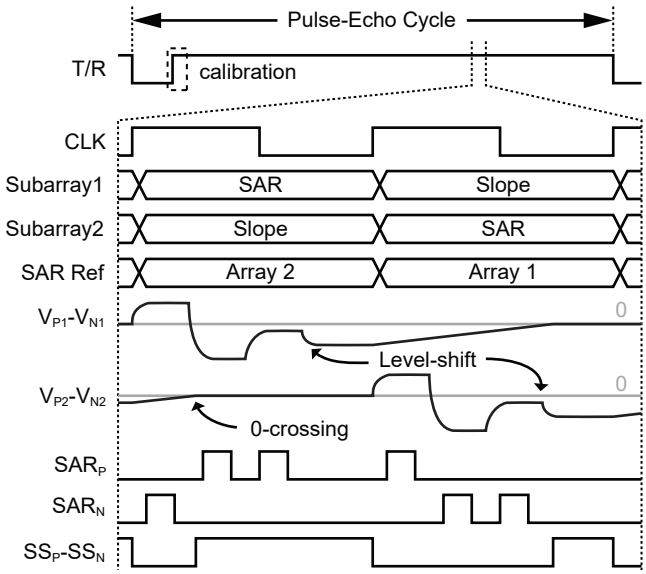

Figure 4.6: Conceptual timing diagram showing essential nodes of the hybrid ADC and how two subarray outputs are digitized by the shared structure.

area-efficient implementation of this delay is achieved by re-using the pointer of one AFE, AFE0, as the reference counter for the delay. Based on ANG, this can be used to implement the delay with a simple multiplexer and a compact reset-set (RS) latch. The resulting S/H-cell switching patterns are shown for a maximum positive and negative steering angle in Fig. 4.5(b). A delay resolution of 20.8 ns is achieved with a range up to 125.0 ns, offering steering capability of the axis of the beam in a ±30°-window.

The conceptual timing of the converter operation is shown in Fig. 4.6. Following the subarray beamformer, the combined charge can be quantized through the positive or negative connection of binary-scaled units of a pre-charged CDAC and detection of the polarity with a discrete-time comparator (DTC). After this SAR conversion, the possible residual charge range between nodes V_{Px} and V_{Nx} has been reduced to the least-significant bits (LSBs) and can thereafter be digitized by applying a differential slope with compact current sources on the same nodes. To have the redundant range between the two stages work for positive and negative decision errors in the SAR conversion, part of the CDAC is switched after the first phase to implement a level shift, placing the SAR residual in the middle of the SS conversion range. As long as the residual is not contaminated and they are within

the redundant range, all SAR decision errors, such as DTC noise, CDAC settling errors, and mismatch between the SAR and SS comparator offset, can be covered.

High area efficiency is achieved by hardware-sharing between two neighboring subarrays, forming one shared ADC structure. The two phases of the conversion are executed in two periods of a 48-MHz clock, twice as high as the ADC sample rate, and while the first subarray performs the SAR conversion, the second applies the slope and vice versa. In this fashion, the SAR reference pre-charger, as well as the slope generator, can be shared and a drawback that is typically introduced in the hybrid architecture can be mitigated: Usually, the combination of a SAR and a SS stage requires the introduction of an asynchronous DTC for an efficient SAR part and a continuous-time comparator (CTC) to avoid a high-frequency comparator clock for the SS[33], [47]. While this is still the case, they can be shared between the two subarrays with the addition of a small pre-amplifier that provides isolation and serves as part of both comparisons. Another benefit of hardware-sharing is that the SAR CDAC can be switched out and slowly pre-charged during slope conversion. Compared to designs with conventional references[33], [47], this allows for the use of a low-bandwidth reference with a constant current drawn from the supply. Moreover, it does not require an additional CDAC used for ping-pong operation as in[15]. To further facilitate application in large imager arrays, critical nodes in the circuit, including the SAR reference, the slope generator, and the DTC offset, are calibrated against mismatch.

As in ultrasound probes, the area underneath the transducer matrix is typically very limited to achieve a scalable, pitch-matched design but there is more space available at the periphery [32], [40], [48], the received signals are brought out of the core as soon as they are quantized. This applies to the return-to-zero (RZ), asynchronous SAR outputs, SAR_P and SAR_N, which are gated versions of the DTC outputs, D_P and D_N, as well as the SS outputs, SS_P and SS_N. The SAR and SS outputs of both converted channels are each carried on one connection to the periphery and correctly merged there to minimize interconnect space.

4.2.4. Datalink

An overview of the datalink is shown following Fig. 4.7. The SAR and SS outputs of two shared ADC structures, serving 12 elements in total, are captured on the periphery by separate receivers. The SAR receiver recovers the SAR output data, as well as a clock that can be used to sample the data in the following stage, directly

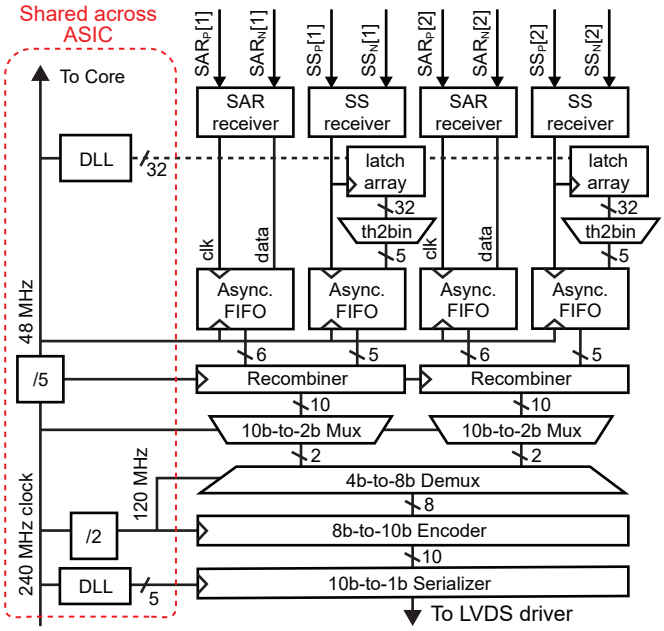

Figure 4.7: Datalink block diagram showing processing of the outputs of 4 ADCs and the clocking scheme shared across the ASIC.

from the asynchronous RZ SAR output [15]. The SS receiver, on the other hand, converts the differential time-domain output of the SS into a short pulse. This pulse is used to latch the output of a delay-locked-loop (DLL) that divides the 48-MHz clock period into 32 segments, corresponding to a 5-bit word. As the SS comparison in the core is based on the same time reference, this word is an accurate representation of the second-stage ADC output. The resulting 32-bit word is then converted from a thermal to a binary code to simplify further processing and can be sampled with the same pulse as the latch array. The asynchronous SAR and SS data can subsequently be synchronized to the periphery clock by dual-clock first-in, first-out (FIFO) memories. To reduce the final data bandwidth to the imaging system, the recombination block merges the 6-bit SAR and 5-bit SS codes into the actual 10-bit output code of the ADC. This is done by summing both parts and removing the redundancy introduced between the two stages in the following manner [47]:

SAR		1	0	0	1	0	1	-1			
SS	+						1	0	1	0	1
Combined		1	0	0	1	0	1	1	1	0	1

The subtraction of the redundancy is implemented with the two's complement. The outputs of two recombiners are subsequently merged through TDM, realized by arranging two 10-bit words at 48 MHz to 8-bit words at 120 MHz. The following structures are based on [15] and first apply 8b10b-encoding to enable a standard transmission protocol [49]. The 10-bit output words are then serialized to a 1.2-Gbps output stream to conventional LVDS drivers with timing provided by a DLL. Both DLLs are based on [50], shared among the whole ASIC and operate on a single 240-MHz system clock provided from an FPGA. A 120-MHz clock is generated locally at the periphery for the encoder and TDM while a 48-MHz clock provides the timing for all core circuitry as well as the data reconstruction on the periphery. While a balanced clock distribution in the core is required as a time reference for the generation of the intended RX and TX beams, the 48-MHz clock phase of the core does not need to be precisely matched to that of the periphery as only the clock period is relevant for clock-data recovery (CDR).

4.3. Circuit Implementation

4.3.1. Timing

As the key enabling block of the system, the implementation of the shared hybrid ADC structure is further detailed in this section. The timing can be followed in Fig. 4.8(c). A non-overlapping (NOV) clock generator, shown in Fig. 4.8(a), creates a division of the 48-MHz system clock, CK_{SYS}. The resulting synchronous NOV signals are used especially in the operation of the SAR reference as well as the SS circuitry and prevent interference from sharing blocks. The SAR reference, shown in Fig. 4.9(a), is configured as a voltage-controlled current source with a calibrated input $V_{CAL\text{-}SAR}$ and source degeneration R_S to increase its linearity and lower its transconductance. The current in the pre-charger is always running and steered between the two DACs of the converter in fixed time intervals, with a short reset period applied at the beginning of each charging. The slope generator in Fig. 4.9(b) is also implemented as a steered voltage-controlled current source between the two parts of the shared ADC structure and calibrated by $V_{CAL\text{-}SS}$. A

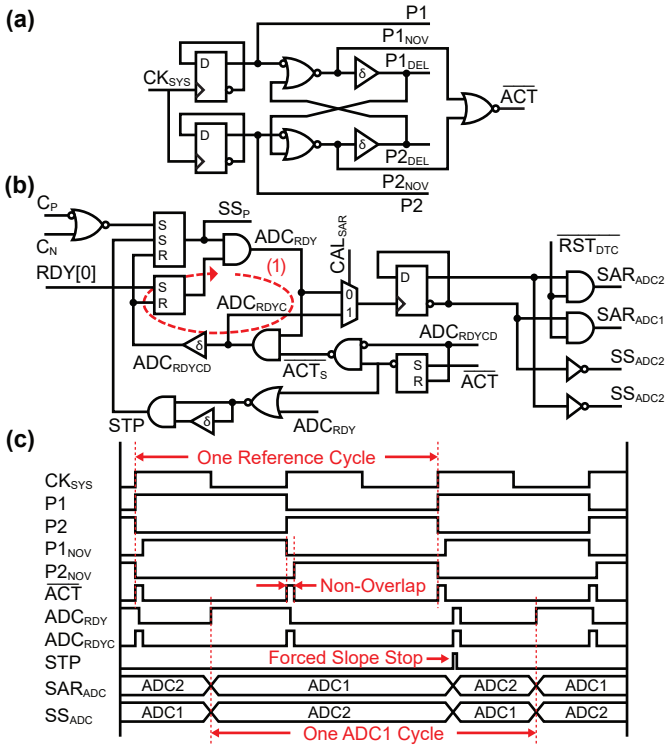

Figure 4.8: (a) Synchronous timing generator of the shared converter. (b) Loop determining the asynchronous ADC timing. (c) Conceptual timing diagram.

very short NOV period SS_x is generated locally to prevent connection of the pre-amplifier input nodes of the two involved ADCs, V_{Px} and V_{Nx}, while still having the slope period closely matched to that of CK_{SYS}. If SS_{RDYx} indicates a SS conversion has finished, the input of the corresponding pre-amplifier is connected together to a mid-rail node V_{CM}, setting up the next conversion.

While the reference circuits require determined timing, particularly the comparators benefit from more flexible control to make most efficient use of the CK_{SYS} period. Feedback loop (1) in Fig. 4.8(b) offers this by applying control signals not based on a clock but based on finished ADC conversion parts. Two area-efficient SR-latches determine a completed conversion from the CTC outputs $C_{P/N}$ and the RDY[0] signal of the last bit in the SAR logic. If both parts are ready, an internal flip-flop (FF) is in regular operation directly toggled with ADC_{RDY}, indicating that the state of the converter structure shifts and the CTC and DTC can be switched,

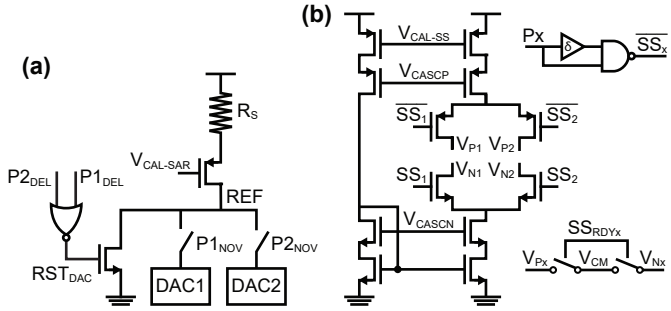

Figure 4.9: (a) Schematic of the CDAC reset and pre-charger. (b) Slope generator schematic with reset and switching blocks.

enabling a longer settling period for the pre-amplifier before the next part of the conversion starts. The reset of the RS latches for the next conversion part is determined by the combination of the ADC_{RDY} and the ACT_S signal, the second being a latched version of the active signal indicating the passing of an NOV period. The signal needs to be latched as the SS conversion can extend over the period in which the slope generator is applied because of the delay of the CTC. To still enable successful conversion, the comparators can be connected longer and, while the slope generator is already shifting to the other converter part, still retrieve the output. In order to prevent loss of synchronization with the periphery in the case of a fault in the SAR residual, a stop signal STP is also issued by ACT_S. This signal can force a stop of the slope conversion by setting the RS latch and has a delay designed to be just above the delay of the CTC. The following SAR conversion typically doesn't suffer from an over-ranging slope conversion as it is timed asynchronously with sufficient margin. The following SS conversion can also still complete successfully as the over-ranging period would usually fall into the conversion range covering the redundant range.

4.3.2. Comparator

Each ADC has its own pre-amplifier to shield the signal to be quantized from the interference of the switching and operation of the following stages as displayed in Fig. 4.10(a). An efficient current-reuse topology is employed and complemented with cascoding transistors to increase the output impedance. Part of the tail current source is split off to enable common-mode regulation of the differential

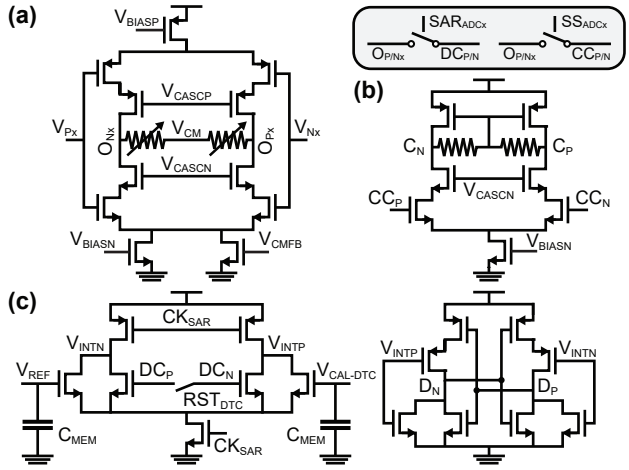

Figure 4.10: (a) Schematic of the pre-amplifier with switches to second stages. (b) Schematic of the continuous-time comparator. (c) Schematic of the discrete-time comparator.

amplifier with a small auxiliary amplifier sensing the output nodes. The structure can be configured to be part of the SAR and SS comparison by adjusting the impedance at the output nodes, O_{Px} and O_{Nx}. During slope conversion, a high impedance is set to provide a first gain stage for the CTC while during SAR conversion a low impedance is implemented to enhance the amplifier bandwidth and SAR timing.

A second gain stage is used in the SS phase to amplify small slope residuals to logic levels within the conversion time. The differential amplifier has a passive common-mode feedback architecture and tail cascodes to increase the output impedance as shown in Fig. 4.10(b). The DTC in Fig. 4.10(c) is based on [51] and, despite the pre-amplifier, still employs an additional dynamic pre-amplifier as the benefit from shielding the continuous pre-amplifier outputs from kick-back during slope conversion outweighs the added cost. It can, moreover, be used to calibrate the offset of the DTC similar to [52], first-order matching the SAR and SS stage offsets given that the large pre-amplifier gain during SS conversion significantly reduces the impact of the second stage continuous amplifier offset.

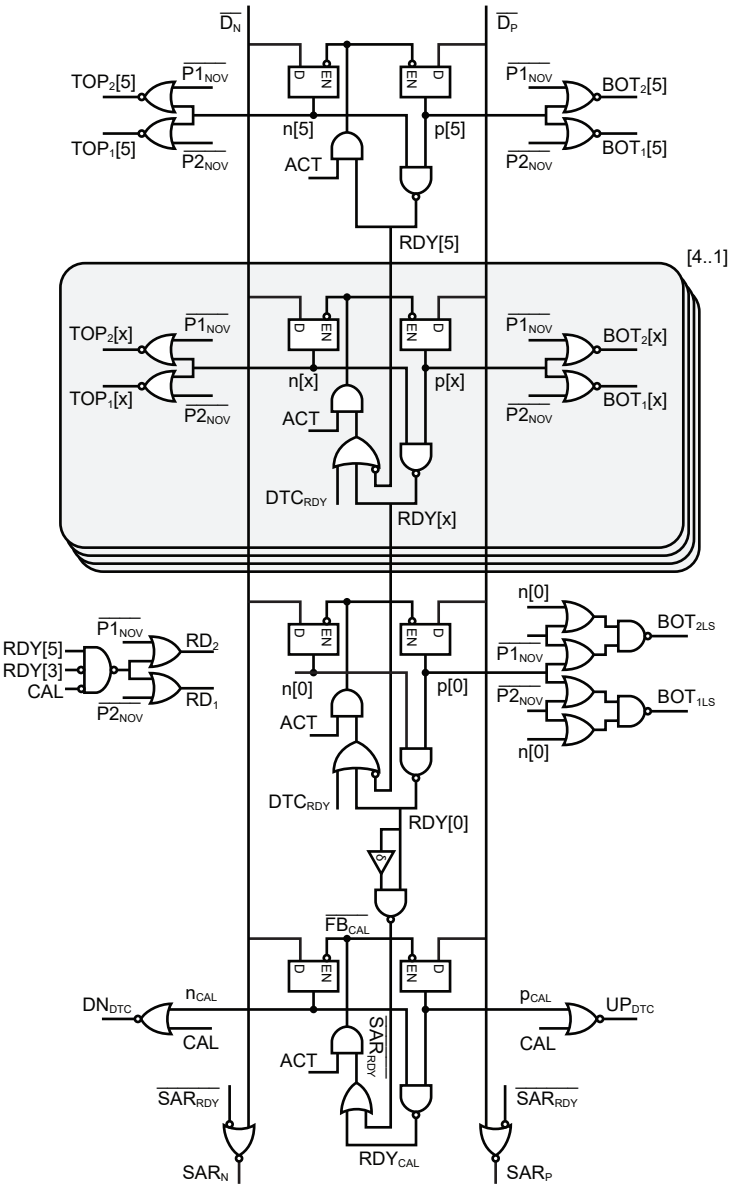

Figure 4.11: Asynchronous ADC logic core determining the CDAC switching, SAR output code and discrete-time comparator calibration.

4.3.3. Logic & CDAC

Fig. 4.11 shows the logic controlling SAR switching. An overview of the CDAC is given in Fig. 4.12(a) and example conversions of one positive and one negative

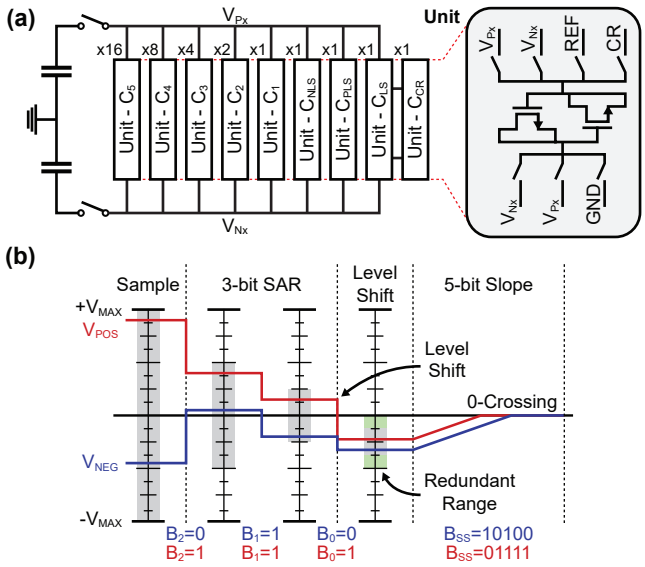

Figure 4.12: (a) Overview of the SAR DAC with unit cell details. (b) Exemplary conversion diagram showing the residual on the sampling capacitors.

input are illustrated in Fig. 4.12(b). The DAC has a binary scaled section, $C_{5..1}$, for the 6-bit SAR conversion and is controlled with TOP_x and BOT_x to switch the unit in either to raise or lower the difference between V_{Px} and V_{Nx}. The structure is laid out symmetrically as multiples of a unit cell to mitigate effects such as mismatch and charge injection. The unit capacitance in the pre-charged state is about 7 fF and five times lower when depleted. Charge-redistribution to create binary charge levels without an exponentially growing CDAC, as in [53], is only applied to generate a level half of C_1. This is used to shift the SAR residual to the middle of the redundant range for slope conversion because matching of that level has less impact on the converter linearity. The process is realized by first including C_{CR} during the pre-charging of the CDAC with Px_{NOV} and then, controlled by RD_x, sharing its charge with the unit used for level-shifting, C_{LS}, through the shared node CR. This is done between the first and third SAR comparison unless SAR or SS calibration is performed. Regardless of the outcome of the last SAR bit, C_{LS} is always switched in to lower the residual with BOT_{xLS}. The last SAR bit decision does however influence the switching of the two remaining DAC units, the regularly pre-charged C_{PLS} and the empty unit C_{NLS}, as shown in Fig. 4.13(b). In regular operation, C_{PLS} is switched in for a positive SAR residual, effectively

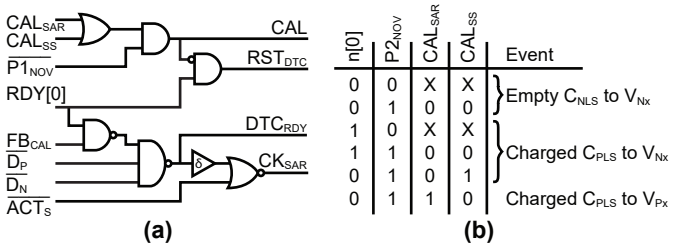

Figure 4.13: Asynchronous dynamic comparator clock as well as reset generator schematics in (a) and level shifter state diagram in (b).

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mapping it onto the negative range as it is similar to C_1 in charge. C_{NLS}, on the other hand, is switched in with the same polarity but only for negative SAR residuals with the purpose of closer matching of the voltage attenuation posed by the CDAC for both cases. The process is illustrated in Fig. 4.12(b) and enables the slope to always run in the same direction, reducing the SS complexity.

The SAR logic is based on latches due to their area efficiency and works together with the asynchronous DTC timer in Fig. 4.13(a). To ensure locking of the result of a DTC decision and settling of the CDAC before the next comparison, an additional delay is introduced in the SAR clock generator. To also avoid sampling more than one bit per comparator decision, delay cells could be added between the stages of the SAR logic. But in this design, it is instead chosen to lock the stages with DC_{RDY} to save power and area. In order to still function well in the case of an over-ranging SS conversion, the whole latch array is cleared with ACT and the SAR clock CK_{SAR} is halted by the set active signal ACT_S. This makes sure that there is no switching of the CDAC before the correct sample is applied and that the new SAR conversion only begins after the correct comparator is switched in.

4.3.4. Calibration

The last stage of the SAR logic is used to calibrate the offset of the DTC. After the last SAR comparison, the pre-amplifier is disconnected and the input of the DTC is shorted together with RST_{DTC}, such that the following comparison samples the polarity of the offset [15]. To optimize the precision, the next comparison is not triggered regularly but delayed by halting the seventh CK_{SAR} pulse of the SAR cycle, effectively enhancing settling. This is achieved with a delayed SAR_{RDY} and FB_{CAL} signal, as shown in Fig. 4.11. The sampled offset polarity is then used to

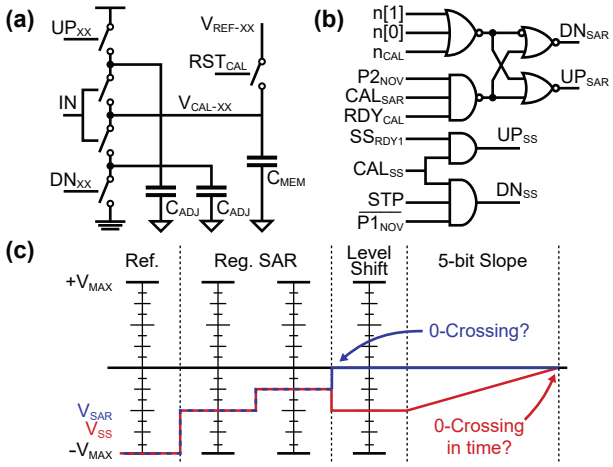

Figure 4.14: Conceptual diagram of the calibration charge pumps in (a), the related SAR and SS controls in (b) and calibration switching overview in (c).

switch the control inputs of a regulator for the $V_{CAL\text{-}DTC}$ node of the DTC, UP_{DTC} and DN_{DTC}. All calibration circuits in this design work in a negative feedback loop and with charge pumps as conceptually displayed in Fig. 4.14(a). The comparator calibration can, except for during SAR or Slope calibration, determined with CAL, always run in the background but isn't required to complete each conversion cycle. To minimize the chance of losing synchronization with the periphery, and therefore one PE cycle, the calibration step is therefore not required for setting ADC_{RDY} and is skipped without harming the operation if there is a seventh SAR decision that takes a long time to converge.

The SAR and SS references are additionally calibrated to adjust for inter-stage gain errors, process mismatch and temperature variation. The procedure first follows regular SAR operation with a negative full-scale reference input provided through the PGA and then makes use of the C_{PLS} DAC unit cell to assess the current status. As listed in Fig. 4.13(b) and illustrated in Fig. 4.14(c), it is used to either fully reduce the residual to zero for SAR calibration or, for slope calibration, to get a residual equal to the maximum SS input, including the redundant range. Using the same cell, just with different polarity, enables accurate slope calibration to the maximum SAR residual range irrespective of a pre-amplifier offset. However, as the offsets of the two pre-amps can be different, calibration is only obtained with one DAC. The other part of the shared ADC structure still performs DTC offset cancellation in parallel. While this one-sided calibration generally introduces an

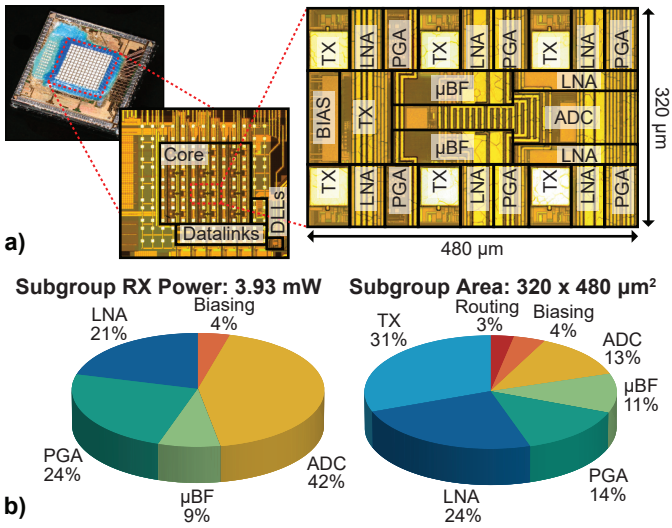

Figure 4.15: (a) Micrograph of the chip including transducer matrix array with magnifications of the core and subgroup areas. (b) Distribution of receive power and area per subgroup of 3×2 elements.

offset between the two converters due to pre-amplifier offset differences, there are no implications from DAC mismatch beyond regular linearity investigation and no significant performance difference could be measured between shared structures.

The modified residuals are ultimately used to first adjust the SAR reference, $V_{\text{CAL-SAR}}$, based on detecting whether there was a zero-crossing in the seventh comparator decision. This is realized by checking the three least significant bits (LSBs) of the SAR ADC, as shown in Fig. 4.14(b). The additional delay for improved settling in the seventh comparator cycle is still applied while the comparators are not switched early to ensure the calibration completes. The slope control voltage, $V_{\text{CAL-SS}}$, on the other hand, is adjusted based on letting the full residual run in a regular SS operation. It is then detected if it was completed early with SS_{RDY1}, or needed to be stopped with STP.

4.4. Experimental Results

The reported design has been fabricated in a 0.18-µm HV BCD process with an active area of about 1.8 mm^2 for the 8×9 element core and about 0.8 mm^2 for the periphery circuitry. A chip with a prototype transducer array manufactured on

its surface is shown in Fig. 4.15(a). It measures 5×5 mm^2 to ease the prototype transducer manufacturing and includes two rings of dummy transducers to reduce edge effects of the small array. The array is designed to have a center frequency of 6 MHz and a fractional bandwidth in the order of 50%. A magnification shows the pitch-matched floor plan of a 3×2 element subgroup consisting of element-level pulsers, two 3×1 element subarray beamformers and two hardware-sharing ADCs. The transmit circuits operate from a 65-V HV supply, a 5-V supply to drive the pulser transistors and a 1.8-V supply for logic-level control. All receive circuitry is powered from a 1.8-V supply with the addition of a 1.2-V supply for the DLL delay cells and a 2.3-V supply for the SAR reference. An overview of the area and receive power distribution per subgroup is given in Fig. 4.15(b). Due to area-intense HV isolation, the pulser circuits (TX) occupy the largest part of the subgroup area with 31 %, while the hybrid ADCs cover only 13 % of the space and consume about as much power as the analog frontend. As the TX operation has a very small duty cycle, the total power consumption is dominated by the receiver, with 0.65 mW/element in the core and 1.23 mW/element including the datalink and LVDS drivers.

Electrical and acoustic experiments have been conducted. The chips are wire-bonded to separate daughter boards and samples for electrical characterization have additional wire-bonds to connect transducer pads to the PCB while acoustic samples have a co-integrated transducer array. All daughter boards are mounted on a common, custom mother board that is connected to a commercial FPGA [54]. Measurements are conducted by observing the ADC outputs as provided through the datalink, received by the FPGA and forwarded to a PC. Characterization of the TX part has previously been shown in [35] and is not covered in this section.

4.4.1. Electrical Measurements

The characterization of the receive transfer function shown in Fig. 4.16 is obtained by providing sinusoidal inputs of varying frequency to the transducer pads from a waveform generator and referring the ADC output to the output of the AFE. The circuit shows the expected mid-band gain range of 54 dB in 10 steps from -6 dB to 48 dB with an 8.1-MHz cut-off frequency in the highest gain setting. The difference among the gain steps in low-frequency roll-off is caused by the feedback configuration and does not affect the imaging as the output is filtered around the center frequency of the transducer. Fig. 4.17(b) shows the time-domain recording

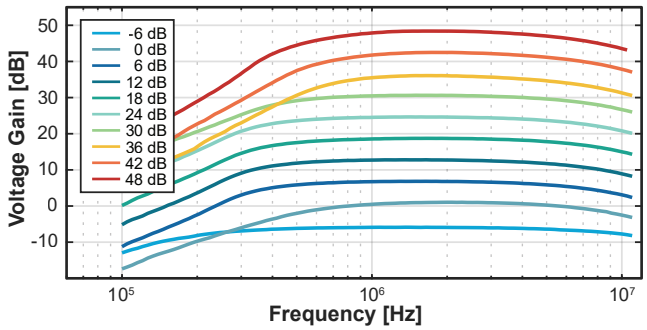

Figure 4.16: Receive transfer function measured across frequency for all gain settings of the analog frontend.

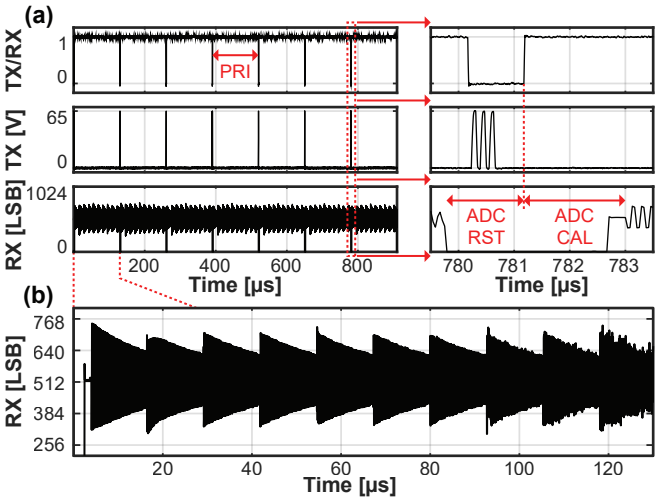

Figure 4.17: (a) TX/RX control, TX voltage and RX output code recorded with the intended pulse-repetition-interval (PRI), with zoom-in of the switching period. (b) Recording of one RX output with an exponentially decaying sinusoidal signal at the analog frontend input and active time gain compensation.

of an ADC output code with an exponentially decaying 6-MHz sinusoidal signal provided at the input of the analog frontend. By switching through the 10 gain settings of the analog frontend, the output amplitude can be kept within the observable range, verifying functional time-gain compensation within one receive period, with a small settling time after gain switching. Combined with the ability to operate at the intended PRF of 7.7 kHz, corresponding to a pulse-repetition-interval (PRI) of 130 µs, as demonstrated in Fig. 4.17(a), this verifies that the chip

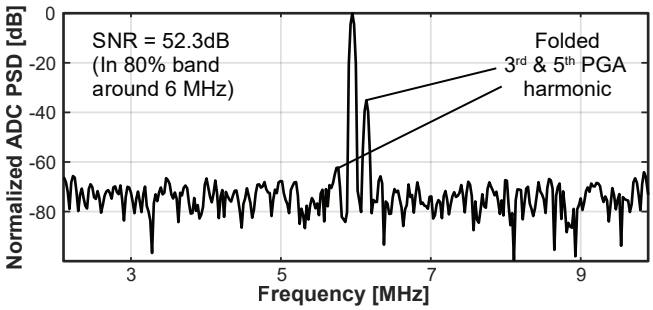

Figure 4.18: Power spectral density plot showing the peak SNR of the entire receive signal path with a 5.95-MHz sinusoidal input to the analog frontend.

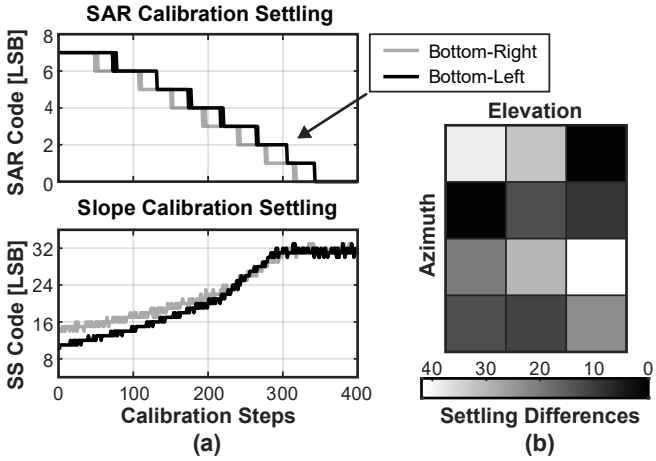

Figure 4.19: (a) Example of the SAR and SS calibration procedures of two different ADCs. (b) Heatmap showing the relative difference in the total calibration settling time from a common starting point across the ASIC.

enables recording of the full imaging depth at the targeted frame rate.

The peak ADC output power spectral density is shown in Fig. 4.18, measured with a 5.95-MHz sinusoidal signal from a waveform generator. As the waveform is provided at the analog frontend input, the whole receive path is characterized to a peak SNR of 52.3 dB, with a folded -35-dB third and -62-dB fifth harmonic from the PGA output stage in an 80 % bandwidth around the transducer center frequency.

A test mode in which the ADC output of one channel can be read without recombination of the SAR and slope output data is employed to follow the ADC

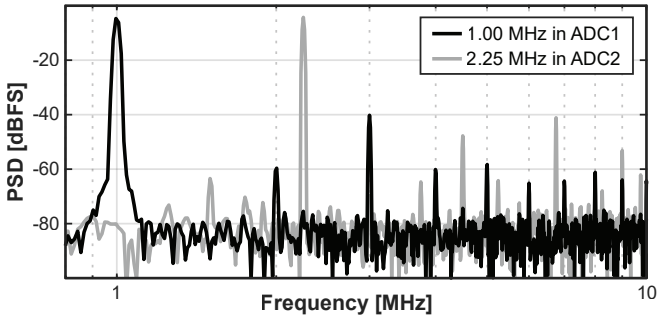

Figure 4.20: Interference test showing the power spectral densities of both outputs of one shared ADC structure with concurrent 1-MHz and 2.25-MHz inputs.

calibration procedures. The global starting potentials for the SAR and slope reference can be individually set in a reset state and are prior to this test placed away from the final settling points. Fig. 4.19(a) shows how the SAR and slope local calibration nodes converge to the final values at the example of the bottom-right and bottom-left output codes of the SAR and slope stage. The SAR algorithm tries to fully reduce a full-scale input, leading to a settled value at an output code of zero. The slope algorithm, on the other hand, adjusts the slope current to detect the zero-crossing of a full-scale slope stage input just at the end of the associated time interval and therefore settles around the maximum slope output code. An overview of the combined SAR and slope calibration time until a settled state is reached from the same starting point is shown per shared ADC structure in Fig. 4.19(b), giving an indication of the channel-to-channel mismatch.

To investigate how the high integration density, as well as hardware-sharing within each subgroup and at the periphery, affect the cross-talk between channels, an electrical measurement, studying the outputs of the two co-integrated subgroup ADCs, is performed. Their inputs can be accessed separately and are concurrently driven by two outputs of a waveform generator, in this example at 1.00 MHz and 2.25 MHz. The corresponding output spectra of the two ADCs are both plotted in Fig. 4.20 and show no significant tones at the fundamental or harmonic frequencies of the other channel. This implies that a circuit cross-talk better than -75 dBc is achieved and that other sources like mechanical cross-talk in the transducer array should be dominant.

Table 4.1 summarizes the performance of the hybrid ADC and gives a comparison to the state-of-the-art. In contrast with general-purpose converters, this

Table 4.1: Prior Art comparison in miniature ultrasound probe ADCs

	This Work	JSSC'21 [32]	VLSI'19 [33]	JSSC'18 [15]
Technology	**180 nm BCD**	180 nm	180 nm	180 nm
Architecture	**SAR & SS**	SAR	SAR & SS	SAR
Resolution	**10 bit**	10 bit	10 bit	10 bit
Sample Rate	**24 MHz**	20 MHz	30 MHz	30 MHz
Low BW Driver	✓	×	×	✓
Reference Included	✓	×	×	✓
Area *	**0.010 mm²**	0.026 mm²	0.013 mm²	0.046 mm²
Power *	**0.82 mW**	1.23 mW	1.14 mW	1.42 mW

* Per Subarray

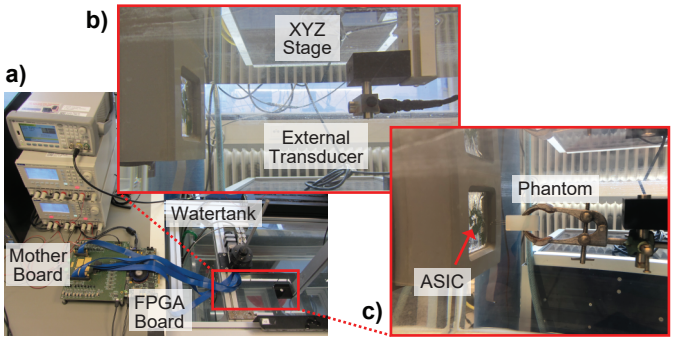

Figure 4.21: (a) Overview of acoustic measurements setup. (b) Inset showing watertank with external transducer. (c) Imaging experiment details.

design implements several application-oriented features like direct integration with a subarray beamformer, allowing for a low-bandwidth ADC driver, and including a low-bandwidth SAR reference. Therefore, Table 4.1 compares the design with prior ADC designs targeting miniature ultrasound probes. Set against the most comparable design [15], the ADC occupies more than 4x less area and consumes more than 1.5x less power. Even in comparison with the more general designs [32], [33], the efficient architecture enables the lowest reported area and power consumption.

4.4.2. Acoustic Measurements

An overview of the acoustic measurement setup is given in Fig. 4.21(a). All acoustic measurements are obtained with the daughter-board and ASIC with transducer array directly interfacing with a watertank. Fig. 4.22 shows the input-referred voltage noise spectral density in the highest gain setting with the transducer ele-

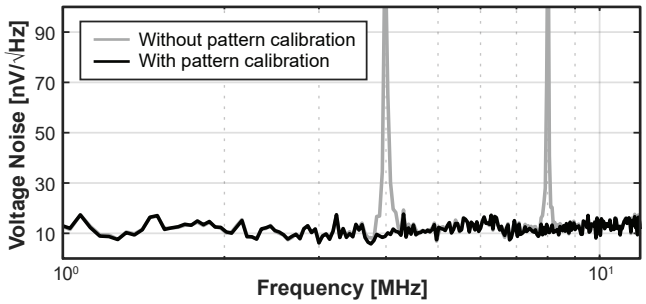

Figure 4.22: Input-referred spectral voltage noise density with and without calibration of the static mismatch pattern of the subarray beamformer.

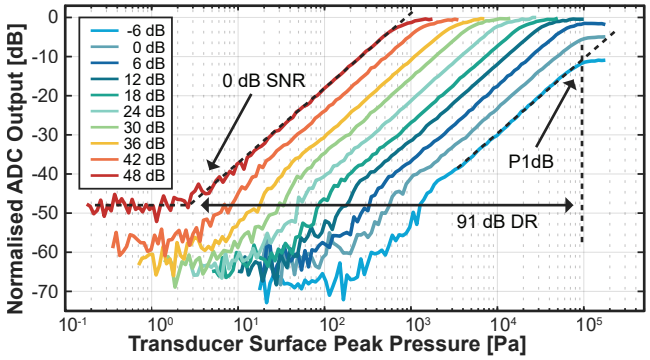

Figure 4.23: ADC output measured during sweep of the transducer surface pressure in all gain settings, showing a 91-dB dynamic range.

ments loaded by water. Two tones appear in the spectrum at $f_s/6$ and its second harmonic, f_s being the sampling frequency of the ADC. These are generated by mismatch of the subarray beamforming cells and can be removed by recording and subtracting the static pattern as shown. The input-referred voltage noise density is 12.7 nV/$\sqrt{\text{Hz}}$ at 6 MHz, around 5 nV/$\sqrt{\text{Hz}}$ higher than what the electronics are designed for, with the difference being attributed to the thermal noise of the transducer.

Fig. 4.23 displays a sweep of the transducer surface peak pressure with measured ADC output for all gain settings, used to characterize the dynamic range of the receive path. The pressure waves are generated from an external commercial transducer [55] connected to a waveform generator that transmits sinusoidal waves at 5.5 MHz as shown in Fig. 4.21(b). The displayed surface pressure is calibrated with a commercial hydrophone [56] with known sensitivity in the place of the ASIC

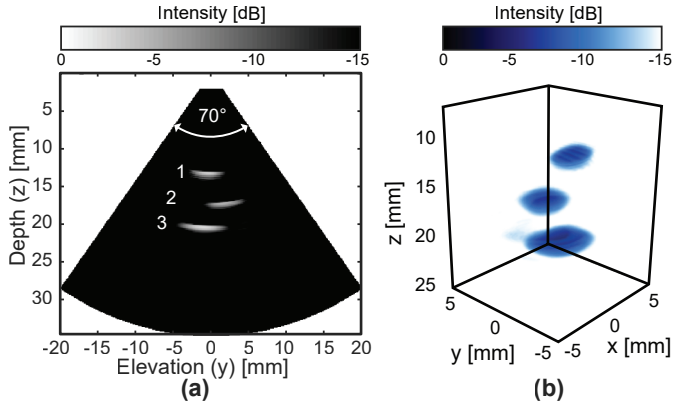

Figure 4.24: (a) Elevation plane image of the 3-needle phantom recorded at 1000 volumes/s with the prototype. (b) Rendered 3D image of the same recording.

before the measurement. A total dynamic range of 91 dB is recorded between the 0-dB SNR point of the highest and the 1-dB compression point of the lowest gain setting.

An overview of the measurement setup used for imaging experiments is given in Fig. 4.21(c). A phantom of three needles with a total spacing of 7 mm is immersed in a watertank about 13 mm from an acoustic window used to interface with a daughter board carrying a chip with co-integrated transducers. Cables with a length of 1 m connect the PCB assembly to an FPGA board that receives the high-bandwidth LVDS data via a motherboard and forwards it to a measurement PC that performs the image reconstruction based on conventional delay-and-sum operations. In seven transmit/receive cycles, the ASIC first excites 6-MHz pressure waves with 65-V pulses and then records generated echoes from the phantom with the seven subarray beamformer settings. Fig. 4.24 shows the resulting image once in an elevation plane in (a) and once as a rendered 3D image in (b). While the aperture is too small to provide the resolution of a full array, the needle heads can clearly be distinguished in 3D space, demonstrating the functionality of the prototype.

A summary of the system characteristics and comparison to the prior art in catheter-based ultrasound systems [6], [15], [32], [33], [40] is provided in Table 4.2. This work describes the first design to integrate element-level HV transmitters and analog frontends, subarray beamforming, and in-probe digitization in a scalable fashion for 3D imaging. A dedicated architecture enables the highest reported

TABLE 4.2: COMPARISON WITH THE PRIOR ART IN CATHETER-BASED ULTRASOUND IMAGERS

	This Work	JSSC'21 [32]	JSSC'20 [40]	VLSI'19 [33]	JSSC'18 [15]	TUFFC'16 [6]
Technology	**180nm BCD**	180nm	180nm BCD	180nm	180nm	N/A
Transducer	**2D PZT**	2D PMUT	1D CMUT	2D PZT	2D PZT	2D PZT
Array Size	**8 × 9**	6 × 6	64	4 × 4	6 × 24	60 × 14
Integrated Transducer	✓	✗*	✓	✓	✓	✓
Center Frequency	**6 MHz**	5 MHz	7 MHz	5 MHz	5 MHz	5.6 MHz
Pitch-matched	✓	✗†	✓	✓	✓	✓
Element Pitch	**160 µm × 160 µm**	250 µm × 250 µm	205 µm × 1800 µm	150 µm × 150 µm	150 µm × 150 µm	110 µm × 180 µm
Integrated TX	✓	✓	✓	✗	✗	✓
Max. TX Voltage	**65 V**	13.2 V	60 V	N/A	N/A	40 V
Digitization	✓	✓	✗	✓	✓	✗
Receiver Architecture	**AFE + µBF + ADC + Datalink**	AFE + ADC	AFE	AFE + ADC	AFE + µBF + ADC + Datalink	AFE + µBF
Channel Reduction	**12-fold**	N/A	N/A	N/A	36-fold	15 to 20-fold
Supported Frame Rate	**1000 vol/s**	N/A	N/A	N/A	200 vol/s	50 vol/s
Active Area / Element	**0.032 mm²** §	0.063 mm²	0.464 mm²	0.023 mm²	0.026 mm² §	N/A
RX power / Element	**1.23 mW** §	1.14 mW	5.2 mW	1.54 mW	0.91 mW §	< 0.12 mW
Input DR	**91 dB**	N/A	82 dB	N/A	85 dB	N/A
Peak SNR	**52.3 dB**	57.8 dB ‡	N/A	49.8 dB	52.8 dB	N/A

* Transducers on separate board connected with wires.
† Scalability limited by transducer connection outside of pitch.
§ Including the Datalink and LVDS drivers.
‡ ADC only, excluding AFE.

frame rate with a channel-count reduction sufficient to enable an array with less than 100 data channels in the catheter when scaled to the full size.

4.5. Conclusion

A transceiver ASIC combining HV transmission with subarray beamforming and in-probe digitization for catheter-based 3D ultrasound probes has been presented. A pitch-matched design is facilitated by an area- and power-efficient hybrid beamforming ADC tailored to the application in large imaging arrays. The novel architecture enables a high frame rate of 1000 volumes/s while also providing sufficient data channel reduction through subarray beamforming and time division multiplexing. A prototype with a co-integrated transducer matrix has been manufactured and successfully applied in a 3D imaging experiment. Together with competitive power consumption and large dynamic range, the system is a promising solution for future miniature ultrasound probes.

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5

A high-frame-rate ultrasound ASIC with multi-level load modulation datalink

This chapter is based on the publication "A Pitch-Matched High-Frame-Rate Ultrasound Imaging ASIC for Catheter-Based 3D Probes" in preparation for publication in the IEEE Journal of Solid-State Circuits.

5.1. Introduction

Ultrasound imaging is a popular tool in medical treatments due to its relatively safe nature, cost-effectiveness, and compatibility with minimally invasive interventions [1], [2]. A special class of imaging devices used for the latter are catheter-based probes. These enable high-resolution images taken directly next to the area of interest in the body. The probes are disposable and purpose-built for their application in procedures like intravascular ultrasound (IVUS) [3] or intracardiac echocardiography (ICE) [4], [5]. While IVUS is commonly used in procedures such as plaque detection in the vascular system and can typically work with a

smaller imaging array [6]–[8], ICE is applied in a variety of cardiovascular interventions with more demanding requirements on the imaging depth and resolution [9], [10].

Particularly in upcoming 3D probes with 2D transducer arrays, these requirements lead to significant challenges in the design of ICE catheters. While 2D imagers with 1D transducer arrays commonly apply passive probes with direct element connection to the imaging system [11], [12], the higher cable count, crosstalk and attenuation across thinner cables for 2D transducer matrices lead to the application of ASICs in ultrasound imaging catheters [9], [13]. The basic functionality of the electronics includes ultrasound transmission (TX) and reception (RX) on each array element to maximize the imaging aperture in the limited space of the catheter, amplification of the received echoes for robust signal transmission, and communication with an imaging system outside the body [14], [15]. But as for 3D imaging, the transducer pitch in the azimuthal and elevation direction has to be designed for low impact on image quality [10], there is little space for circuitry that is matched to the pitch of the transducer. A pitch-matched design is a requirement for scalability to the about 1000 elements of a full 3D ICE design [9], [10] but leads to a high requirement on the integration density of the circuits. Prior 3D ICE designs have thus been limited to a subset of the desirable functionality as they could not integrate transmit beamforming [15], only low-voltage transmission [16], no transmit functionality at all [17], [18], or had to strongly limit the achievable volume acquisition rate [9].

The biggest challenge in the transition to 3D probes is posed by the communication with the imaging system. Catheters with a diameter of around 3 mm have to accommodate all TX and RX channel signals next to common connections like power and additional controls [9]. To reduce the number of TX cables, pulses are often generated on the ASIC. The configuration data can be provided via a serial link into local registers [19]–[21] or an efficient shift register (SR) [14], [22] before the next TX phase and delays for TX beamforming can be generated with local counters. However, this leads to large registers and counter cells for a dense array with a large number of delay steps. An alternative is to implement TX control in a row/column (R/C) approach [23]–[26]. This minimizes the amount of associated circuitry underneath the element but, in turn, limits the amount of possible TX patterns for application in a 3D ICE probe. A similar challenge is faced when externally generated pulses are only passed or blocked on the chip instead of local pulse generation [8], [25], [27].

Reduction of RX cables in the catheter has previously been achieved by multiplexing of transducer signals on fewer connections over multiple transmit/receive (T/R) cycles [27], [28]. To avoid the associated loss in frame rate, other designs have made use of the wider bandwidth of the channel compared to the imaging frequency. In these, several RX signals are multiplexed on a single connection within one T/R cycle [29]–[31]. While if applied for sensitive analog signals, the channel-to-channel crosstalk can become an issue [32], particularly for digital signals, this can be done with a low impact on the signal integrity [15]. Nevertheless, the limited bandwidth across thin cables in the catheter restricts the maximum cable-count reduction achievable with this method in both cases.

Another approach is to apply subarray beamforming, also known as microbeamforming (μBF) [33]. This shifts part of the RX beamforming into the catheter by delaying and summing the received signals of a subarray of elements. However, it comes at the cost of less raw data being available in the final image reconstruction and reduced frame rate as multiple acquisitions are required per reconstructed volume [34]. While the former limits the effectiveness of imaging algorithms, the latter can preclude the use of modes like high-frame-rate blood flow or electromechanical wave imaging [35]. These disadvantages can be mitigated while achieving significant cable-count reduction by a combination of subarray beamforming and digital time-division multiplexing. This has been shown with element-level digitization with subsequent digital beamforming [36], [37], digitization of the output of analog beamformers [15], [18], [38], and mixed schemes [39]. However, even more can be gained from the digital transmission as ultrasound imaging can tolerate higher bit error rates (BER) than most communication links [40]. While current digital probe designs commonly rely on conventional low-voltage differential signaling (LVDS) [15], [17], [18], [41] with relatively low BER, BER could potentially be traded to reduce the circuit area and power consumption. Moreover, it could allow for a lower cable count by dividing the total output data bandwidth across fewer channels with a higher transmission rate.

An additional aspect to consider in the design of the amplification for large transducer arrays is the common-mode interference across the channels. Each individual frontend amplifier actually has a reduced noise requirement before it limits the global performance as the transducer noise increases with decreasing size [42], [43]. The uncorrelated noise can then still reveal weaker signals after beamforming in the imaging system with an SNR gain of $\sqrt{N}$ for N combined signals [44]. As more elements are summed for a smaller pitch, the final signal-to-noise ratio

is, to first order, equal for different element sizes in a transducer array of a given size [45]. But correlated noise between channels effectively reduces the maximum gain achievable through beamforming, meaning it should remain well below the noise floor despite the larger number of channels. This challenging requirement of ultrasound frontend design has received little attention in the scientific literature.

In this chapter, a pitch-matched ASIC with a co-integrated transducer array with a pitch of 160 µm × 160 µm is presented. The design builds on the foundation laid in [15] with a 4x larger array and novel circuitry to form a comprehensive ultrasound imager architecture. On-chip TX control is implemented by a compact combination of an R/C and an SR approach that offers all required beam patterns. Additional area savings are achieved by encoding the delay of the TX beamformer as the difference from its neighbor, similar to [21], and re-using the shift-register cells as counters for delay generation. Local biasing schemes for the transducer and analog frontend (AFE) amplifiers enable quick settling of the input after the TX phase and a lower impact of correlated noise on the final image. Additionally, a multi-level pulse amplitude modulation (PAM) channel combined with TDM and µBF achieves an RX cable-count reduction of 18 while still enabling a high frame rate of 1000 volumes/s. To reduce the heating of tissue in the patient, the driver is implemented as a load modulation (LM) architecture, reducing the power consumption of the channel at the tip of the catheter.

This chapter is organized as follows. The architecture and system design considerations are described in Section 5.2. Section 5.3. provides circuit implementation details on the TX beamformer, analog frontend, and LM data transmission. The fabricated prototype, measurement setup, and results are discussed in Section 5.4. The chapter concludes with a comparison to the prior art and a conclusion.

5.2. System Design

5.2.1. Overview

Fig. 5.1(a) provides an overview of the developed system. A matrix of 16×18 transducer elements is designed for directly interfacing the presented ASIC as shown in Fig. 5.1(b). The array is 4x larger than that presented in chapter 4 and equivalent to a quarter of the aperture of the envisioned final ICE probe. The 160-µm-pitch transducer stack is a revised version of the concept shown in [46]. The circuitry interfaces with the PZT elements through individual connections made

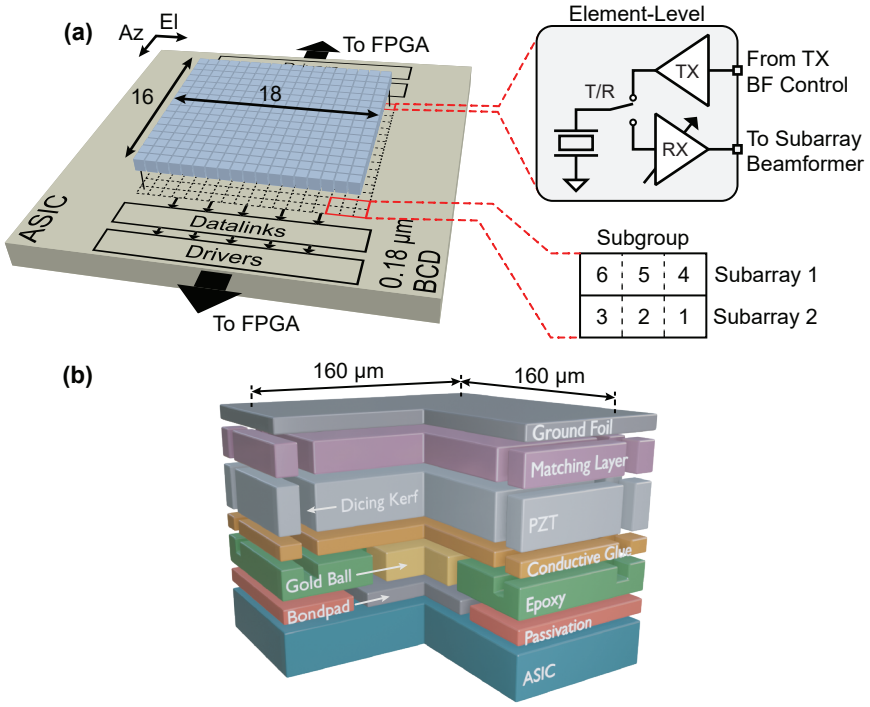


Figure 5.1: (a) Conceptional drawing of transducer stack. (b) Overview of chip assembly with details on the matrix organization.

with a gold contact on the bottom side and a common aluminum ground foil on the top.

On the side of the chip, implementation in a 0.18 µm BCD technology offers a trade-off between the ability to integrate high-voltage (HV) TX-related structures and low-voltage (LV) logic as well as RX-related structures. Each element is connected to individual TX and RX paths to efficiently use the space inside the catheter. An isolating T/R switch between the two paths protects the receiver from HV breakdown during transmission. The receiver also implements time gain compensation (TGC) to manage the dynamic range (DR) requirement of ICE. While imaging is often done with a range of only 40 dB, ultrasound attenuation inside the human body can lead to a total DR in the order of 100 dB within one T/R cycle [15]. But as the attenuation is time-dependent, TGC can still reduce the DR to the following components by complementing it with a time-varying gain [13]. The matrix is further grouped into subarrays of three elements each and subgroups of two subarrays each. To enable a frontend layout matched to

the pitch of the transducer element, all backend circuitry, such as the datalinks and data output drivers, are pushed to the periphery. This enables the design of subgroups as unit cells that can be replicated to create a larger aperture. The periphery-level circuitry is designed in units as well and only occupies two sides, the top serving the upper and the bottom serving the lower half of the matrix, to allow scaling along one direction.

This design serves as a prototype to evaluate the architecture and shown techniques for application in a full ICE probe. While all of the functionality required for the realization of the 64×18-element imaging scheme presented in chapter 2 is included, only one-fourth of the aperture in the azimuth direction is accommodated in this step. To characterize the performance of the 1D subarray beamformer in the elevation direction and the imaging approach, the full aperture is implemented along that axis. The beamformer of just three elements enables a high frame rate as only few acquisitions are required per volume. The full probe targets a 10-cm imaging depth and thus operates at a pulse-repetition-frequency (PRF) of 7.7 kHz considering the speed of sound in human tissue. Being able to image with just seven fan-shaped beams per frame, this results in a total frame rate of up to 1000 volumes/s. The seven steps employ a TX beam with 10.7° divergence in the elevation and 70° divergence in the azimuth direction and steer the subarray beamformer in a ±30°-window in the elevation direction accordingly to achieve a field of view of 70°×70°×10 cm [10].

5.2.2. Architecture

Fig. 5.2 shows the architecture implemented in the presented design. The topology is building on what has been discussed in chapter 4 and the TX part is based on the unipolar pulser with embedded T/R switch introduced in chapter 3. In this design, control of the TX beamforming (TX BF) is realized with per-element digital delay cells that are configured in a mixed scheme: While global steering information is provided on the level of rows or columns of elements to save area, individual control is supplied by a shift register spanning the whole matrix. To minimize the number of connections inside the catheter, the shift register is also used to load the row and column data as well as all global configuration settings. The entire shift register content of about 1.5 kb can be loaded in around 15 µs at a clock frequency of 100 MHz. The SR is updated during the RX period and thus forms an upper limit to the PRF at about 66 kHz, irrespective of the imaging depth.

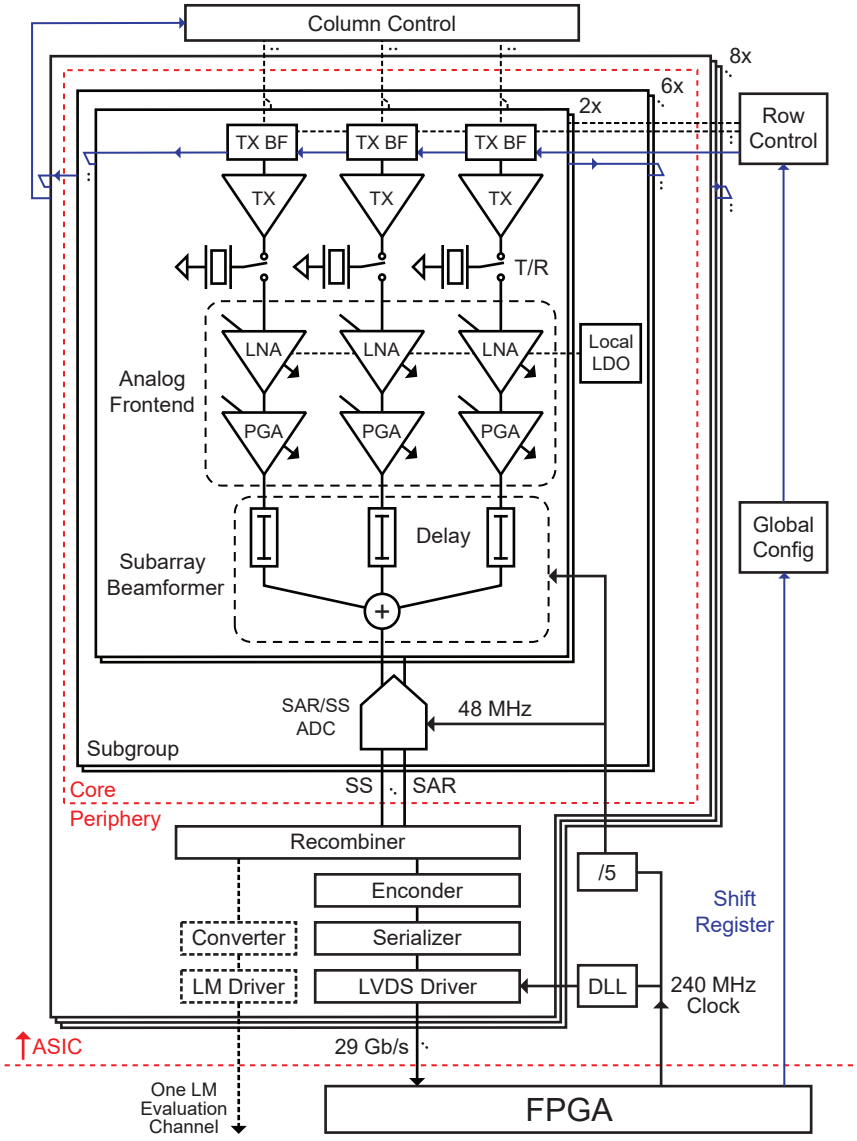


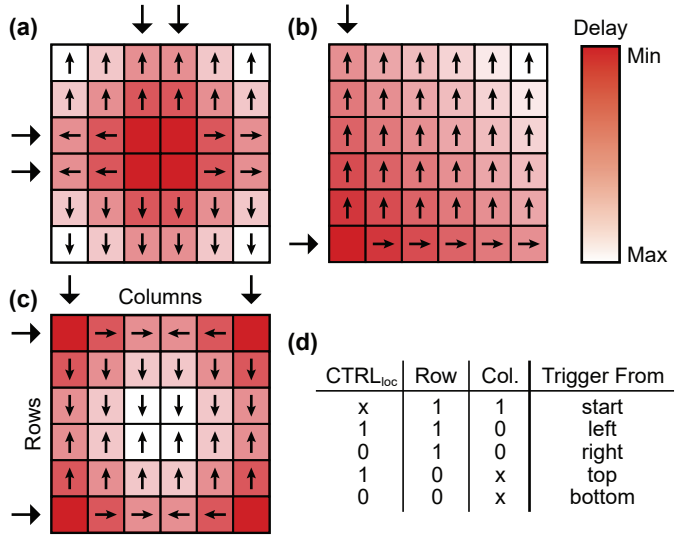
Figure 5.2: Architecture overview showing how element-level circuitry, subarray beamformers, and a shared ADC structure per subgroup are combined. The arrangement of the shift register and row/column approach is sketched and a global view of the data management and clocking is provided.

On the receiver side, each element is individually connected to a low-noise amplifier (LNA), followed by a second-stage programmable gain amplifier (PGA) that

also acts as a single-ended-to-differential converter. The LNA can be discretely switched in steps of 18 dB from -12 to 24 dB and the second stage can be configured in steps of 6 dB from 6 dB to 24 dB. Together, they implement TGC with a range of 54 dB in 10 steps of 6 dB from -6 dB to 48 dB. The LNA architecture is a modified version of the design in [47] to enable operation with HV transmitters and seamless gain switching during echo reception. As the received signal is most sensitive at this point, a local regulator for the LNA supplies is installed on the subgroup level here as well to reduce the effect of common interference across the whole array. The PGA is based on [48] and [18], again adapted to get full TGC range within one T/R cycle and thus full frame rate.

The digitization from chapter 4 is adopted with the same parameters in this design since both implementations target the same application. Three elements are combined in the elevation direction for analog subarray beamforming in the charge domain. Two neighboring subarrays are combined for layout with a shared hybrid beamforming analog-to-digital converter (ADC) in a subgroup. The ADC combines a successive approximation register (SAR) first stage and single-slope (SS) second stage and operates at 24 MSps per channel with a resolution of 10 bits. To allocate all hardware in the core, the SAR and SS outputs are individually transferred to the periphery.

On the periphery, two datalink configurations have been included. The regular one features recombination of the SAR and SS output to 10-bit words, 8b10b encoding [49], and serialization to conventional LVDS drivers. In the process, 4-fold time division multiplexing (TDM) is applied, leading to a rate of 1.2 Gbps per channel and, together with 3-fold subarray beamforming and considering the differential nature of the signals, a total cable count reduction factor of 6. The second setup only serves one channel and provides a parallel path from the recombination to a multi-level encoder and an LM driver. This enables conventional access via field-programmable gate arrays (FPGAs) [50] to the whole array for convenient imaging while providing an evaluation platform for the novel datalinks discussed in Section 5.3.4. The periphery and core are timed by shared dividers and delay-locked loops (DLLs) working on a 240-MHz clock provided by the FPGA.



$CTRL_{loc}$	Row	Col.	Trigger From
x	1	1	start
1	1	0	left
0	1	0	right
1	0	x	top
0	0	x	bottom

Figure 5.3: (a)-(c) Examples of TX beamformer delay patterns with arrows indicating the delay propagation for a 6×6 array: Centered diverging wave, diagonal plane wave & focused wave. (d) Decision table for the delay propagation based on shift register and row/column input.

5.3. Circuit Implementation

5.3.1. TX Beamformer

To achieve a compact TX BF implementation, the system operates by passing a single trigger signal through the entire array based on relative delays between neighboring elements. For further area savings while still enabling the creation of all required beam patterns, control of the propagation direction is done from the R/C level but also with one local bit from the SR, $CTRL_{loc}$. Fig. 5.3 displays examples of TX patterns that can be generated with the presented method. The targeted imaging scheme [10] relies on diverging waves that propagate delay from the center outwards as shown in (a). But it is also possible to create other common patterns, such as the angled plane waves in (b) or focused waves in (c). The graphs also demonstrate how these patterns are created by indicating the starting position and row/column control with arrows along the side of the matrix. Arrows in the matrix are pointing from the element that the trigger signal was received from and Fig. 5.3(d) presents the complete element-level logic table.

The circuit of an SR BF cell is shown in Fig. 5.4. The local delay value is

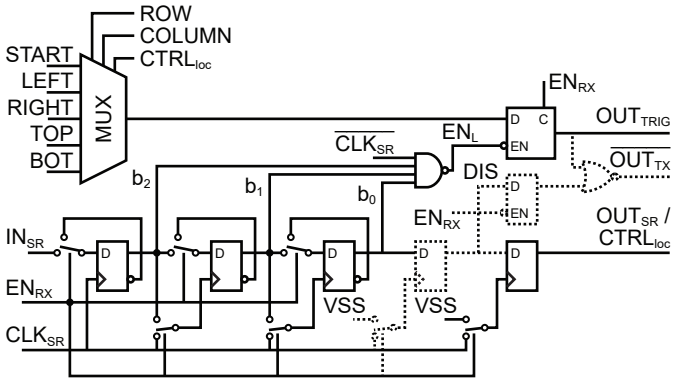


Figure 5.4: Circuit details of a TX beamformer cell with additional local pulse disabling in dashed lines.

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loaded into three flip-flops (FFs) as part of the SR with the SR input, IN_{SR}, and clock, CLK_{SR}. As the delay information is only required during the TX phase, loading of the delay cells in the SR is done during RX without additional hold cells. Moreover, an area-efficient implementation is reached by repurposing the unused SR cells to counters during TX based on the T/R control signal, EN_{RX}. The reconfiguration can be done by switching the FF data inputs to an inverting feedback loop around the cell and using the data output of lower-order bits as the clock input of higher-order bits, leading to only a few switches as overhead instead of more FFs. The number of delay steps equals 2^N, N being the number of counter cells, and the actual delay is determined by the frequency of CLK_{SR} during TX as it remains connected to the least-significant bit (LSB), b_2. In this design, the 100-MHz SR clock is maintained during TX and there are three counter cells per element, leading to a total of eight steps from 0 ns to 70 ns.

The counter rotation is converted to an enable signal for a latch, EN_L, by detecting its highest value with a negative-AND (NAND) gate. Including an inverted version of CLK_{SR} can block any glitches in the asynchronous counter and clearing the latch during RX with EN_{RX} prevents any TX triggers in the wrong phase. Selection of the latch input is made with a multiplexer (MUX) controlled by the R/C signals and the output of the last element-level SR cell that serves as $CTRL_{loc}$ but also as the output to the SR of the next element, OUT_{SR}. Five different input triggers can be selected, LEFT to BOT indicating the output triggers, OUT_{TRIG}, of all neighboring elements and START being the initial external trigger. Fig 5.5 shows a timing diagram with an example of loading the element SR during RX

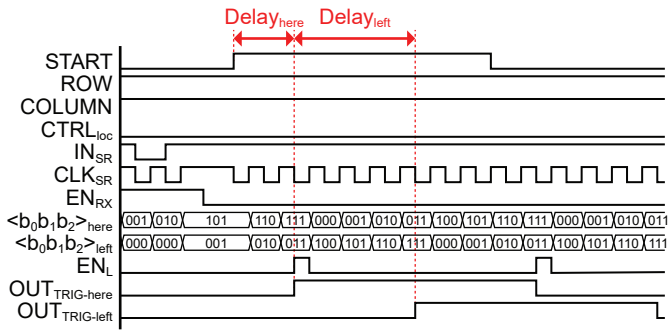

Figure 5.5: Timing diagram showing the SR loading of a TX beamformer cell, subsequent pulsing based on the delay from the START trigger, and further propagation to the cell on the left.

before delaying the external trigger by two steps and even later having the left neighbor pass it further. In the transition between RX and TX, CLK_{SR} is held high such that the counter maintains its state. If it were low, the FFs would toggle depending on their current status. As the states are still unique in that case, the circuit can still be operated but an extra mapping between codes is required.

The dashed circuitry is optional and has been included in this ASIC to support additional debugging by excluding single elements from the entire imaging operation. The implementation adds one bit in the local SR to receive a disable signal, DIS, and latches it such that it is also available during the RX phase. By not directly using OUT_{TRIG} to control the pulser but manipulating it with a negative-OR (NOR) gate to OUT_{TX}, elements can be permanently connected to the HV supply. At the same time, the rest of the array can function as usual as the trigger is still being passed.

Next to a compact design, TX beamforming by shifting an LV trigger signal through the system also has the benefit of being able to dynamically change the number of pulses and even pulse frequency if required. One potential drawback for some applications is that only delays smaller than the pulse width can be generated as EN_L needs to latch during the active interval. However, this is commonly no issue for ultrasound imaging as is analyzed in the following. Typical ultrasound imager arrays remain at a pitch of half of the center transmit wavelength, λ, as that moves grating lobes out of the picture [51]. As the relative difference in distance, D, from a virtual source between neighboring elements can at most be equal to the element pitch, it can be shown that the maximum possible delay for these devices is half of the pulse period and thus in the coverable range:

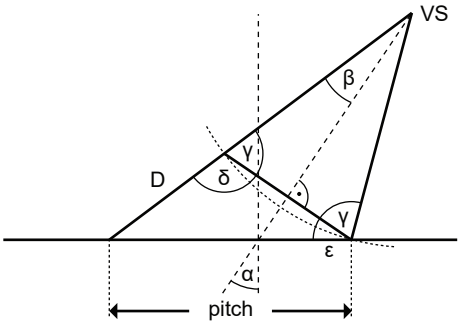

Figure 5.6: Drawing showing the difference D in excitation of two elements with a certain pitch in order to create a steered diverging wave.

$$DEL = \frac{D}{c} = \frac{\frac{\lambda}{2}}{\lambda \cdot f} = \frac{T}{2} \tag{5.1}$$

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where DEL is the required delay between elements, c is the speed of sound, f is the center frequency, and T is the pulse period. A way to determine the delay between neighbors for any pitch is shown using the diagram in Fig. 5.6. The relative distance from the virtual source, VS, can be calculated with

$$D = \frac{sin(\alpha)}{cos(\beta)} \cdot pitch \tag{5.2}$$

where α is a known angle determining beam steering and β is a known angle determining beam divergence. The equation is found by applying the law of sines on the lower triangle based on angles δ and ε, found with trigonometric equations, and can be used to derive the required delay by DEL = D/c. Although the pitch is slightly above half of λ, this results in maximum delays in the order of 70% of the 80-ns pulse width for the shown design with the intended 10° divergence and maximum steering angle of 30° [10].

5.3.2. LNA

The LNA architecture is based on the design presented in [34] but has been extended to enable co-integration with TX and high-frame-rate operation. Fig. 5.7(a) shows a simplified schematic of the prior design with a direct connection of the input node, V_{IN}, to the transducer element and input biasing to V_{ref} through a high-impedance path, R_{IN}. A compact implementation is reached by a split capacitor feedback network [52], an efficient inverter-based amplifier core, and dynamic

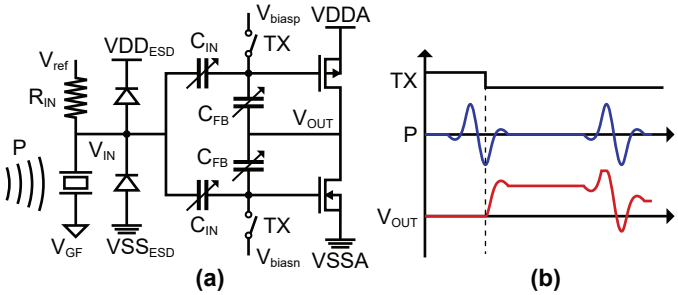


Figure 5.7: (a) Simplified schematic of an inverter-based amplifier with split capacitor feedback and dynamic biasing. (b) Illustration of how the initial transducer state and forward biasing diodes due to large inputs can lead to offset issues with dynamic biasing.

biasing to potentials V_{biasx}. Discrete TGC is achieved by reconfiguration of the capacitor network comprised of C_{IN} and C_{FB} between receive cycles.

5

While the shown techniques have led to a receiver with state-of-the-art power and area efficiency, they also lead to issues in the transition to a high-frame-rate imaging system with TX and RX on each element. To illustrate this, Fig. 5.7(b) shows two common problems that can be experienced in a transducer frontend with incoming pressure waves, P, and dynamic biasing. To achieve quick settling following TX, the dynamic biasing is synchronized to the T/R cycle and active until shortly after TX is completed. The first issue is that, since echoes start returning immediately after the ultrasound transmission, the switching can never be guaranteed to take place at a moment in which no signal is present. As pulsing and dynamic biasing in a short time window require a reference with a relatively low impedance, the final DC operating point will be signal-dependent and can lead to a large offset. The second issue is that strong incoming signals, which often occur shortly after TX due to low initial attenuation in the medium, can lead to clipping due to the electrostatic discharge (ESD) protection diodes or the internal rails. This would change the DC operating point even during active RX, with no possibility to recover in a pure dynamic biasing implementation.

Irrespective of these external effects, the limitation to biasing in a short time interval before reception also leads to issues if one would switch through all gain levels of the discrete TGC scheme due to non-ideal switching procedures. Finally, the transducer needs to be biased to a reference, V_{ref}, being e.g. just the direct current (DC) level of a bipolar pulser [14] or a mid-rail reference if the pulsing goes all the way to the negative rail [53]. Since this would need to happen in a short

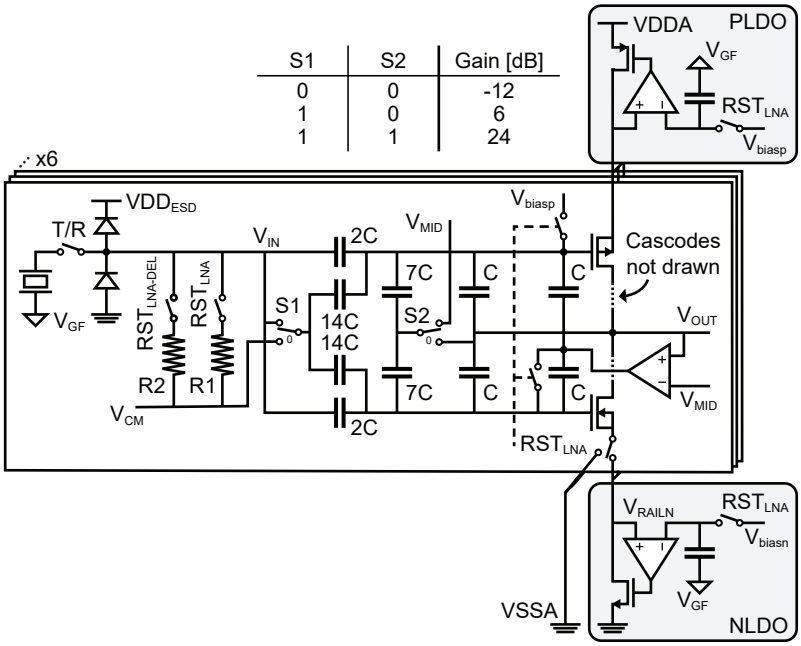


Figure 5.8: Conceptual schematic of the inverter-based low noise amplifier (LNA) showing gain switching, transducer biasing, and supply regulators.

time interval after TX, it cannot be covered by the high-impedance connection with R_{IN} for a design with TX and RX on the same element.

Fig. 5.8 shows the implemented design with proposed changes. The LNA is still applying dynamic biasing to quickly settle all critical nodes in a short time window after the possibly high disturbance of HV TX. To target the issues discussed above, this is assisted by the connection of the transducer to a mid-rail potential, V_{CM}, via resistors. The switches are controlled with RST_{LNA} and $RST_{LNA\text{-}DEL}$ to always close at the beginning of an RX period. R1 is in the order of 50 kΩ and used to raise the transducer top plate from its initial state of 0 V after pulsing to V_{CM} in a time frame of 100s of ns to not lose too much RX time but also not cause a second transmission. R2 is around 1 MΩ and connected longer, in the order of µs, to settle any offset due to large inputs received shortly after TX but then also disconnected as it is a potential source of noise and interference from other channels.

Next to the added resistive components, the biasing has also been modified compared to [34] by adjusting the way in which the inverter transistors are oper-

ated. During initial dynamic biasing, the upper transistor is still directly connected to a biasing voltage, V_{biasp}, and the lower transistor is still driven by an amplifier in a feedback loop to force the LNA output voltage, V_{OUT}, to a local mid-rail potential, V_{MID}. However, this amplifier is not switched out and shorted after that but instead connected to two capacitors in parallel with the feedback capacitors of the LNA. This gives the structure a low-frequency path to correct for effects like disturbances from gain switching or residual issues in the transducer biasing. Due to the low bandwidth of the additional amplifier and the capacitive attenuation towards the output, its noise contribution in the signal bandwidth as well as the power and area are negligible compared to the entire LNA.

The capacitor ratios and unit cells, C, of 45 fF are as in [34]. The input capacitors are held at the same potential the transducer is biased to, V_{CM}, before being switched in to minimize introduced disturbance in the RX period. Similarly, the feedback capacitors are connected to the same potential V_{out} is driven to via the low-bandwidth loop after being switched out. After these capacitors are settled, there is also the option of removing them from V_{MID} in order to remove the noise from that source.

To mitigate the low power supply rejection ratio (PSRR) of the inverter-based topology [54], the LNA employs the local regulators [55] as in [34]. In this design, they are shared on the subgroup level and it can be chosen to switch to the analog ground, VSSA, instead of the negative low-dropout regulator (LDO) to investigate differences. Additionally, the dynamically set references of both LDOs are capacitively coupled to the ground foil node of the transducer, V_{GF}. This enables the architecture to also reject variations of the ground foil node that would otherwise be amplified with the signal. Combined with the improved PSRR, this aims to reduce the common mode interference across channels and thus maximize the possible gain from RX beamforming.

5.3.3. PGA

The circuit implementation of the PGA is based on the compact architecture shown in [18] but modified as the original structure can't support high-frame-rate operation and has a limited output swing. The main issue with volume acquisition at a high rate is presented following Fig. 5.9. The prior design is similar to Fig. 5.9(a) and achieves gain switching by adding a capacitor to the virtual ground of an amplifier in a capacitive feedback configuration. While the constant load presented

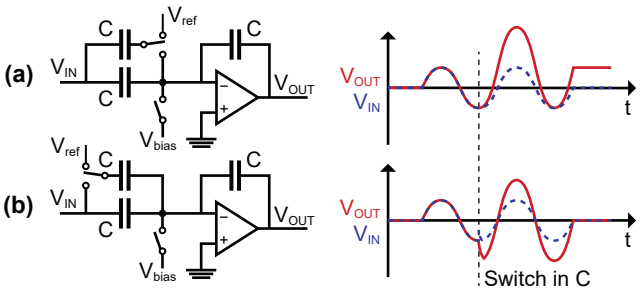
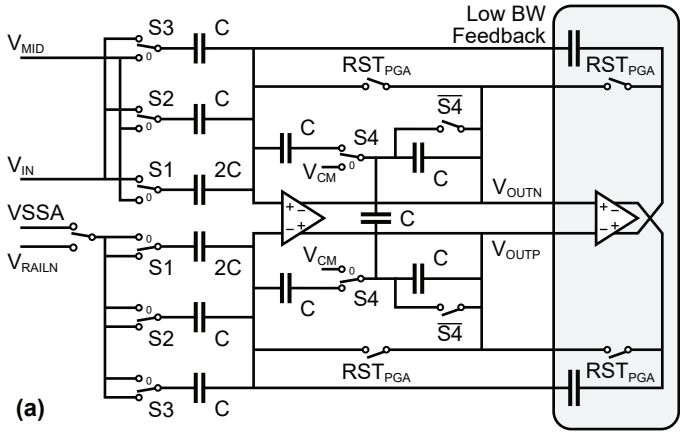


Figure 5.9: Impact of switching the gain of an amplifier in a dynamically biased capacitive feedback in active operation from: (a) the back; (b) the front.

to the driving stage of this setup is beneficial, this switching alters the operating point of the setup and leads to an offset if done during active operation. As the system is dynamically biased with V_{bias}, it can not recover over time and even with a low-bandwidth correction path, the possibly large step could lead to a significant loss of image information.

With the approach illustrated in Fig. 5.9(b), on the other hand, this can be avoided since the virtual ground node is not affected when the capacitor is switched from the input. The input experiences a short settling depending on the driver but then continues operation without an offset. In the proposed design, the configuration of Fig. 5.9(b) is adopted to enable gain switching during echo reception and thus high-frame-rate. Fig. 5.10(a) shows the schematic implementation with a compact T-type feedback [48] and Fig. 5.10(b) presents the associated logic table to determine the gain depending on the switch settings. To minimize the disturbance from gain switching, the input capacitors are connected to the output DC level of the LNA and the feedback capacitors are connected to a mid-rail potential, V_{CM}, when not in the loop. The LNA has sufficient phase margin and bandwidth to operate with the switching capacitance at its output and achieve quick settling.

Similar to [18], the structure is held in reset during TX to enable quick settling of the operating point after HV pulsing, but in addition to that, a low-bandwidth feedback path has been introduced. This enables the correction of any remaining disturbance caused by switching during one T/R cycle while adding little area and power consumption compared to that of the entire PGA. Particularly the switching of the T-type network can lead to non-ideal behavior as the capacitors can not be switched to a known reference, as is the case for the input capacitors. The feedback amplifier is implemented as a differential gain stage with a bandwidth of



(b)

S1	S2	S3	S4	Gain [dB]
0	1	1	0	6
0	1	0	1	12
0	1	1	1	18
1	1	1	1	24

Figure 5.10: Sketch of the programmable gain amplifier (PGA) displaying gain switching and the implementation of a low-bandwidth feedback amplifier.

around 1 MHz. As it is not part of determining the gain, the capacitors of the low-bandwidth path can be adjusted in a trade-off between attenuation of additional noise and achievable correction range. In this design, the unit capacitance, C, is 33 fF and the additional capacitors are 9 fF to arrive at a noise contribution more than 3 times lower than that of the main amplifier in the signal range.

The configuration as a single-ended-to-differential converter from the prior design is kept to enable differential operation of the ADC and dummy switches are placed in the bottom branch of the feedback network as well to balance the design. However, instead of connecting to a mid-rail supply, the bottom branch is driven relative to the reference of the single-ended input. This ensures that no interferers are unintentionally amplified with the received signal and is realized by mirroring the negative rail connection of the LNA. The telescopic amplifier has moreover been replaced by a two-stage miller-compensated differential amplifier with an auxiliary amplifier to provide common-mode feedback. The division in a first gain stage and a high-swing output stage can show bandwidth and power consumption similar to [18] while providing a larger output swing for the ADC and not leading to gain deviation.

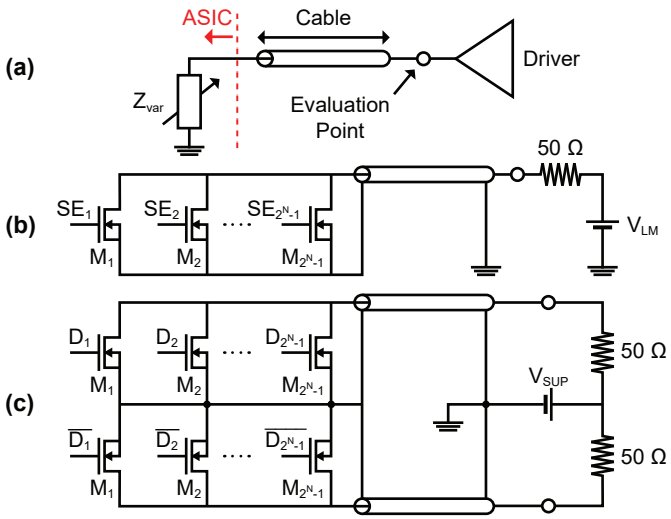


Figure 5.11: (a) Block diagram summarizing the idea of load modulation. (b) Example of a single-ended load modulation implementation. (c) Example of a differential load modulation implementation.

5.3.4. Datalink

To explore possibilities to reduce the RX-related cables in the catheter, this design leverages the relatively relaxed BER requirement of ultrasound imaging [40]. By applying a multi-level PAM driver, several bits are transmitted in one symbol, allowing for a higher throughput without increasing the symbol rate which would cause limitations due to the low bandwidth of the thin cables [56]. To reduce the power consumption associated with data transmission at the tip of the catheter, where heating must be limited to ensure safe operation in the human body [57], the driver has moreover been implemented based on load modulation (LM) [27]. Instead of direct driving, this only switches a variable load impedance, Z_{var}, on the chip with a driver on the other end of the cable as shown in Fig. 5.11(a). This enables measurements at an evaluation point outside the body with part of the power consumption shifted to the system side where heating is not an issue.

In this design, single-ended and differential multi-level LM implementations are investigated. Fig. 5.11(b) gives an overview of the single-ended setup with the variable load being implemented by $2^N - 1$ transistors with scaled widths M_x, N being the number of bits per symbol. The array is controlled with a thermometer code in SE_x and forms a divider with the termination resistance to a power supply, V_{LM}, on the system side. The differential configuration in Fig. 5.11(c) relies on

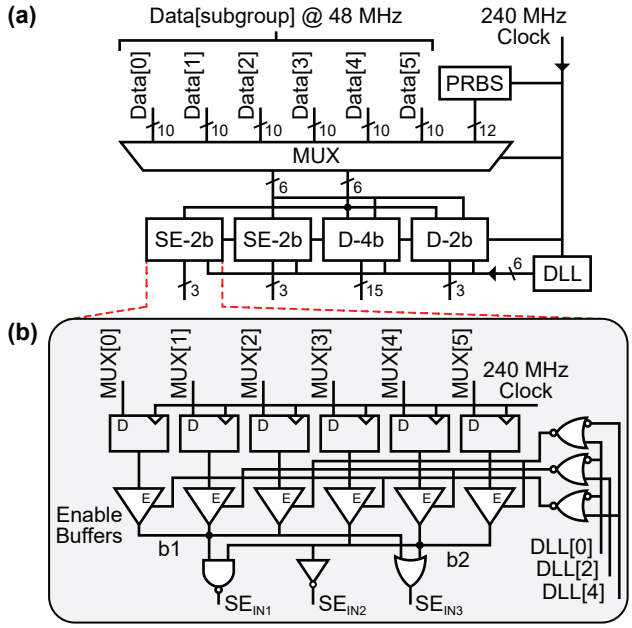


Figure 5.12: (a) Overview of the data and control configuration for the multi-level signaling. (b) Details of a single-ended implementation with two bits per symbol.

the same mechanism but introduces a second, inverted path with the same scaling via a second cable. While a differential channel takes an additional cable, more power consumption, and circuit area, the gained rejection of common interference compared to the single-ended structure can be beneficial in a narrow catheter with multiple parallel connections. Additionally, the shared return current in the ASIC will be constant to first order, reducing possible cross-talk between channels, and the differential signal swing is twice as high for the same supply. This potentially enables a higher bandwidth per channel at the same BER as the single-ended setup and makes differential signaling an interesting part of this study.

Fig. 5.12(a) gives an overview of the realized test setups in this design and their control. The 60 recombined data bits from six ADC pairs operating at 48 MHz are multiplexed into 12-bit words at 240 MHz. Based on this input, three different configurations are being analyzed in parallel: a differential driver with 2 bits per symbol at 1.44 GSps, a differential driver with 4 bits per symbol at 0.72 GSps, and two single-ended drivers with 2 bits per symbol at 0.72 GSps that share the total data input. All of these achieve the targeted RX data cable reduction

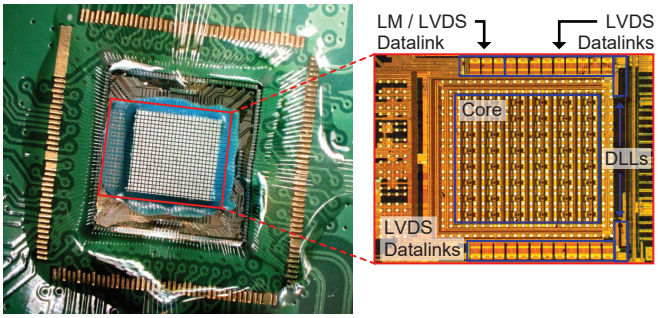


Figure 5.13: Micrograph of a chip with transducer stack on its surface and an inset showing the global floorplan below.

of 18 to ultimately arrive at a total of 64 data connections for the full probe [10] and enable the direct comparison of all schemes. The timing is provided by a DLL that creates six phases out of the input clock to accommodate the highest transmit frequency.

The internal structure of the control blocks is shown by the example of a single-ended cell in Fig. 5.12(b). After synchronization of the recombined and multiplexed ADC outputs to the input clock, an array of buffers is used to drive two outputs, b1 and b2. The buffers can be disabled to have a high output impedance and effectively multiplex onto one output based on the overlap of phases from the DLL. Local generation of the overlap avoids the need for distributing a high-frequency clock and is done with one layer of logic gates. For the single-ended setup, only every second DLL output phase is required to realize the 0.72-GSps output stream. In the last stage, the binary signal is converted to a thermometer representation for the LM driver based on logic gates.

The system also provides a second path with a pseudo-random bit sequence (PRBS) generator to be able to investigate the BER. It is implemented as a linear-feedback shift register (LFSR) of 20 cells with 12-bit parallel output [58].

5.4. Experimental Results

5.4.1. Electrical Measurements

An overview of the manufactured device is given in Fig. 5.13. The design implements one-fourth of the final intended aperture in the azimuth direction and the

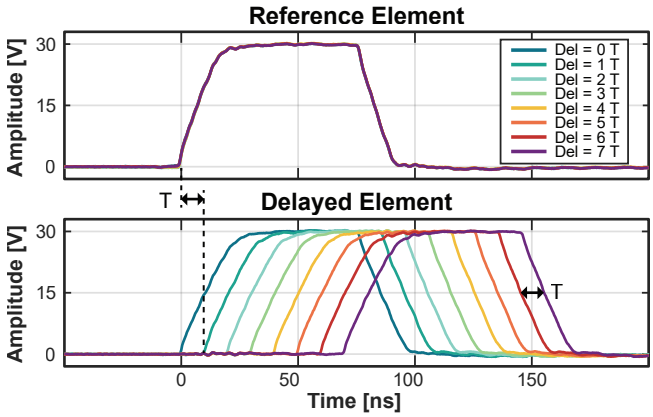


Figure 5.14: Measurement of the transmit delay between two neighboring elements with configurations from the minimum to the maximum setting.

full aperture in the elevation direction. The ASIC is fabricated in a 180-nm HV BCD technology and a transducer stack with 160-μm pitch is manufactured on its surface. In the inset, the global floorplan is showing a separation in two halves with datalinks on the top and bottom, enabling further scaling of the unit-cell-based structure along the horizontal axis.

Fig. 5.14 shows the electrical characterization of the transmit beamformer. Two neighboring elements are each connected with a capacitor to mimic the capacitive load of a single transducer element at about 2 pF. The delay between them is swept through all the configurations from zero to seven unit time periods, T. The interval is determined by the clock frequency of the time reference and in this case 10 is ns.

To investigate the implemented scheme for common-mode interference rejection around the first-stage amplifier, an experiment with an intentionally injected interferer is carried out. Fig. 5.15 displays the root mean square (RMS) ADC output caused by an amplitude sweep of a 6-MHz sinusoidal signal driven onto the ground foil node with the LNA input being connected to it in the highest gain setting. To study the effects, the two configurations of the negative supply connection of the LNA, either to the shared analog ground node or the local negative supply regulator, are compared. The larger ground foil interference required to elevate the output code from the noise floor in the case of LNA connection to the local regulator shows the effectiveness of the suppression.

The settling of biasing points in the presence of input signals is studied with

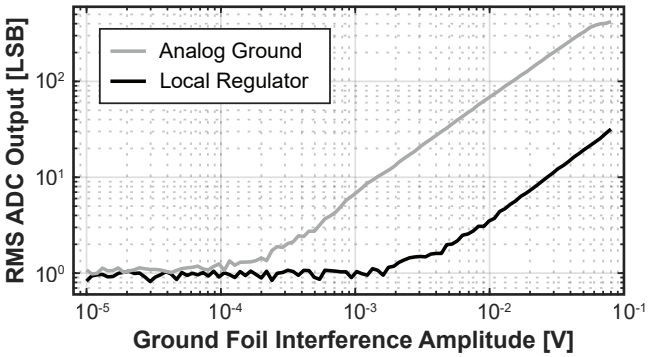


Figure 5.15: Measured ADC output relative to the amplitude of an interfering signal applied to the ground foil node in the case of low-noise amplifier connection to the shared analog ground or local negative supply regulator.

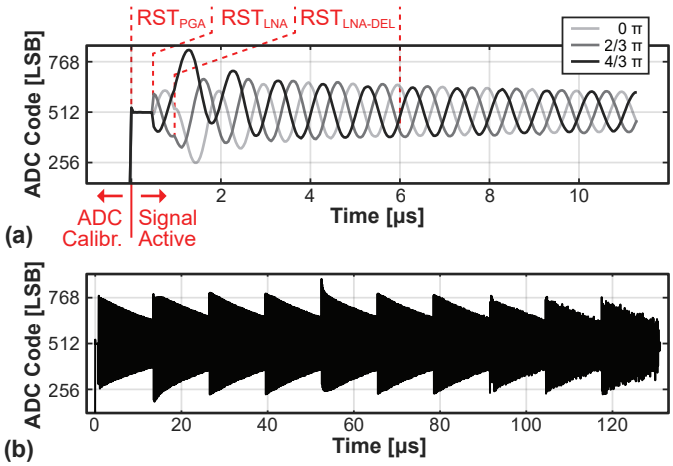


Figure 5.16: (a) Initial converter output code settling for an exponentially decaying sinusoidal input with 3 different phases with indicated amplifier biasing times. (b) Converter output code showing settling during a full transmit/receive cycle with time gain compensation and an exponentially decaying sinusoidal input.

a 2-pF capacitor, modeling the capacitive component of the transducer element, in series with an arbitrary waveform generator (AWG). Fig. 5.16(a) shows the ADC output at the beginning of a receive phase with three different phases of an exponentially decaying 1-MHz sinusoidal input in the lowest gain setting. The signal is active before the dynamic biasing is completed and shows the response

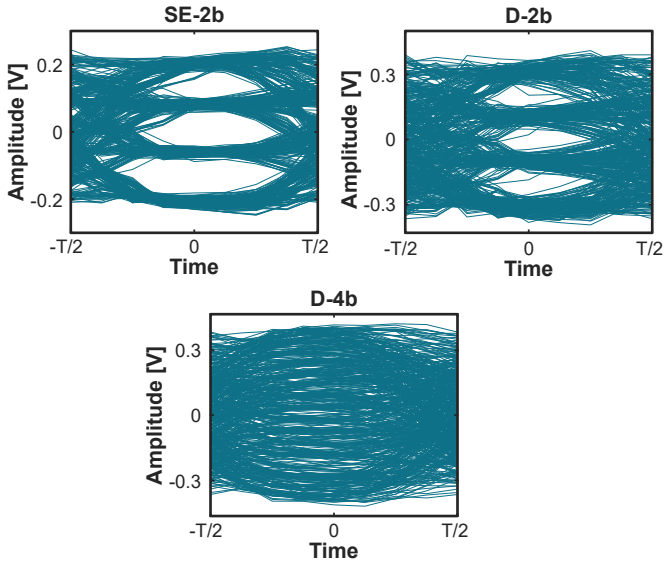


Figure 5.17: Eye diagrams of all load modulation datalink configurations with a V_{LM} of 0.7 V, data rates of 2.88 Gbps, and a 1-m assembly of 42-AWG micro-coax cables.

to different initial states of the high-impedance input node when actual reception is started. Typically, RST_{PGA} would be asserted longer than RST_{LNA} to optimize settling but it is in this case disabled earlier as it would otherwise mask the output signals needed to study the behavior. In this example, RST_{PGA} is active 500 ns after the start of input signaling with RST_{LNA} and $RST_{LNA\text{-}DEL}$ being asserted 500 ns and 5 µs longer respectively. The recorded outputs show a signal-dependent offset introduced after the completion of dynamic biasing and subsequent recovery provided by the resistive input biasing and the low-bandwidth amplifier feedback paths. Fig. 5.16(b) additionally shows the ADC output during a full T/R cycle with an exponentially decaying 6-MHz input from an AWG. TGC is used from the lowest to the highest gain setting to maintain the output code level and it can be observed how non-ideal steps in the gain are compensated by the implemented biasing techniques.

Fig. 5.17 shows the eye diagrams of all load modulation datalink configurations as measured based on the output of the PRBS generator. The data is acquired at a supply voltage, V_{LM}, of 0.7 V with a 1-m assembly of 42-AWG micro-coax cables. While the single-ended version has a clear opening, the differential topologies show more disturbance and even complete closure for the channel with 4 bits per symbol.

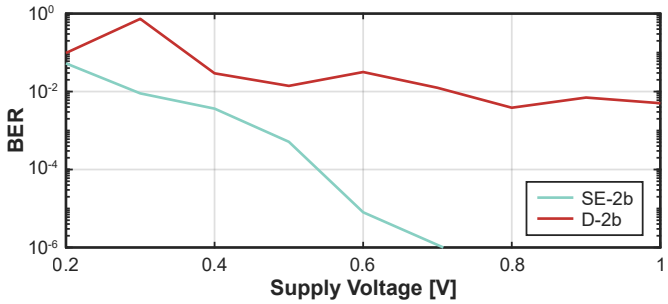


Figure 5.18: Display of the bit error rate (BER) vs. the supply voltage for the two load modulation configurations with 2 bits per symbol, offering a data rate of 2.88 Gbps.

The degradation in differential signaling can be explained by the transmission across two micro-coax cables and a significant improvement is expected if the arrangement is replaced by a twinax cable or a twisted pair.

A study of the BER in relation to the applied V_{LM} on the system side is shown in Fig. 5.18. The test data is generated by the on-chip PRBS generator, measured with an oscilloscope, and compared to the ideal values after reception at the measurement computer. While the differential channel with 4 bits per symbol is excluded due to insufficient performance, both channels with two bits per symbol show an improvement of the BER with increased supply voltage. The single-ended case clearly performs best with the applied cable assembly and can achieve a BER of 10^{-6} at a V_{LM} of about 0.7 V. As the degradation of B-mode ultrasound images is unnoticeable at a BER of 10^{-6} [40], this implies that imaging is possible at a total measured power consumption of about 3.6 mW for the single-ended channel. Of that total, less than 2.1 mW is spent in the chip due to dissipation in the receiver termination of 50 Ω and the cable resistance of 9 Ω, resulting in an on-chip energy consumption of about 1.5 pJ/bit. While an extended setup with dedicated receivers and cable assemblies in an arrayed fashion is required to study the approach in detail, this proof-of-concept shows the high potential of multi-level load modulation datalinks in ultrasound imaging probes.

5.4.2. Acoustic Measurements

An experiment investigating the noise behavior of the array is presented in Fig. 5.19. The figure shows the RMS outputs of a sample with transducer elements while be-

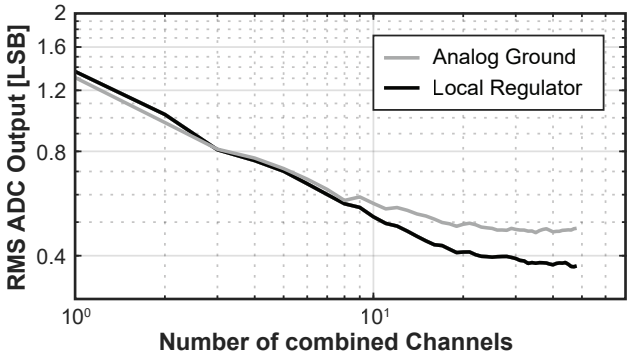


Figure 5.19: Investigation of the noise output of the array relative to the number of combined channels with the low-noise amplifiers being connected to the shared analog ground or local negative supply regulators.

ing loaded by water and recording in the highest gain setting without an input signal. To study the effect on the noise floor, the experiment is conducted with the negative rail of the LNA being connected to the shared analog ground or local supply regulators. In both cases, there first is an exponential reduction in the amplitude before the two curves flatten off at different effective array sizes. The initial decline is close to the anticipated $\sqrt{N}$ improvement of uncorrelated interference for N combined signals [44] but gets limited by the presence of correlated interference between channels. The reduction in common interference and thus improvement of potential beamforming gain for the LNA connection to the local regulator compared to the direct analog ground connection can be explained with an enhanced PSRR. Noise on the shared power rails appears common to all elements and can, even in this reduced-size prototype and without active input, pose a limit to the beamforming gain.

Characterization of the TX beamforming functionality is shown in Fig. 5.20, following the example patterns demonstrated in Fig. 5.3. The measurements are obtained with the chip assembly being submerged in water and facing a commercial hydrophone [59]. By translation of the hydrophone with an xyz-stage during repeated transmission from the prototype, C-planes in parallel to the transducer surface are captured. These evaluate the maximum peak pressure at each position and are compared to simulations [60] based on the same set of delays. Fig. 5.20(a) shows the simulated pressure profile at a 5-cm distance from the array for the transmission of a diverging wave on the left and the corresponding hydrophone measurement on the right. Fig. 5.20(b) similarly shows the results for a plane

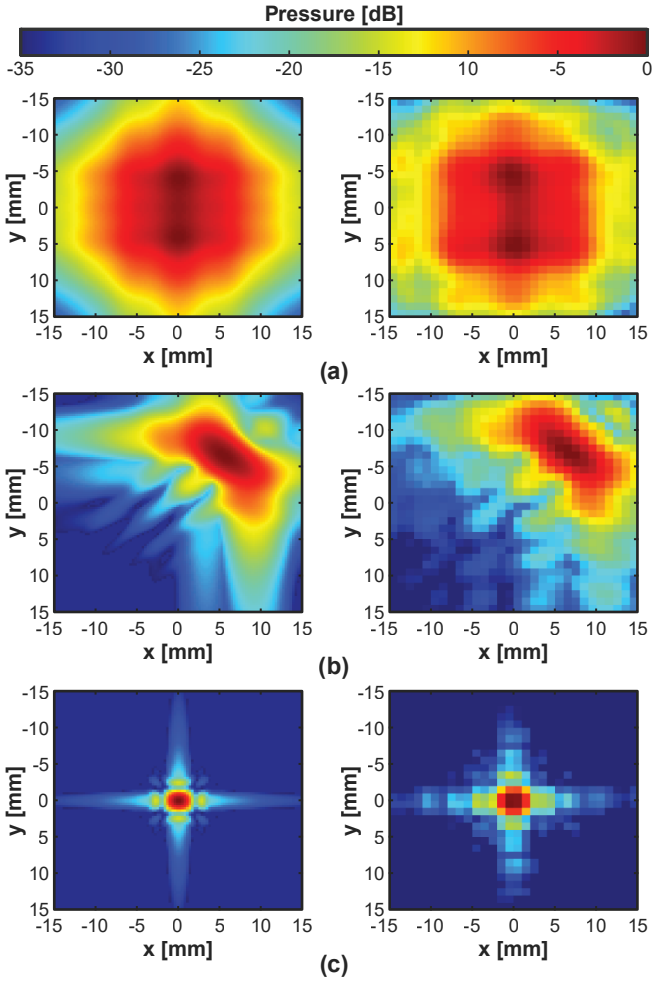


Figure 5.20: Comparison of simulated C-planes on the left and corresponding measured C-planes on the right for: (a) A diverging beam at 5 cm from the array; (b) A plane wave steered to the north-east at 5 cm from the array; (c) A focused beam at 2 cm from the array.

wave angled at 10° to the north-east at a distance of 5 cm from the array and Fig. 5.20(c) shows a plane 2 cm from the array with the TX beamforming focusing at its center. Good agreement between the measured and simulated profiles in all cases verifies the capability of creating the most common patterns applied in ultrasound imaging.

To verify imaging functionality, a commercial 3D wire test phantom [61] has

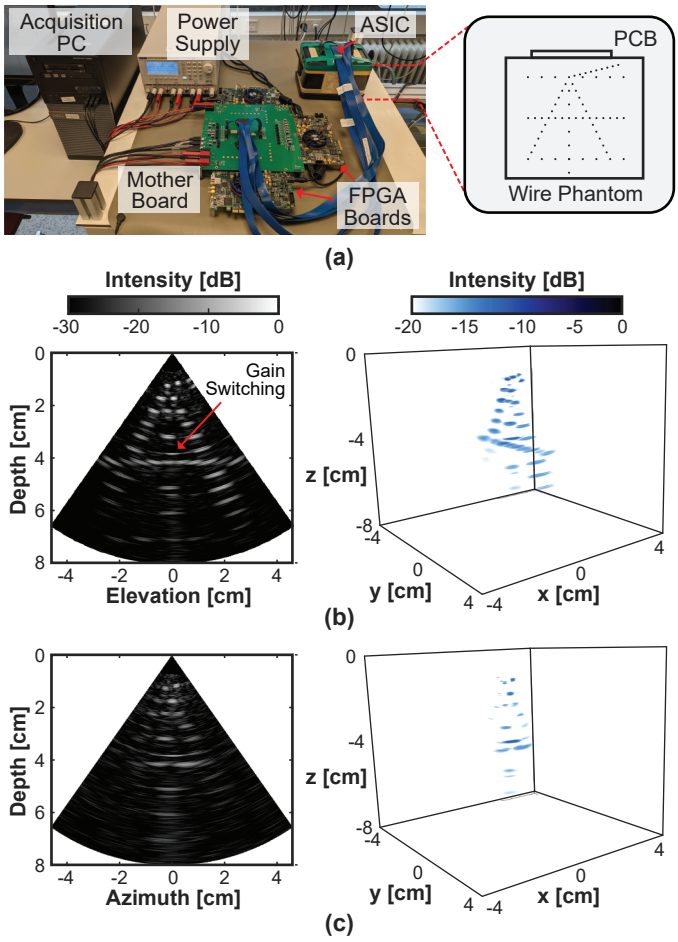


Figure 5.21: (a) Measurement setup used for imaging verification with details of the 3D wire phantom. (b) Reconstructed image plane in the elevation direction with 3D render. (c) Reconstructed image plane in the azimuth direction with 3D render.

been studied with the setup shown in Fig. 5.21(a). The ASIC is mounted on a custom daughterboard that faces the surface of the phantom. The daughterboard provides local decoupling and connects to a motherboard with active components for supply regulation and signal conditioning via 1-m cables. The acquired receive data from the 24 LVDS channels is captured and stored by commercially-available FPGA boards [50] in real-time. Each FPGA board offers 8 high-speed transceivers and three boards are thus used in parallel, while one of them additionally acts as

a control host for the ASIC configuration per T/R cycle. The acquired data is downloaded to a computer that initiates measurement routines and performs image processing.

Fig. 5.21(b) shows a reconstructed image with the wires aligned in the azimuthal direction of the array, so that they show up as point scatterers in the elevation plane. The upper seven gain settings of the TGC have been applied in each T/R cycle to maintain a suitable dynamic range in the signal path across the attenuating phantom. A switching artifact can be observed when the LNA transitions to its highest gain setting while PGA gain steps are barely noticeable. The artifact is caused by non-ideal switching resulting in a step in the RX signal and appears at a 0° azimuth and elevation angle after RX beamforming as the entire array is switching simultaneously. Given its deterministic nature, the artifact doesn't inherently harm the imaging and can potentially be compensated for during data processing.

As off-axis reflections don't propagate back to the ASIC, the wire targets appear almost as points rather than lines in the 3D plot. The behavior along the other dimension is thus evaluated by rotating the chip to align with the azimuth direction as displayed in Fig. 5.21(c). The lower opening angle in the azimuth render is caused by the application of the ultimately targeted imaging scheme described in [10]. This scans a volume of 70° × 70° × 10 cm at 1000 volumes/s with seven fan-shaped beams with little divergence in the elevation direction and large divergence in the azimuth direction. As this prototype implements the full intended aperture in the elevation direction, the functionality of the 1D subarray beamformer and TX beamforming can be fully verified. But as the aperture in the azimuth direction is 4x smaller, the prototype with an approximately square array only shows an opening angle close to that of one elevation fan beam of approximately 20° with this imaging scheme.

Table 5.1 summarizes the system and gives a comparison to the prior art in catheter-based ultrasound imagers. The system complements an earlier design described in chapter 4 with an integrated TX beamformer and a novel multi-level load modulation while still providing the highest reported frame rate. This completes the architecture and shows good performance in a 4x larger array. The transmit voltage was lowered to investigate if relatively rapid transducer degradation in the prior design could be caused by pulsers malfunctioning in acoustic samples due to latchup-like phenomena. The theory that a resonant transducer could cause sufficiently high substrate charge injection is supported by the effect

Table 5.1: Comparison with the Prior Art in catheter-based ultrasound imagers

	This work	JSSC'22 [15]	JSSC'21 [16]	VLSI'19 [17]	JSSC'18 [18]	TUFFC'16 [9]
Technology	**180nm BCD**	180nm BCD	180nm	180nm	180nm	N/A
Transducer	**2D PZT**	2D PZT	2D PMUT	2D PZT	2D PZT	2D PZT
Array Size	**16 x 18**	8 x 9	6 x 6	4 x 4	6 x 24	60 x 14
Center Frequency	**6 MHz**	6 MHz	5 MHz	5 MHz	5 MHz	5.6 MHz
Pitch-Matched	✓	✓	✗ †	✓	✓	✓
Element Pitch	**160 µm x 160 µm**	160 µm x 160 µm	250 µm x 250 µm	150 µm x 150 µm	150 µm x 150 µm	110 µm x 180 µm
Included Transmit	**30 V**	65 V	13.2 V	✗	✗	40 V
Transmit Beamforming	**internal**	external	internal	✗	✗	internal
Receiver Architecture	**AFE + µBF + ADC + Datalink**	AFE + µBF + ADC + Datalink	AFE + ADC	AFE + ADC	AFE + µBF + ADC + Datalink	AFE + µBF
Digitization	✓	✓	✓	✓	✓	✗
Elements / RX cable	**18** §	6	0.5	0.5	18	15 to 20
Data Transmission	**Multi-Level LM** §	LVDS	N/A	LVDS	LVDS	analog
Supported Frame-Rate	**1000 vol/s**	1000 vol/s	N/A	N/A	200 vol/s	50 vol/s
Active Area / Element	**0.030 mm²** §	0.032 mm² §	0.063 mm²	0.023 mm²	0.026 mm² §	N/A
RX Power / Element	**~1.1 mW** §	1.23 mW §	1.14 mW	1.54 mW	0.91 mW §	< 0.12 mW
Peak SNR	**52.2 dB**	52.3 dB	57.8 dB ‡	49.8 dB	52.8 dB	N/A

† Scalability limited by a non-integrated transducer array and its connection outside of the pitch.
§ With the proposed Datalink and drivers. ‡ ADC only, excluding AFE.

not being visible in the presented second design, which trades maximum voltage for additional lateral isolation structures. A better trade-off could be achieved in a silicon-on-insulator (SOI) technology that does not rely on lateral spacing as much as the applied junction-isolated process used in this project.

5.5. Conclusion

A transceiver ASIC implementing a comprehensive architecture for catheter-based high-frame-rate 3D ultrasound imaging probes has been presented. A compact on-chip TX beamformer design that can provide all required beam patterns is achieved by the combination of an area-efficient row/column and a flexible shift register approach. The impact of common interference and settling in the analog frontend have been investigated and mitigation methods have been presented. The application of time-division multiplexing, subarray beamforming, and a load modulation, multi-level data transmission channel has led to a high cable-count reduction while reducing the power consumed on the chip and still offering a high frame rate. A prototype chip has been manufactured and successfully applied in a high-frame-rate, 3D imaging experiment to verify the functionality.

A more detailed characterization of the design is ongoing at the time of writing but outside the scope of this thesis.

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6

Conclusion

This thesis has presented the development of a high-frame-rate 3D intracardiac echocardiography (ICE) probe concept from the evaluation of the idea to a functional prototype. In this chapter, the main contributions of the work are summarized, followed by a compilation of general findings gained in the process. The chapter concludes with an outlook on future opportunities in the design of 3D ICE catheters but also in the development of ultrasound probes in general.

6.1. Main Contributions

Proposition of an imaging scheme and probe design for high-frame-rate 3D ICE catheters (chapter 2)

We have investigated the potential for 3D high-frame-rate intracardiac echocardiography and proposed an imaging scheme with an associated probe design that enables it. Restricting subarray beamforming to a small subarray in elevation direction allows for a volume acquisition with only 7 fan-shape beams for an imaging rate of 1000 volumes/s and a sufficient cable count reduction for the realization of the electronics. Essential parameters such as beam divergence, center frequency, and matrix dimensions have been optimized based on system-level simulations.

Implementation of the HV ultrasound transmitter with the lowest HV transistor count (chapter 3)

It has been shown how a compact unipolar pulser with an embedded transmit/receive switch and a capacitive high-voltage (HV) level shifter can realize the ultrasonic HV transmit circuit with the lowest reported HV transistor count and area while not having any static power consumption. The topology is specifically optimized to be insensitive to transients on the HV supply as in probes with limited local supply decoupling, such as imaging catheters, pulsing can lead to disturbances on the supply rails. Pulsing with up to 65-V has been evaluated in electrical and acoustic tests with a 6-MHz center frequency PZT transducer array.

Implementation of an area- and power-efficient hybrid beamforming ADC for massively arrayed applications (chapter 4)

A hybrid analog-to-digital converter (ADC), combining an efficient charge-sharing successive-approximation-register (SAR) first stage and a compact single-slope (SS) second stage, has been developed to address power and area requirements in catheter-based probes. Application in large ultrasound imaging arrays is facilitated by directly interfacing the ADC with a charge-domain subarray beamformer and generating the SAR reference using a power-efficient local reference generator. Additional hardware-sharing between neighboring channels ultimately has led to the lowest reported area and power consumption across miniature ultrasound probe ADCs. The functionality and performance within the receive signal chain have been demonstrated in electrical experiments.

Realization of the first architecture to combine element-level HV pulsers and AFEs, μBF, ADCs, and datalinks for ultrasound imaging (chapter 4)

The first architecture to combine element-level HV transmitters and analog frontends (AFEs), subarray beamforming (μBF), in-probe digitization, and datalinks in a scalable fashion for catheter-based probes has been presented. A pitch-matched design is enabled by an efficient split between the core circuitry and a periphery block, the latter including a datalink performing clock-data-recovery (CDR) and time-division multiplexing (TDM), which leads to a 12-fold total channel-count reduction. The feasibility of the scheme has been demonstrated with an 8×9-element prototype applied in electrical, acoustic, and imaging experiments with up to 1000 volumes/s.

Implementation of a fully functional pitch-matched transceiver ASIC for interconnect-limited ultrasound probes (chapter 5)
A 16×18-element ultrasound imager with a fully functional transceiver ASIC for catheter-based probes has been realized. Transmit beamforming is implemented on the chip with a combination of a shift register and a row/column approach to address the common interconnect challenge. Additional cable count and power reduction in the receiver part of the design have been explored with a multi-level load modulation datalink. It has further been discussed how common-mode interference can limit beamforming gain and a strategy to reduce its impact with local regulators has been shown. The setup has been characterized in electrical measurements and imaging experiments to verify high-frame-rate imaging capability.

6.2. General Findings

While pursuing the core target of a high-frame-rate 3D ICE concept, several interesting findings on the investigated subjects but also bordering matters have been made. In the following, the main findings are summarized:

- The main challenges in the design of high-frame-rate 3D ICE ASICs are power consumption, circuit area, and output data bandwidth. The first is mainly restricted due to the maximum permissible generation of heat in the human body while the second and third are strongly constrained by the available space inside intracardiac catheters. (chapter 1)
- In catheter-based ultrasound probes with limited local decoupling, large transient currents during high-voltage pulsing on an ASIC can lead to a significant disturbance on the HV supply due to inductance in the loop. The disturbance can cause capacitive HV level shifters without a high-side latch to lose their state and result in indeterministic pulser behavior. (chapter 3)
- With architectures and building blocks having been extensively explored and described, the application environment usually provides the main challenge for ADC design. In catheter-based ultrasound probes, the main complications are the HV co-design, massively arrayed structure, and power as well as area limitations. (chapter 4)
- A hybrid ADC combining a SAR and a SS stage can provide an efficient implementation and particularly lead to a small area for arrayed charge-sharing-

based topologies as no second digital-to-analog converter (DAC) bank is required. (chapter 4)

- Using a transducer during the transmit and the receive phase can maximize the aperture in area-constraint applications but requires a T/R isolation switch as well as a transducer biasing network during reception. (chapter 3 & 5)

- Dynamic biasing synchronized to the transmit/receive (T/R) cycles of a system can be an efficient approach for the design of sensitive circuitry in the presence of HV pulsing. The disturbance from nonideal switching during discrete time-gain compensation within one T/R cycle can be compensated for with an additional low-bandwidth biasing path. (chapter 4 & 5)

- To first order, the signal-to-noise ratio (SNR) of a single large transducer is equal to that of an array of multiple smaller transducers with the same total area after receive beamforming. While this means that in a receiver array, the power spent for reduction of the noise per path can be reduced relative to the single-element case, correlated noise between channels has to be carefully designed for. (chapter 4 & 5)

- Power consumption in the output data transmission is a significant part of the total budget in digital 3D ICE probes. As limited reduction can be achieved in the energy per transmitted bit, reduction in the transmitted data is the most effective method to limit its share. (chapter 4 & 5)

- The resonant behavior of transducers can lead to the forward biasing of p-n junctions in the DMOS devices of BCD technologies if connected on the transducer side. To prevent latch-up from occurring, guard rings and sufficient spacing should be considered. (chapter 5)

- The combination of a shift register and a row/column approach allows for a transmit beamformer implementation that is compact and reconfigurable between individual T/R cycles while still being flexible in the generation of transmit patterns. (chapter 5)

- In the design of a 3D ICE catheter essentially only the power spent at the probe tip is of interest to limit heating inside the patient. This makes load modulation an interesting technique for data transmission as part of the power consumption can be shifted to the system. Multi-level signaling can

additionally provide a way to trade a relatively relaxed bit error rate (BER) for more power savings. (chapter 5)

- The design of a system with the demonstrated complexity relies heavily on good models and computer-aided design (CAD) tools. These are quite mature for the bipolar-CMOS-DMOS (BCD) technology applied in this project but not as advanced for the transducer design and especially the transducer-to-ASIC interface. The project planning should take this into account.

6.3. Future Work

Transmit Integration and Functionality

Although the high-voltage transmitter discussed in chapter 3 features the smallest reported design with the least amount of HV transistors, it still occupies about a third of the total element area. This is mostly due to the large lateral dimensions of the junction isolation in the applied BCD technology. An alternative would be the implementation with deep trench isolation (DTI) or even in a silicon-on-insulator (SOI) technology. The dielectric applied in DTI achieves lateral isolation with much lower spacing requirements and combined with the vertical isolation of the insulator in an SOI wafer, full dielectric isolation can be provided [1].
This can either enable higher transmit voltages in the same area due to more relaxed voltage breakdown conditions or provide more space at the same transmit voltage to realize additional functionality. One possibility would be to adjust the pulser for bipolar operation to increase the energy efficiency [2]. Another option would be to reduce the power consumption and increase flexibility in the pulse shape by opting for a multi-level topology [3].

Impact of Image Processing on Probe Design

Despite the strong application-specific nature of integrated circuits designed for co-integration with transducers in ultrasound imaging probes, design choices in the application-specific integrated circuit (ASIC) are regularly still made on the block level. While this simplifies the procedure, the implications for the actual imaging are sometimes hard to estimate and wrong decisions or over-design can occur. In chapter 5, it was e.g. shown how, based on the results of a recent study on the impact of BER on ultrasound imaging quality [4], the number of cables and power consumption in an ICE probe could be significantly reduced compared to

prior conventional data transmission approaches. Similar studies on a system or circuit model combined with an ultrasound simulation tool like Field II [5] could enable additional findings and assist in the architecture design.
An aspect that would be quite interesting in this context is the investigation of ADC design for ultrasound probes. One could e.g. study how parameters like its linearity affect the image quality in different operating modes. Another relevant topic is how a sparsity of ultrasound signals can be exploited to reduce output data bandwidth. This is already explored in processing [6], [7] but is yet to be efficiently integrated with existing technologies.

Full-aperture high-frame-rate 3D ICE

The ASIC shown in chapter 5 could be extended to the full aperture described in chapter 2. The current version implements the full size in elevation but only a fourth in azimuth direction although the core circuitry is matched to the pitch of the transducer elements and all circuitry is in principle designed in unit cells that can be replicated with a low threshold. The main reason for this is that the combined output data bandwidth in the order of 100 Gb/s would exceed the capabilities of the current measurement setup based on discrete components and general-purpose evaluation boards. In addition to that, the shown multi-level load modulation datalink cannot work with standard receivers available as e.g. interfaces of an FPGA or discrete components.
One option to handle this in a future design would be by co-design of an application-specific receiver chip. An array of high-speed, low-resolution ADCs could digitize the multi-level signals and the data could be parallelized into multiple conventional datalinks to an external memory at a lower speed.

Advanced Ultrasound Imaging System Assemblies

A large part of the area and power concerns in current ultrasound imaging catheter ASICs are caused by the limitation to planar structures and suboptimal technology options. Transmit-related circuitry would ideally be implemented in a dedicated process with voltage capabilities in the 100s of volts while especially the digital parts of the receive chain could be significantly more area and power efficient in more miniaturized technology nodes. But since ultrasound imaging requires HV transmission as well as subsequent echo reception and designs commonly combine all parts on one chip, both sides currently have to make compromises. One path to investigate for future designs would thus be the possibility of co-integration of multiple chips, each dedicated to its specific function, in one probe. The issues

of high interconnect density for large 2D transducer matrices and lateral space limitation in narrow catheters could potentially be relieved by 3D stacking of ICs and vertical connection with through-silicon-vias (TSVs) [8].
In line with this, the design could be modified to be compatible with transducers based on microelectromechanical systems (MEMS), such as piezoelectric micromachined ultrasonic transducers (PMUTs) [9] or capacitive micromachined ultrasonic transducers (CMUTs) [10]. While the current assemblies with bulk-piezoelectric material are also vertically assembled, the process is quite labor-intensive [11] and MEMS-based technologies could provide a cheaper, more reliable alternative that would suit the application of disposable ICE catheters.

Optical Data Transmission Links

There could be an opportunity in the switch from conventionally applied micro-coaxial cables to fewer optical fibers with a much larger associated bandwidth. In [12], a 25.8 Gb/s optical datalink for future application in IVUS probes has recently been demonstrated by Li *et al.* While there is still an integration challenge with the electronics and probe, it has thus been shown that the size constraints for the inclusion of a vertical-cavity surface-emitting laser (VCSEL) in catheter-based imaging probes are feasible. This could reduce the data cable count for the imaging scheme presented in chapter 2 to only four. Additionally, one could explore if instead of integrating a VCSEL in the catheter, it is also possible to just modulate an externally provided optical signal to save power at the tip of the probe [13], similar to the idea of electrical load modulation discussed in chapter 5.

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Summary

This thesis describes the design of application-specific integrated circuits (ASICs) for high-frame-rate 3D intracardiac echocardiography (ICE) probes. The work follows the whole process from the analysis of the application to the testing of a prototype with all envisioned functionality. It starts with the evaluation of the main challenges posed by ultrasound imaging from the tip of a catheter with a diameter in the order of 3 mm and its implications on the circuit design. A broad literature review in the field of ICE probe development but also regarding general ultrasound electronics provides the basis for this work and motivates later design choices. A high-frame-rate 3D imaging scheme is developed based on the needs of the application and leads to the design targets of the imager array and electronics. The final ASIC architecture is reached over the course of two prototypes to enable the evaluation of block-level functionality and advanced debugging. The thesis provides a detailed description of the circuit implementation with introduced novelties and shows characterization results in the electrical as well as acoustic domain. In the following, the contents of each chapter of the main matter are summarized in one paragraph.

Chapter 1

The first chapter is an introduction to the thesis and begins with a motivation regarding the significance of minimally-invasive procedures in view of the global impact of cardiovascular diseases. Out of the pool of medical imaging systems, ultrasound and in particular ICE procedures are thereafter identified as attractive tools to provide guidance for these closed-chest interventions. An overview of traditional ultrasound setups without ASICs in the probe is given and it is discussed how evolving applications lead to a requirement for in-probe circuits. This is followed by a summary of the common targets and techniques in the design of ultrasound ASICs. Zooming closer to the application, developments in the design of intracardiac imaging catheters are subsequently reviewed from its early stages in the 1950s to the current state of the art. This leads to a detailed analysis of the current challenges faced in the field, from power consumption in order to avoid excessive tissue heating to cable count in the narrow catheter, and identification

of opportunities for the presented work. The chapter concludes with an overview of the division and organization of the thesis.

Chapter 2

A discussion of the value of high-frame-rate 3D ICE to image phenomena like electromechanical waves in the heart is presented in this chapter and leads to the propositions of an imaging scheme for a 3D ICE probe. The design employs only 1D subarray beamforming in the elevation direction and can thus achieve a high frame rate while reducing the channel count sufficiently for realization in a 10-Fr catheter. To suppress the grating-lobe artifacts associated with subarray beamforming in the elevation direction, a limited number of fan-shaped beams with a wide azimuthal and narrow elevational opening angle are sequentially steered to insonify slices of the region of interest. An angular weighted averaging of reconstructed sub-volumes further reduces the grating lobe artifacts. We optimize the transmit beam divergence and central frequency based on the required image quality for electromechanical wave imaging. Numerical simulation results show that a set of 7 fan-shaped transmission beams can provide a frame rate of 1000 volumes/s and a sufficient spatial resolution to visualize the electromechanical wave propagation on a large 3D surface.

Chapter 3

In this chapter, a compact high-voltage (HV) transmit circuit for dense 2D transducer arrays used in 3D ultrasonic imaging systems is presented. Stringent area requirements are addressed by a unipolar pulser with an embedded transmit/receive switch. Combined with a capacitive HV level shifter, it forms the ultrasonic HV transmit circuit with the lowest reported HV transistor count and area without any static power consumption. The balanced latched-based level shifter implementation makes the design insensitive to transients on the HV supply caused by pulsing, facilitating application in probes with limited local supply decoupling, such as imaging catheters. A prototype of 8×9 elements was fabricated in TSMC 0.18-μm HV BCD technology and a PZT transducer matrix with a pitch of 160 μm is manufactured on the chip. Electrical characterization as well as acoustic results obtained with the 6 MHz central frequency transducer are demonstrated at up to 65 V transmit amplitude.

Chapter 4

An ASIC for 3D, high-frame-rate ultrasound imaging probes is presented in this

chapter. The design is the first to combine element-level, HV transmitters and analog frontends, subarray beamforming, and in-probe digitization in a scalable fashion for catheter-based probes. The integration challenge is met by a hybrid analog-to-digital converter (ADC), combining an efficient charge-sharing successive-approximation-register (SAR) first stage and a compact single-slope second stage. Application in large ultrasound imaging arrays is facilitated by directly interfacing the ADC with a charge-domain subarray beamformer, locally calibrating inter-stage gain errors, and generating the SAR reference using a power-efficient local reference generator. Additional hardware-sharing between neighboring channels ultimately leads to the lowest reported area and power consumption across miniature ultrasound probe ADCs. A pitch-matched design is further enabled by an efficient split between the core circuitry and a periphery block, the latter including a datalink performing clock-data-recovery and time-division multiplexing (TDM), which leads to a 12-fold total channel-count reduction. Evaluation could be performed with the same assembly as used in the transmitter characterization and the functionality has been demonstrated electrically as well as in acoustic imaging experiments at up to 1000 volumens/s.

Chapter 5

This chapter describes the extension of the functionality of the first prototype in a second, also larger, version of the design. To reduce the number of cables in the catheter while maintaining a small footprint per element, transmit (TX) beamforming is realized on the chip with a combination of a shift register (SR) and a row/column approach. A compact beamformer design is further enabled by delay-encoding relative to the neighboring element and re-using SR cells for delay counting. To explore an additional cable-count reduction in the receiver part of the design, a channel with a combination of TDM, subarray beamforming, and multi-level data transmission is also included. This achieves an 18-fold cable-count reduction and minimizes the power consumption in the catheter by a load modulation (LM) cable driver. It is further explored how common-mode interference can limit beamforming gain and a strategy to reduce its impact with local regulators is discussed. The chip was fabricated in TSMC 0.18-µm HV BCD technology and a 2D PZT transducer matrix of 16×18 elements with a pitch of 160 µm and a center frequency of 6 MHz was manufactured on the chip again. The functionality and operation of up to 1000 volumes/s are demonstrated in electrical and acoustic imaging experiments.

Chapter 6

The last chapter concludes the thesis by providing an overview of the presented work and summarizing essential achievements. Several original contributions have been made, including propositions in the HV transmitter, receive frontend, and datalink of an ultrasound imaging ASIC but also the novel system architecture and imaging scheme themselves. The chapter also lists several, more general, findings on the system and circuit level design that have been obtained in the course of the work. In the end, an outlook on possible future opportunities for ultrasound imaging catheters is given, ranging from circuit-level improvements on the transmitter to 3D IC stacking and the potential of signal processing or optical interconnect.

Samenvatting

Dit proefschrift beschrijft het ontwerp van toepassingsspecifieke geïntegreerde schakelingen (ASICs) voor 3D intracardiale echocardiografie (ICE) katheters met een hoge framesnelheid. Het werk beschrijft het hele analyse proces voor de applicatie tot en met het testen van een prototype met alle beoogde functionaliteit. Het proefschrift begint met de evaluatie van de belangrijkste uitdagingen van ultrasone beeldvorming vanaf de punt van een katheter met een diameter in de orde van 3 mm en de implicaties ervan voor het circuitontwerp. Een brede literatuurstudie op het gebied van de ontwikkeling van ICE-katheters en algemene ultrasone elektronica, vormt de basis voor dit werk en motiveert latere ontwerpkeuzes. Een architectuur voor 3D-beeldvorming met hoge framesnelheid is ontwikkeld op basis van de benodigdheden voor de toepassing en de eisen voor de transducer matrix en bijbehorende elektronica voor beeldvorming zijn ervan afgeleid. De definitieve ASIC architectuur is na de ontwikkeling van twee prototypes vastgesteld om de functionaliteit van het systeem op blokniveau te kunnen evalueren en een geavanceerde debugging mogelijk te maken. Het proefschrift geeft een gedetailleerde beschrijving van de implementatie van de schakeling met geïntroduceerde innovaties en toont karakteriseringsresultaten in zowel het elektrische als het akoestische domein. In de volgende paragrafen worden de hoofdzaken van elk hoofdstuk samengevat.

Hoofdstuk 1

Het eerste hoofdstuk is de inleiding van het proefschrift en begint met een motivatie met betrekking tot het belang van minimaal invasieve procedures, gegeven de mondiale impact van hart- en vaatziekten. Uit de verzameling van medische beeldvormingssystemen worden echografie en in het bijzonder ICE-procedures vervolgens geïdentificeerd als aantrekkelijke instrumenten om begeleiding te bieden in deze gesloten-borst-interventies. Daarna wordt een overzicht gegeven van traditionele medische ultrageluid opstellingen zonder ASICs in de katheter en er wordt behandeld hoe evoluerende toepassingen leiden tot een vereiste voor circuits in de katheter. Dit wordt gevolgd door een samenvatting van de gemeenschappelijke doelen en technieken in het ontwerp van ultrageluid ASICs. In de context van

de eerdergenoemde toepassing worden de ontwikkelingen in het ontwerp van intracardiale beeldvormende katheters vervolgens behandeld vanaf de vroege stadia in de jaren 1950 tot de huidige stand van de techniek. Dit leidt tot een gedetailleerde analyse van de huidige uitdagingen in het veld, zoals het energieverbruik om overmatige weefselverwarming te voorkomen, de hoeveelheid kabels in de smalle katheter en waar het gepresenteerde werk verdere verbeteringen kan bieden. Het hoofdstuk wordt afgesloten met een overzicht van de indeling en organisatie van het proefschrift.

Hoofdstuk 2

De waarde van 3D ICE met hoge framesnelheid voor het afbeelden van fenomenen zoals elektromechanische golven in het hart wordt in dit hoofdstuk behandeld waarna het systeem architectuur voor een 3D ICE-katheter wordt geïntroduceerd. Het ontwerp maakt alleen gebruik van 1D subarray beamforming in de elevatierichting waardoor een hoge framesnelheid kan worden bereiken terwijl het aantal kanalen voldoende wordt verminderd om in een 10-Fr katheter te kunnen worden geïmplementeerd. Om de grating lobe artefacten geassocieerd met subarray beamforming in de elevatierichting te onderdrukken, wordt een beperkt aantal waaiervormige bundels met een brede azimutale en smalle elevatie-openingshoek achtereenvolgens gestuurd om segmenten van het interessegebied te verduisteren. Een hoekgewogen middeling van gereconstrueerde subvolumes vermindert de grating lobe artefacten verder. We optimaliseren de zendbundeldivergentie en centrale frequentie op basis van de vereiste beeldkwaliteit voor elektromechanische golfbeeldvorming. Numerieke simulatieresultaten laten zien dat een set van 7 waaiervormige transmissiestralen een framesnelheid van 1000 volumes/s en een voldoende ruimtelijke resolutie kan bieden om de elektromechanische golfvoortplanting op een groot 3D-oppervlakte te visualiseren.

Hoofdstuk 3

In dit hoofdstuk wordt een compact hoogspannings (HV) zendcircuit gepresenteerd voor dichte 2D-transducerarrays die worden gebruikt in 3D ultrasone beeldvormingssystemen. Een strenge oppervlakte beperking motiveert het gebruik van een unipolaire pulser met een ingebouwde zend-/ontvangstschakelaar. Gecombineerd met een capacitieve HV level shifter, vormen deze het ultrageluid HV-zendcircuit met de laagste gerapporteerde HV-transistortelling en oppervlak zonder enig statisch energieverbruik. De HV level shifter op basis van een gebalanceerde latch maakt het ontwerp ongevoelig voor transiënten op de HV-voeding veroorzaakt

door pulsen, wat de toepassing in katheters met beperkte lokale voedingsontkoppeling, zoals beeldvormende katheters, vergemakkelijkt. Een prototype van 8×9 elementen is gefabriceerd in een TSMC 0.18-µm HV BCD fabricage proces en een PZT-transducermatrix met een pitch van 160 µm is op de chip gefabriceerd. Elektrische karakterisering en akoestische resultaten die zijn verkregen met de 6-MHz centrale frequentietransducer worden gedemonstreerd bij een zendamplitude tot en met 65 V.

Hoofdstuk 4

In dit hoofdstuk wordt een ASIC voor 3D-katheters met hoge beeldsnelheid voor echografie gepresenteerd. Het ontwerp is het eerste dat HV-zenders en analoge frontends op elementniveau, subarray beamforming en in-katheter digitalisering op een schaalbare manier integreert binnen de katheter. De integratie-uitdaging wordt aangegaan door een hybride analoog-naar-digitaalomzetter (ADC), waarbij een successive approximation (SAR) architectuur (in een eerste trap) en een single-slope architectuur (in een tweede trap) is gecombineerd. De toepassing in grote ultrasone beeldvormingsarrays wordt vergemakkelijkt door de ADC rechtstreeks te verbinden met een ladingsdomein subarray beamformer, lokaal versterkingsfouten tussen de fasen te kalibreren en de SAR-referentie te genereren met behulp van een energiezuinige lokale referentiegenerator. Door onder andere aangrenzende kanalen hardware te laten delen, bereikt het ontwerp het laagste oppervlakte en energieverbruik van alle gerapporteerde ADCs voor ultrageluid katheters. Een op oppervlakte afgestemd ontwerp wordt verder mogelijk gemaakt door een efficiënte splitsing tussen de kerncircuits en een periferieblok, waarbij de laatste een data-link omvat die klok-gegevensherstel en time domain multiplexing (TDM) uitvoert, wat de totale hoeveelheid kanalen 12-voudig verminderd. Evaluatie is uitgevoerd met dezelfde testopstelling als gebruikt bij de karakterisering van de zender en de functionaliteit is zowel elektrisch als in akoestische beeldvormingsexperimenten aangetoond tot 1000 volumes/s.

Hoofdstuk 5

Dit hoofdstuk beschrijft de uitbreiding van de functionaliteit van het eerste prototype in een vergrote tweede versie van het ontwerp. Om het aantal kabels in de katheter te verminderen met behoud van een kleine footprint per element, wordt op de chip zend (TX) bundelvorming gerealiseerd met een combinatie van een schuifregister (SR) en een rij/kolombenadering. Een compact bundelvormer-ontwerp wordt verder mogelijk gemaakt door delay encoding ten opzichte van het naburige

element en het hergebruik van SR-cellen voor het tellen van de vertragingsstappen. Om een extra reductie van het aantal kabels in het ontvangergedeelte van het ontwerp te onderzoeken, is ook een kanaal geïmplementeerd met een combinatie van TDM, subarray beamforming en een multi-level datatransmissie. Dit zorgt voor een 18-voudige vermindering van het aantal kabels en minimaliseert het energieverbruik in de katheter door een last modulatie (LM) kabeldriver. Verder wordt behandeld hoe common-mode interferentie de versterking van de bundelvorming kan beperken en hoe de impact hiervan verminderd kan worden met lokale spanningsregelaars. De chip is gefabriceerd in een TSMC 0.18-μm HV BCD fabricage proces en een 2D PZT transducer matrix van 16×18 elementen met een pitch van 160 μm en een middenfrequentie van 6 MHz is opnieuw op de chip gefabriceerd. De functionaliteit en werking tot maximaal 1000 volumes/s worden gedemonstreerd in elektrische en akoestische beeldvormingsexperimenten.

Hoofdstuk 6

Het laatste hoofdstuk sluit het proefschrift af met een overzicht van het gepresenteerde werk en een samenvatting van de belangrijkste verworvenheden. Er zijn meerdere originele bijdragen geleverd, waaronder in de HV-zender, de ontvangstfrontend en datalink van een ASIC voor ultrasone beeldvorming. Echter, ook de nieuwe systeemarchitectuur en wijze van beeldvorming bevat innovaties. Het hoofdstuk somt ook een aantal, meer algemene bevindingen op over het ontwerp op systeem- en circuitniveau die in de loop van het werk zijn gepresenteerd. Uiteindelijk wordt een blik geworpen op toekomstige mogelijkheden voor ultrasone beeldvormingskatheters, variërend van verbeteringen op circuitniveau aan de zender tot 3D IC-stapeling en potentiële verbeteringen met behulp van signaalbewerking of optische interconnectie.

List of abbreviations

1D	One-Dimensional
2D	Two-Dimensional
3D	Three-Dimensional
ADC	Analog-to-Digital Converter
AF	Atrial Fibrillation
AFE	Analog Frontend
ASIC	Application-Specific Integrated Circuit
AWG	Arbitrary Waveform Generator
BCD	Bipolar-CMOS-DMOS
BER	Bit Error Rate
BF	Beamformer
CAD	Computer-Aided Design
CDAC	Capacitive Digital-to-Analog Converter
CDR	Clock-Data Recovery
CMOS	Complementary Metal-Oxide-Semiconductor
CMUT	Capacitive Micromachined Ultrasound Transducer
CNR	Contrast-to-Noise Ratio
CT	Computed Tomography
CTC	Continuous-Time Comparator
CVD	Cardiovascular Disease
DAC	Digital-to-Analog Converter
DAS	Delay-and-Sum
DC	Direct Current
DFE	Decision Feedback Equalization
DFF	D-Flip-Flop
DLL	Delay Locked Loop
DR	Dynamic Range
DTC	Discrete-Time Comparator
DTI	Deep Trench Isolation

ECG	Electrocardiogram
ESD	Electrostatic Discharge
EW	Electromechanical Wave
EWI	Electromechanical Wave Imaging
FDA	Food and Drug Administration
FDM	Frequency-Division Multiplexing
FF	Flip-Flop
FIFO	First-in First-out
FPGA	Field-Programmable Gate Array
GL	Grating Lobe
GLR	Grating Lobe Residual
HV	High-Voltage
IC	Integrated Circuit
ICE	Intracardiac Echocardiography
IVUS	Intravascular Ultrasound
LDO	Low-Dropout Regulator
LFSR	Linear-Feedback Shift Register
LM	Load Modulation
LNA	Low-Noise Amplifier
LSB	Least-Significant Bit
LSV	Lateral Shift-Variance
LV	Low-Voltage
LVDS	Low-Voltage Differential Signaling
MEMS	Microelectromechanical Systems
MIM	Metal-Insulator-Metal
MOM	Metal-Oxide-Metal
MOSCAP	Metal-Oxide-Semiconductor Capacitor
MRI	Magnetic Resonance Imaging
MSB	Most-Significant Bit
MUX	Multiplexer
NAND	Negative-AND
NOR	Negative-OR
NOV	Non-Overlapping
PAM	Pulse Amplitude Modulation
PCB	Printed Circuit Board
PE	Pulse-Echo

PGA	Programmable-Gain Amplifier
PMUT	Piezoelectric Micromachined Ultrasound Transducers
PRBS	Pseudo-Random Bit Sequence
PRF	Pulse Repetition Frequency
PRI	Pulse Repetition Interval
PRNG	Pseudo-Random Number Generator
PSF	Point-Spread-Function
PSRR	Power Supply Rejection Ratio
PVT	Process/Voltage/Temperature
PZT	Lead Zirconium Titanate
R/C	Row/Column
RMS	Root Mean Square
RS	Reset-Set
RX	Receive
RZ	Return-to-Zero
S/H	Sample-and-Hold
S2D	Single-Ended to Differential
SAP	Subaperture Processing
SAR	Successive-Approximation-Register
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SOI	Silicon-on-Insulator
SR	Shift Register
SS	Single-Slope
T/R	Transmit/Receive
TDM	Time-Division Multiplexing
TEE	Transesophageal Echocardiography
TGC	Time Gain Compensation
TSV	Through Silicon Via
TTE	Transthoracic Echocardiography
TX	Transmit
VCSEL	Vertical-Cavity Surface-Emitting Laser
WHO	World Health Organization
µBF	Micro-Beamforming

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Yannick Hopf
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About the author

Yannick Hopf was born in Seligenstadt, Germany in July 1991.

He received his B.Sc. and M.Sc. degree (*cum laude*) in electrical engineering from the Technical University of Darmstadt, Darmstadt, Germany, in 2014 and 2017 with the M.Sc. graduation being honored with the Eckelmann AG price for the best degree in his year. Since 2018, he is pursuing a Ph.D. degree in electrical engineering at the Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands, with a focus on ASIC design for 3D high-frame-rate medical ultrasound imaging.

In his spare time, he enjoys socializing, dancing, cultural events, and traveling.