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Performance Optimization of SSHC Rectifiers for Piezoelectric Energy Harvesting

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***Abstract*—In the past decades, inductor-based synchronized switch harvesting on inductor (SSHI) rectifiers have been widely employed in many active rectification systems for piezoelectric energy harvesting. Although SSHI rectifiers achieve high energy extraction performance compared to passive full-bridge rectifier (FBR), the performance greatly depends on the inductor employed. While a larger inductor can achieve higher performance, the system form factor is also increased, which is counter to system miniaturization in many applications. To solve this issue, an efficient synchronized switch harvesting on capacitors (SSHC) rectifier was proposed recently. Instead of using large inductors, the SSHC rectifier employs on-chip or off-chip flying capacitors to achieve comparable or higher performance. In previous studies, the flying capacitors are chosen equal to the inherent capacitance of the piezoelectric transducer (PT) to achieve 1/3 voltage flipping efficiency(η_F) for a 1-stage SSHC rectifier and 4/5 flipping efficiency for a 8-stage SSHC rectifier. This brief presents that the flipping efficiency can be further increased to 1/2 for a 1-stage SSHC rectifier if the flying capacitor is chosen to be much larger than C_P and the 4/5 flipping efficiency can be achieved by employing only 4 flying capacitors.**

***Index Terms*—Energy harvesting, piezoelectric transducer, synchronized switch harvesting on inductor (SSHI), synchronized switch harvesting on capacitors (SSHC), switched capacitors, power conditioning, rectifiers.**

I. Introduction

ALONG with the development of Internet of Everything, wireless sensing networks (WSN) act as essential roles interconnecting between the real world and the Internet. Although electrochemical batteries have remained the primary energy sources for such systems due to the high energy density, certain sensors and sensor systems require to operate over significant periods of time much longer than the lifetime of electrochemical batteries. Battery usage may be both impractical and costly due to the requirement for periodic recharging and/or replacement. In order to address this challenge and extend the operational lifetime of wireless sensors, there has been an emerging research interest on harvesting ambient vibration energy [1], [2], [3], [4].

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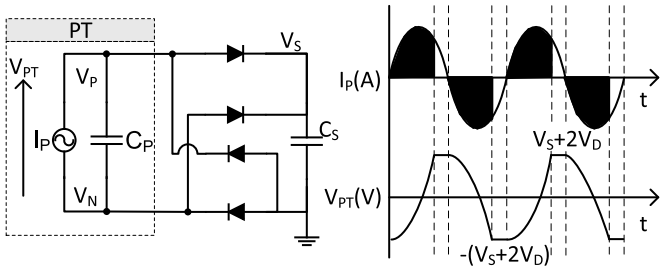

Fig. 1. Full-bridge rectifier for piezoelectric VEH and the associated waveform.

Piezoelectric materials are widely used in vibration energy harvesters (VEH) as mechanical-to-electrical transducers due to their relatively high power density, scalability and compatibility with conventional integrated circuit technologies. A typical piezoelectric VEH can provide a power density of around 10-500μW cm^{-2}, which sets a significant constraint on designing the associated power conditioning interface circuit. The interface circuit not only must consume ultra low power, but it also should be able to recover the power as effectively as possible from the piezoelectric transducer (PT). Full-bridge rectifiers are widely used in commercial energy harvesting systems due to their simplicity and stability; however, they set high threshold voltages for the generated energy to be extracted by the circuit.

Fig. 1 shows a full-bridge rectifier connected with a piezoelectric transducer (PT) and the associated waveform. While the vibrating is at or close to its resonance frequency, a piezoelectric VEH can be modeled as a current source I_P connected in parallel with a plate capacitor C_P. In order to transfer the generated energy from the PT to the storage capacitor C_S, the voltage across the PT, V_{PT}, should attain $\pm(V_S + 2V_D)$. Hence the energy used to charge the internal capacitor C_P from $V_S + 2V_D$ to $-(V_S + 2V_D)$ (or vice-versa) is wasted. The wasted charge in a half vibration cycle can be expressed as:

$$Q_{wasted} = 2C_P(V_S + 2V_D) \tag{1}$$

Therefore, the peak-to-peak open-circuit voltage generated by the PT, V_{PP}(open), should be greater than $2(V_S + 2V_D)$ to make sure that there is remaining charge flowing into C_S after Q_{wasted} is wasted. In large excitation levels, the charge loss Q_{wasted} may take a small part of the total charge generated by the PT. However, in small excitation levels where V_{PP}(open) is below or marginally higher than $2(V_S + 2V_D)$, there will be no charge or very little charge that can be transferred to C_S.

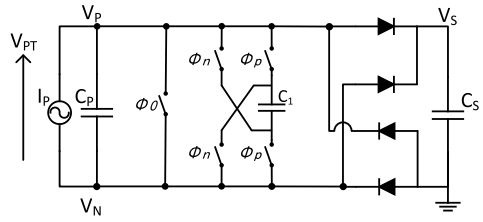

Fig. 2. A 1-stage SSHC rectifier for piezoelectric energy harvesting.

The black areas shown in Fig. 1 show the charge loss caused by charging C_P from $\pm(V_S + 2V_D)$ to $\mp(V_S + 2V_D)$.

In order to improve the power efficiency and minimize the charge waste caused by charging C_P, many active interface circuits have been reported [5], [6], [7], [8], [9], [10]. Among all interface circuits for piezoelectric VEH, synchronized switch harvesting on inductor (SSHI) rectifier, proposed by Badel et al. [11], is one of the most efficient circuits with nearly no charge waste assuming that the inductor is chosen large enough. It performs synchronous charge inversion on C_P through an RLC system using an inductor controlled by synchronized switches [12]. However, the limitation of the SSHI rectifier is the need for a large off-chip inductor. To address this issue, synchronized switch harvesting on capacitor (SSHC) rectifier has been proposed [13], which performs the energy extraction using flying capacitors instead of inductors. The [13] uses some flying capacitors with equal capacitance to C_P to achieve high performance. However, it has to use at least 8 separate flying capacitors to achieve 4/5 flipping efficiency (η_F). This brief investigates a SSHC rectifier achieving 4/5 flipping efficiency using 4 flying capacitors with larger capacitance but the same SMD package. The experiment results show that the flipping efficiency can be improved highly even with less flying capacitors.

II. SSHC Interface Circuit

Fig. 2 shows the design of a 1-stage SSHC rectifier where only 1 switched capacitor C_1 is used to synchronously flip the voltage V_{PT}. In order to perform the charge inversion, five analogue switches driven by three pulse signals (ϕ_p, ϕ_0 and ϕ_n) are used. The three non-overlapping switching signals are synchronously generated to turn ON the five switches sequentially in a given order. The order of the three pulses depends on the polarization of the voltage V_{PT}.

The working principle of the one-stage SSHC rectifier is described as follow. Before I_P reaches zero-crossing point, all the five switched are kept open and the generated charge by the PT flows into the storage capacitor C_S. The voltage polarization across the PT is assumed that $V_{PT} > 0$; hence the top and the bottom diodes are conductive and $V_{PT} = V_S + 2V_D$ during this time. At the moment of I_P zero-crossing point, a pulse ϕ_p is generated to let charge in C_P flow into C_1. At the next phase, ϕ_0 turns on the switch across the PT and clears the remaining charge in C_P. Then, a pulse ϕ_n follows; C_1 is connected to the PT in an opposite sense, hence V_{PT} goes to a negative value and a part of charge is inverted as a result. For flipping the voltage across the PT when $V_{PT} > 0$, the order of the three non-overlapping signals is $\phi_p \rightarrow \phi_0 \rightarrow \phi_n$. While in the other case of $V_P < V_N$, the order of the three signals should be $\phi_n \rightarrow \phi_0 \rightarrow \phi_p$.

A. Performance Analysis With $C_1 = C_P$

As discussed, the SSHC rectifier is able to invert some charge stored in C_P and it is useful to calculate how much charge is inverted and the condition to achieve this performance. Before the zero-crossing moment, it is assumed that V_{PT} is positive and it equals to $V_S + 2V_D$, noted as $V_0 = V_S + 2V_D$ for simplicity. C_1 is assumed to have no charge at the beginning hence the voltage across C_1, V_{C1}, is 0V. At the first zero-crossing moment of I_P, ϕ_p is turned ON firstly because V_{PT} is positive. C_P and C_1 are connected and the charge flows into C_1 until the voltages across the two capacitors are equal. As the total charge keeps unchanged, the voltage across C_P and C_1 at the end of the first phase is:

$$V_{PT-1} = V_{C1-1} = \frac{C_P}{C_P + C_1} V_{PT-0} \tag{2}$$

At the second phase, a pulse ϕ_0 is generated. The remaining charge in C_P is cleared and the charge in C_1 is unchanged. Hence, the voltage across C_P and C_1 at the end of the second phase is:

$$V_{PT-2} = 0, V_{C1-2} = V_{C1-1} = \frac{C_P}{C_P + C_1} V_{PT-0} \tag{3}$$

At the phase ϕ_n, C_1 is connected with C_P again in an opposite sense to charge C_P to a negative voltage. As the total charge in the two capacitors is the remaining charge in C_1 shown in (3), hence the voltages of V_{PT-3} and V_{C1-3} at the end of the third are:

$$|-V_{PT-3}| = V_{C1-3} = -\frac{C_P C_1}{(C_P + C_1)^2} V_{PT-0} \tag{4}$$

It can be seen that V_{PT} is a negative value at the end of the zero-crossing moment. By setting the derivative of the expression in (4) at 0, it can be found that V_{PT-3} attains its minimum value while $C_1 = C_P$. Therefore, when $C_P = C_1$, the minimum value of V_{PT} at the end of the first charge inversion is:

$$V_{PT-3} = -V_{C1-3} = -\frac{1}{4} V_0 \tag{5}$$

The resulting voltage in (5) is obtained after the first charge inversion and the initial voltage across C_1 is assumed at 0V at the beginning. However, before the second zero-crossing moment, V_{C1} is no longer 0 V, but $\frac{1}{4}V_0$. As a result, for the second flip cycle, more charge is inverted in the second zero-crossing moment compared to the first one due to the initial V_{C1} built in the first cycle. The remaining charge in C_1 keeps accumulating; hence, the resulting $|V_{PT}|$ at the end of the n^{th} inversion stage is:

$$\begin{aligned} |V_{PT}| &= ((\frac{1}{4})^n + \ldots + (\frac{1}{4})^2 + \frac{1}{4})V_0 \\ &= \sum_{1 \le i \le n} (\frac{1}{4})^i V_0 = \frac{\frac{1}{4} - (\frac{1}{4})^n}{1 - \frac{1}{4}} V_0 \\ &\longrightarrow \lim_{n \to \infty} |V_{PT}| = \frac{1}{3} V_0 \end{aligned} \tag{6}$$

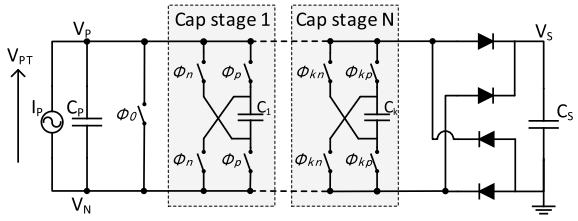

Fig. 3. Schematic of N-stage SSHC rectifier with multiple capacitors.

TABLE I
THE FLIPPING EFFICIENCY WITH DIFFERENT N AND C_K

Stage numbers N	$\eta_F(C_k = C_P)$	$\eta_F(C_k = 455C_P)$
1	1/3	1/2
2	1/2	2/3
3	3/5	3/4
4	2/3	4/5
5	5/7	5/6
6	3/4	6/7
7	7/9	7/8
8	4/5	8/9

While n tends to infinity, $|V_{PT}|_{n\to\infty} = \frac{1}{3}V_0$, which means one third of charge can be inverted theoretically while $C_1 = C_P$. The voltage flipping efficiency η_F can be further increased by employing more capacitor stages. A N-stage SSHC rectifier just simply copies the "cap stage" N times and insert them in the rectifier as shown in the Fig. 3 and C_k is the flying capacitor. When there are N cap stages, there are 2N + 1 switch phases. The simulated voltage flipping efficiency (η_F) with $C_k = C_P$ for 1-, 2, 4- and 8-stage SSHC rectifier are given in the middle of Table I.

B. Performance Analysis With $C_1 >> C_P$

For most of macroscopic and MEMS PTs, C_P typically varies between a few nF to several tens of nF. While C_1 needs to be equal to C_P in previous papers, however, the capacitor C_1 cannot be easily implemented on-chip due to the large capacitance; hence, the switched capacitors in SSHC rectifiers are usually implemented off-chip. For a tiny commercial SMD ceramic capacitor, the capacitance varies in a wide range (e.g., for the specified 6.3 V with ±10% tolerance, the same package of 0805 [2012 Metric] X7R covers the capacitance from 220 pF to 10 μF). Hence, it is interesting to analyze if the system performance can be further improved by using a C_1 with much larger capacitance but with a same SMD package size. It is assumed for a 1-stage SSHC rectifier, the voltage across the C_P and the flying capacitor C_1 before flipping is V_{PT-0} and V_{C1-0}. When the C_P dumps the charge to C_1, the new voltage V_{PT-1} and V_{C1-1} can be expressed as follows

$$V_{PT-0}C_P + V_{C1-0}C_1 = V_{PT-1}C_P + V_{C1-1}C_1 \quad (7)$$

$$V_{PT-1} = V_{C1-1} \quad (8)$$

When the C_P is cleared, the new voltage V_{PT-2} and V_{C1-2} across C_P and C_1 can be expressed as

$$V_{PT-2} = 0, V_{C1-2} = V_{C1-1} \quad (9)$$

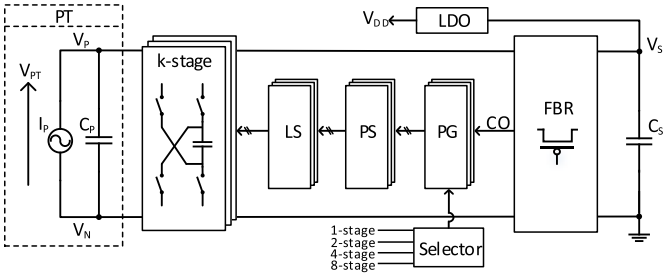

Fig. 4. Simplified system architecture of the proposed SSHC rectifier.

After flipping, the voltage across C_P and C_1, V_{PT-3} and V_{C1-3} can be expressed as

$$V_{C1-3}C_1 = |V_{PT-3}C_P| + V_{C1-3}C_1 \quad (10)$$

$$V_{PT-3} = V_{C1-3} \quad (11)$$

Considering steady state condition, before and after flipping, there is a relationship between the voltage across C_1

$$V_{C1-0} = V_{C1-3} \quad (12)$$

Therefore, combining (7)-(12), the flipping efficiency of the 1-stage SSHC (η_{F-1}) can be derived as

$$\eta_{F-1} = |\frac{V_{PT-3}}{V_{PT-0}}| = \frac{C_1}{C_P + 2C_1} \quad (13)$$

Therefore, (13) shows that the flipping efficiency totally depends on the capacitance ratio of C_1 and C_P. Similarly, the flipping efficiency of a 2-stage SSHC (η_{F-2}) can be expressed as

$$\eta_{F-2} = \frac{2C_k}{C_P + 3C_k} \quad (14)$$

Furthermore, from above all equations, if there are N stages flying capacitors employed, the voltage flip efficiency (η_F) with capacitance C_k can be calculated by

$$\eta_F = \frac{NC_k}{C_P + (N+1)C_k} \quad (15)$$

Thus, (15) shows that both more capacitors and larger capacitance are employed resulting in higher flipping efficiency. Hence, the system form factor can be further reduced by using a large capacitance. When multi-stage SSHC rectifiers are taken into the analysis ($C_1 = C_2 = \ldots C_8 = 455C_P$), the voltage flipping efficiency (η_F) is shown in the right of Table I. Compared with the equal capacitor as shown in the middle of Table I, the voltage efficiency is generally higher when using larger capacitors. It can also be seen that the efficiency achieves 4/5 when four capacitors are employed, while the model with $C_k = C_P$ requires 8 off-chip capacitors to achieve this performance. However, by using the same 8-stage SSHC rectifier with $C_k >> C_P$, the flipping efficiency is up to 8/9. Hence, the new design reduces the required off-chip capacitor number from 8 to 4 to achieve 4/5 voltage flipping efficiency and achieves higher flipping efficiency with the same stages. This improvement is particularly useful to reduce the system form factor for the energy harvesters to be implemented in space-limited locations.

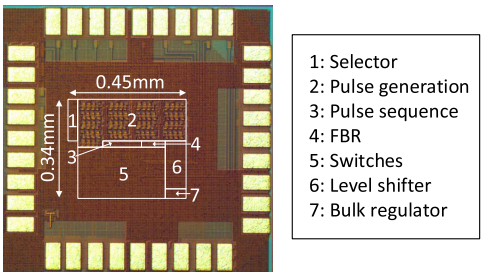

Fig. 5. Chip micrograph.

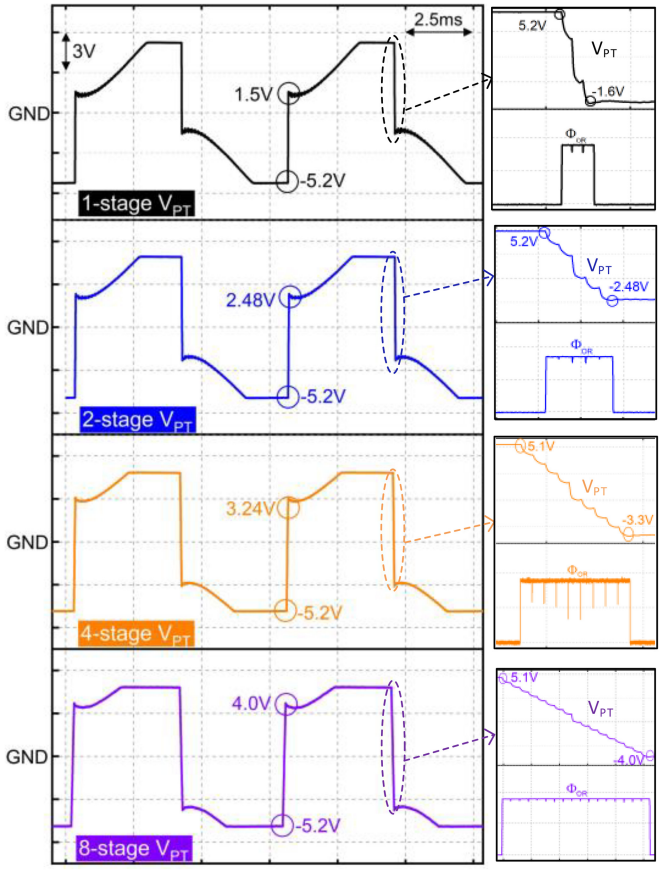

Fig. 6. Measured waveform of 1-, 2-, 4- and 8-stage SSHC with $C_k = C_P$.

III. Circuit Implementation

This design was fabricated in a TSMC 180 nm BCD CMOS process. The withstand voltage of the transistors is 5 V. The system architecture of the proposed SSHC rectifier is shown in Fig. 4. The configurable SSHC rectifier is designed to verify the relationship between the flipping efficiency and number of stages with different flying capacitors. When the rectifier is cut-off, the CO, coming out of the FBR, generates a rising edge which indicates the time to flip V_{PT}. Therefore, switch pulses are generated by pulse generation (PG) and sequenced by the PS. Through the level shifters (LS), the shifted pulses are used to drive the switches during V_{PT} flipping. The digital selector block is employed to decide how many stages are used in the SSHC rectifier. It has four choices: 1-, 2-, 4- and 8-stage which are tuned by the off-chip inputs. Corresponding chip micrograph is shown in Fig. 5 which occupies 0.153 mm^2 in total.

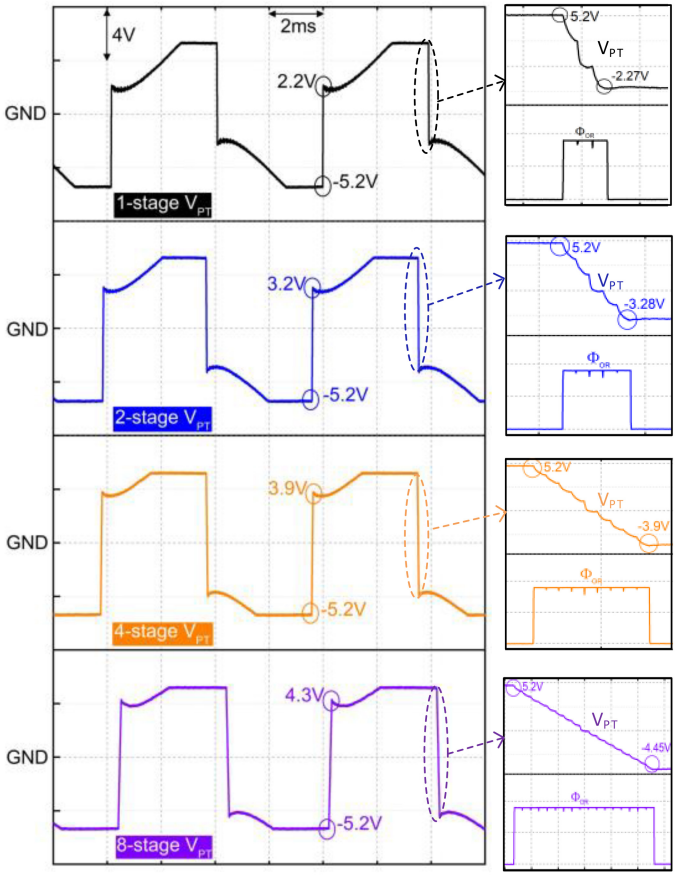

Fig. 7. Measured waveform of 1-, 2-, 4- and 8-stage SSHC with $C_k = 455C_P$.

IV. Experiments

In order to evaluate the performance and verify the simulation results, a commercially available PT (PEH-S129-H5FR-1803YB) is employed and the measured internal capacitance of this PT is C_P = 22 nF. The PT is excited at its natural frequency of 130 Hz. The input open circuit voltage (V_{OC}) is 2 V. The storage capacitor C_S is 100 μF - 0805 [2012 Metric] X5R. The employed capacitance of the flying capacitors are: 22 nF - 0805 [2012 Metric] X7R for the verification of $C_k = C_P$, and 10 μF - 0805 [2012 Metric] X7R for the verification of $C_k = 455 \times C_P$.

Fig. 6 shows the measured V_{PT} of the 1-, 2-stage, 4-stage and 8-stage SSHC rectifier with $C_1 = C_P$ = 22 nF. The Fig. 6 shows the flipping moment of V_{PT}. The pulse signal "ϕ_{OR}" on the right is the logical OR of all the ϕ switch signals due to the limited number of probes of the oscilloscope. The switch phases can be clearly seen from the figure that the flipping efficiency was measured to be around 28.85% (1.5 V over −5.2 V) with 1-stage SSHC rectifier. While the flipping efficiency rises to 47.69% (2.48 V over −5.2 V) by employing 2 capacitors. When 4 and 8 capacitors are employed, the flipping efficiency are found to be around 62.31% (3.24 V over −5.2 V) and 76.92% (4.0 V over −5.2 V) respectively.

The measured V_{PT} of the 1-, 2-, 4- and 8-stage SSHC rectifier with $C_1 = 455C_P$ = 10 μF are shown in Fig. 7. The flipping efficiency of 1-stage and 2-stage SSHC rectifier are around 42.31% (2.2 V over −5.2 V) and 61.54% (3.2 V over

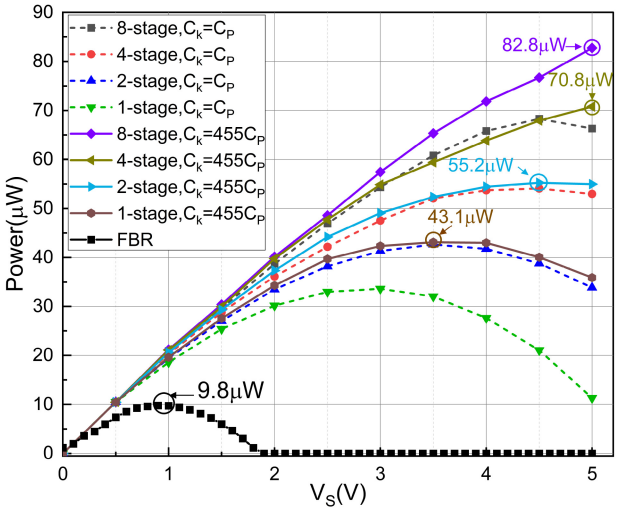

Fig. 8. Measured output power with different configurations.

$-5.2\,\mathrm{V}$) respectively. When 4- and 8-stage SSHC rectifiers are working, the corresponding flipping efficiency are around 75% (3.9 V over $-5.2\,\mathrm{V}$) and 82.70% (4.3 V over $-5.2\,\mathrm{V}$), which indicates that for the same flipping efficiency obtained by 8-stage SSHC with $C_1 = C_P$ can be obtained by a 4-stage SSHC with $C_1 >> C_P$. When the same stage SSHC is configured, a higher flipping efficiency can be achieved by using a larger flying capacitor.

Fig. 8 shows the output power of the FBR and 1-, 2-, 4-, and 8-stage SSHC with $C_k = C_P$ and $C_k = 455C_P$. The input V_{OC} is 2 V. Compared with the SSHC rectifier by using $C_k = C_P$, the proposed SSHC rectifier with $C_k = 455C_P$ reduces the stage number of the SSHC rectifier by half, while achieving almost the same output power. When use the same stage SSHC rectifier, the proposed SSHC with larger capacitance always has high output power. The peak power of the FBR rectifier is $9.8\,\mu\mathrm{W}$. The peak power for the proposed 1-, 2-, 4- and 8-stage SSHC rectifier with $C_1 = 455C_P$ are $43.1\,\mu\mathrm{W}$, $55.2\,\mu\mathrm{W}$, $70.8\,\mu\mathrm{W}$ and $82.8\,\mu\mathrm{W}$. Compared with the FBR, the maximum power enhancement is up to 8.4×.

V. Conclusion

In previous SSHC rectifier studies, the capacitance of the employed capacitors (C_k) is selected to be equal to the internal capacitor of the PT (C_P) to achieve 1/3 voltage flipping efficiency for a 1-stage SSHC and 4/5 voltage flipping efficiency for an 8-stage SSHC. This brief presents that, when the capacitors have to be off-chip implemented, the voltage flipping efficiency can be further increased if the capacitors are chosen with much higher capacitance than the C_P, which means $C_k >> C_P$. The measured results demonstrate that the system form factor of an SSHC energy harvester can be further reduced by employing larger capacitors to achieve high performance, which is particularly useful when energy harvesters are implemented in space-limited locations, such as miniaturized wireless sensors and biomedical implants.

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