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Class-D amplifiers (CDAs) are widely used in audio applications where a high power efficiency is required. As most audio sources are digital nowadays, implementing digital-input CDAs results in higher levels of integration and lower cost. However, prior open-loop digital-input CDAs suffer from high jitter sensitivity and output-stage distortion. In [1], jitter sensitivity at small signal levels is mitigated using a buck-boost converter that adaptively lowers the supply at the expense of extra external components and reduced power efficiency. Prior closed-loop digital-input CDAs employing multi-bit current-steering [2] or resistive [3] DACs are less sensitive to jitter, but their DR is limited to about 115dB. DAC non-idealities and intermodulation distortion are also challenges, and prior works only achieved a peak THD+N of about –98dB [2,3]. This paper presents a digital-input CDA that achieves high DR by combining a low-noise capacitive DAC (CDAC) with dedicated techniques to mitigate DAC mismatch, ISI, and intermodulation distortion. A prototype implemented in a 0.18µm BCD process achieves 120.9dB DR and –111.2dB peak THD+N. Furthermore, it can deliver 13W/23W at 10% THD into an 8Ω/4Ω load with a 90%/86% efficiency.

To avoid the thermal and/or 1/*f* noise of current-steering or resistive DACs, a CDAC can be used to drive a closed-loop CDA based on the capacitively-coupled chopper-amplifier (CCCA) topology presented in [4]. Potential intermodulation between the DAC output waveform, which contains DAC images around multiples of f_S as well as shaped quantization noise, and the various chopping and PWM tones must then be carefully mitigated. Figure 3.1.1 (top) shows an architectural overview of this capacitively-coupled chopper digital-input CDA. A 24-bit digital input is up-sampled to f_S=768kHz (16×48kHz), reduced to 8 bits by a 6th-order digital ΔΣ modulator (DSM1), and then converted into the analog domain by a CDAC. The latter drives a closed-loop CDA with an embedded CCCA front-end, a 14.4V 3-level PWM-based output stage, and feedback after the LC filter, enabling low noise and suppressing LC filter nonlinearity [4]. To compensate for the LC filter's phase shift, the loop filter must implement at least one zero, which inevitably causes some overshoot in its response to DAC transitions. At large signal levels, this will saturate the output stage and thus reduce the CDA's linear output range. To keep the overshoot small, an 8-bit DAC is used, resulting in only a 0.5dB loss in the CDA's linear output range. Together with DSM1, the DAC achieves an SQNR of 136dB, a maximum stable amplitude (MSA) of 0.99FS, and a signal-to-jitter-noise ratio (SJNR) of 131.5dB when driven by a 768kHz clock with 100ps of white clock jitter.

Chopping mitigates the CDA's 1/*f* noise and is performed at $f_{CHOP}=f_S/2$ to exploit the spectral nulls in the shaped quantization noise at multiples of f_S and, thus, avoid noise folding. As shown in Fig. 3.1.1 (bottom), the chopping and DAC input transitions are aligned. After each transition, the CCCA will slew briefly before settling. To eliminate the resulting nonlinearity and DAC ISI, a dead-band (DB) is introduced, which starts just before the chopping and DAC code transitions. During the DB, the CCCA is briefly disconnected from the rest of the loop filter. However, the resulting sample-and-hold operation also folds down (thermal) noise around integer multiples of f_S. A 20ns DB is chosen as a compromise between CCCA settling and noise folding. The loop filter output is re-modulated by a 3-level analog PWM modulator switching at f_{PWM}=4.992MHz, which is an odd (13th) harmonic of f_{CHOP}. This avoids intermodulation distortion between the chopping and PWM sidebands [4]. However, this also means that f_{PWM} (=6.5f_S) is not located at a multiple of f_S, so some quantization noise folding will occur. Fortunately, the quantization noise around f_{PWM} is attenuated by the sinc roll-off of the DAC spectrum and the lowpass characteristics of the CDA's STF, so the folded noise is negligible (< –150dBFS).

To reduce the complexity of the DEM scheme needed to achieve high linearity, the 8-bit DAC is segmented. As shown in Fig. 3.1.2, the input of the MSB segment (D_1) is produced by a second digital modulator (DSM2), while the LSB segment is driven by the shaped quantization error (D_2) [5]. Ideally, no input-related content should be present in D_2 such that the gain mismatch of the two DAC segments contributes only shaped noise. In [2,5], a 1st-order DSM is used, which could produce idle tones at small signal levels, leading to harmonic content in D_2. The gain mismatch between the segments will then allow some of this content to leak into the output. In this work, a 2nd-order DSM is used to alleviate the idle tone issue. This also reduces quantization noise leakage by about 20dB compared to a 1st-order DSM2. A 2-bit overlap is introduced between the 2 segments to accommodate the extra swing caused by the shaped quantization noise of DSM2. D_1 and D_2 thus drive two sub-DACs with 8× and 1× weights, respectively. The (digitally) chopped DAC output $D_{IN}\phi_{CH}V_{REF}$ is applied to a CCCA, which forms the loop filter's error amplifier. The CCCA amplifies V_{ERR} (=$D_{IN}V_{REF}$–V_{OUT}/8) with a gain of 8× (=32×8C_U/C_{GAIN}, since D_2 does not contain the input signal), which attenuates the noise contribution from the rest of the loop filter by 18dB, while also ensuring that the CCCA does not clip due to the DAC images when a 20kHz full-scale input is applied. A total DAC capacitance (288C_U) of 3.5pF is used such that the parasitic capacitance at the summing node does not degrade the feedback factor around the CCCA opamp. This implies a unit capacitance C_U of 12fF, which, together with C_{FB} and C_{GAIN}, is implemented with MOM capacitors due to their high voltage rating.

Unit-element mismatch within the two sub-DACs is addressed with real-time (RT) DEM [6], which produces no idle tones and achieves better SNDR at the chosen OSR (=19.2) than data-weighted averaging (DWA). Furthermore, since the DAC elements are driven by a PWM-like signal, their individual mismatch contribution is reduced at small input levels as the dutycycle of their PWM inputs approaches 50%. With RTDEM, however, code changes larger than 1 may cause nonlinear ISI [6], which will happen quite often since the DAC input is chopped. In this work, this source of nonlinearity is also eliminated by the DB. The timing control scheme to align RTDEM, DB, and chopping in both LV and HV domains is shown in Fig. 3.1.3. A 49.92MHz (=65f_S) master clock (MCLK) is employed to define the DB and control the timing of RTDEM, where 1 MCLK cycle is allocated to the DB and 64 cycles to RTDEM. The number of transitions in the remaining time is signal-independent and thus distortion-free. RTDEM is realized using a cyclic shift register that loads thermometer-coded input data in parallel, which is then rotated to ensure that every DAC element is used equally outside the DB. Since the CDA has a nominal full-scale output of ±14.4V, the feedback chopper is realized with LDMOS switches that must be driven through level shifters, which have ~2ns delay. To avoid high-voltage transients, timing skew between the feedback chopper and DAC is minimized using a replica level shifter [4]. As a result, the DAC code transition (ϕ_{DAC}), HV, and LV chopping transitions (ϕ_{CHHV} and ϕ_{CHLV}) are aligned and fully covered by the DB.

The capacitively-coupled digital-input CDA is prototyped in a 0.18µm BCD process and occupies an area of 7.5mm² (Fig. 3.1.7). An Audio Precision APx555 audio signal analyzer provides the 24-bit digital input and captures the CDA output. For flexibility, the interpolation filter and digital DSMs are implemented in an FPGA. The RTDEM and timing logic (Fig. 3.1.3) is implemented on-chip and consumes about 460µW from a 1.8V supply. Figure 3.1.4 (top) plots the output spectrum when the CDA drives an 8Ω load with a –10dBFS sinewave input at 1kHz, corresponding to 1W of output power. The measured THD+N is –108.6dB. The output spectrum at –60dBFS is shown in Fig. 3.1.4 (bottom), where an SNR of 60.9dB is achieved, indicating that this CDA has a DR of 120.9dB. Figure 3.1.5 (top) shows the measured THD+N across output power for a 1kHz input. The peak THD+N is –111.2dB and –106.6dB for 8Ω load and 4Ω load, respectively. The output power at 10% THD is 13W and 23W for 8Ω load and 4Ω load, respectively. Figure 3.1.5 (bottom) plots the THD+N vs. input frequency.

Figure 3.1.6 compares the performance of this work with other state-of-the-art digital-input CDAs. It is the only capacitively-coupled digital-input CDA. Compared to other high-voltage (>10V) CDAs, it achieves the best peak THD+N (14B lower than [3]), the highest dynamic range (5.4dB higher than [3]), and the lowest A-weighted integrated output noise (2× lower than [3]).

Acknowledgement:
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References:

[1] W. H. Sun et al., "A 121dB DR, 0.0017% THD+N, 8× Jitter-Effect Reduction Digital-Input Class-D Audio Amplifier with Supply-Voltage-Scaling Volume Control and Series-Connected DSM," *ISSCC*, pp. 486-487, Feb. 2022.
[2] A. Matamura et al., "An 82mW ΔΣ-Based Filter-Less Class-D Headphone Amplifier with -93dB THD+N, 113dB SNR and 93% Efficiency," *ISSCC*, pp. 432-433, Feb. 2021.
[3] E. Cope et al., "A 2×20W 0.0013% THD+N Class-D Audio Amplifier with Consistent Performance up to Maximum Power Level," *ISSCC*, pp. 56-57, Feb. 2018.
[4] H. Zhang et al., "A 121.4dB DR, -109.8dB THD+N Capacitively-Coupled Chopper Class-D Audio Amplifier," *ISSCC*, pp. 484-485, Feb. 2022.
[5] R. Adams et al., "A 113 dB SNR Oversampling DAC with Segmented Noise-Shaped Scrambling," *IEEE JSSC*, vol. 33, no. 12, pp. 1871-1878, Dec. 1998.
[6] S. -H. Wen et al., "A -117dBc THD (-132dBc HD3) and 126dB DR Audio Decoder with Code-Change-Insensitive RT-DEM Algorithm and Circuit Technique for Relaxing Velocity Saturation Effect of Poly Resistors," *ISSCC*, pp. 482-483, Feb. 2022.

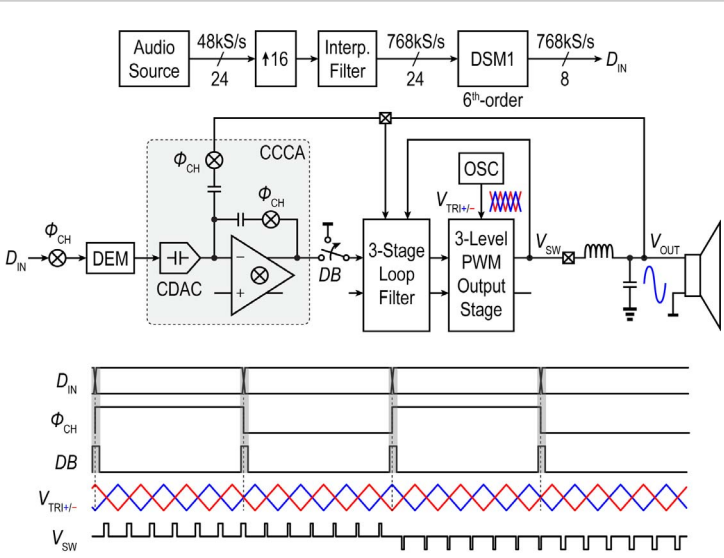

Figure 3.1.1: Architecture of the proposed capacitively-coupled digital-input Class-D audio amplifier.

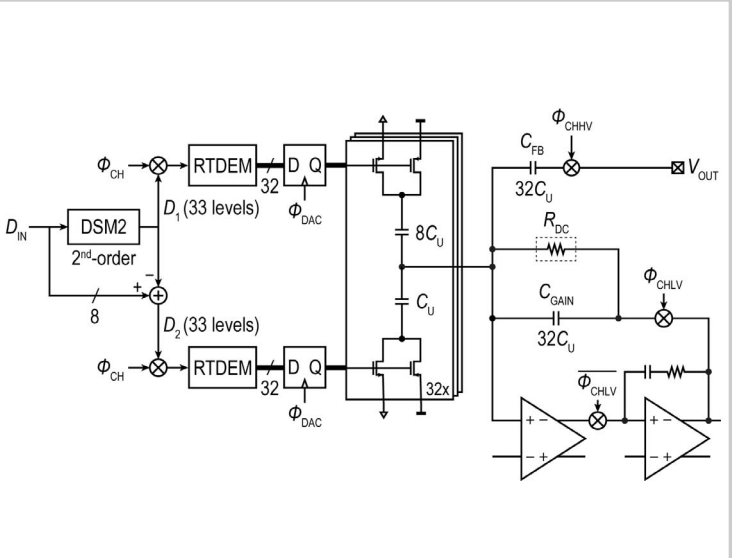

Figure 3.1.2: Simplified schematic of the 8-bit CDAC with noise-shaped segmentation and the capacitively-coupled summing node of the loop filter.

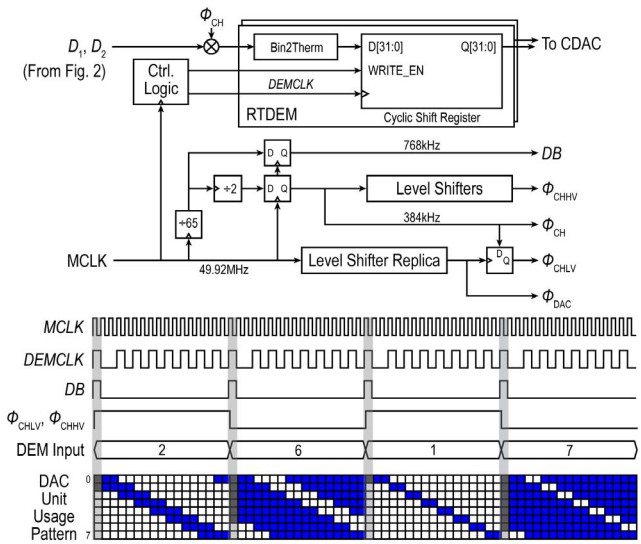

Figure 3.1.3: (top) Timing control circuitry of the CDAC, RTDEM, and chopping, and (bottom) its timing diagram (for a 9-level sub-DAC, the actual implementation uses two 33-level sub-DACs).

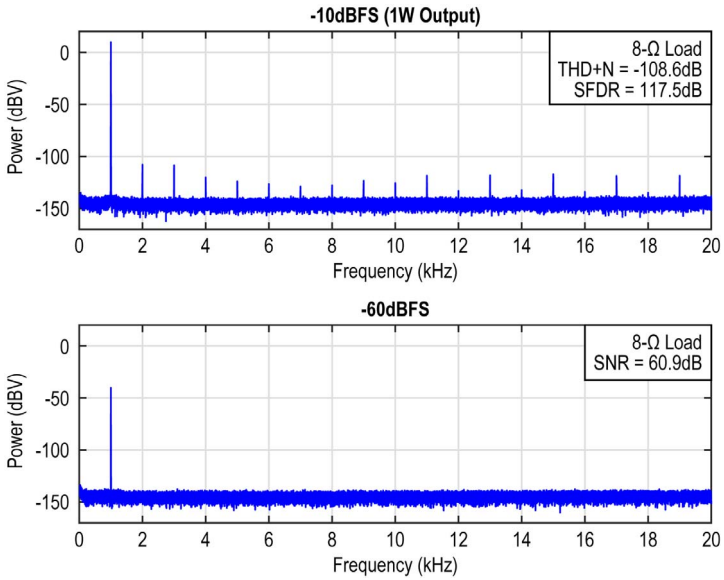

Figure 3.1.4: Measured output spectra (256k-point FFT, 4× averaged).

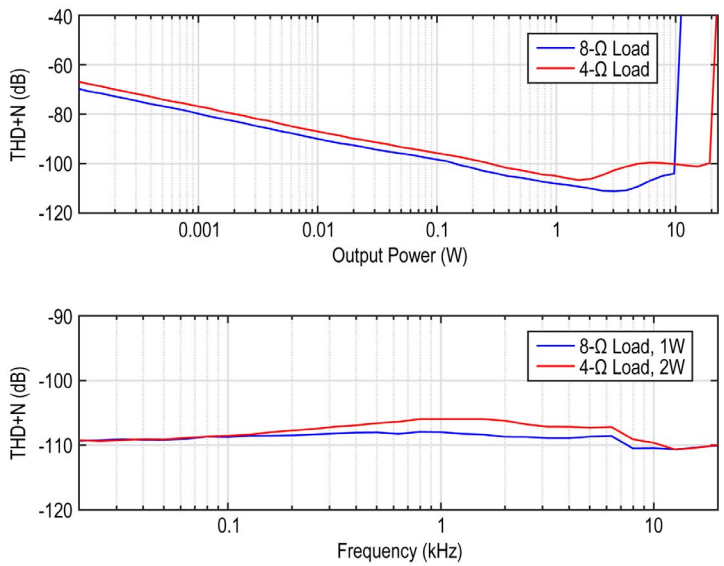

Figure 3.1.5: Measured THD+N (top) at 1kHz across output power, and (bottom) across input frequency.

	This Work	E. Cope ISSCC 2018 [3]	D. Schinkel JSSC 2017	J.-M. Liu JSSC 2012	T. Ido ISSCC 2006	ADI SSM3582A
Process	**180nm BCD**	180nm BCD	140nm BCD SOI	0.35/3μm CMOS	-	-
Area (mm^2)	**7.5**	4.3	-	-	23(1)	-
Architecture	**Closed-Loop**	Closed-Loop	Closed-Loop	Open-Loop	Closed-Loop	Closed-Loop
DAC Type	**CDAC**	RDAC	IDAC	-	IDAC	-
Supply (V)	**14.4**	8~20	25	18	35	4.5~16.5
$I_{Q,PVDD}$ (mA)	**13.9**	20.5	-	9.4	-	12.3
R_{LOAD} (Ω)	**8/4**	8/4	4	8	4/6/8	8/4
$P_{OUT,MAX}$ (W)	**13/23**	20	80	13	130/99/74(1)	18/32
Efficiency η	**90%/86%**	90%	>90%	88%	81%(1)	94%/91%
THD+N @ 1kHz	**-111.2/-106.6**	-97.2(2)/-93.1(2)	-88.6	-62.5	-94.9	-94(2)
DR (dB)	**120.9**	115.5	115	84	113	109
A-wt. Output Noise ($μV_{RMS}$)	**9.3**	20	34	-	-	36
PSRR (dB) (Freq./Hz)	**97~78 (20~20k)**	80~50 (20~20k)	88~60 (100~20k)	-	-	88 (1k)
Suppress LC Filter Distortion	**Yes**	No	Yes	No	No	No

(1) Output stage is off-chip
(2) Extracted from figure

Figure 3.1.6: Performance summary and comparison with state-of-the-art monolithic high-voltage (>10V) digital-input CDAs.

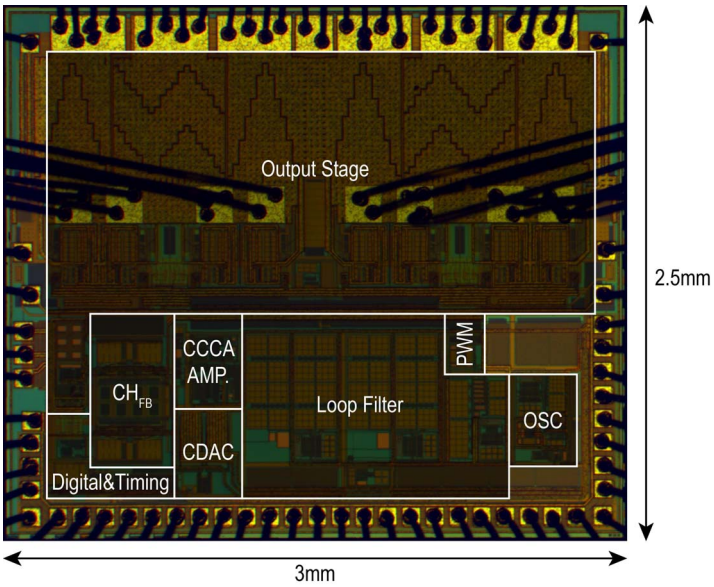

Figure 3.1.7: Die micrograph.

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