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DOI
10.1109/ISSCC42615.2023.10067656

Publication date
2023

Document Version
Final published version

Published in
2023 IEEE International Solid-State Circuits Conference, ISSCC 2023

3.2 A Chopper-Stabilized Amplifier with a Relaxed Fill-In Technique and 22.6pA Input Current

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In chopper amplifiers, the interaction between the input signal and the chopper clock can cause intermodulation distortion (IMD). This is due to amplifier delay, which causes signal transitions generated by the input chopper to arrive at the amplifier's output slightly later than the corresponding clock transitions of the output chopper. This causes large signal-dependent spikes in the final output, which can significantly degrade amplifier linearity, especially at input frequencies near even multiples of the chopping frequency F_{CH}, which will cause IMD tones near DC. In [2-4], spread-spectrum clocks are used to convert such tones into noise-like signals. However, this increases the noise floor, without solving the underlying problem. Recently, it has been shown that such spikes can be eliminated by using the fill-in technique [1], in which two identical OTAs are chopped in quadrature, allowing a spike-free output to be generated by switching between their outputs in a ping-pong fashion.

Figure 3.2.1 illustrates how the delay of a chopped main OTA (G_{m1}) causes large spikes in its output current (I_{out1}) around the chopping transitions. By switching to the output of a fill-in OTA, a spike-free output current can be generated, thus mitigating chopper-induced IMD. In [1], this switching was done with a 50% duty-cycle, and so two chopped OTAs with the same low offset and 1/f noise are required. In this work, the fill-in OTA is only used briefly, greatly relaxing its offset and 1/*f* noise requirements and obviating the need for chopping. This approach also saves power, since the relaxed fill-in OTA can be turned "off" most of the time. Furthermore, the reduced input switching activity compared to [1], and the use of non-overlapping chopper clocks results in more than 25× less input current.

To mitigate the ripple at the chopping frequency F_{CH} caused by their up-modulated offset, the chopped OTAs in [1] were also auto-zeroed. However, the noise-folding inherent to auto-zeroing then causes a noise "bump" around F_{CH}. In this work, since the fill-in OTA is not chopped, only the offset of the main OTA needs to be reduced. This is achieved by a continuous-time ripple-reduction loop (RRL), which does not suffer from noise folding and thus, results in a flat noise spectrum.

A simplified block diagram of the proposed chopper-stabilized amplifier is shown in Fig. 3.2.2. It consists of a main amplifier (A_{MAIN}), whose offset (and 1/*f* noise) will appear between its input terminals when it is used in a negative feedback configuration, where it can be sensed and corrected by a chopped auxiliary amplifier. In this work, the offset of a two-stage main amplifier (folded-cascode 1st stage and Class AB 2nd stage) is suppressed by a three-stage auxiliary amplifier. To mitigate its own offset (V_{os1}), the auxiliary amplifier employs a chopped OTA (G_{m1}, folded-cascode), followed by an integrator (G_{mINT}, folded-cascode, $C_{int1,2}$ = 36pF), and a correction OTA (G_{mCOR}, telescopic). The fill-in OTA (G_{m2}) is a non-chopped replica of G_{m1}. Simulations show that its offset (< 1mV) has a negligible effect on the residual offset of the overall amplifier and causes a small (< 3μV_{rms}) tone at $2F_{CH}$ (40kHz). Similarly, its 1/*f* noise also has a negligible effect, resulting in an overall 1/*f* noise corner of only 2Hz in simulation.

The choppers are driven by a constant-V_{GS} clock generator to ensure that their charge injection mismatch, and hence the resulting residual offset and input current, is insensitive to input voltage. The clock generator also generates the non-overlapping clocks needed to guarantee that the switches of the input chopper are never all turned "on", thus eliminating a potential source of input current.

The RRL consists of two capacitors $C_{s1,2}$ (3.6pF) that sense the triangular ripple caused by V_{os1} at the output of the integrator formed by G_{mINT} and $C_{int1,2}$. The resulting current is then demodulated and integrated by the RRL integrator formed by G_{mINT1} and $C_{int3,4}$ (9pF each). Its output is applied to G_{mRRL}, which cancels V_{os1} by injecting a correction current into G_{m1}. Since the amplitude of the ripple is limited by the offset of G_{mINT1}, this is auto-zeroed with the help of C_{AZ1} and C_{AZ2} (4pF each).

However, the RRL can also create chopper-induced IMD, since the signal transitions caused by its ripple-demodulating choppers are delayed by the RRL integrator before they reach the output choppers of G_{m1}. In this design, this extra source of IMD is suppressed in two ways. First, the contribution of the RRL to the output current of G_{m1} is minimized by using a large G_{m1}/G_{mRRL} ratio. However, this is limited to ~600× by the swing of G_{mINT1} and the expected magnitude of V_{os1}. In simulation, this limits the resulting IMD to -100dB. To lower this further, a sample-and-hold is used to freeze the input of G_{mRRL} just before each chopping transition. Further lowpass filtering is achieved by using a small sampling capacitor C_s (=0.5pF) to drive a larger hold capacitor C_H (=7.2pF). These measures ensure that the overall IMD is not limited by the RRL.

Since G_{m2} is only used briefly, it can be turned "off" most of the time. To ensure that the process of turning it "on" and "off" does not itself cause input spikes and more distortion, three measures are taken. First, the OTA's bias current is not completely turned off, but just significantly reduced (by 11×) to mitigate the change in the various biasing voltages. Second, a lowpass filter at the gates of the switched bias current sources of G_{m2} is used to slow down the bias-current transitions. Finally, these bias sources are isolated from the main bias-current generator and other blocks by an extra layer of current mirrors. Simulations show that these measures ensure that the resulting spikes are well below the noise floor, while incurring only a small power penalty. Switching the bias current of the fill-in OTA with a 20% duty-cycle (to allow sufficient settling) then results in a 76% power saving.

The opamp is realized in a 0.18μm CMOS BCD process (Fig. 3.2.7) and has an active area of 0.57mm^2. It draws 620μA from a 5V supply, which drops to 530μA when the fill-in OTA is duty-cycled, a 15% power saving. The power breakdown (Fig. 3.2.5) shows that the contribution of the fill-in OTA is then only 10%. The opamp's voltage noise density is shown in Fig. 3.2.3 without chopping, with chopping and with the fill-in OTA turned "on" and "off" and compared with the extracted voltage noise density of [1]. Without chopping, the opamp has a 1/*f* noise corner frequency of about 2kHz. With chopping, the use of an RRL eliminates the noise bump seen in [1], resulting in a flat noise floor with a lower (12nV/√Hz) spectral density. The measured 1/*f* corner is below 10Hz and is not affected when the fill-in OTA is enabled. Furthermore, no extra tones are created when it is duty-cycled, confirming the effectiveness of the various spike-mitigation measures. Some crosstalk from the external clock can be observed at 20, 60 and 80kHz.

A step response measurement shows the opamp has a slew rate of 2V/μs (up) and 1.4V/μs (down), with no extra ringing due to the RRL. Measurements on 15 samples with a 2.5V input CM voltage and F_{CH} = 20kHz, show that the opamp's offset does not exceed 0.8μV and that its input current remains below 4pA (Fig. 3.2.3 Bottom). Enabling and disabling fill-in only changes the offset slightly, confirming that not chopping the fill-in OTA does not significantly worsen the overall offset.

The input current at mid-supply is about 4pA, which, as predicted in [6], is roughly 4× larger than that of an AZ-stabilized amplifier realized in a similar process [6]. Measurements show that the input current at mid-supply increases linearly with F_{CH}, indicating that it is mainly due to the charge injection mismatch of the input chopper switches. Figure 3.2.3 shows the input current vs input voltage characteristic of three samples: a typical sample, and two worst-case samples. All three draw more input current at low input voltages. Measurements of an un-connected pad show a similar trend, indicating that most of the input current at low input voltages is due to ESD diode leakage.

With the opamp configured as a buffer, a single 1V_{rms} 79kHz (~4F_{CH}) input tone results in the output amplitude spectrum shown in Fig. 3.2.4 (Top). Without the fill-in technique (left), a large -102dB IMD tone is present at 1kHz ($4F_{CH}$-F_{in}). With fill-in enabled, this drops by 24dB, to -125.7dB (right). Measurements on 5 samples show that the achieved IMD spreads between 123dB and 134.4dB, demonstrating good robustness. With a similar 39kHz tone (~$2F_{CH}$), the IMD tone is –112.8dB without fill-in and -128.5dB with fill-in, a 16dB improvement. At lower input frequencies (<5kHz), the IMD tones are below the -140dB noise floor. When two input tones are applied (79 and 80kHz, 0.5V_{rms} each), the resulting amplitude spectrum is shown in Fig. 3.2.5. Without chopping, the IMD at 1kHz is –112.4dB, which increases to –106.9dB with chopping and with fill-in disabled. Enabling fill-in restores the IMD to –112.4dB, demonstrating that it effectively suppresses chopper-induced IMD. Without fill-in, measurements show that the residual ripple amplitude at $2F_{CH}$ is around 0.7μV_{rms}. With fill-in, this increases to 2.5μV_{rms} for a worst-case sample with the largest fill-in OTA offset.

Figure 3.2.6 summarizes the opamp's performance and compares it to the state-of-the-art. It achieves similar IMD (-125.7dB @ 79kHz ~$4F_{CH}$), with a much simpler architecture. Among the chopper amplifiers, it achieves the lowest input current (22.6pA max), only beaten by an AZ amplifier [5], with a trimmed input current and much higher IMD (-44dB). Compared to [1], it achieves 25× less input current and a lower flat white noise level (12nV/√Hz) at similar supply current levels.

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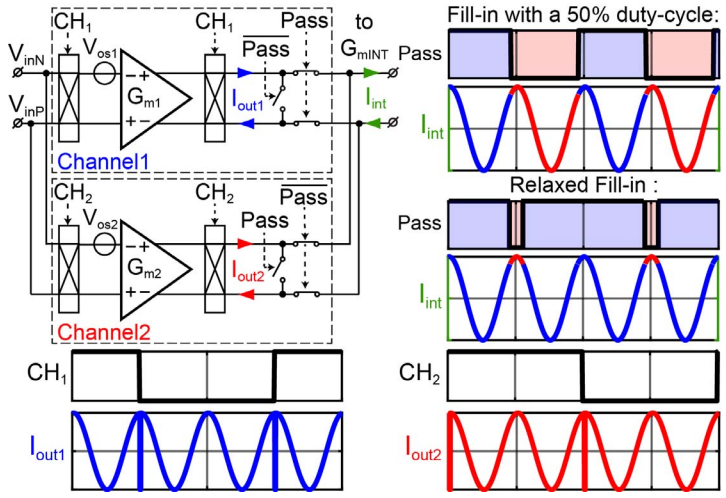

Figure 3.2.1: Fill-in implementation with two chopped OTAs and multiplexing switches (top left), the chopping signals and the resulting output current with spikes (bottom) and the timing diagram for two implementations of multiplexing (top right).

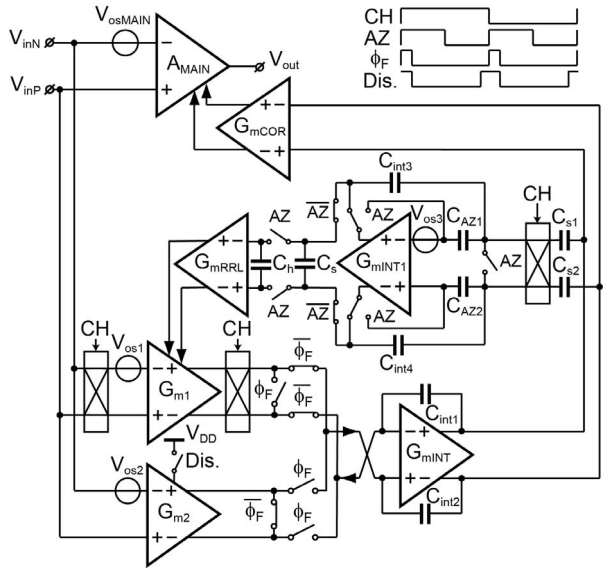

Figure 3.2.2: Simplified block diagram of the proposed Chopper-Stabilized Operational Amplifier.

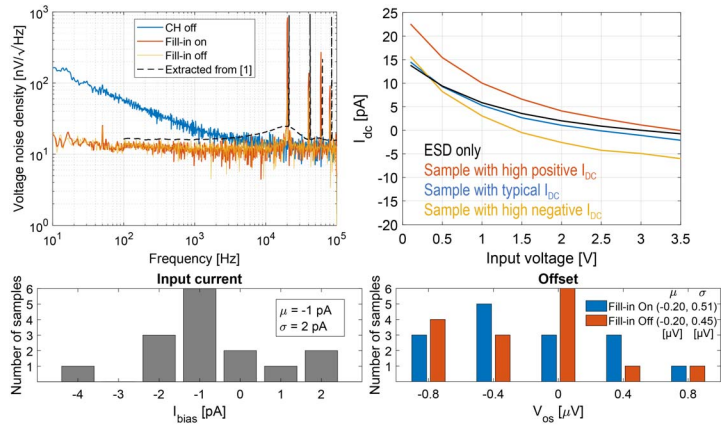

Figure 3.2.3: Voltage noise density vs frequency (top left) and input current vs input voltage (top right). Histogram of the offset and input current at 2.5V for 15 samples (bottom).

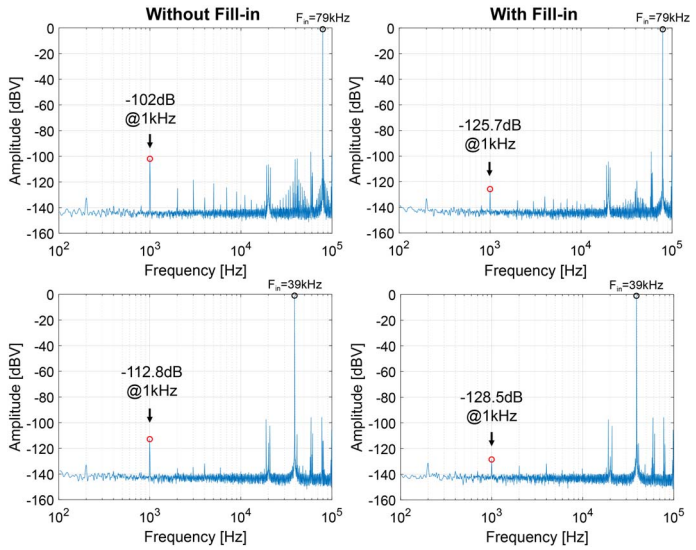

Figure 3.2.4: Measured amplitude spectrum (10 Averages) with a single-tone test for F_{in} = 79kHz (Top) and F_{in} = 39kHz (bottom) without and with fill-in (left & right respectively).

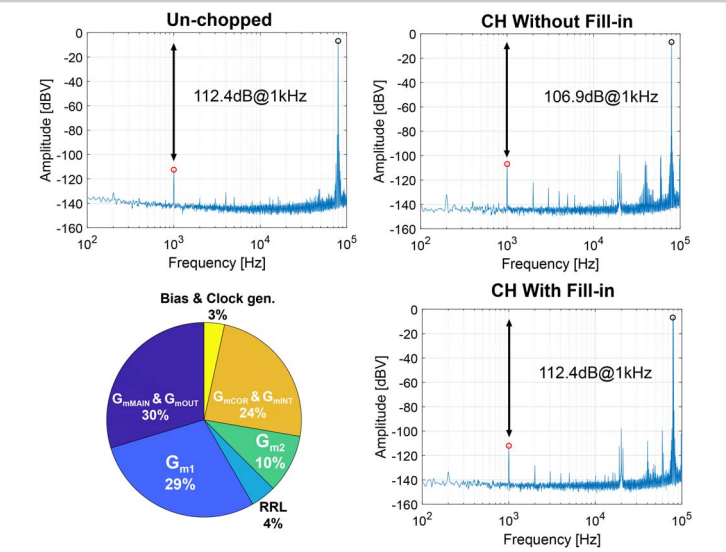

Figure 3.2.5: Two-tone test all in a non-inverting buffer configuration for un-chopped (top left), chopped without fill-in (top right) and chopped with fill-in (bottom right). Power breakdown (bottom left).

	This work	[1] Rooijers 2020	[2] AD8551	[3] AD8571	[4] Ivanov	[5] Rooijers 2019
DOC technique(s)	**Chopping + RRL**	Chopping + AZ	AZ	AZ	Chopping + RRL	AZ + Chopping
DOC frequency (kHz)	**20**	20	4	2 to 4	50 to 150	15
IMD tone (dB)	**f_{in}=79kHz -102 (No Fill-in) -125.7 (Fill-in)**	f_{in}=79kHz -97.7 (No Fill-in) -125.9 (Fill-in)	f_{in}=0.5kHz -80 (Single) -	f_{in}=0.5kHz - -90 (Spread)	f_{in}=1kHz -103 (Single) -122.7 (Spread)	f_{in}=16kHz -44 (Single) -
Offset (Max)	**0.8μV**	0.8μV	5μV	5μV	3.5μV	0.6μV
Input current (Max)	**22.6pA**	600pA	50pA	50pA	200pA	0.2pA
Voltage Noise Density (nV/√Hz)	**12**	16	42	51	6.5	20
GBW (MHz)	**4.2**	4.2	1.5	1.5	10	1.45
Slew rate (V/μs)	**2 (up) 1.4 (down)**	1.7	0.4	0.4	5	-
PSRR (dB)	**124**	124	130	130	135	125
Supply voltage	**5V**	5V	5V	5V	1.8-5.5V	1.8V
Supply current (mA)	**0.62 (Duty off) 0.53 (Duty on)**	0.55	0.85	0.85	1.65	0.21
Die Area (mm²)	**1.25**	1.25	-	-	1.626	1.4

Figure 3.2.6: Performance summary and comparison with previous works.

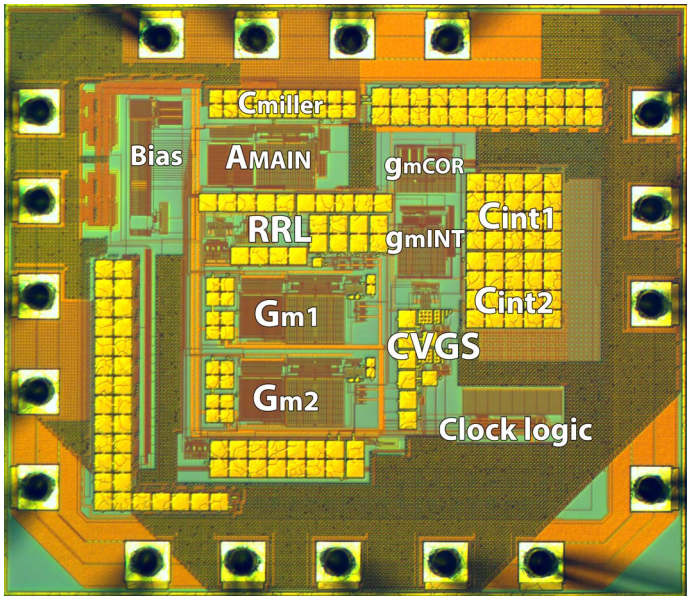

Figure 3.2.7: Die micrograph of the fabricated chip.

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