

A 13.56MHz Fully Integrated 91.8% Efficiency Single-Stage Dual-Output Regulating Voltage Doubler for Biomedical Wireless Power Transfer

Lu, Tianqi ; Chang, Zu Yao; Jiang, Junmin; Makinwa, Kofi; Du, Sijun

DOI

[10.1109/CICC57935.2023.10121186](https://doi.org/10.1109/CICC57935.2023.10121186)

Publication date

2023

Document Version

Final published version

Published in

Proceedings of the 2023 IEEE Custom Integrated Circuits Conference (CICC)

Citation (APA)

Lu, T., Chang, Z. Y., Jiang, J., Makinwa, K., & Du, S. (2023). A 13.56MHz Fully Integrated 91.8% Efficiency Single-Stage Dual-Output Regulating Voltage Doubler for Biomedical Wireless Power Transfer. In *Proceedings of the 2023 IEEE Custom Integrated Circuits Conference (CICC)* (pp. 1-2). IEEE. <https://doi.org/10.1109/CICC57935.2023.10121186>

Important note

To cite this publication, please use the final published version (if applicable). Please check the document version above.

Copyright

Other than for strictly personal use, it is not permitted to download, forward or distribute the text or part of it, without the consent of the author(s) and/or copyright holder(s), unless the work is under an open content license such as Creative Commons.

Takedown policy

Please contact us and provide details if you believe this document breaches copyrights. We will remove access to the work immediately and investigate your claim.

Green Open Access added to TU Delft Institutional Repository

'You share, we take care!' - Taverne project

<https://www.openaccess.nl/en/you-share-we-take-care>

Otherwise as indicated in the copyright section: the publisher is the copyright holder of this work and the author uses the Dutch legislation to make this work public.

A 13.56MHz Fully Integrated 91.8% Efficiency Single-Stage Dual-Output Regulating Voltage Doubler for Biomedical Wireless Power Transfer

Tianqi Lu¹, Zu-yao Chang¹, Junmin Jiang², Kofi Makinwa¹, and Sijun Du¹

¹Delft University of Technology, Delft, the Netherlands

²Southern University of Science and Technology, Shenzhen, China

Dual-output regulating rectifier is highly desired in wireless power transfer (WPT) for sub-100mW bioimplants. Such rectifiers perform voltage rectification and dual-output regulation simultaneously, thus avoiding post DC-DC conversions and cascaded power losses [1-4]. However, the conventional dual-output structure suffers from a low voltage conversion ratio (VCR) (<1) due to the full bridge rectifier (FBR) topology (Fig. 1), severely limiting the receiver operation when wireless link condition varies [1-2]. In order to extend the operational range without increasing the power demand from the transmitter, [3] presents a charge-pump based dual-output rectifier; however, it uses 10 power transistors (PTs) and 8 off-chip capacitors, degrading the power conversion efficiency (PCE) and increasing the integration cost. Alternatively, the current-mode dual-output rectifier can realize a VCR higher than 1, but the output power is limited to less than 10mW [4], which is insufficient for advanced bioimplants. In this work, a 13.56MHz single-stage dual-output voltage doubler (DOVD) is proposed to address the above limitations, which employs only two PTs and a fully integrated design. It can achieve a peak VCR of 1.78 and outputs power up to 81mW with a 91.8% peak PCE.

The proposed DOVD consists of two PTs, S_P and S_N , and two output capacitors, C_{L1} and C_{L2} , in the power stage. Fig. 1 shows the working principle of the DOVD with 4-phase operation. When both outputs, V_{DC1} and V_{DC2} , need to be charged, the DOVD operates in Φ_1 , where both S_P and S_N are enabled to deliver power to C_{L1} and C_{L2} , respectively. When only V_{DC1} needs to be charged, the DOVD switches to Φ_2 , where S_N is disabled so that only C_{L1} is charged. In Φ_3 , S_P is disabled, and the DOVD charges C_{L2} through S_N to build V_{DC2} . Due to the stack topology of C_{L1} and C_{L2} , V_{DC1} also increases slightly when C_{L2} is charged, but this can then be compensated by the controller, as will be explained later. When both V_{DC1} and V_{DC2} do not require energy from the AC input, the DOVD enters Φ_4 , the freewheeling phase, where both S_P and S_N are disabled.

Fig. 2 presents the architecture of the proposed DOVD with controller and the operation principle of the dual-output regulation. S_P (or S_N) is controlled by the delay-compensated comparator CMP_P (or CMP_N) through the gate driver $Driver_P$ (or $Driver_N$), functioning as a power-efficient active diode when enabled. To eliminate the dual-output cross-regulation issue, the parallel pulse frequency modulation (PPFM) controller is proposed, regulating V_{DC1} and V_{DC2} in two distinct hysteresis windows independently. If V_{DC1} (or V_{DC2}) reaches the lower hysteresis threshold, S_P (or S_N) will be enabled by signal EN_P (or EN_N) to charge C_{L1} (or C_{L2}). When V_{DC1} (or V_{DC2}) reaches the upper hysteresis threshold, S_P (or S_N) will be disabled. Selectively enabling the two PTs results in the 4-phase operation. In the freewheeling phase (Φ_4), an over-voltage protection block is activated by the controller (S_{OVP}) to limit the open-circuit V_{AC} .

Fig. 3 shows the circuit implementation of the PPFM controller. To regulate V_{DC1} and V_{DC2} , the controller firstly employs two op-amp comparators (CMPs) to compare the divided versions of V_{DC1} and V_{DC2} with a reference voltage V_{REF} generated on chip. The hysteresis window for V_{DC1} (or V_{DC2}) regulation is defined by the positive feedback resistor R_5 (or R_6) and the resistive voltage divider. The control signals EN_P , EN_N and S_{OVP} are then derived from the CMP outputs, V_{FB1} and V_{FB2} , synchronized with the CLK signal (recovered from V_{AC}). Therefore, EN_P , EN_N and S_{OVP} will not change until V_{AC} roughly equals V_{DC2} , resulting in a zero-voltage phase switching avoiding switching noise and efficiency degradation.

When the DOVD works in Φ_2 (or Φ_3) where S_N (or S_P) is disabled, V_{AC} can level up during the half period without resistive loading. The amplitude of V_{AC} can easily go lower than $-|V_{TH,N}|$ (or higher than $(V_{DC1}+|V_{TH,P}|)$). To avoid the undesired channel conduction in S_N (or

S_P), $Driver_N$ (or $Driver_P$) is designed to clamp V_{GN} (or V_{GP}) to the adaptive biasing V_{MIN} (or V_{MAX}), which tracks the minimum (or maximum) voltage in the system, when S_N (or S_P) is disabled, as shown in Fig. 3.

To drive S_P (or S_N) properly at 13.56 MHz, the delays in CMP_P (or CMP_N) and $Driver_P$ (or $Driver_N$) need to be compensated, or reverse currents and extra conduction losses could pop up. Therefore, CMP_P and CMP_N are designed to be switched-biased push-pull comparators with adaptive delay compensation blocks [5] (Fig. 3). By sampling V_{AC} at the turn-on/off moment of S_P (or S_N) and comparing it to V_{DC1} (or GND) by the error amplifier, the gate-driving delay can steer the feedback loop tuning the bias current in the push-pull comparator, then aligning the turn-on/off timing of S_P (or S_N). The coupling/loading-insensitive delay compensation results in a high PCE. Moreover, shield switches are used to introduce V_{MIN} (or V_{MAX}) into CMP_N (or CMP_P), ensuring robust transistor shutoff when CMP_N (or CMP_P) is disabled in Φ_2 (or Φ_3).

The proposed DOVD was fabricated in the 180nm BCD process, occupying a chip area of 0.4/3.68mm² with/without capacitors. The on-chip resonance capacitor C_{RX} (518pF) is implemented by MIM capacitors; C_{L1} and C_{L2} are MOS/MIM stacking capacitors (3.9nF each). Fig. 4 shows the measured steady state operation waveforms and load transient waveforms of the DOVD. In the steady state, V_{AC} amplitude changes dramatically, notifying 4-phase operation, which can also be verified by EN_P and EN_N . V_{DC1} and V_{DC2} are regulated at 3.6V and 1.8V, respectively, within preset hysteresis windows. The load transient waveforms were measured when R_{L1} was changed between 500 Ω and 4k Ω in both directions and R_{L2} was kept equal to 2k Ω . No voltage undershoot/overshoot is observed at the transient moments, and more importantly, the cross-regulation issue is not observable because, by the nature of the proposed PPFM controller, the response of load transient is theoretically instantaneous and only determined by the preset hysteresis windows [6].

The top half of Fig. 5 shows the self-startup setting and the measured self-startup operation of the DOVD. During startup, the DOVD is forced to work as a passive voltage doubler by diode-connecting S_P and S_N . A V_{TH} -based startup detector is designed to activate the DOVD mode when V_{DC1} reaches $V_{TH,ST}$ (3V). The bottom half of Fig. 5 shows the measured VCR and PCE results of the DOVD. A VCR larger than 1 is easily obtained at V_{DC1} , thanks to the voltage doubler topology. The peak VCR reaches 1.78 when $R_{L1}=R_{L2}=4k\Omega$. Because only two PTs, with gate-driving delay compensated, are employed in the power stage, a high PCE is attained. The peak PCE reaches 91.8% when the total output power P_{OUT} is 33.5mW, and the PCE keeps higher than 87% when P_{OUT} is larger than 30mW.

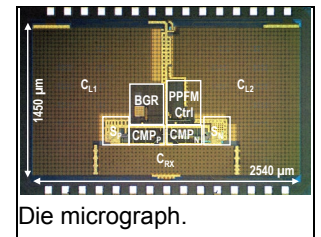
Fig. 6 compares the proposed DOVD with state-of-the-art regulating rectifiers. This work is the only one simultaneously achieving: 1) dual-output regulation, 2) higher-than-1 VCR, 3) up-to-81mW available P_{OUT} , while keeping a state-of-the-art PCE. By fully Integrating the resonance and output capacitors on chip, this work also achieves the smallest receiver volume (1.97mm³) and the highest power density (41.12mW/mm³) among the designs in the table.

Acknowledgement:

The authors would like to acknowledge EUROPRACTICE for MPW and design tool support.

References:

- [1] F. Marefat *et al.*, ISSCC, Feb. 2020.
- [2] F. -B. Yang *et al.*, VLSI, Jun. 2022.
- [3] Z. Xue *et al.*, CICC, Apr. 2018.
- [4] H. S. Gougheri *et al.*, TBioCAS, vol. 13, no. 5, Oct. 2019.
- [5] L. Cheng *et al.*, JSSC, vol. 51, no. 3, Mar. 2016.
- [6] J. Tang *et al.*, ISSCC, Feb. 2021.



Die micrograph.

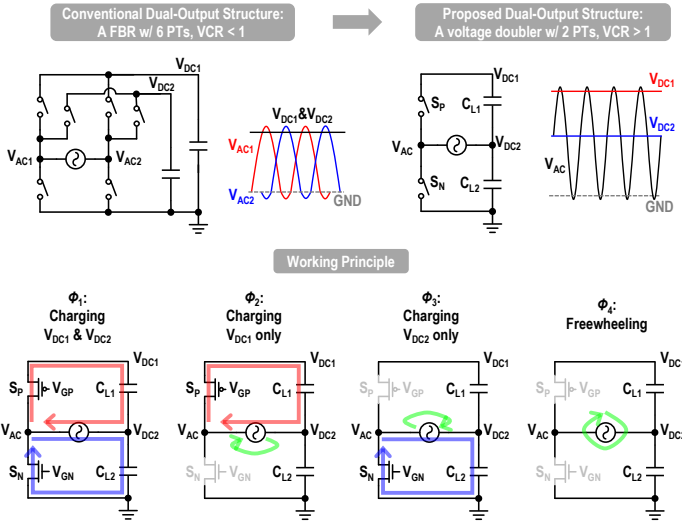


Fig. 1. Conventional dual-output rectifier, and the proposed dual-output voltage doubler structure and its working principle.

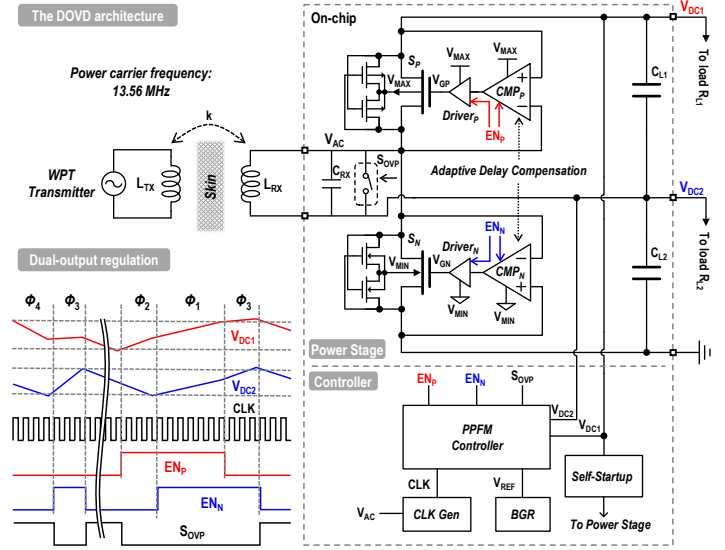


Fig. 2. Architecture of the proposed DOVD with controller, and the operation principle of its dual-output regulation.

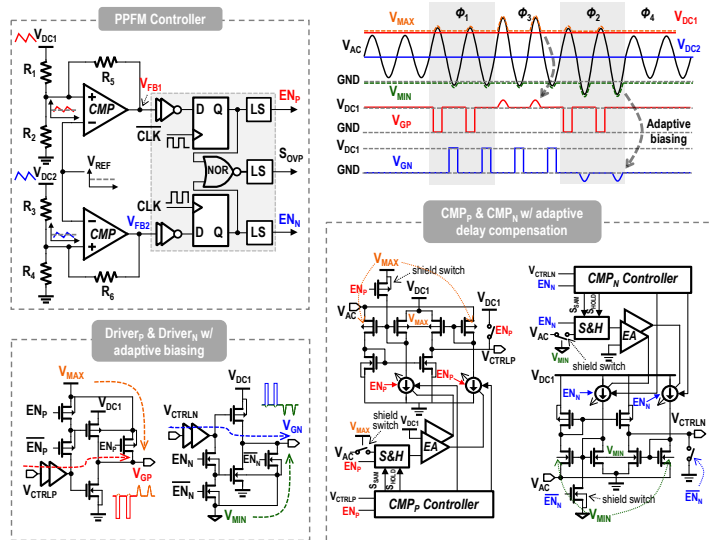


Fig. 3. Circuit implementations of the PPFM controller, the PT drivers and the PT driving comparators.

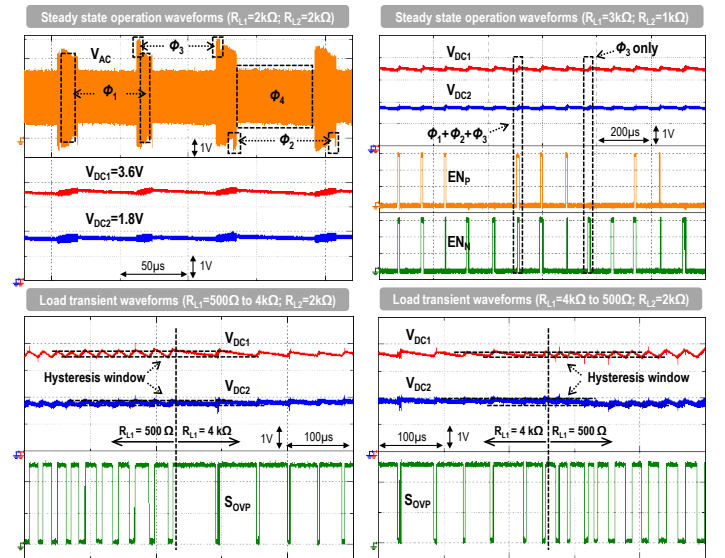


Fig. 4. Measured steady-state waveforms and load transient responses.

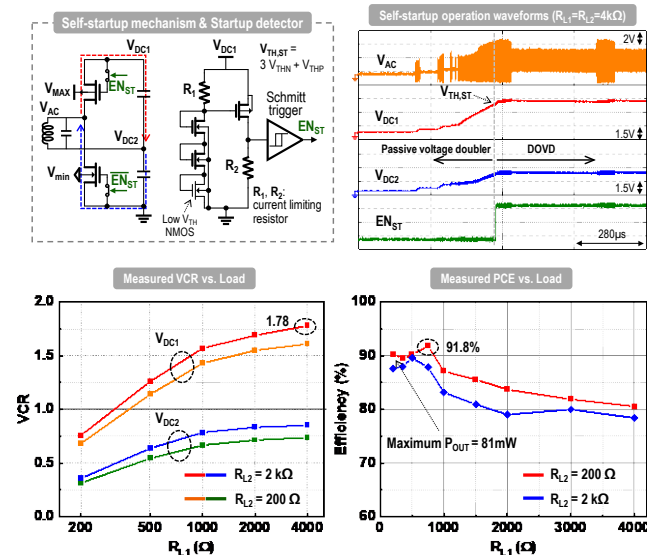


Fig. 5. The schematic and measured operation waveforms of the self-startup setting, and the measured VCR and PCE results.

	This work	[1] ISSCC 2020	[2] VLSI 2022	[3] CICC 2018	[4] TBCAS 2019
Technology	180-nm BCD	180-nm CMOS	180-nm CMOS	180-nm CMOS	350-nm CMOS
Input frequency	13.56 MHz	2 MHz	6.78 MHz	13.56 MHz	1 MHz
Chip area	0.4 mm ² (w/o caps); 3.68 mm ² (w/ caps)	6 mm ²	2.32 mm ²	0.66 mm ²	2.7 mm ²
Receiver topology	Dual-output regulating voltage doubler	Dual-output full-bridge rectifier	Dual-output full-bridge rectifier	Charge-pump based dual-output rectifier	Current mode dual-output rectifier
# of power transistors	2	6	6	10	5
Fully integrated (off-chip components)	Yes	No (2 capacitors)	No (2 capacitors)	No (8 capacitors)	No (2 capacitors)
Receiver volume ^a	1.97 mm ³	5.64 mm ³	3.44 mm ³	8.56 mm ³	3.66 mm ³
Output voltages (# of regulated outputs)	1.8 V, 3.6 V (2)	1.5 V, 2.5 V (2)	3.7 V, 5 V (2)	1.7 V, 2.75 V (2)	2.6 V, 3.9 V (2)
Peak VCR	1.78 (R _{L1,2} =4kΩ)	0.83**	0.85**	2.75	4.88**
Maximum P _{OUT}	81 mW (R _{L1,2} =200Ω)	65 mW	300 mW	10 mW	45 mW
Peak PCE	91.8% (@ 33.5mW)	90.75% (@ 65 mW)	91.7% (@ 200** mW)	79% (@ 7.1 mW)	75.3% (@ 4.7 mW)
Power density ^{***}	41.12 mW/mm ³	11.52 mW/mm ³	8.02 mW/mm ³	1.17 mW/mm ³	12.29 mW/mm ³

^a Assuming off-chip capacitors have the most compact cases on PCB based on their values.

** Estimated from plotted data.

*** Calculated by $\frac{\text{Maximum } P_{OUT}}{\text{Receiver volume}}$

Fig. 6. Performance summary of the proposed DOVD and comparison to state-of-the-art designs.