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DOI
10.1109/TPEL.2023.3262728

Publication date
2023

Document Version
Final published version

Published in
IEEE Transactions on Power Electronics

A Single-Stage Three-Mode Reconfigurable Regulating Rectifier for Wireless Power Transfer

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***Abstract*—In this article, we propose a reconfigurable regulating rectifier with a wide operational range for wireless power transfer. The proposed three-mode rectifier achieves a broad range voltage regulation without global loop control to minimize the chip area occupation. Compared with previous work, more working modes and greater voltage gain allow the proposed rectifier to regulate lower input power, which extends the voltage regulation range. A local loop control scheme is proposed for voltage rectification with three modes. It adaptively senses the duty cycle of the mode signal to determine the working mode of the rectifier, and configure the rectifier to the desired mode for voltage regulation. The proposed system was designed and fabricated in a 180-nm BCD technology with an active area of 1.17 mm^2. The measurement results show that the proposed system can rectify wide-range input ac power to a regulated output. The achieved voltage conversion ratiois between 0.95X and 2.68X, with a peak power conversion efficiencyat 87.4%.**

***Index Terms*—Implantable biomedical devices, reconfigurable rectifier, regulating rectifier, wireless power transfer (WPT).**

I. Introduction

WIRELESS power transfer (WPT) has been widely used to charge smartphones, smart watches, biomedical implants, wearable electronic devices, and implantable medical devices (IMDs) [1]. WPT techniques can reduce the size of power units of implanted devices by eliminating bulky batteries [2], [3]. It can also avoid the extra risk to patients caused by the limited battery capacity, which requires regular replacement by operations [4]. A WPT system usually consists of a power transmitter (TX) and a power receiver (RX), as shown in Fig. 1.

Manuscript received 7 December 2022; revised 10 February 2023 and 22 March 2023; accepted 25 March 2023. Date of publication 28 March 2023; date of current version 19 May 2023. Recommended for publication by Associate Editor J. Acero. *(Corresponding author: Sijun Du.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3262728.

Digital Object Identifier 10.1109/TPEL.2023.3262728

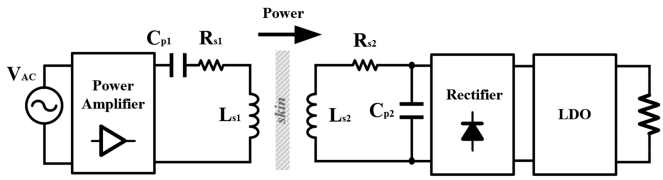

Fig. 1. WPT system for IMDs.

On the TX side, the primary coil driven by a power amplifier can generate magnetic fields and ac power to the secondary coil. The RX rectifies the received ac power followed by a low dropout regulator (LDO) to provide a stable dc voltage for the load [5][6].

In actual applications, the coupling coefficient of the primary and secondary coils is sensitive to their unpredictable direction and distance, which means the received ac power amplitude varies significantly. Thus, to make the IMDs operate in varying conditions, the output voltage of the rectifier should keep stable while the input ac power varies in a large range, which requires a high system voltage gain and high power efficiency.

The system voltage gain, A_{sys}, of a WPT system is the product of the power-link voltage gain, A_{link}, and the voltage conversion ratio (VCR) of the rectifier, M, $(A_{\text{sys}} = A_{\text{link}} \times M)$ [7]. The term A_{link} is the ratio of the voltage collected by the secondary coil to the input voltage supplied by the primary coil, which can be improved by reducing the distance between the primary and secondary coils. The term VCR is the ratio of dc output voltage to the peak value of received ac voltage. High system power efficiency can help reduce the generated heat, which will eventually be absorbed by human tissue [8]. Similar to the system voltage gain, the system power efficiency, η_{sys}, is determined by the power-link efficiency, η_{link}, and the rectifier power-conversion efficiency, η_{rec} $(\eta_{\text{sys}} = \eta_{\text{link}} \times \eta_{\text{rec}})$, where η_{link} is the ratio of power delivered to the secondary coil to the power transmitted by the primary coil, and η_{rec} is the ratio of rectified output dc power to received ac power of the secondary coil. The power-link voltage gain A_{link} and efficiency η_{link} depend on the size of the coil, quality factor, and coupling factor between two coils, which are determined by physical implementations. Hence, improving the VCR and power-conversion efficiency are the key challenges for the receiver circuit design in a WPT system.

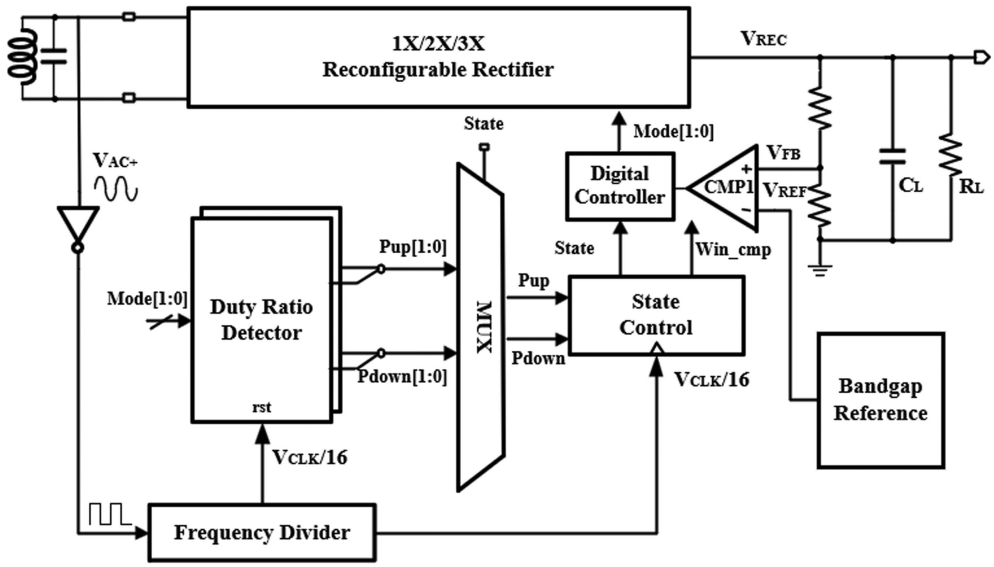

Fig. 2. Architecture of the proposed system.

In previous works, poststage and one-stage WPT systems have been implemented, which can achieve voltage regulation with a reasonable VCR and good power-conversion efficiency. For example, a 13.56-MHz CMOS near field inductive-link power supply for IMDs was proposed [5]. In this work, a voltage doubler is employed to generate a dc voltage fed to an LDO to generate a stable dc output. But the power-conversion efficiency is degraded due to the cascaded stages. For one-stage systems, a resonant regulating rectifier (3R) was proposed in [9] for voltage regulation, which consists of a bridge rectifier and a charge pump. However, three off-chip diodes are used in the circuit, which degrades the power conversion efficiency due to diode voltage drop. Reconfigurable 3R rectifiers with 1X/2X mode were proposed in [10] and [11], alternating ways to offer stable dc output without using an LDO. However, it requires a data communication unit to wirelessly transmit information back to the TX side and utilizes FPGA to code and decode the message. The minimization of system is limited by large data communication units. In [12], a three-mode rectifier was proposed, which includes 0X/\sfrac12X/1X operational modes to achieve voltage rectification. Still, it requires large input amplitude ac power to reach desired voltage level, which leaves a smaller margin for preferable human tissue-specific absorption rate (SAR) [13], [14].

In this article, a three-mode regulating rectifier is proposed, which achieves a wide-range voltage regulation without global loop control to minimize the chip area occupation. Compared with previous works [5], [9], [10], [11], [12], more working modes and greater voltage gain allow the proposed rectifier to regulate lower input power, which extends the voltage regulation range with high power conversion efficiency.

The rest of this article is organized as follows. In Section II, the architecture of the proposed three-mode rectifier and the operating principles are presented. The impedance analysis of the reconfigurable rectifier, the system voltage gain, and energy efficiency in different loading conditions will also be discussed. Circuit implementations are given in Section III and Measurement results are shown in Section IV. Finally, Section V concludes this article.

II. Proposed WPT Receiver System

A. Architecture of the Proposed System

The architecture of the proposed wide input-range rectification system is shown in Fig. 2, which consists of a three-mode reconfigurable rectifier, one comparator, CMP1, two duty ratio detectors, two 2-to-1 multiplexers, a state control unit, and a digital controller. This work applies parallel-resonant connection to the RX coil due to its low current handling requirement [15]. The received signal can be modeled as an ac voltage source. To extend the operation range, the proposed rectifier is configured amongst three working modes 1X, 2X, and 3X. However, to minimize the ripple voltage, it should only switch between two adjacent working modes in the steady state, depending on the comparison result of CMP1. To determine the desired working mode, two duty ratio detectors are also used. In this work, a 2-bit signal, {Mode_1, Mode_0}, is used to represent three working modes. When Mode_1 is "0" and Mode_0 is "0," the rectifier will work in the 1X mode. When Mode_1 is "0" and Mode_0 is "1," it is switched to the 2X mode. When Mode_1 is "1" and Mode_0 is "1," the rectifier will enter the 3X mode. Thus, we get two mode-switching states: switching between 1X and 2X modes, and switching between 2X and 3X modes. These two mode-switching states are represented by the State signal in Fig. 2. As given in Table I, when the rectifier switches between 1X and 2X modes, the State signal is "0." When the rectifier switches between 2X and 3X modes, the State signal is "1."

The mode-switching state that the rectifier works with is determined by the duty ratios Mode_1 and Mode_0. When the duty ratio of Mode_1 or Mode_0 reaches very close to 0% or 100%, it means that the current mode-switching state cannot regulate the output voltage to the desired level; the State signal will then be changed to adjust the gain of the rectifier. For example, as shown in Fig. 3, when the State signal is "0," the rectifier switches

TABLE I
MODE SIGNAL VERSUS STATE AND CMP1

$MODE\_1,0$ / CMP1 / State	1	0
0	0, 0	0, 1
1	0, 1	1, 1

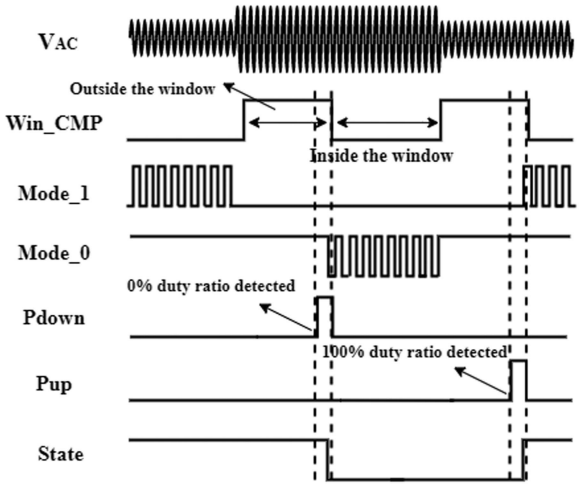

Fig. 3. Waveform of the proposed rectifier.

between 1X and 2X modes by switching the signal Mode_0 between "0" and "1." If the duty cycle of Mode_0 keeps close to 100% for a number of periods (16 periods in this design) of the input ac signal, it means the 2X mode cannot regulate the dc output, $V_{\rm REC}$, to reach the required voltage level due to the low input ac energy. Thus, the signal Pup goes high, and the signal State will switch to "1." The rectifier will then switch between 2X and 3X modes to get a larger output voltage. To achieve this dynamic reconfiguration, we only need to monitor the duty ratio of the signal Mode_0. The 2-to-1 multiplexers are used to make sure that only Pup_0 and Pdown_0 from the Mode_0 duty ratio detector are used for the state control unit.

Alternatively, when the State signal is "1," and the Mode_0 signal continues to be "0" for more than 16 periods of the input ac signal, it means the input ac voltage is too high to maintain the desired voltage level. Then, the signals Pdown goes high and State goes low. As a result, the mode-switching state is changed from 2X/3X to 1X/2X, as shown in Fig. 3.

To control the State signal, a window comparator is also required. To monitor the output voltage, a feedback signal $V_{\rm FB}$ is generated by a resistive divider and compared with two reference voltage levels, $V_{\rm REF\_TOP}$ and $V_{\rm REF\_LOW}$, to form a window in-between. When $V_{\rm FB}$ is within the window, Win_CMP is "0." On the other hand, if it is outside the window, Win_CMP is "1." Only when the output voltage level is out of the window, Pdown and Pup from the 2-to-1 multiplexer will be sent to the state control unit. As long as the output is maintained in the desired voltage range, the State signal would not change regardless of the duty ratios of Mode_0 and Mode_1.

TABLE II
DRIVING SIGNALS FOR POWER SWITCHES

$Mode\_1$	$Mode\_0$	S_1	S_2	S_3	S_4	S_5	S_6	S_7
0	0	ON	ON	OFF	OFF	OFF	ON	OFF
0	1	OFF	OFF	ON	ON	ON	ON	OFF
1	1	OFF	OFF	ON	ON	ON	OFF	ON

B. Three-Mode Rectifier Structure

Fig. 4(a) shows the proposed three-mode reconfigurable rectifier. There are eight power switches ($M_{n1\sim2}$, $M_{p1\sim3}$, and $S_{5\sim7}$), four comparators (CMP$_{2\sim5}$), and three capacitors in this design. In the initial relaxed state, capacitors C_1 and C_2 are slowly charged and $V_{\rm REC}$ starts increasing. The start signal St will be switched to "1" when $V_{\rm REC}$ reaches a certain level, indicating the circuit has started from the cold state. Then, the rectifier will work in the normal operation modes. Depending on the feedback mode signals, Mode_1 and Mode_0, the rectifier is configured into one of the 1X, 2X, and 3X modes by turning ON or OFF specific power switches. The ON/OFF states of all the seven power switches are given in Table II. The operation of each mode is explained as follows.

Fig. 4(b) shows the equivalent structure of the proposed 1X/2X/3X rectifier working in different modes. The detailed configurations for the three operation modes are given in the following.

When Mode_1 and Mode_0 are both "0," the rectifier works in the 1X mode [see Fig. 4(c)]. The switches S_1, S_2, and S_6 are turned ON, and the PMOS power switches M_{P1} and M_{P2} are cross connected. In this state, the two comparators, CMP2 and CMP3, are also enabled to form a full-wave bridge rectifier.

When Mode_1 is "0" and Mode_0 is "1," the 2X mode is activated, as shown in Fig. 4(d). S_1 and S_2 are turned OFF; S_3, S_4, S_5, and S_6 are turned ON. CMP3 and CMP4 are enabled. M_{P1} and M_{N1} become active diodes controlled by comparators. $V_{\rm ac-}$ is clamped at $V_{\rm OUT}/2$ due to the capacitive divider. The full-wave voltage doubler is formed, which is composed of two series-connected half-wave rectifiers.

Fig. 4(e) shows the 3X mode when Mode_1 is "1" and Mode_0 is "1." In this mode, S_3, S_4, S_5, and S_7 are turned ON, S_6 is turned OFF, and an extra capacitor, C_3, is connected to the rectifier. The transistor M_{P3} becomes an active diode, which is controlled by CMP5. The rectifier becomes a voltage tripler, which combines a voltage doubler and a half-wave rectifier.

In the 1X mode, the input resistance of the rectifier is approximately $R_L/2$. In the 2X mode, the rectifier forms a voltage doubler and the equivalent input resistance is $R_L/8$. In the 3X mode, the rectifier is configured as a voltage doubler and a half-wave rectifier. Assuming all fly capacitors, C_1, C_2, and C_3, have the same value, and the output capacitor of the proposed system is significantly larger than flying capacitors; the output power of the rectifier in the 3X mode can be expressed as follows:

$$P_{\rm out} = \frac{V_{\rm dc}^2}{R_L} = \eta_{\rm rec}\frac{V_{\rm ac}^2}{2R_{\rm in}} = \eta_{\rm rec}P_{\rm in} \tag{1}$$

where $P_{\rm in}$ and $P_{\rm out}$ are the input and output power of the rectifier, respectively, $R_{\rm in}$ and R_L are the input impedance and load

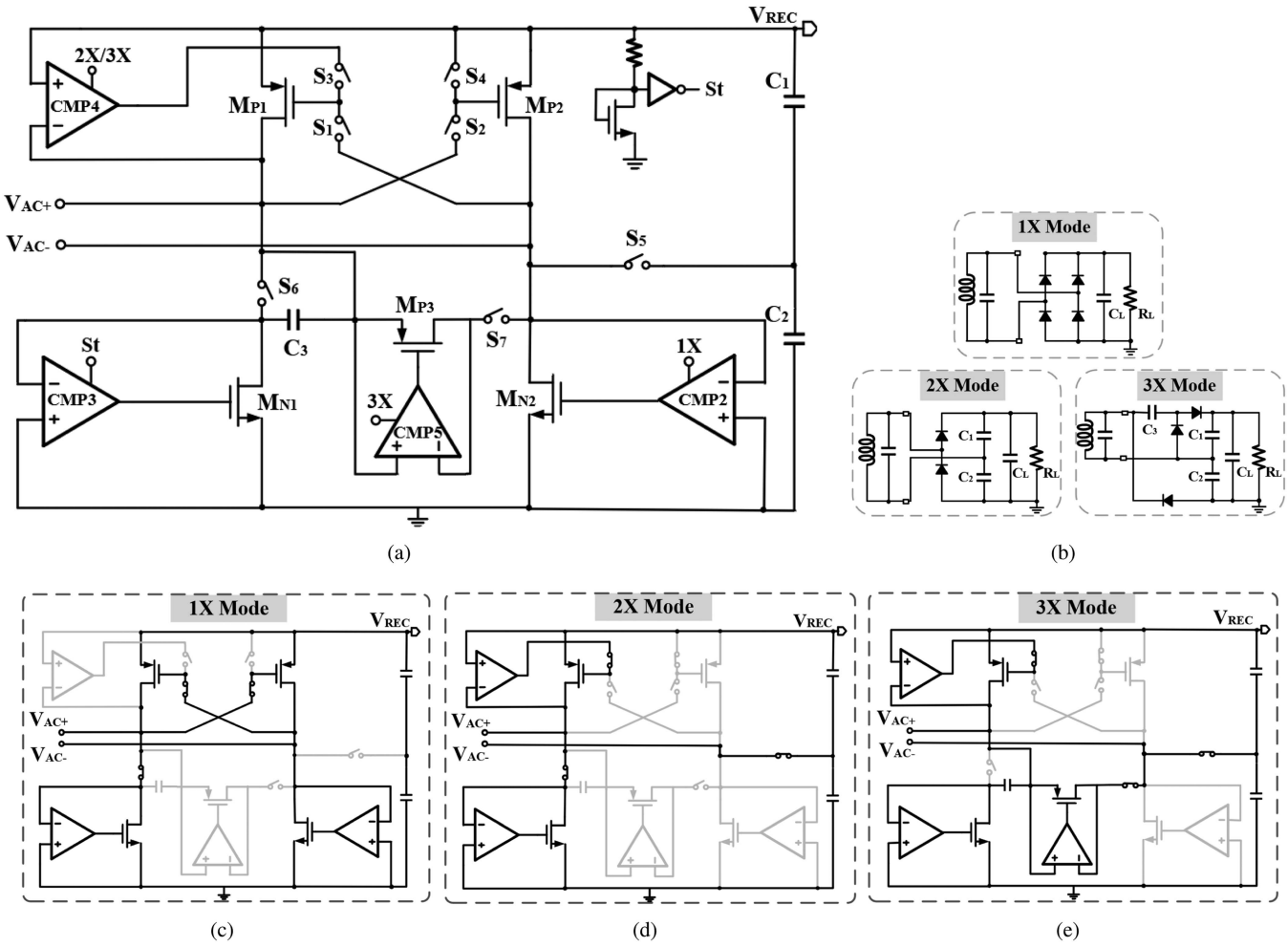

Fig. 4. (a) 1X/2X/3X rectifier. (b) Equivalent models. (c) 1X mode. (d) 2X mode. (e) 3X mode.

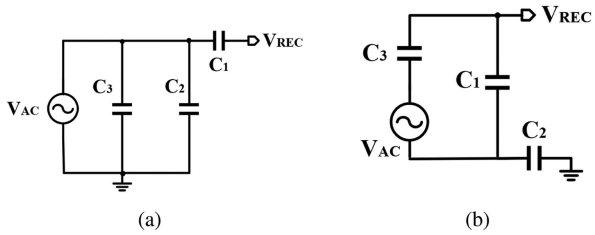

Fig. 5. (a) Negative cycle. (b) Positive cycle.

resistance of the rectifier, respectively, and η_{rec} is the power conversion efficiency. According to [16], η_{rec} can be described as follows:

$$\eta_{\text{rec}} = \frac{E_0}{E_{\text{in}}} \approx \frac{V_{\text{dc}} \cdot Q_0}{V_{\text{ac}} \cdot Q_{\text{in}}} \tag{2}$$

where E_{in} is the input energy of the rectifier, E_{out} is the output energy of the rectifier, and Q_{in} and Q_{out} are the input and output charges of the rectifier in one cycle, respectively. The equivalent circuit diagram of negative and positive cycles for the 3X mode rectifier is shown in Fig. 5. Capacitors C_3 and C_2 are charged to the peak value of the input voltage V_{ac} in a parallel connection in the negative cycle of the input. During the positive cycle of the input, the top plate of capacitor C_1 sees a total of two times the peak value of the input voltage V_{ac} due to voltage clamper C_3. Then, we get three times the peak value of input voltage V_{ac} at the output. In this work, the capacitor C_3 is connected in parallel with the C_1 and in series with C_2. All the fly capacitors, C_1, C_2, and C_3, have the same capacitance. In the negative half cycle, all output charge comes from the capacitor C_1. Thus, the charge Q_1 from C_1 is $Q_{\text{out}}/2$. The input charge in the negative cycle, Q_{in1}, is $Q_3 + Q_2 + Q_1$. In the positive half cycle, the charge from C_3 flows to C_1 and the output, the charge from C_2 is the difference between Q_1 and Q_3. The input charge in the positive cycle, Q_{in2}, is Q_3. The terms Q_1, Q_2, and Q_3 can be written as follows:

$$Q_1 = \frac{Q_{\text{out}}}{2} \tag{3}$$

$$Q_3 = Q_1 + \frac{Q_{\text{out}}}{2} \tag{4}$$

$$Q_2 = Q_3 - Q_1. \tag{5}$$

Combining (3), (4), and (5), we have

$$Q_{\text{in}} = Q_{\text{in1}} + Q_{\text{in2}} = Q_3 + Q_1 + Q_2 + Q_3 = 3Q_{\text{out}}. \tag{6}$$

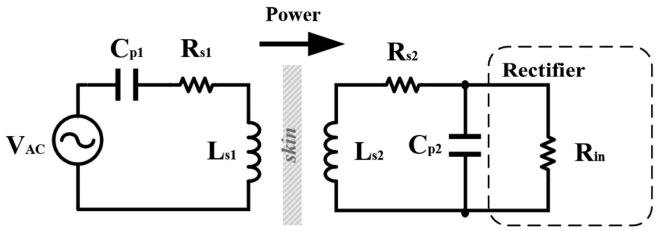

Fig. 6. Induction model of the proposed system.

The VCR is defined as follows:

$$M = \frac{V_{\text{REC}}}{V_{\text{ac}}}. \tag{7}$$

According to the (2), the rectifier's power conversion efficiency can be

$$\eta_{\text{rec}3X} = \frac{M_{3X}}{3}. \tag{8}$$

Combining the (1), (7), and (8), the input resistance in the 3X mode is given as follows:

$$R_{\text{in}3X} = \frac{R_L}{6M_{3X}}. \tag{9}$$

The input impedance of the rectifier can hugely affect the quality factor of the secondary *LC* tank loaded by the rectifier, which has an impact on the system power efficiency η_{sys} and system voltage gain A_{sys}. The coupled voltage may vary in different working modes. The details will be discussed in the following section.

C. Analysis of Proposed Rectifier

In a WPT system for biomedical implants, the system power efficiency η_{sys} is very important. High system power efficiency can reduce the generated heat absorbed by human tissue (SAR). Besides, the system power gain, A_{sys}, is also important since it will affect the input voltage of the rectifier. In this section, the system power efficiency η_{sys} and the system power gain A_{sys} under different working modes and load conditions will be analyzed.

In IMD applications, the weak coupling between the primary and secondary coils is common due to skin and bones. Thus, the primary (TX) coil prefers series matching to generate a larger magnetic field, and the secondary (RX) coil prefers parallel matching to lower the current handling capability requirement. The induction model of the proposed system is shown in Fig. 6. As shown in the figure, the primary coil has inductance L_{s1} and small series resistance R_{s1}. Wireless power driven by the primary coil is coupled to the secondary coil with an inductance of L_{s2} and a small series resistance of R_{s2}. Parallel-connected resonant capacitor C_{p2} is applied to match with the input impedance of rectifier R_{in}.

We assume the equivalent quality factor of the inductors L_{s1} and L_{s2} are Q_1 and Q_2, respectively. According to [7], the power-link efficiency η_{link} is described as follows:

$$\eta_{\text{link}} = \frac{k^2 Q_1 Q_2^2}{\left(1 + \frac{Q_2}{Q_\alpha} + k^2 Q_1 Q_2\right)(Q_\alpha + Q_2)} \tag{10}$$

where k is the coupling factor between the primary and secondary coils. Quality factors of unloaded primary and secondary coils are $Q_1 = \omega_0 L_{s1}/R_{s1}$ and $Q_2 = \omega_0 L_{s2}/R_{s2}$, respectively. The quality factor of the secondary coil loaded by the rectifier is $Q_\alpha = \omega_0 C_{p2} R_{in}$. Hence, the system power efficiency, η_{sys}, under three working modes can be written as follows:

$$\eta_{\text{sys}1X} = \eta_{\text{link}}(Q_{\alpha 1X}) \cdot M_{1X} \tag{11}$$

$$\eta_{\text{sys}2X} = \eta_{\text{link}}(Q_{\alpha 2X}) \cdot \frac{M_{2X}}{2} \tag{12}$$

$$\eta_{\text{sys}3X} = \eta_{\text{link}}(Q_{\alpha 3X}) \cdot \frac{M_{3X}}{3} \tag{13}$$

where $Q_{\alpha 1X} = \omega_0 C_{p2} R_{\text{in}1X}$, $Q_{\alpha 2X} = \omega_0 C_{p2} R_{\text{in}2X}$, and $Q_{\alpha 3X} = \omega_0 C_{p2} R_{\text{in}3X}$. According to [16], if we assume R_{in} is large enough, we have $Q_\alpha \gg 1$. As a result, the power-link gain A_{link} can be approximately written as follows:

$$A_{\text{link}} = \frac{knQ_1Q_2}{k^2Q_1Q_2 + 1 + Q_2/Q_\alpha} \tag{14}$$

where $n = \sqrt{L_2/L_1}$. Combining (7) and (14), the system voltage gain A_{sys} under the three working modes is

$$A_{\text{sys}\_iX} = A_{\text{link}}(Q_{\alpha\_iX}) \cdot M_{iX} \tag{15}$$

where i equals 1, 2, or 3, corresponding to the 1X, 2X, or 3X working mode, respectively. The system voltage gain A_{sys} is not only related to the VCR M, but also to the system link gain, A_{link}. If the received signal amplitude of the 2X mode is significantly smaller than that of the 1X mode despite the twice VCR, the output signal amplitude in the 2X mode is not necessarily higher than that in the 1X mode. The same theory applies to the 3X mode. According to (14), for a reconfigurable rectifier, the change of Q_α has an impact on the system link gain A_{link}. Q_α is mainly affected by the input impedance of the reconfigurable rectifier. Therefore, the load condition can significantly affect the system voltage gain [17]. Under different load conditions, the voltage gain in the 3X mode, A_{sys_3X}, can be smaller than that in the 2X mode, A_{sys_2X}. Thus, to analyze the performance of the 3X mode, we need to determine the voltage-gain break-even value of the load resistance, at which $A_{\text{sys}\_3X} = A_{\text{sys}\_2X}$. Using (15), the break-even value of the load resistance between 2X and 3X modes, R_{Lb}, can be described as follows:

$$R_{Lb} = \frac{2Q_2}{\omega_0 C_{p2}(1 + k^2 Q_1 Q_2)} \cdot \frac{M_{2X} \cdot M_{3X}}{VCR_{3X} - M_{2X}}. \tag{16}$$

According to [16], the voltage-gain break-even value of the load resistance between 1X and 2X modes, R_{La}, can be described as follows:

$$R_{La} = \frac{2Q_2}{\omega_0 C_{p2}(1 + k^2 Q_1 Q_2)} \cdot \frac{M_{1X} \cdot M_{2X}}{M_{2X} - M_{1X}}. \tag{17}$$

When the load resistance is smaller than R_{La}, the 1X system voltage gain is larger than the 2X system voltage gain, even

though the VCR of the 2X mode is larger than that of the 1X mode. Thus, the output voltage of the 1X mode can still be larger than that in the 2X mode. Only when the load resistance is larger than R_{La}, the rectifier can switch from 1X mode to 2X mode to gain a higher output voltage. Similarly, when the load resistance is smaller than R_{Lb}, the 2X system voltage gain is larger than the 3X system voltage gain. Thus, to make sure that the whole system can normally work, the load resistance of the system must be higher than R_{Lb}.

In addition, the system power transfer efficiency can also be influenced by the input impedance of the rectifier. From the (10), (11), (12), and (13), the break-even value of the load resistance in the 2X and 3X modes is

$$R_{Lm} = \frac{2M_{2X}M_{3X}Q_2}{\omega_0 C_2}\sqrt{\frac{10}{(1+k^2Q_1Q_2)(M_{3X}^2 - M_{2X}^2)}}. \tag{18}$$

According to [16], the break-even value of the load resistance in the 1X and 2X modes is

$$R_{Ln} = \frac{2M_{1X}\cdot M_{2X}Q_2}{\omega_0 C_2}\sqrt{\frac{3}{(1+k^2Q_1Q_2)(M_{2X}^2 - M_{1X}^2)}}. \tag{19}$$

To demonstrate how the load condition will influence the system voltage gain, A_{sys}, and system power transfer efficiency, η_{sys}, we set the parameters of the primary coil and secondary coil close to those we will use in the measurements. For the primary coil, $L_1 = 1.4\,\mu$H and $Q_1 = 60$. For the secondary coil, $L_2 = 450$ nH and $Q_2 = 19$. The coupling factor is $k = 0.06$. The ac input frequency is 6.78 MHz. Thus, the system voltage gain, A_{sys}, and system power transfer efficiency, η_{sys}, under different load conditions are illustrated in Fig. 7. It is shown in Fig. 7(a) that when the load resistance is smaller than R_{La} (region 1), the 1X gain is higher than the 2X gain while both 2X and 3X modes cannot normally work. In region 2, the 3X gain is still smaller than the 2X gain. Only when the load is higher than R_{Lb} (region 3), the whole system can work properly.

The system power efficiency η_{sys} for different loading conditions are shown in Fig. 7(b). We can see that the 1X mode can achieve the highest efficiency under a heavy load, with lower R_L (region 4). But with the increase of load resistance, the system power efficiency is gradually decreasing. Under medium load conditions (region 5), 2X mode achieves the highest efficiency. In region 6, when the load resistance is higher than R_{Lm}, 3X mode system efficiency becomes the highest.

With the three modes, the proposed rectifier can be adaptively configured when the input ac amplitude changes due to coupling variation, which is realized with a duty ratio detector and a state control unit. The detailed circuit implementations are presented in the next section.

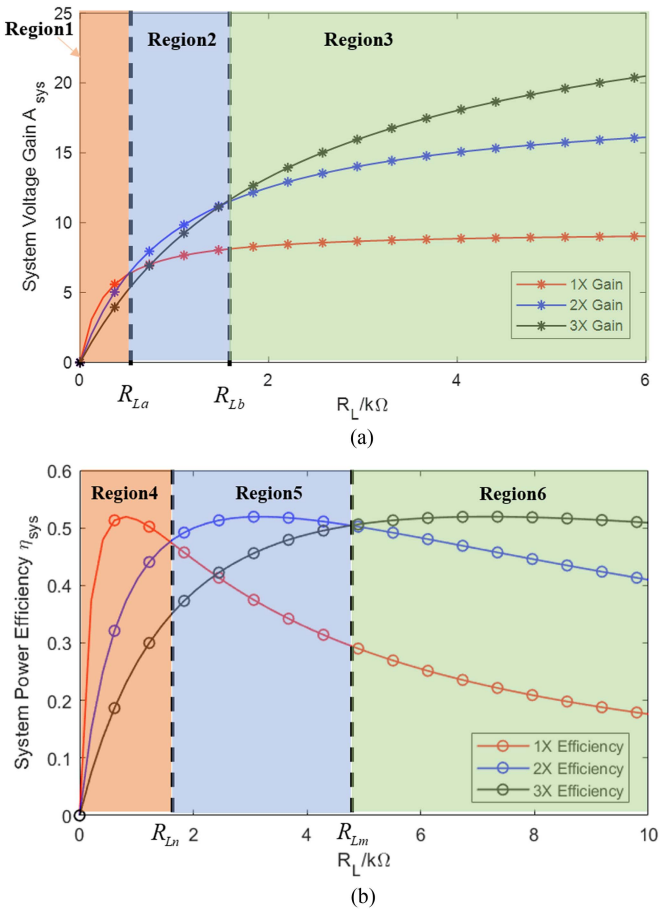

Fig. 7. (a) System voltage gain A_{sys} versus load resistance R_L. (b) System power efficiency η_{sys} versus load resistance R_L.

III. Circuit Implementation

A. Duty Ratio Detector

Since there are three working modes in the proposed reconfigurable rectifier, two switching states are needed for the rectifier, which are 1X/2X and 2X/3X. These three working modes are represented by a 2-bit signal, Mode, when it is 2'b00, 2'b01, or 2'b11. To allow the rectifier to adjust itself when the input amplitude changes, a local loop is required to detect the duty ratio of both bits of the Mode signal and reconfigure the rectifier to the correct working mode. Thus, a fast duty ratio detector is needed in our design. The structure of the duty ratio detector used in our design is shown in Fig. 8. The duty ratio is detected by controlling the charging and discharging of the small capacitors in one cycle [18]. The two upside switches are controlled by the Mode signal; the current provided by a constant current source will flow to only one of the small capacitors, C_{d1} and C_{d2}, at a time. A total of two resistive dividers are placed in parallel with the capacitors to obtain 1% of the voltage across the capacitors. If the duty ratio of Mode signal is 100%, only C_{d1} is charged whereas C_{d2} keeps at 0 V. In this case, 1% of the voltage across C_{d1} is found to be higher than that on C_{d2} in the right-hand side comparator. The comparison result will be shown in the comparator output signal, P_{up}. As a result, the rectifier will change the switching state from 1X/2X to 2X/3X to achieve a higher voltage gain. Similarly, if the duty ratio of Mode signal is 0%, the left-hand side comparator output, P_{down}, becomes "1." As a result, the rectifier moves from the 2X/3X state to the 1X/2X state to achieve lower voltage gain. At the end of each cycle, the charge in the two capacitors, C_{d1} and C_{d2}, will

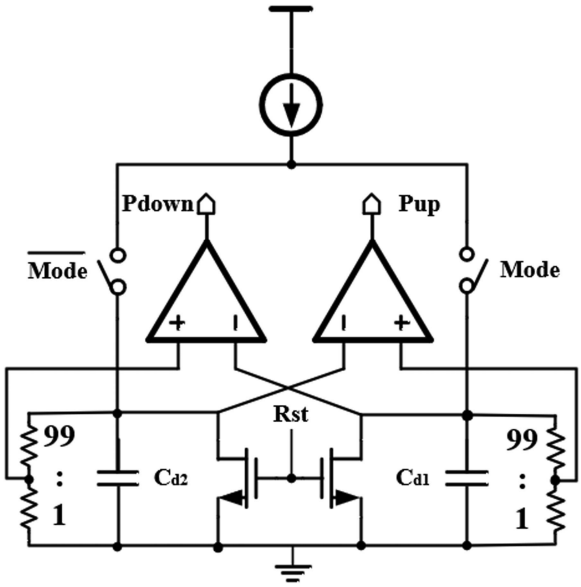

Fig. 8. Duty ratio detector.

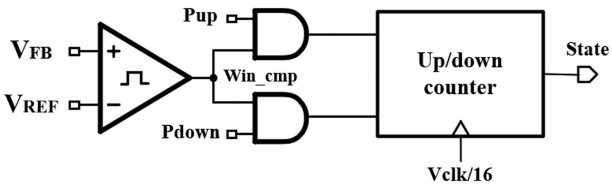

Fig. 9. State control.

be cleared by the Rst signal. The detecting cycle is 16 times the input ac signal period.

B. State Control

The other requirement for the change of mode-switching state is the comparison result of the window comparator. Only when the output voltage is not in the window can the mode-switching state change. The structure of the state control unit is shown in Fig. 9 . When the output voltage is out of the window, Win_cmp will be "1." P_{up} and P_{down} can be fed into up/down counter to change State, which chooses between 1X/2X and 2X/3X states. The sampling period of the up/down counter is synchronized with the duty ratio detector. Only the result of P_{up} and P_{down} at the highest top plate voltage will be sampled to change State.

C. Unbalanced Comparator

To reduce the conduction loss in the power switches, MOSFET switches should be well designed with large sizes. These large switches result in large gate capacitance and large comparator delay driving the active rectifier inaccurately. Besides, the reverse leakage current from the load capacitor may flow back into the rectifier, which degrades the efficiency of the rectifier [19], [20], [21], [22], [23]. By using unbalanced biasing techniques, offsets are added for the comparators CMP2 $\sim$ 4, resulting in higher rectifier efficiency [24]. Fig. 10(a) is the

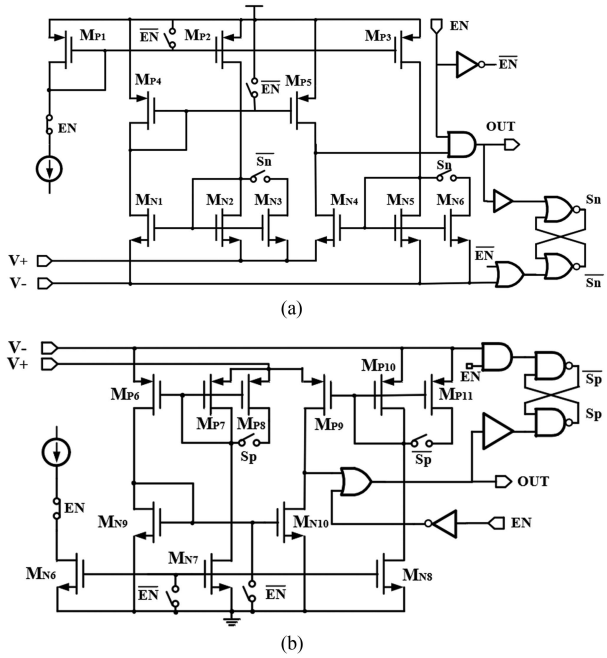

Fig. 10. (a) Schematic of CMP2 and CMP3. (b) Schematic of CMP4.

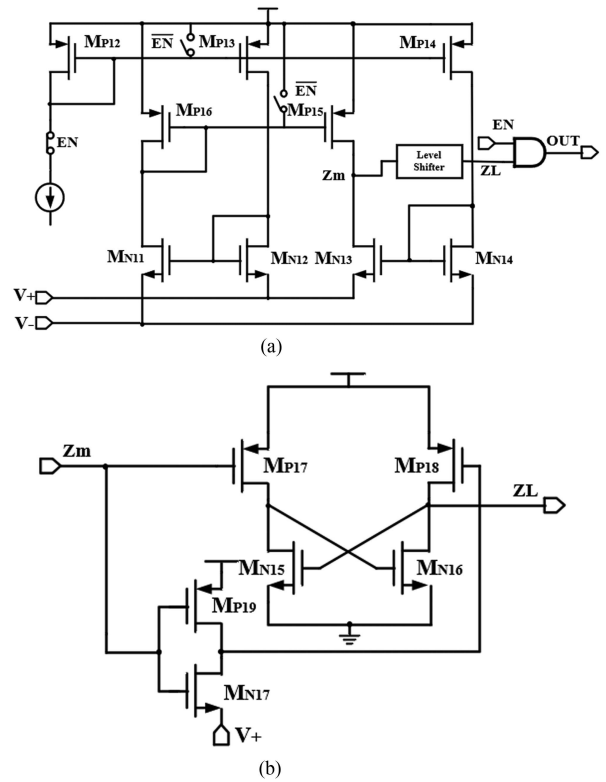

Fig. 11. (a) Schematic of CMP5. (b) Level Shifter.

schematic of the comparators that drive NMOS power switches. Fig. 10(b) is an up–down mirror structure for driving PMOS power switches. The comparator CMP5 is shown in Fig. 11(a). When the rectifier is in the 3X mode, $V-$ equals V_{ac-}, and $V+$ is fluctuating. Thus, the input of CMP5 cannot directly connect to the logic gate. The output of this comparator cannot pull down to

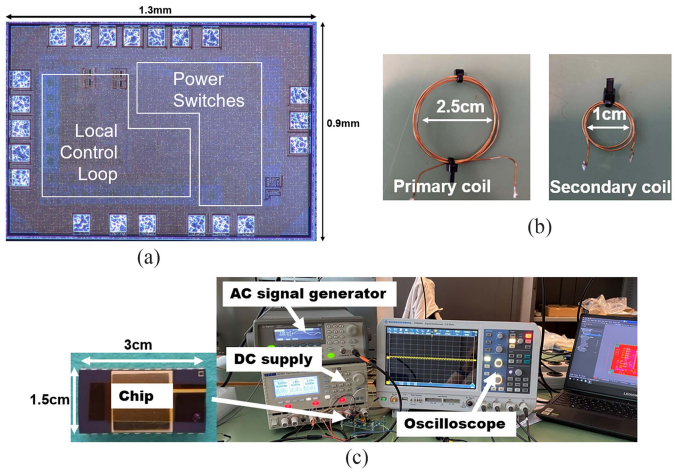

Fig. 12. (a) Chip die photo. (b) Primary coil and secondary coil. (c) Test setup.

TABLE III
PARAMETERS OF COILS

Coils	Diameter	Inductance	Quality factor	Resistance
Primary coil	2.5cm	1.3μH	52	1.06Ω
Secondary coil	1cm	250nH	12	0.87Ω

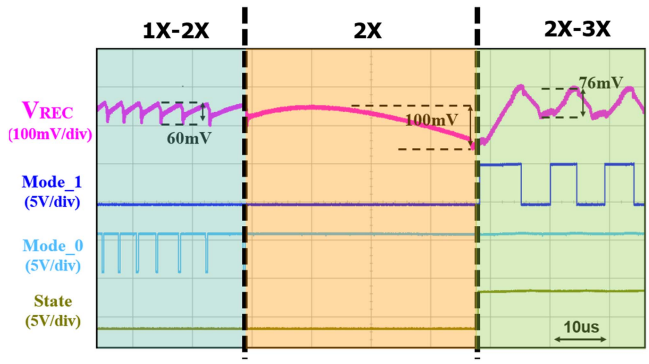

Fig. 13. Measured waveform of the proposed rectifier.

zero. A level shifter is applied to solve this problem [25], which is shown in Fig. 11(b). Since there is no delay compensation technique applied for this comparator. A series of delay cells are used at the output. In this way, M_{P3} can only be open for a fixed period in each cycle, which can reduce the conduction loss.

IV. MEASUREMENTS

The proposed three-mode reconfigurable rectifier was fabricated in a 180-nm BCD process. The die photo is shown in Fig. 12(a), with the active area occupying 1.3 mm $\times$ 0.9 mm. The photos of the primary and secondary coils are shown in Fig. 12(b). Table III summarizes their diameters and quality factors. In this work, a 6.78-MHz carrier frequency is used for powering biomedical implants.

Fig. 12(c) shows the measurement setup with the TX and RX boards. Fig. 13 shows the measured waveform of the proposed

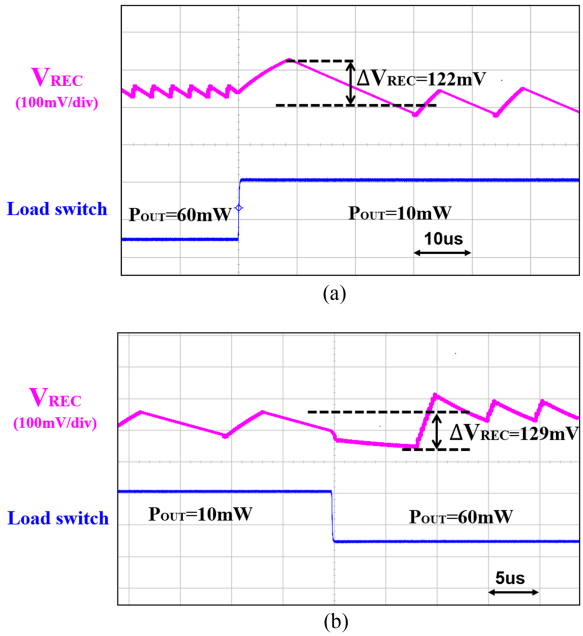

Fig. 14. Load shift transient (a) Heavy load to light load. (b) Light load to heavy load.

three-mode rectifier with local loop control. The rectifier can switch between 1X and 2X modes, or between 2X and 3X modes, depending on the required output voltage and input ac amplitude. The output voltage is regulated at 5 V. At first, when the input voltage amplitude is larger than 2.5 V, the rectifier switches modes between 1X and 2X to maintain a stable output of 5 V. In this case, the measured output voltage ripple is 60 mV. Then, with the decrease of received input ac amplitude, it can be observed that the duty ratio of Mode_0 signal is becoming larger because the rectifier needs to work in the 2X mode for a longer time. When the duty ratio of Mode_0 reaches 100%, the mode-switching state needs to change from 1X–2X mode to 2X–3X mode. To change the state, State will become "1," V_{REC} changes about 100 mV. With the whole system's VCR gradually increasing, the input ac amplitude will become smaller. This is due to the change of load condition because a higher VCR means a smaller input impedance of the rectifier. This explains why 3X starts with a relatively large duty ratio. Then, with the decrease of input signal V_{ac}, the rectifier needs a larger gain to maintain the required output. The duty ratio of Mode_1 continues to be larger. The voltage ripple when the rectifier switches between 2X and 3X is about 76 mV. To further reduce the ripple for powering sensitive biomedical devices, several techniques can be employed, including a narrower hysteresis window, a larger load capacitor, and a higher carrier frequency.

Fig. 14 shows the transient response under load changes. The top signal is the rectified output voltage from the rectifier, and the second signal is the switch signal to choose between the heavy load and light load conditions (low when a heavy load is chosen). When the output power changes from heavy load (60 mW) to light load (10 mW), the output V_{REC} can still be regulated at 5 V. The figure is shown in Fig. 14(a). The overshoot voltage is measured at 122 mV. When the output power changes from

TABLE IV
COMPARISONS WITH THE STATE-OF-THE-ART DESIGNS

	2013 JSSC [9]	2015 JSSC [26]	2017 JSSC [12]	2019 TPE [27]	2021 JSSC [28]	**This work**
Process	0.35 μm	0.35 μm	0.35 μm	0.18 μm	0.25 μm	**0.18 μm**
Resonant frequency	6.78MHz	2MHz	6.78 MHz	0.5 MHz	6.78 MHz	**6.78 MHz**
Rectifier Structure	3R Rectifier	Rectifier +LDO	3-Mode Rectifier	Rectifier+PWM	0X/1X Rectifier	**1X/2X/3X Rectifier**
Chip Area(RX)	5.52 mm^2	14.44 mm^2	4.8 mm^2	0.943 mm^2	2.07 mm^2	**1.17 mm^2**
Off-chip Components	5 diodes, 3 capacitors	3 capacitors	1 capacitors	1 inductor, 1 capacitor	1 capacitors	**4 capacitors**
V_{OUT}	5 V	3 V	5 V	1.5 V$\sim$2 V	5 V	**5 V**
Maximum output power	6 W	1.45 W	6 W	80 mW	400 mW	**110 mW**
Peak receiver efficiency	86%	76%	92.2%	88.2%	92.9%	**87.4%**
Receiver efficiency(@65mW)	30%*	70%*	80%*	88%*	87%*	**87.4%**
VCR	$<$1	N/A	$<$1	0.73$\sim$2	$<$1	**0.95$\sim$2.68**

$*$ Estimated value

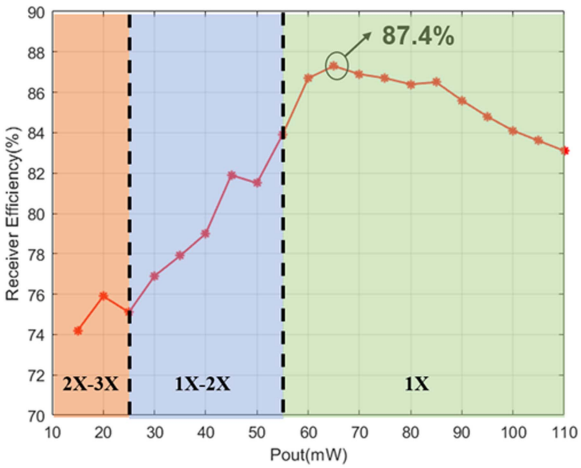

Fig. 15. Measured receiver efficiency.

light load to heavy load, the output V_{REC} can still be regulated at 5 V, and the undershoot voltage is measured at 129 mV, as shown in Fig. 14(b).

The measured rectifier efficiency for different P_{OUT} ranging from 15 to 110 mW is measured and plotted in Fig. 15. The whole system is self-powered with the output voltage. In light-load conditions, the switching loss of the active switches dominates. The total switching loss is about 1.82 mW when the total output power is 15 mW; hence, the switching loss takes 12.2% of the total output power. With the increase of output power in heavy-load conditions, the conduction loss becomes dominant, and the total switching loss is about 2.14 mW, which takes only 4.2% of the total 60 mW output power. The rectifier then works with 1X mode to maintain high efficiency. At $P_{\text{OUT}} = 65$ mW, the receiver reaches its peak efficiency at 87.4%. A total of three test chips were measured under room temperature, and the efficiency variation among the chips is smaller than 1%.

Table IV tabulates the performance comparisons between the proposed rectifier and some selected state-of-the-art designs. The table shows that our design occupies the second smallest chip area while achieving the widest VCR range (up to 2.68$\times$). Although Fan and Mohd Daut [27] showed a comparable VCR range with 0.73–2, it employs a large inductor to achieve output regulation, which enlarges the area occupation. Besides, the receiver efficiency is also an important figure for biomedical WPT systems. Despite the moderate peak receiver efficiency amongst prior works, the proposed design receiver efficiency at low-power biomedical applications achieves satisfactory performance with a wide VCR range.

V. CONCLUSION

A 6.78-MHz three-mode operational reconfigurable rectifier for a WPT system is proposed in this article. The proposed system can be adaptively configured to operate in one of the 1X/2X/3X modes to gain a stable output, which shows the widest VCR range among the state-of-the-art designs. Thus, for low-power biomedical applications, this system can work in a much wider input range to obtain a stable output voltage with a local control loop while maintaining a satisfactory high efficiency at a low-power range. The wider operational range is especially useful in biomedical low-power applications, whereas the wireless power-link conditions vary unpredictably and largely due to weak coupling conditions. The measured VCR range of the proposed rectifier is between 0.95 and 2.67. The measured maximum output power and peak power efficiency are 110 mW and 87.4%, respectively. The output voltage ripple is achieved at 60 mV during normal operations. The overshoot and undershoot voltages during load-varying transients are measured at 122 and 129 mV, respectively.

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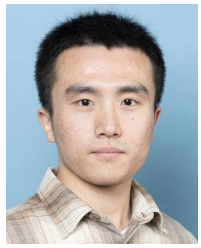

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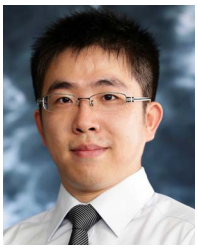

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