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A Pitch-Matched Low-Noise Analog Front-End With Accurate Continuous Time-Gain Compensation for High-Density Ultrasound Transducer Arrays

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***Abstract*— This article presents a compact analog front-end (AFE) circuit for ultrasound receivers with linear-in-dB continuous gain control for time-gain compensation (TGC). The AFE consists of two variable-gain stages, both of which employ a novel complementary current-steering network (CCSN) as the interpolator to realize continuously variable gain. The first stage is a trans-impedance amplifier (TIA) with a hardware-sharing inverter-based input stage to save power and area. The TIA's output couples capacitively to the second stage, which is a class-AB current amplifier (CA). The AFE is integrated into an application-specific integrated circuit (ASIC) in a 180-nm high-voltage BCD technology and assembled with a 100 μm-pitch PZT transducer array of 8 × 8 elements. Both electrical and acoustic measurements show that the AFE achieves a linear-in-dB gain error below ±0.4 dB within a 36-dB gain range, which is >2× better than the prior art. Per channel, the AFE occupies 0.025 mm^2 area, consumes 0.8 mW power, and achieves an input-referred noise density of 1.31 pA/$\sqrt{\text{Hz}}$.**

***Index Terms*— Application-specific integrated circuit (ASIC), pitch-matched analog front-end (AFE), time-gain compensation (TGC), trans-impedance amplifier (TIA), ultrasound imaging, variable gain amplifier (VGA).**

I. Introduction

APPLICATION-SPECIFIC integrated circuits (ASICs) play a key role in the miniaturization of 3-D ultrasound imaging devices. ASICs minimize interconnection wires, reduce power consumption, and improve image quality in various ultrasound systems. For instance, they have been successfully employed in catheter-based ultrasound devices that enable real-time 3-D image-guided interventions through intracardiac echocardiography (ICE) [1], [2] and intravascular ultrasound imaging (IVUS) [3]. ASICs are also required for emerging wearable ultrasound devices, such as the device targeted in this work: a cap-like wearable device with built-in integrated circuits providing high-resolution 3-D ultrasound images through transfontanelle ultrasonography (TFUS) for monitoring brain activity in premature neonates [4], [5]. For real-time 3-D ultrasound imaging, a high-density 2-D transducer array needs to be integrated in a pitch-matched fashion with analog front-end (AFE) circuits that process the echo signals received by the transducer elements [6].

A key challenge in ultrasound AFE design is to handle the large dynamic range (DR) of the echo signals due to propagation attenuation. The amplitude of an ultrasound wave decreases as it propagates through the medium being imaged, i.e., the human body. Not only the transmitted pulse but also the returning echo signals are attenuated [7]. The amplitude A_z of an ultrasound wave can be expressed as

$$A_z = A_0 e^{-\mu_0 z}$$

where A_0 is the initial amplitude at the surface of the ultrasound transducer, μ_0 is the amplitude attenuation factor, and z is the propagation distance of the acoustic wave in the medium. The equation indicates that the ultrasound wave decays exponentially. Besides, it decays faster at higher frequency because μ_0 is proportional to the frequency of the ultrasound wave. In a typical medium, e.g., the human brain, the attenuation factor is about 0.435 dB · cm^{-1} · MHz^{-1} [8], implying that a 10-MHz ultrasound wave is attenuated by 35 dB after traveling a round-trip distance of 8 cm, corresponding to the desired 4-cm imaging depth in the mentioned neonatal brain-monitoring application. This leads to an overall DR of 75 dB if an instantaneous DR of about 40 dB is required at any depth. Taking the wide bandwidth of the ultrasound transducer into account, this poses considerable challenges to the circuit design and would lead to a power-hungry analog to digital

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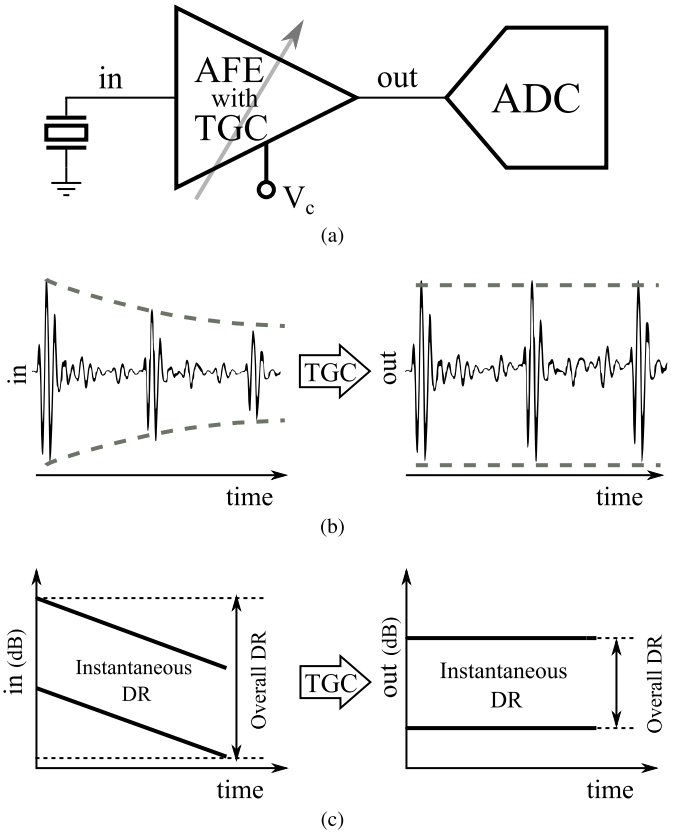


Fig. 1. (a) Block diagram of the AFE with TGC function followed by an ADC. (b) Input and output signals of the AFE with TGC function. (c) Evolution of DR as a function of time with TGC function.

converter (ADC) if the ultrasound signal would be directly digitized.

Time-gain compensation (TGC) is a technique to compensate for the attenuation by adjusting the gain of the AFE as a function of time, as illustrated in Fig. 1(a). Besides providing low-noise amplification, the AFE also provides TGC by providing gain that increases exponentially with time, as depicted in Fig. 1(b). The aforementioned 75-dB DR is thus reduced to about 40 dB after the AFE with TGC function as shown in Fig. 1(c). This is essential to relax the complexity of the back-end circuitry, e.g., the ADC.

Image artifacts may appear when the TGC function does not match the attenuation rate in the medium [8]. E.g., in B-mode imaging, inappropriate compensation gain would result in image-brightness variations in uniform tissue. This implies that a well-designed TGC should have linear-in-dB gain control with a gain error as small as possible throughout the overall gain range. Other types of image artifacts associated with switching transients of the interfacing electronics should also be minimized in the AFE design, such as the gain-switching artifacts [9], and the transmission/reception (TX/RX) switching artifacts [10].

In this article, we present a compact, pitch-matched AFE combined with TGC function that achieves a $>2\times$ better linear-in-dB gain error than prior designs [9], [11], [12], while consuming less power and occupying less area [13]. The

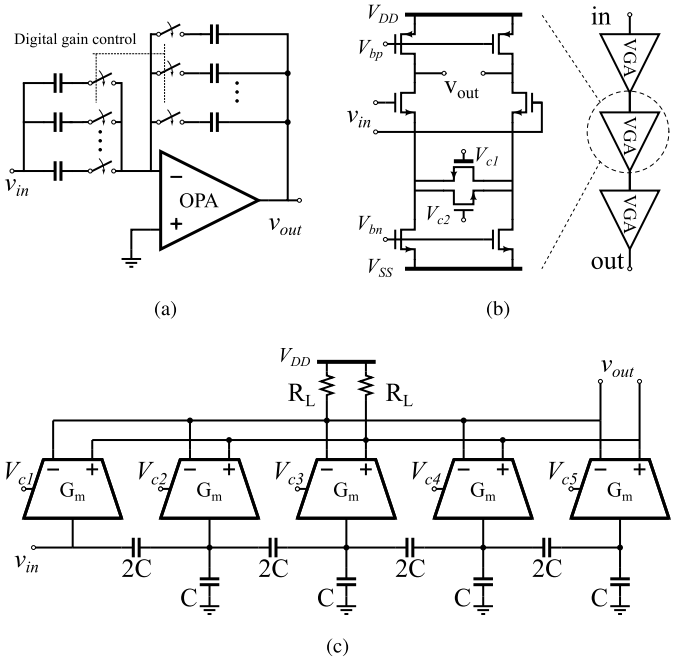


Fig. 2. Circuits to implement TGC. (a) Discrete-time PGA [6]. (b) Analog VGA [14]. (c) Interpolating VGA [15].

AFE is equipped with a novel complementary current-steering network (CCSN) that interpolates between discrete gain steps and employs a hardware sharing topology to reduce the area and power consumption. Thus, the gain of the AFE can be controlled in a linear-in-dB fashion without any abrupt gain changes by a continuously ramping analog control voltage. The AFE biases the transducer to ground level, which prevents voltage changes on the transducer between pulse transmission (TX), where a unipolar high-voltage pulse is imposed on the transducer, and echo reception (RX), thus reducing the possibility of imaging artifacts associated with TX/RX switching [10]. As a proof of concept targeting the mentioned neonatal brain-monitoring application, a 100-μm pitch 10-MHz transducer array consisting of 8×8 elements has been built on top of the pitch-matched AFE to demonstrate its functionality in a miniaturized ultrasound probe.

This article is organized as follows. Section II reviews the prior art and categorizes different TGC architectures according to the way an exponential gain curve is approximated. Section III describes the architecture design of our AFE and presents the theoretical basis of the novel CCSN. Section IV presents the detailed circuit implementation. Section V describes the fabricated prototype, as well as the electrical and acoustic measurement results. This article ends with conclusions.

II. Prior Art

Various amplifier topologies that vary their gain linearly in dB can be used to implement TGC. These amplifiers are widely used in different applications such as mobile TV [15], wireless communication systems [14], and ultrasound imaging systems [9]. These designs can be further divided into three

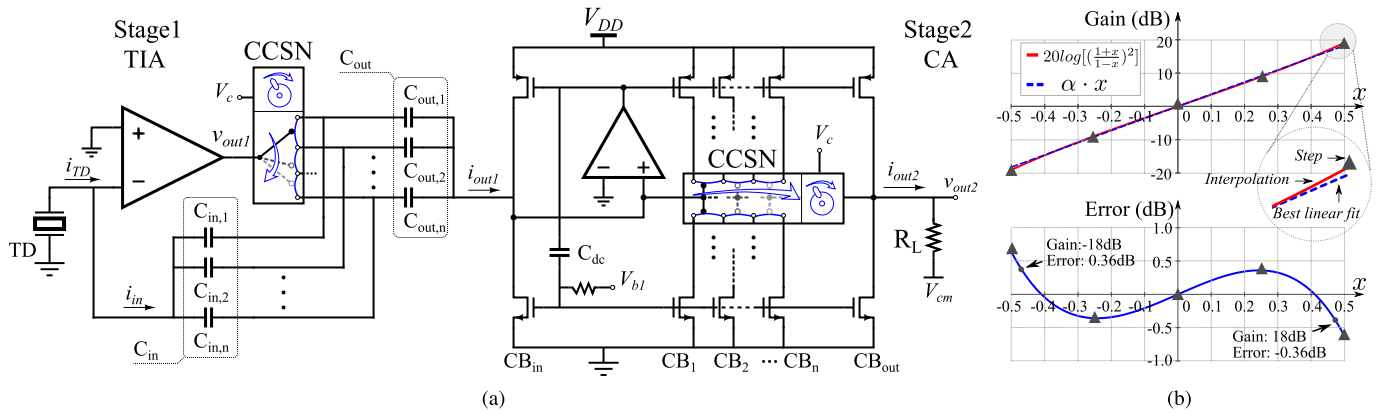


Fig. 3. (a) Two-stage AFE with CCSNs. (b) Realized pseudo-exponential interpolation with error relative to a linear-in-dB gain curve.

categories, i.e., discrete-time programmable gain amplifiers (PGAs) [6], [16], analog variable-gain amplifiers (VGAs) [11], [14], [17], and interpolating VGAs [9], [15], [18], [19].

A discrete-time PGA utilizes a passive or active feedback network to generate discrete gain steps controlled by a digital signal, as illustrated in Fig. 2(a). In modern integrated circuits, these gain steps are generally defined by matched devices, and can thus be precisely distributed on an exponential trajectory. However, for an ultrasound imaging system, the switching transients between adjacent steps would lead to imaging artifacts if these steps are spaced far apart. Finer gain steps mitigate such artifacts but likely require a large chip area [20], and therefore are hard to realize in a pitch-matched AFE design with small pitch size.

A continuous TGC function can be implemented with an analog VGA, and various techniques can be used to approximate the exponential gain curve, e.g., using multiple open-loop stages as depicted in Fig. 2(b) [14]. In each stage, a first-order pseudo-exponential function is generally implemented, e.g., $(1 + x/1 - x)$ [17], [21], which results in a gain error of less than 0.5 dB within a overall gain range of 15 dB. A wider gain range can be obtained by cascading gain stages, resulting in a $(1 + x/1 - x)^n$ curve, at the cost of lower signal-chain bandwidth. However, these open-loop structures are usually vulnerable to temperature and process variation.

An interpolating VGA makes a good tradeoff between the aforementioned solutions. As illustrated in Fig. 2(c), it establishes a few exponentially spaced gain steps and employs analog interpolation to smoothen out the gain curve between adjacent gain steps. This solution is less sensitive to temperature and process variation, as the gain steps are accurately defined by a matched network, e.g., a C-$2C$ capacitor ladder [9], [15]. It also has no abrupt gain transition between two steps, hence mitigates the artifact issue to some extent. Nevertheless, the interpolation process still deviates from the ideal exponential trajectory and the interpolation error even dominates the overall linear-in-dB gain error [9].

As will be explained in Section III, we introduce a novel CCSN that interpolates the gain steps along a second-order

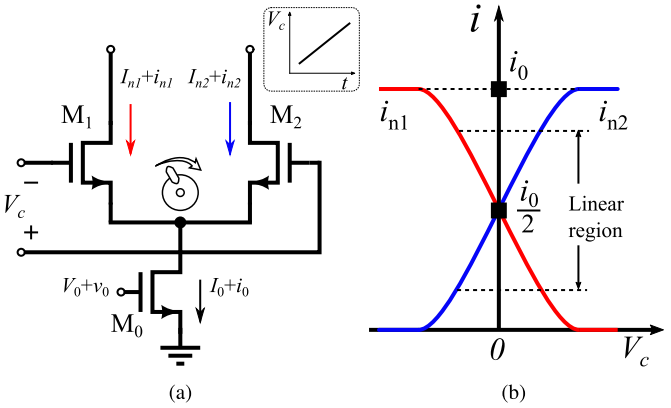


Fig. 4. (a) NMOS current-steering pair with inset showing the control voltage as a function of time. (b) AC currents of NMOS pair as a function of control voltage V_c.

pseudo-exponential trajectory resulting in very small gain error in the overall gain range. In combination with the scalable feedback network and hardware-sharing technique among different channels, we build a compact and accurate linear-in-dB TGC AFE circuit.

III. Architecture Design

A. Two-Stage Interpolating VGA

As aforementioned, precise linear-in-dB gain can be obtained by a multistage VGA realizing a higher-order pseudo-exponential function. In this work, we propose a two-stage interpolating VGA as depicted in Fig. 3(a). The first stage consists of a trans-impedance amplifier (TIA) with a feedback capacitor array C_{in}, followed by a capacitor array C_{out} that couples to the virtual ground of the second stage and thus turns the TIA's output voltage v_{out1} into a current signal i_{out1}. The large loop gain of the TIA and the low input impedance of the second stage guarantee i_{out1} to be a precisely scaled version of the transducer signal current i_{TD}, and the ratio of i_{out1} to i_{TD} is defined by the two capacitor arrays, C_{in} and C_{out}, and the CCSN, as will be elaborated below.

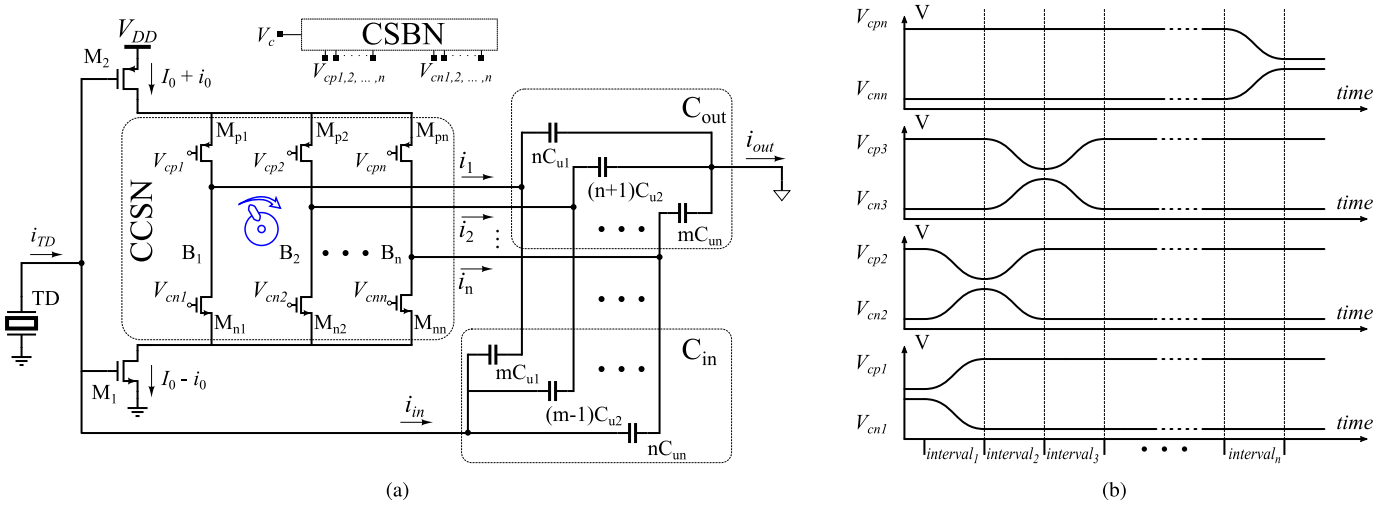


Fig. 5. (a) Simplified circuit diagram of the TIA with CCSN. (b) Bias voltages of the CCSN as a function of time.

The second stage is a class-AB current-mirror-based current amplifier (CA), in which the discrete gain steps are precisely defined by a series of current branches CB_{in},CB_1,…,CB_n,CB_{out}. The ratio of the CA's output current i_{out2} to i_{out1} is defined by the ratio of the number of branches connected to its input and the number connected to the output. The output current signal i_{out2} is then converted to a voltage via a load resistor R_L.

The n gain steps of both stages follow a $(1 + x/1 - x)$ trajectory resulting in a $(1 + x/1 - x)^2$ function that is an accurate approximation of the required exponential gain-curve with a theoretical gain error below ±0.36 dB in an overall 36-dB range. The CCSNs interpolate between these discrete gain steps by steering the signal current between the adjacent steps such that the interpolation also follows a $(1 + x/1 - x)$ trajectory. Thus, as illustrated in Fig. 3(b), the overall gain trajectory always follows a $(1 + x/1 - x)^2$ function, and therefore it significantly reduces the linear-in-dB gain error.

B. Analysis of Current-Steering Pair

As depicted in Fig. 4(a), an NMOS current-steering pair consisting of NMOS transistors M_1 and M_2 steers the current signal flowing through M_0 from one output to another in accordance with the applied control voltage V_c. The ac current i_0 and the dc current I_0 are both continuously directed from M_1 to M_2 controlled by a linear ramp-up signal V_c. The total currents flowing through M_1 and M_2 can be expressed in two parts, the large-signal currents $I_{n1,2}$ [22] and the small-signal currents $i_{n1,2}$ [15]

$$I_{n1,2} \approx \frac{1}{2} I_0 \mp \frac{1}{2}\sqrt{\beta I_0 - \frac{1}{4}(\beta V_c)^2} \cdot V_c \tag{1}$$

$$i_{n1,2} \approx \left(\frac{1}{2} \mp \frac{\sqrt{\beta} V_c}{4\sqrt{I_0 - \frac{1}{4}\beta V_c^2}}\right) \cdot i_0 \tag{2}$$

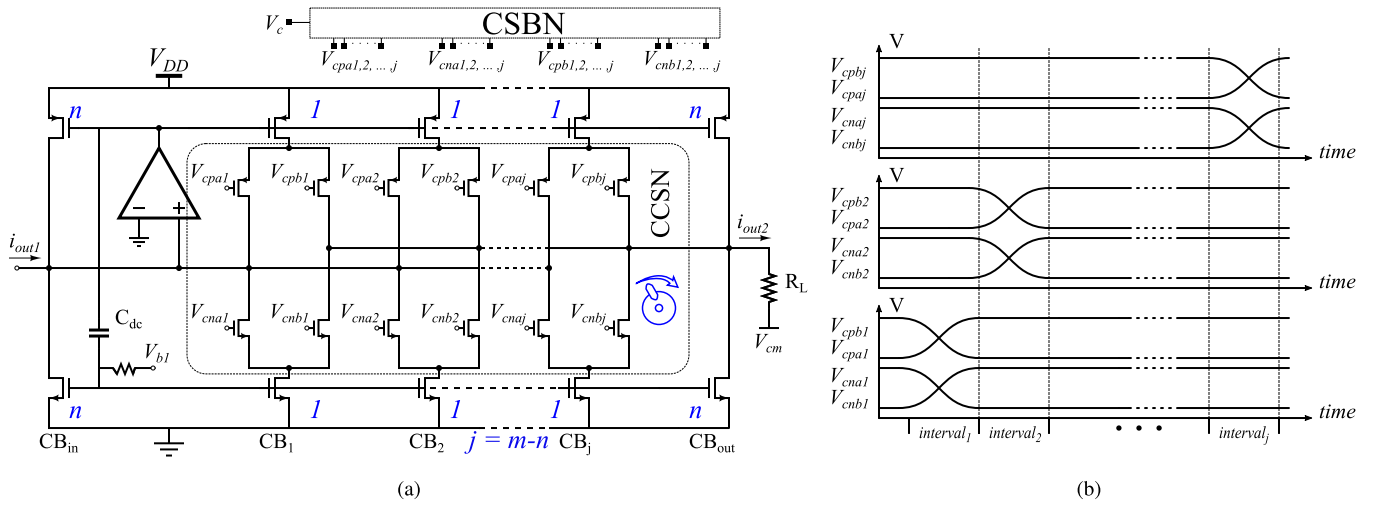
where i_0, I_0 are the ac current and dc current flowing through M_0, $\beta = \mu_0 C_{ox}(W/L)_{1,2}$ and $(W/L)_{1,2}$ is the aspect ratios of M_1 and M_2. The currents i_{n1} and i_{n2} are approximately linear functions of i_0 and the control voltage V_c if the absolute value of V_c is small, while $I_{n1,2}$ are nonlinear components that should be canceled in the circuit.

C. TIA With CCSN

A simplified circuit diagram of the TIA with CCSN is shown in Fig. 5(a). A current-steering bias network (CSBN) converts the TGC control voltage V_c into a series of gate-control voltages for the CCSN, which are V_{cn1},V_{cn2},…,V_{cnn} and V_{cp1},V_{cp2},…,V_{cpn}, as depicted in Fig. 5(b). The TIA employs an inverter-based amplifier formed by M_1 and M_2 with dc bias current I_0 and ac signal current i_0. The CCSN consists of n branches B_1–B_n, formed by PMOS steering array M_{p1}–M_{pn} and NMOS steering array M_{n1}–M_{nn}, and steers the ac signal currents $\pm i_0$ to the virtual ground of TIA and the virtual ground of the next stage via the feedback capacitor array (C_{in}) and the feed-forward capacitor array (C_{out}), respectively.

At the beginning of receive interval [see Fig. 5(b)], the ac currents $\pm i_0$ are steered into the first capacitive divider of the capacitor arrays C_{in} and C_{out} via the only active steering branch B_1, corresponding to the lowest gain from i_{TD} to i_{out}. Throughout the receive interval, the CCSN steers the currents from branch to branch, interpolating between the exponentially spaced capacitive divider ratios, thus gradually increasing the gain. At the end of the receive interval, all currents go to the final branch B_n, corresponding to the highest gain. As derived in the Appendix, this interpolation process follows a pseudo-exponential trajectory, leading to an accurate linear-in-dB gain sweep.

Note that this operation is different from the current-steering reported in [9], where a noncomplementary current-steering network interpolates between the exponentially spaced gain steps of a capacitive ladder network. This interpolation is nonexponential, resulting in larger errors compared to a linear-in-dB sweep. Moreover, in contrast with the capacitor values in a C-$2C$ ladder network, the unit capacitors C_{u1}–C_{un} in our capacitive dividers can be sized independently. The unit



(a) (b)

Fig. 6. (a) CA with CCSN. (b) Bias voltages of CCSN as a function of time.

capacitors associated with the low-gain steps need to be sized large enough to avoid saturating the amplifier, while those associated with the high-gain steps, at which the signal-current amplitude is smaller due to the exponentially decaying nature of the input signal, can be scaled down to save area.

D. CA With CCSN

A similar CCSN is used in the second stage of the AFE, which is a class-AB CA with a local feedback loop [23], as illustrated in Fig. 6(a). Instead of using capacitor arrays, as in the first stage, the CA employs current-mirrors to define the gain steps, which consist of an input current branch (CB_{in}), an output current branch (CB_{out}) and j unit current branches (CB_1–CB_j), where $j = m\text{-}n$. The input and output branches both comprise n unit branches. At the beginning of the RX phase, all unit current branches attach to the input branch via the CCSN, resulting in a current gain of (n/m). The CCSN adjusts the current mirror ratio across all the intermediate gain steps $(n+1/m-1), (n+2/m-2), \ldots, (m-1/n+1)$ throughout the RX phase until all unit branches attach to the output branches resulting in a final gain of (m/n). A similar analysis as presented in the Appendix can be applied to the interpolation of all the gain steps of the CA. The resulting current-gain trajectory is still exponential if the gate bias voltages are properly applied as illustrated in Fig. 6(b). The local negative feedback loop formed by the amplifier, dc level-shifter capacitor (C_{dc}), and input branch (CB_{in}) effectively reduces the input impedance of the CA and operates the current mirror in a class-AB mode.

IV. Circuit Design

A. Hardware Sharing TIA

A variety of amplifier topologies have been used in different ultrasound applications, e.g., the conventional two-stage amplifier [24], the single-ended inverter-based amplifier [6] and the differential current-reuse amplifier [3], [9]. A figure-of-merit called the noise efficiency factor (NEF) has been introduced in [25] to compare power/noise efficiency among different types of amplifiers. The conventional two-stage amplifier and differential current-reuse amplifier have relatively poor theoretical NEFs of 2 and 1.4, respectively, while NEF of the single-ended inverter-based amplifier are close to 0.7 [26], which makes it an attractive candidate. Nevertheless, the single-ended inverter-based amplifier suffers from supply/ground interference since it acts as a common-gate amplifier to these interferences. Voltage regulators have been introduced to suppress these interferences at the cost of additional power consumption [6], but this reduces the power efficiency.

By noticing that the ultrasound system has multiple input channels, we can reduce area and power consumption by sharing hardware among the channels, e.g., the ground/supply regulators [6]. We propose a hardware-sharing TIA as the AFE's first stage which is illustrated in Fig. 7(a). The power supply and ground voltage regulators ($Reg_{n,p}$) are shared among four TIA channels. The mesh [27] and its biasing circuit control the bias current of the voltage regulators and the inverter-based amplifiers: a bandwidth-control circuit dynamically adjusts the bandwidth of the TIA via the mesh devices in accordance with the exponentially growing gain, as will be discussed in Section IV-B. The local feedback loops of the two voltage regulators effectively decouple the four channels and also attenuate interferences from the power supply and ground.

Four high-efficiency inverter-based amplifiers process the ultrasound signals from four transducers. The amplifier of the first channel is formed by M_1, M_2, and C_1, C_2. dc level-shifting capacitors C_1 and C_2 serve two purposes. They allow M_1 and M_2 to be biased at optimal gate voltages V_{R1} and V_{R2}, independent of the input bias level, thus maximizing the output swing of the inverter-based amplifier [6]. Moreover, they allow the amplifier's input to be biased at a well-defined ground level during the receiving phase. The latter plays a crucial role in preventing image artifacts when switching from transmit to receive. The ratio of five capacitive dividers are $(3/11), (5/9), \ldots, (11/3)$, respectively, corresponding to the gain steps described by (6) with parameters $m = 11$ and $n = 3$. Proper scaling of the unit capacitor was applied to

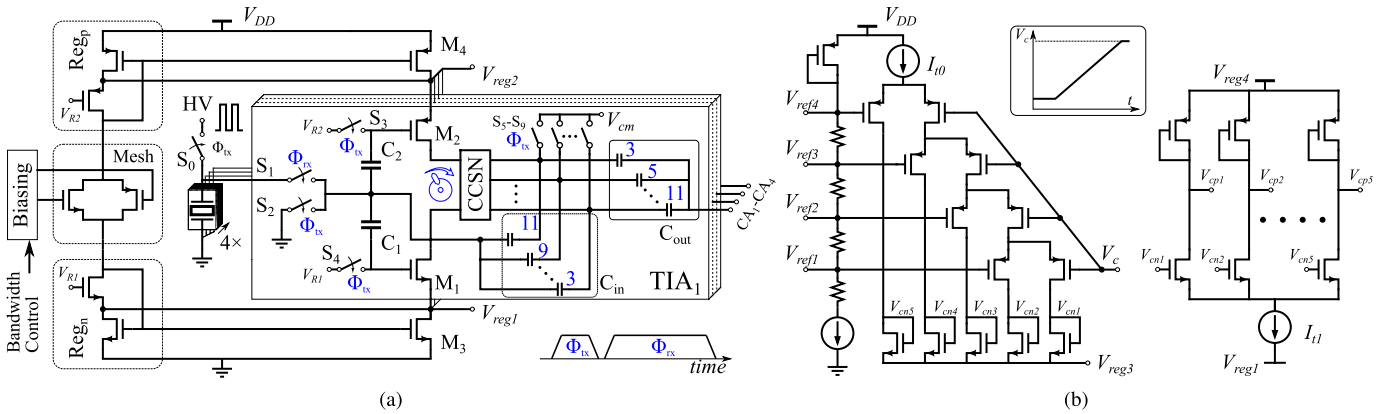


Fig. 7. (a) Circuit diagram of the hardware-sharing TIA with CCSN. (b) CSBN of the TIA.

those dividers leading to a 30% less area compared to a design with identical unit capacitors in the dividers. A five-tap CCSN interpolates between these gain steps resulting in a total gain range of 22.6 dB. During the TX phase (Φ_{tx}), high-voltage switch S_0 is closed and high-voltage switch S_1 is open, and a unipolar high-voltage pulse (0–36 V) is applied to the transducer to transmit an acoustic pulse. In the meanwhile, the level-shifting capacitors C_1 and C_2 are reset via switches S_2–S_4, and all capacitive dividers are reset via switches S_5–S_9. At the beginning of the RX phase (Φ_{rx}), the transducer is connected to the TIA via the switch S_1. Noting that as the voltage on the top plate of the transducer is kept at ground level between the end of the TX phase and the RX phase, imaging artifacts associated with the transition from TX to RX are thus minimized. The CCSN of TIA then begins to traverse five capacitive dividers along the pseudo-exponential trajectory.

The CSBN, which generates the bias voltages for the CCSN (see Fig. 5), is based on the circuit reported in [9], as depicted in Fig. 7(b). As the TGC control voltage V_c is swept along a linear ramp-up curve, the tail current I_{t0} is steered from the rightmost diode-connected NMOS transistor to the leftmost creating five gate bias voltages (V_{cn1}–V_{cn5}) for the NMOS transistors of the CCSN. These five voltages are also mirrored to five NMOS transistors which direct the tail current I_{t1} from the leftmost diode-connected PMOS transistor to the rightmost resulting in the bias voltages (V_{cp1}–V_{cp5}) for the PMOS transistors of CCSN, as shown in Fig. 5(b). I_{t1} is a scaled version of the static bias current I_0 of the inverter-based amplifier in Fig. 5(a). All these NMOS/PMOS transistors are properly scaled to guarantee that the NMOS and PMOS current-steering pairs of the CCSN divide the dc bias current I_0 and ac current i_0 at the same rate. Voltage regulators similar to those in Fig. 7(a) are used to generate V_{reg3} and V_{reg4} in Fig. 7(b), which define the output swing of the inverter-based amplifier. The CSBN is shared among four channels to save area and power consumption without introducing noticeable noise into the main signal chain.

B. Bandwidth-Control Circuit

The close-loop bandwidth of the TIA should be above the −3 dB bandwidth of the transducer, which is about 14 MHz in this design, in the presence of the wide current-gain range. The closed-loop bandwidth $\mathrm{BW_{CL}}$ derived from the current transfer function $i_{\mathrm{out1}}/i_{\mathrm{TD}}$, can be expressed as

$$\mathrm{BW_{CL}} \approx \frac{g_{\mathrm{mn}} + g_{\mathrm{mp}}}{C_{\mathrm{p}}} \cdot \frac{1}{1 + \frac{C_{\mathrm{out}}}{C_{\mathrm{in}}} + \frac{C_{\mathrm{out}}}{C_{\mathrm{p}}}} \tag{3}$$

$$C_{\mathrm{in}}, C_{\mathrm{out}} = \left(\frac{m+n}{2} \mp \frac{m-n}{2} \cdot S_{\mathrm{ra}}\right) \cdot C_{\mathrm{u}}$$
$$S_{\mathrm{ra}} \in [-1, 1] \tag{4}$$

where g_{mn} and g_{mp} are the trans-conductance of the input NMOS transistor M_1 and PMOS transistor M_2, respectively. C_{p}, C_{in}, and C_{out} are the transducer's capacitance, the feedback capacitance, and the output capacitance of the TIA, respectively, as shown in Fig. 5(a). C_{u} is the unit capacitance, and S_{ra} is the steering ratio as a linear function of the TGC control voltage V_{c}, defined in the whole gain range. Substituting (4) to (3) and assuming $C_{\mathrm{u}} \ll C_{\mathrm{p}}$ gives

$$\mathrm{BW_{CL}} \approx \frac{g_{\mathrm{mn}} + g_{\mathrm{mp}}}{C_{\mathrm{p}}} \cdot \frac{1 - \frac{m-n}{m+n} \cdot S_{\mathrm{ra}}}{2}. \tag{5}$$

Equation (5) implies that the bandwidth of the TIA is a linear function of the steering ratio S_{ra} resulting in 3.67× bandwidth shrinking during the RX phase. This wide variation of the bandwidth poses a challenge to the TIA loop design in terms of stability, power consumption, and noise performance unless gain-dependent bandwidth compensation is applied. Therefore, we propose a dynamic-biasing scheme in which the transconductance of the inverter-based amplifier is continuously adjusted by changing the bias current to match the change of the steering ratio S_{ra}.

As depicted in Fig. 8(a), the TGC control voltage V_{c} is compared to the same reference voltages V_{re1}–V_{ref4} [see Fig. 7(b)] by four PMOS differential pairs with diode-connected NMOS transistors as their load. Thus, the circuit generates a series of gate-control voltages V_{bn1}–V_{bn4} and V_{bp1}–V_{bp4}, which continuously adjust the current-mirror ratio and the bias current of the TIA via four NMOS current-steering pairs, as shown in Fig. 8(b). The adjustment of the bias current changes the transconductance of the TIA which compensates the closed-loop bandwidth in (5). The dynamic-current-mirror ratios at the beginning and the end of the RX phase

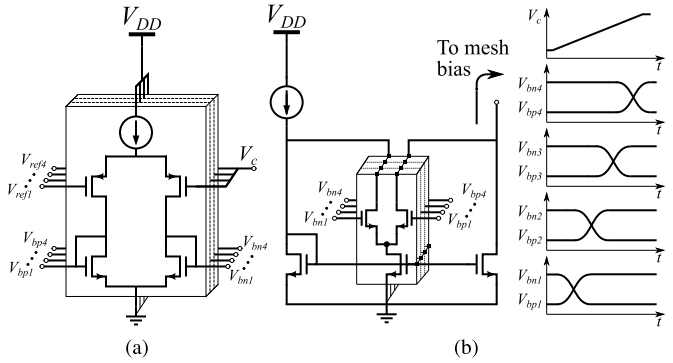


Fig. 8. (a) CSBN of the bandwidth-control circuit. (b) Dynamic current mirror with diagrams showing the TGC control voltage and the bias voltages as a function of time.

were carefully selected based on the simulation to guarantee sufficient loop stability and a roughly constant closed-loop bandwidth.

C. Class-AB CA

As depicted in Fig. 9(a), the variable-gain CA is based on a class-AB current mirror [23] of which the current-mirror ratio is continuously tuned by the CCSN. The CA consists of four unit current branches CB_1–CB_4 and the associated input–output current branch. A four-tap CCSN adjusts the current mirror ratio across five gain steps (2/6), (3/5), . . . , (6/2) throughout the RX phase resulting in a total gain range of 19.1 dB. These five gain steps again can be described by (6) with parameters $m = 6$ and $n = 2$. The bandwidth of the local feedback loop is designed to be at least a factor of two higher than the TIA's bandwidth throughout the overall gain range. Thanks to the class-AB operation and the fast local feedback loop, the CA only has minor impact on overall bandwidth of the AFE, thus making the first TIA stage to be the main limiting factor of the bandwidth. The output current i_{out2} of the CA is converted into a voltage v_{out2} via a load resistor R_L and fed to an output driver to drive an off-chip load.

A CSBN, shown in Fig. 9(b), generates the gate-control voltages for the CCSN of the CA. The TGC control voltage V_c is compared to a series of reference voltages V_{ref1}–V_{ref4} via four NMOS differential pairs with diode-connected PMOS loads, similar to the bandwidth control circuit shown in Fig. 8(a). The generated CCSN control voltages V_{cna4}–V_{cna4} and V_{cnb1}–V_{cnb4} are converted to V_{cpa1}–V_{cpa4}, and V_{cbp1}–V_{cbp4} via four NMOS differential pairs with diode-connected PMOS loads. By properly sizing the NMOS differential pairs and the PMOS loads of the CSBN, the dc components of the CCSN are largely canceled by the complementary structure and thus do not saturate the output branch CB_{out}. The residual dc components introduce a low-frequency signal to the output voltage v_{out2} that changes at the same speed as the TGC control voltage V_c. Fortunately, the frequency of V_c is out of the signal bandwidth and therefore the low-frequency signal associated with it can be easily filtered out. Voltage regulators similar to those in Fig. 7(a), shared by four CAs, generate the local supply rails $V_{\text{regc1,2,3}}$ and thus attenuate interference from the power supply and ground.

D. Noise Analysis

The first TIA stage and the second CA stage have different contributions to the total input-referred noise at different AFE gains. At the highest gain setting, the noise of the TIA dominates the input-referred noise. The noise of the CA only has a small impact due to the high gain of the first TIA stage. More specifically, the major noise sources in the TIA are the MOS devices in the inverter-based amplifier and the hardware-sharing regulators, while the high-voltage TX/RX switch only has a minor impact, as it was sized such that it contributes only 10% of the total noise. The feedback capacitors do not contribute thermal noise, whereas the CCSNs of the TIA contribute part of the noise during the interpolation. The noise of the TIA decreases as the TGC function moves toward the high gain region due to the dynamic-biasing scheme of the bandwidth-control circuit, thus significantly improving the power efficiency of the first TIA stage compared to a constant-biasing solution. At the low gain setting, the second CA stage dominates the final noise level due to the lower gain of the preceding stage and the larger dc bias current as a result of more unit current branches attaching to the input current branch of the CA. Nevertheless, the amplitude of input signal also becomes larger and signal-to-noise ratio (SNR) is even improved because the signal increases faster than the noise level, as will be elaborated in Section V.

V. Experimental Results

A. ASIC Prototype

An ASIC prototype chip was fabricated in a 180-nm high-voltage BCDMOS process (see Fig. 10). The chip contains eight AFE channels, divided into two groups of four that share hardware, which are connected via multiplexers to the 64 transducer elements, and element-level pulsers capable of driving the elements with 36 V unipolar pulses. Four AFE channels with shared hardware occupy $200 \times 500\ \mu\text{m}^2$, corresponding to $0.025\ \text{mm}^2$ per channel. The 64 transducer channels are arranged into an 8×8 array which enables direct integration between the ASIC and PZT transducers in a pitch-matched fashion.

B. Electrical Characterization

For electrical characterization, an input current was generated by applying an external voltage signal to an on-chip capacitor of 1 pF that mimics a transducer element. Fig. 11(a) shows the AFE's gain measured at different frequencies as a function of the TGC control voltage V_c. 8-, 10-, and 12-MHz sinusoidal current inputs were used in the measurement which correspond to 40% transducer bandwidth. As expected, the gains of the AFE at different frequencies are approximately dB-linear functions of the control voltage V_c, and thus the TGC function is obtained by applying a linear ramp-up control voltage. The gain errors with respect to ideal linear-in-dB curves are extracted and depicted in Fig. 11(b), which are all

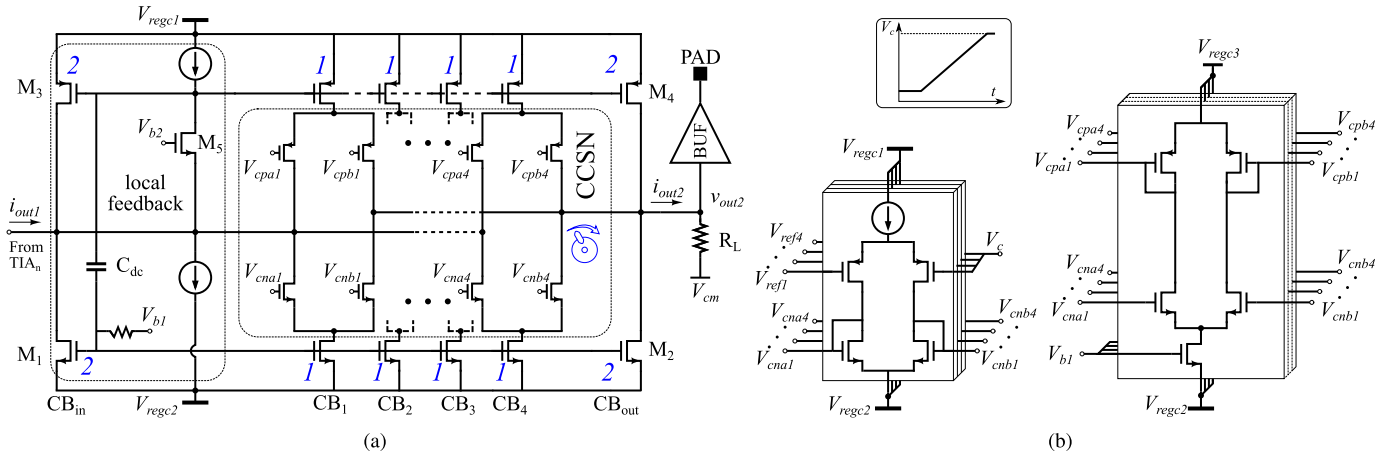


Fig. 9. (a) Circuit diagram of the CA with CCSN. (b) CSBN of the CA.

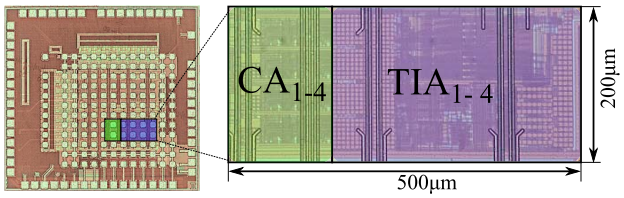


Fig. 10. Micrograph of the 64-channels transceiver ASIC, with inset showing the layout of four AFE channels with shared circuitry (PADs removed).

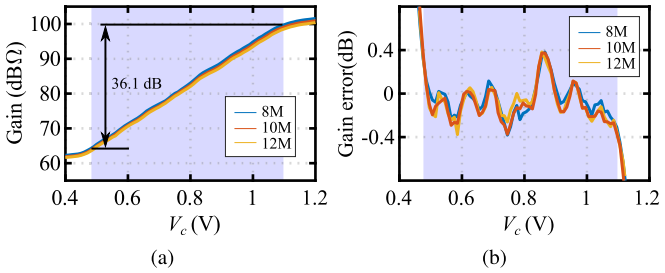


Fig. 11. (a) Measured AFE gain at three frequencies as a function of V_c. (b) Calculated linear-in-dB gain errors.

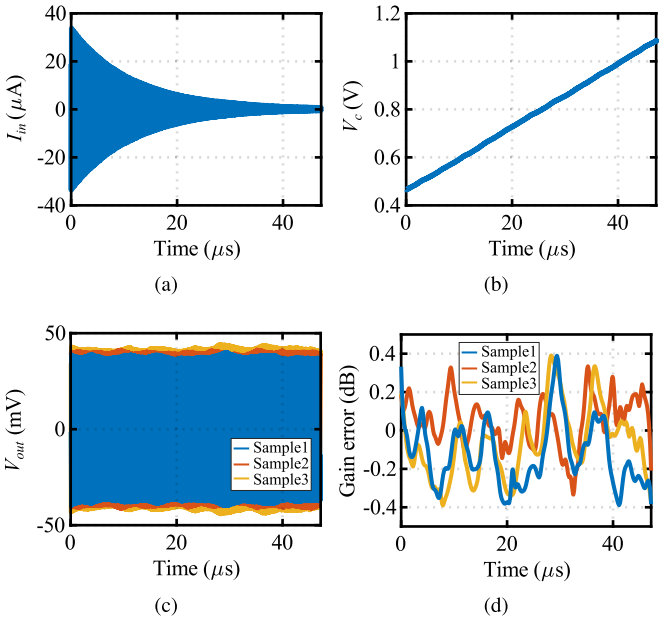


Fig. 12. (a) Exponentially decaying input current. (b) Applied TGC control signal. (c) Measured AFE output voltages of three test samples. (d) Corresponding linear-in-dB gain errors.

below ±0.4 dB within a 36.1-dB overall gain range. Fig. 12 shows the transient response of the AFE obtained by applying a 10-MHz sinusoidal current with a peak-to-peak amplitude that decays exponentially in 48 μs from 64 to 1μA [see Fig. 12(a)]. This corresponds an overall 36.1-dB input amplitude change. The same linear ramp-up voltage was applied to the TGC control inputs of three test samples [see Fig. 12(b)], resulting in three output waveforms measured at each AFE's output as shown in Fig. 12(c). The extracted envelopes [see Fig. 12(d)] show that the AFEs adequately compensate for the decay with gain errors all below ±0.4 dB.

Fig. 13(a) shows the transfer function measured at different TGC control voltages (V_c), as well as a −3-dB bandwidth curve across the overall control voltage range. As depicted in Fig. 13(b), the measured −3-dB bandwidth at different TGC control voltages changes between 17.5 and 25.4 MHz, resulting in a less than ±20% variation around 21.7 MHz across the gain range. Thanks to the proposed bandwidth-control circuit, the −3-dB bandwidth changes only slightly compared to the factor of about 100 gain variation of the AFE.

The output noise density of the AFE was measured by connecting the same on-chip 1-pF capacitor at the input of the TIA to the ground and sweeping the TGC control voltage V_c. The input-referred noise density was calculated by dividing the measured output noise density by the measured gain, resulting in a series of input-referred noise spectra at different TGC control voltages, as shown in Fig. 14(a). The noise floor averaged from 6 to 14 MHz is shown in Fig. 14(b), as a function of the TGC control voltage. The noise decreases for higher gains and reaches 1.31 pA/$\sqrt{\text{Hz}}$ at a TGC control voltage of about 1.1 V, where the gain error still falls below ±0.4 dB. At the lowest gain where gain error still satisfies

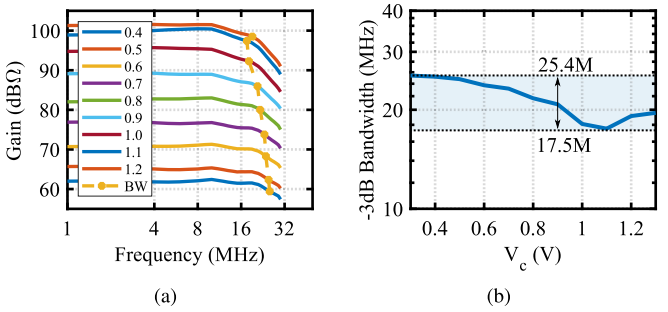


Fig. 13. (a) Measured gain transfer function. (b) −3-dB bandwidth as a function of TGC control voltage V_c.

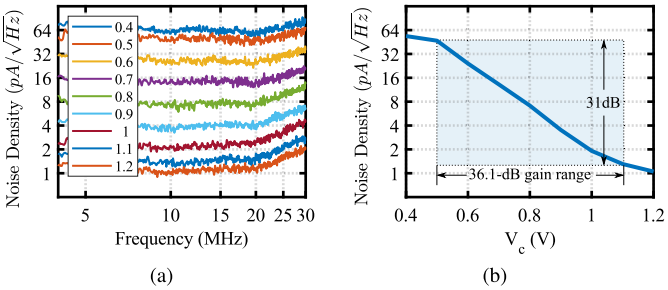


Fig. 14. (a) Measured input-referred noise spectra, (b) Measured in-band noise density as a function of TGC control voltage V_c.

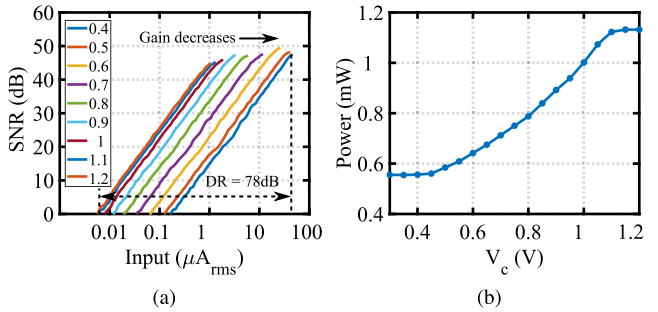


Fig. 15. (a) Measured SNR as a function of the input current in different TGC's control voltage. (b) Measured power consumption as a function of TGC control voltage (V_c).

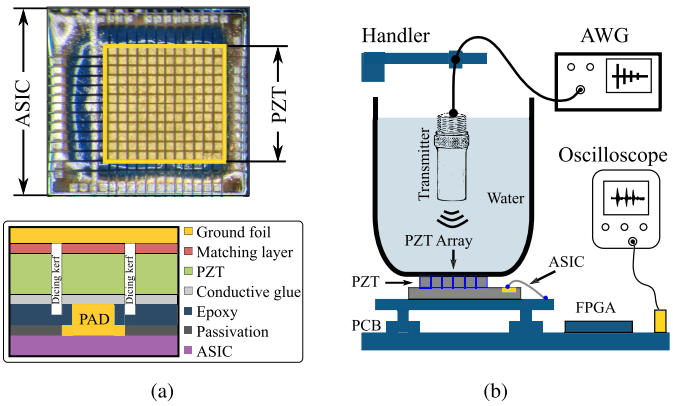


Fig. 16. (a) Micrograph of the ASIC with PZT transducers on top and a cross-sectional view showing PZT-on-CMOS integration. (b) Measurement setup of the acoustical characterization of the TGC function.

the boundary condition of ±0.4 dB, the noise floor is about 47 pA/$\sqrt{}$Hz. The noise floor grows by about 31 dB, but still falls behind the input signal, which grows by about 36 dB in the overall TGC gain range. Therefore, the SNR improves as the TGC gain moves toward the low-gain region. The trend of the SNR improvement toward the low-gain region is verified by a DR measurement as depicted in Fig. 15(a), where the SNR was measured as a function of the input current at different TGC control voltages. The DR of the proposed AFE is about 78 dB, which is measured as the ratio of the highest input signal level at the 1-dB compression point and the lowest input signal level at which the input signal power equals the noise power.

The power-supply rejection (i.e., the attenuation from the supply to the output) was measured to be 22.6 dB at 10 MHz frequency, sufficient to prevent noise and interference from the supply from limiting the performance of our prototype. Simulations show that this is limited by the V_{cm} buffer in our prototype (see Fig. 3) and can readily be improved.

Fig. 15(b) shows the measured power consumption as a function of the TGC control voltage. As expected, the power consumption varies along the measured curve to compensate the bandwidth variation during the RX phase, resulting in an average power consumption of 0.8 mW from a 1.8-V supply voltage provided that the TGC control voltage changes properly to generate a 36-dB TGC gain range.

C. Acoustical Characterization

Fig. 16(a) shows the micrograph of a fabricated prototype with PZT transducers on top of the ASIC fabricated using the piezoelectric layer (PZT)-on-CMOS technology described in [28]. An 8 × 8 transducer array with a 100-μm pitch, surrounded by a ring of protecting dummy elements, was directly built on the ASIC by means of mechanical dicing. The bottom electrodes of the transducer elements connect to the ASIC's bond pads via gold bumps, leading to minimized parasitic capacitance. The common ground electrodes of the transducers were connected to the PCB through the ground foil [not shown in Fig. 16(a)].

For characterization of the TGC function, a small water tank was mounted on top of the prototype, with an external single-element ultrasound transmitter submerged in the water [see Fig. 16(b)]. A series of exponentially decaying pulses were generated by an arbitrary waveform generator (AWG), which excite the transmitter to generate the corresponding exponentially decaying ultrasound waves. The acoustic signal is converted into electrical signal by the PZT elements. The ASIC applies TGC function to the received current and outputs the compensated signal to an off-chip buffer connected to an oscilloscope. An FPGA controls the operation of the ASIC, e.g., switching between TX and RX phases, and also triggers the oscilloscope to record the received ultrasound data.

Noting that the attenuation of ultrasound waves in the water is negligible, the 10-MHz single-element transmitter was excited by a train of seven pulses modulated by an exponentially decaying envelope to emulate the attenuation, with a decay rate tuned to match an attenuation factor of

TABLE I
PERFORMANCE COMPARISON

	This work	[3]	[24]	[9]	[11]	[12]
Process	**180-nm BCD**	180-nm HVCMOS	180-nm BCD	180-nm BCD	180-nm CMOS	/
Pitch-matched	**Yes(100 μm)**	No	No	No	No	No
AFE Type	**TIA**	TIA	TIA	TIA	VGA (2)	Voltage amp.
TGC Type	**Interpolating**	Discrete	Discrete	Interpolating	Analog	Interpolating
−3-dB BW	**17.5 MHz**	16 MHz	10 MHz	7.1 MHz	3.1 MHz	50 MHz
Maximum gain	**102 dBΩ**	119 dBΩ	116 dBΩ	107 dBΩ	37 dB	38 dB
Effective gain range (1)	**36 dB**	12 dB	12 dB	33 dB	37 dB	37 dB
Gain error	**±0.4 dB**	±3 dB	±3 dB	±1 dB	±1.4 dB	±0.9 dB
Input-referred noise density	**1.31 pA/$\sqrt{\text{Hz}}$ @10 MHz**	2.0 pA/$\sqrt{\text{Hz}}$ @13 MHz	0.4 pA/$\sqrt{\text{Hz}}$ @5 MHz	1.7 pA/$\sqrt{\text{Hz}}$ @5 MHz	8.6 nV/$\sqrt{\text{Hz}}$ @2 MHz	4.1 nV/$\sqrt{\text{Hz}}$ @5 MHz
Transducer capacitance	**1 pF**	0.7 pF	2 pF	15 pF	/	/
Power consumption	**0.8 mW**	0.79 mW	1.4 mW	5.2 mW	0.96 mW	52 mW
Area	**0.025 mm^2**	0.027 mm^2	0.028 mm^2	0.12 mm^2	0.025 mm^2	/

(1) Gain range that satisfies the specified gain error.
(2) Not including the LNA which is required before the VGA.

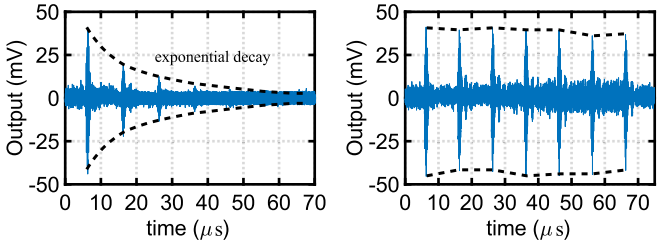


Fig. 17. (a) Uncompensated ASIC output with the TGC function disabled. (b) Compensated ASIC output with the TGC function enabled.

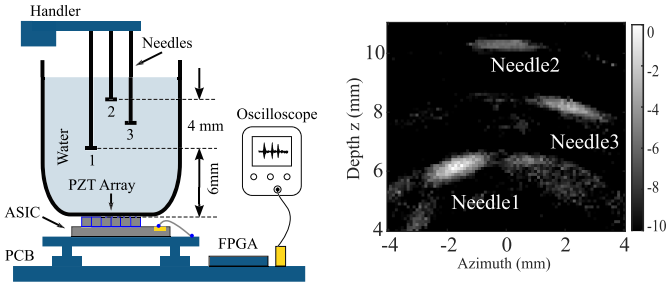


Fig. 18. (a) Setup for imaging experiment. (b) B-mode image showing the position of the needles.

0.4 dB · cm^{-1} · MHz^{-1}. As depicted in Fig. 17(a), the ultrasonic-pulse train was received by the AFE with its TGC function deactivated by keeping the TGC control voltage at a constant level during the RX phase, leading to a 36-dB signal attenuation within 60 μs at the AFE's output, which is in line with the preset attenuation rate. In the following measurement, the AFE processed the same incoming ultrasound pulses with the TGC function activated, compensating the exponentially decaying envelope, resulting in a voltage output with an amplitude variation smaller than ±0.36 dB, as shown in Fig. 17(b).

The same test bench was reconfigured for an imaging experiment, as shown in Fig. 18(a), in which the single-element transmitter was replaced by three needle reflectors positioned at 6, 8, and 10 mm from the transducer surface. A plane wave was transmitted by driving all the elements with 30-V pulses. As shown in Fig. 18(b), a B-mode image was reconstructed from the data acquired at each AFE's output, clearly showing the needle positions even with the relatively small aperture size.

The performances and characteristics of our work and the prior art have been summarized in Table I for comparison. Compared to AFEs with discrete-time TGC [3], [24], comparable performances have been achieved, but with a wider gain range and without introducing gain-switching and virtual ground-switching transients that could lead to image artifacts. Compared to AFEs with interpolating [9], [12] and analog TGCs [11], a >2× better linear-in-dB gain error is obtained in a wider effective gain range with less area and power consumption, as demonstrated both in the electrical and acoustic measurements.

VI. CONCLUSION

This article has presented a pitch-matched AFE with continuous TGC function. The presented CCSN interpolates exponentially-spaced gain steps with a pseudo-exponential interpolation scheme, leading to a small linear-in-dB gain error and fewer passive devices than in solutions based on many small discrete gain steps. The hardware-sharing topology and inverter-based amplifiers used in the AFE further reduce the area and power consumption. The dynamic biasing scheme smoothly compensates for the bandwidth variation caused by the gain change of the TGC function without deteriorating the SNR, thus providing a nearly constant gain-bandwidth product and better power efficiency. To the authors' best knowledge, the prototype is the first reported work that combines a continuous TGC function into a pitch-matched layout with a 100 μm-level pitch size. All these features make the solution promising for next-generation miniaturized 3-D ultrasound imaging devices.

APPENDIX

In this Appendix, the gain trajectory of the TIA is derived at first. For simplicity, we assume only two adjacent steering branches are activated simultaneously in every time interval, e.g., only steering branches B_1 and B_2 are activated in the first time inverval$_1$ [see Fig. 5(b)]. The current-gain steps between i_{out} and i_{in} can be expressed by a unified pseudo-exponential function

$$\frac{i_{\text{out}}}{i_{\text{in}}} = \frac{1+\frac{m-n}{m+n}\cdot y}{1-\frac{m-n}{m+n}\cdot y}$$
$$y = \left\{-1, -1+\frac{2}{m-n}, \ldots, 1\right\} \tag{6}$$

where the expression of discrete variable y corresponds to the beginning of each time interval interval$_1$–interval$_n$ [see Fig. 5(b)], e.g., $y = \{-1, -1 + (2/m - n)\}$ corresponds to the first two gain steps of the time interval$_{1,2}$, i_{out} is the feed-forward current coupling to the virtual ground of the next stage, i_{in} is the feedback current identical to the transducer's input current i_{TD} as a result of the negative feedback loop, and m and n are the number of unit capacitors associated with steering branch B_1.

The CCSN interpolates between these two exponentially-spaced gain steps. Provided the trans-conductances of M_1 and M_2 [see Fig. 5(a)] are designed to be equal and the gate bias voltages change properly as depicted in time interval$_1$ in Fig. 5(b), the PMOS current-steering pair ($M_{\text{p1}}/M_{\text{p2}}$) divides the currents flowing through M_2 at the same ratio as the NMOS current-steering pair (M_{n1}/M_{n2}) divides the currents flowing through M_1. The large-signal currents flowing through the CCSN in (1) can be nearly canceled and the first two small-signal output currents i_1 and i_2 of the CCSN branches B_1 and B_2 can be expressed as

$$i_{1,2} = (1 \mp \alpha \cdot V_{c1}) \cdot i_0 \qquad \alpha \cdot V_{c1} \in (-1, 1) \tag{7}$$

based on (2), where $V_{\text{c1}} = V_{\text{cn2}}$ - V_{cn1} is the TGC control voltage in interval$_1$, and α is a constant determined by the MOS transistors. The currents $i_{1,2}$ are linear functions of the control voltage V_{c1}, the ratio of i_2 to i_1 is of the form $((1 + x)/(1 - x))$. These currents divide between the output capacitors and the feedback capacitors connected to steering branches B_1 and B_2. As a result, the total current flowing to the input i_{in}, which due to the feedback in the TIA equals the transducer's signal current i_{TD}, as well as the total current flowing to the output i_{out}, is a linear combination of i_1 and i_2. The current gain during interpolation of first two gain steps can be expressed as

$$\frac{i_{\text{out}}}{i_{\text{in}}} = \frac{ni_1 + (n+1)i_2}{mi_1 + (m-1)i_2}. \tag{8}$$

Substituting (7) into (8) gives

$$\frac{i_{\text{out}}}{i_{\text{in}}} = \frac{1+\frac{\alpha\cdot V_{c1}-(m-n-1)}{m+n}}{1-\frac{\alpha\cdot V_{c1}-(m-n-1)}{m+n}}. \tag{9}$$

Now a steering ratio (S_{r1}) can be defined as

$$S_{r1} = \frac{\alpha \cdot V_{c1} - (m-n-1)}{m-n}$$
$$S_{r1} \in \left(-1, -1+\frac{2}{m-n}\right). \tag{10}$$

Substituting (10) into (9) yields a similar equation as (6), except that instead of discrete variable y, S_{r1} is a continuous linear function of the TGC control voltage V_{c1}, corresponding to the interpolation of the first time interval$_1$. Therefore the current gain during interpolation, which is the ratio of i_{out} to i_{TD}, is also of the form $((1 + x)/(1 - x))$. A repetitive analysis can be applied to the other time intervals interval$_2$–interval$_n$ to prove that the overall gain curve is a pseudo-exponential function of the TGC control voltage.

A similar analysis can be applied to the interpolation of the CA. E.g., at the beginning of each time interval, the gain steps can be expressed with the same function (6). During the interpolation, the current gain ($i_{\text{out2}}/i_{\text{out1}}$) still conforms with (8), (9) and $((1 + x)/(1 - x))$.

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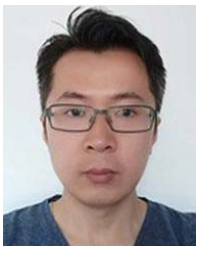

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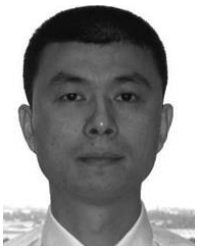

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