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An Intriguing Relation Between the Power Consumption and Number of Antenna Elements in Multi-Beam Phased Arrays

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***Abstract*—An improved system-level power consumption model (PCM) for 5G base station multi-beam phased-array transmit architectures is developed. Using this model, it is shown that an optimum number of antenna elements of the array exists with respect to the total power consumption. The proposed model is benchmarked against a recent study which is shown to underestimate the total power consumed in analog and digital antenna systems by 37% and 126% respectively.**

***Index Terms*—5G, antennas, front-end, multi-beam, phased array, power consumption.**

I. Introduction

In the last decade, there has been exponential growth in the telecommunications industry, particularly in 5th Generation (5G) technology, which is expected to support 25% of the global mobile traffic by 2025 and nearly 60% by 2027 [1]. This rapid large-scale adoption together with other aspects of 5G such as ultra-densification, massive MIMO technology and elevated demands from a large number of simultaneous users, corresponds to an increase in the power consumption of the mobile network infrastructure. This is especially relevant in today's time of unprecedented energy stress and among concerns about climate change, and it necessitates the enhancement of the base station (BS) power consumption optimisation and the use of accurate and application-specific power consumption models (PCM) of the 5G array architectures, in order to directly lower the cost and environmental impact of the network [2], [3] . One way to achieve this is by optimising the number of antenna elements in the phased-array architecture such that an optimally low system power consumption is achieved.

Much of the existing research in 5G applications focuses mainly on the enhancement of the RF performance, whereas the consideration of power consumption was limited in scope at both the system- and component-level. Previous system-level PCMs have explored the impact of antenna scaling and bandwidth [2], [4], [3], [5], spatial multiplexing of users [5], transmitter system parameters and constraints on service quality [6], the trade-off between spectral efficiency and energy efficiency [7].

TABLE I
Scope, use cases & main limitations of surveyed 5G antenna array power consumption models.

Ref.	Tx/Rx	Scheme	f_c (GHz)	BW (MHz)	Cell Size	Num. Users	Main Limitations
[8]	TRx	MBPAA, DMBA	28	500	femto	1	No DSP power.
[7]	Rx	SBPAA, DMBA	>30	1000	-	1	Superficial losses & DSP; cannot extend to Tx.
[4]	Tx	DMBA	28	850	pico	8-32	Not optimised.
[2]	Tx	MBPAA, DMBA	28	100-250	pico	1-67	Large gap from state-of-the-art; superficial DSP.
[5]	TRx	DMBA	60	1760	pico	2,4	Large gap from state-of-the-art.
[9]	Rx	SBPAA, DMBA	28	380	-	2	Cannot extend to Tx.
This work	**Tx**	**MBPAA, DMBA**	**28**	**100-400**	**pico**	**2-32**	

It was a common drawback for the existing models to only account for the power consumption of power amplifiers (PA) and analog-digital converters (ADC/DAC), while excluding other components that have a non-negligible power signature (e.g. signal splitters/combiners, DSP) [7]. Further, due to rapid developments in signal processing and semiconductor technologies, there exists a large gap between many existing PCMs and the state-of-the-art [2], [5]. Finally, previous work often falls short of complying with up-to-date standardisation practices of The 3rd Generation Partnership Project (3GPP). Table I summarises the existing literature and its limitations.

This paper extends previous work on the power consumption modelling and analysis of 5G multi-beam phased array architectures in the 28 GHz 'dense urban enhanced Mobile Broad Band (eMBB)' use case by (a) including a more complete set of circuit components in the model, (b) incorporating the state-of-the-art for the included components, and (c) aligning the model with the latest 3GPP-recommended channel model and effective isotropic radiated power (EIRP) (as per Release 16-18 [10]).

The rest of this paper is organised as follows: Section II describes the modelling methodology, including its scope and validation. Based on this, Sections III-IV present the developed PCM at the system- and component-level, respectively. The model's output and validation results are presented and discussed in Section V. Finally, the main points and conclusions are summarised in Section VI.

II. Methodology

We focus on a single pico-cell scenario in the eMBB use case [5]. The cell is assumed to have one 5G Base Station (BS) in the centre, with U stationary and equidistant User Equipments (UEs) situated along the cell edge at a radius of d_{UE} = 100 m. The 27.5-29.5 GHz frequency band, with an centre frequency of $f_c = 28$ GHz, is chosen as the target frequency range, as it is a strong candidate for 5G broadband communications [11] and compatible with the pico-cell coverage area.

It has been claimed that the transmitter accounts for the bulk of the BS power consumption [2], [3], hence we focus on the transmitter architecture and the corresponding downlink physical RF access layer (from BS to UE). Any other layers (e.g. the network layer) are excluded. On the same note, for the baseband unit (BBU) at the BS, we consider only the power used for baseband (BB) signal computations and exclude the power consumption due to AC-DC conversion, cooling etc.

We focus on the two primary types of beamforming array configurations for concurrent multiple beam generation:

1) Fully-analog active multi-beam phased array antenna (MBPAA), where analog beamforming is carried out using (active) RF phase shifters to control multiple beams simultaneously (see Fig. 1).
2) Fully-digital multi-beam array (DMBA), which involves digital control of individual antenna elements through dedicated RF chains (see Fig. 2).

In-depth explanations of these architectures' radiation patterns and RF performance can be found in [11]. A third type of 'hybrid' architecture, which is a combination of analog and digital beamforming schemes, will be considered in future work.

A. Modelling

First, for each architecture, a system-level model was constructed to estimate the link budget and quantify the number of components required to fulfill the budget. Using this basis, a component-level model was defined to estimate the power consumption of individual components. The two models were integrated to yield the estimated power consumption of the entire system.

B. Validation

The recently published model in [2] was chosen as a benchmark for the system-level PCM proposed in this paper because it analyses the power consumption of the MBPAA and DMBA schemes under a similar use case as this paper. To ensure a fair comparison between the two models, the following link budget and use case parameters from [2] were used in this paper as well: centre frequency f_c, bandwidth BW, cell radius d_{UE}, and number of simultaneous users $U = 17$. The 3GPP recently proposed using a standardised effective isotropic radiated power (EIRP) per beam of $EIRP = 40$ dBm, which was subsequently used in [2] as well as in this paper.

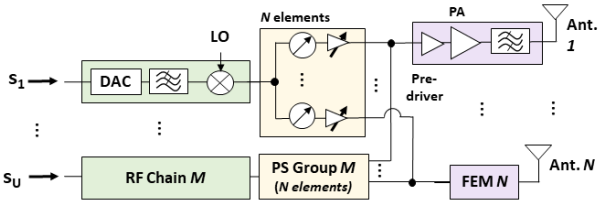

Fig. 1. MBPAA scheme and constituent components.

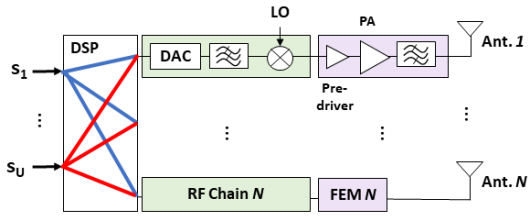

Fig. 2. DMBA scheme and constituent components.

The component-level models were validated against the state-of-the-art for each component. The compilation of component surveys for validation can be found in [12].

III. Model: System-Level

This paper uses the 3GPP UMi C.I. model [13] as the underlying channel model for the estimation of the link budget (the reference model in [2] uses the NYUSIM 2.1 channel model). The link budget is estimated to express the required power at the transmitter, and is presented in Table II.

TABLE II
Link budget per UE.

Symbol	Parameter	Value
f_c	Centre Frequency	28 GHz
BW	Bandwidth	250 MHz
d_{UE}	Distance to UE	100 m
$EIRP$	Tx EIRP per beam	40 dBm
$G_{RX_{AE}}$	Receiver Antenna Gain [10]	5 dBi
NF	Receiver Noise Figure [2]	4 dB
N_{RX}	Num. Receiver Antennas [10]	4
$G_{TX_{AE}}$	Transmitter Antenna Gain [2]	3 dBi
N_{TX}	Num. Transmitter Antennas	*Variable*

On a high level, the system power consumption P_{TOT} can be expressed as the sum of the constituent modules' power consumption, i.e.

$$P_{TOT} = P_{BBU} + P_{RFC} + P_{PSG} + P_{RFamp} + P_{PA} \quad (1)$$

which denote the power consumed by the baseband unit (BBU), RF chain, phase shifter group, RF amplifiers and PAs respectively. The modules can be broken down into smaller constituent components as

$$P_{RFC} = N_{DAC}P_{DAC} + N_{mix,LO}P_{mix,LO} \quad (2)$$
$$P_{PSG} = N_{PS}P_{PS} + N_{VGA}P_{VGA} \quad (3)$$
$$P_{RFamp} = N_{spA}P_{spA} + N_{cbA}P_{cbA} + N_{PD}P_{PD} \quad (4)$$

where spA, cbA and PD refer to the splitter amplifiers, combiner amplifiers and pre-driver amplifiers respectively. Furthermore, there must be at least as many RF chains as the number of independent users U that can be served simultaneously. Table III provides a comparative overview of the number of constituent components in both, MBPAA and DMBA architectures.

At mmW frequencies, splitting and combining losses in the analog circuit can quickly become significant, and their magnitudes are highly implementation-specific. Using a single high-gain amplifier in the circuit for loss compensation runs the risk of signal distortions and non-linearity at high frequencies. To address this in a generalisable way, we assume a binary tree circuit structure with cascaded loss-compensation RF amplifiers placed after every three stages of splitting or combining in the circuit. The number of splitter amplifiers N_{spA} and combiner amplifiers N_{cbA} are therefore a function of the number of transmit antenna elements and simultaneous users respectively. For the given use case of 17 users and a range of 20-320 transmit antenna elements, this gives a range of

$$N_{spA} = 1 \text{ to } 73 \quad (5)$$
$$N_{cbA} = 1 \text{ to } 2 \quad (6)$$

Details of the splitting and combining structure can be found in [12].

IV. Model: Component-Level

This section provides the basic framework for estimating the power consumption of constituent components, namely: PA, DAC, BBU, mixer and local oscillator (LO), phase shifters (PS) and various RF amplifiers. A more extensive model with full explanations and derivations will be published as future work. Table III presents an overview of the system- and component-level PCM described in this paper.

PA: The required transmit power per antenna element $P_{TX_{AE}}$, and the resultant per-PA output power $P_{out_{PA}}$, can be derived from the link budget and use case-related parameters as

$$P_{TX_{AE}} = EIRP + 10\log_{10}(U) - G_{TX_{AE}} - 20\log_{10}(N_{TX}) \quad (7)$$
$$P_{out_{PA}} = P_{TX_{AE}} + IL_{PA} + IL_{BPF} \quad (8)$$

Subsequently, the per-PA power consumption P_{PA} can be expressed as

$$P_{PA} = \frac{P_{out_{PA}}}{PAE} \quad (9)$$

where IL_{PA} and IL_{BPF} are the insertion losses of the PA and BPF respectively, and PAE is the PA's technology-dependent power added efficiency. In this model, we use $IL_{PA} = 1.15$ dB. Furthermore, a power back-off of $PBO = 6$ dB is assumed. Based on the reference model in [2], we choose $PAE = 25.5\%$, which can be achieved using state-of-the-art GaN PAs (average $PAE_{GaN} = 23\%$) or cutting edge CMOS SOI PAs (max. $PAE_{CMOS-SOI} = 25\%$) [12].

DAC: A first-order model of the per-DAC power consumption P_{DAC} was furnished by [15] as

$$P_{DAC} = \frac{1}{2}\left(V_{DD}I_O(2^b - 1) + b \cdot C_p f_s V_{DD}^2\right) \quad (10)$$

where the DAC sampling frequency f_s (Hz), the Effective Number Of Bits b, and the DAC supply voltage V_{DD} are leading contributors. The explanation of parameters and the extended derivation of eq. 10 can be found in [15].

BBU: The baseband unit (BBU) power consumption P_{BBU} arises from the DSP operations involved in digital beamforming, and is proportional to the BBU efficiency η_{BBU}. From [14], P_{BBU} can be expressed as

$$\begin{aligned} P_{BBU} &= (N_{TX}U) \cdot BW \cdot \eta_{BBU} \cdot \gamma_{DSP} \\ &= (N_{TX}U) \cdot P_{DC_{BBU}} \cdot \gamma_{DSP} \end{aligned} \quad (11)$$

where γ_{DSP} represents the power consumption's dependence on beamforming architecture, such that $\gamma_{DSP} = 1$ for DMBA and $\gamma_{DSP} = 0$ for MBPAA. $P_{DC_{BBU}}$ denotes the per-operation power consumption of the BBU.

RF amplifiers: By assuming a minimum FEM PA drive power of 0 dBm, our model can determine the required gain from the RF amplifiers in the circuit, namely the splitter/combiner amplifiers, the PS-group variable gain amplifiers (VGA), and the FEM pre-driver. Higher values of RF pre-driver gain correspond to higher unit power consumption. The computed gain and unit power consumption for the specific use case described in this paper are contained in Table III, while the fully dynamic model will be introduced as part of future work.

Other components: The unit power consumption of CMOS mixer, LO and PS components was estimated by surveying the state-of-the-art. The surveys have been summarised in [12].

TABLE III
NUMBER AND UNIT POWER CONSUMPTION OF CONSTITUENT COMPONENTS.

Abbrev.	Component	Reference [2]			This model		
		MBPAA	DMBA	Unit P_{DC} or Loss	MBPAA	DMBA	Unit P_{DC} or Loss
N_{TX}	Transmit. antennas	20-320 antenna elements					
M	RF chains	U	N_{TX}		U	N_{TX}	
BPF	Bandpass filter	N_{TX}	N_{TX}	-	N_{TX}	N_{TX}	1 dB
spT	Divider	U	0	-	$M(N_{TX}-1)$	0	4 dB
cbT	Combiner	N_{TX}	0	-	$N_{TX}(M-1)$	0	4 dB
DSP	Num. DSP operations (OP)	0	$N_{TX}U$	3.9 mW/OP	0	$N_{TX}U$	10 mW/OP [2], [14]
DAC	Digital-to-analog converter	U	N_{TX}	20 mW	U	N_{TX}	68 mW [15] [12]
$mxLO$	Mixer and LO	$4U$	N_{TX}	40 mW	U	N_{TX}	140 mW [12]
PS	Active phase shifter	MN_{TX}	0	20 mW	MN_{TX}	0	10 mW [4]
VGA	Variable gain amplifier	MN_{TX}	0	-	MN_{TX}	0	15 mW [16]
spA	RF splitter amplifier	-	-	-	eq. 5	0	20 mW [12]
cbA	RF combiner amplifier	-	-	-	eq. 6	0	10 mW [12]
PD	RF pre-driver	-	-	-	1	1	10-40 mW [17]
PA	Power amplifier	N_{TX}	N_{TX}	eq. 9	N_{TX}	N_{TX}	eq. 9

V. SIMULATION RESULTS AND DISCUSSION

Use case-related and key component-related input parameters were set as identical for both the reference model and the proposed model: (a) U = 17 users (b) BW = 250 MHz (c) $EIRP$ = 40 dBm (d) front-end module PA PAE = 25.5% (e) DAC ENOB $b = 8$ bits and (f) BBU efficiency $\eta_{BBU} = 0.04$ mW/MOPS. For the chosen bandwidth, the proposed model uses a DAC sampling frequency $f_s = 3.7$ GHz and supply voltage of $V_{DD} = 2.7$ V [12].

Figure 3 shows the total power consumption P_{TOT} of the MBPAA and DMBA architectures using the proposed model, and compares it to the results of the reference model (see also Table IV). Both models' outcomes display the convex relationship between the total power consumption and the number of transmit antennas, which validates our model, but also reinforces the challenge to the widely held pre-assumption that digital architectures always consume more power than their analog counterparts.

The power consumption estimated using our model is higher than the benchmark, due to the increase in the number of components considered as well as higher unit power consumption values. We conclude that the reference model tends to underestimate the power consumption of the system. At the same time, for this particular use case, the difference between MBPAA and DMBA at the optimum P_{TOT} diminishes to only 5 W. Compared to the reference model, the DMBA P_{TOT} also rises much more steeply with N_{TX} after the optimum has been achieved.

Figure 4 highlights the high contribution of the BBU and mixer-LO in the DMBA scheme, and of the VGAs in the MBPAA scheme. These components are not conventionally considered 'power-hungry', hence efforts to improve their power consumption have been limited. Based on this break-down of the power budget, we observe a clear trade-off between complexity, performance and power consumption in both schemes.

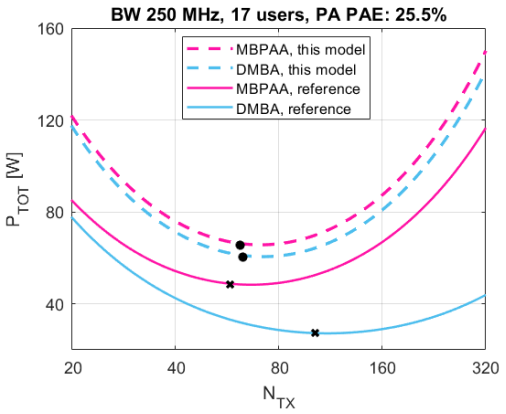

Fig. 3. Comparison of the system's total power consumption using the reference model [2] (solid line) and the proposed model (dashed line). The markers indicate the optimal point for each architecture.

TABLE IV
DIFFERENCE IN OPTIMAL TOTAL POWER CONSUMPTION AND ARRAY SIZE

Architecture	P_{TOT}		N_{TX}	
	Reference [2]	This work	Reference [2]	This work
MBPAA	48 W	66 W	58	62
DMBA	27 W	61 W	102	63

VI. CONCLUSION

Studies on different front-end architectures with respect to the beamforming have been performed. One of principal outcomes from these studies is that regardless of the beamforming method, an optimum number of antenna elements exist with respect to the total power consumption of a multi-beam phased-array architecture. For the first time, a realistic, generalisable, modular and parametric system-level power consumption model (PCM) is designed for 5G mmW multi-beam phased array transmitters in the 28 GHz band, and tailored to the eMBB scenario. The model improves upon the existing literature by incorporating state-of-the-art components, latest regulatory guidelines (3GPP) and considering the RF performance trade-off for analog and

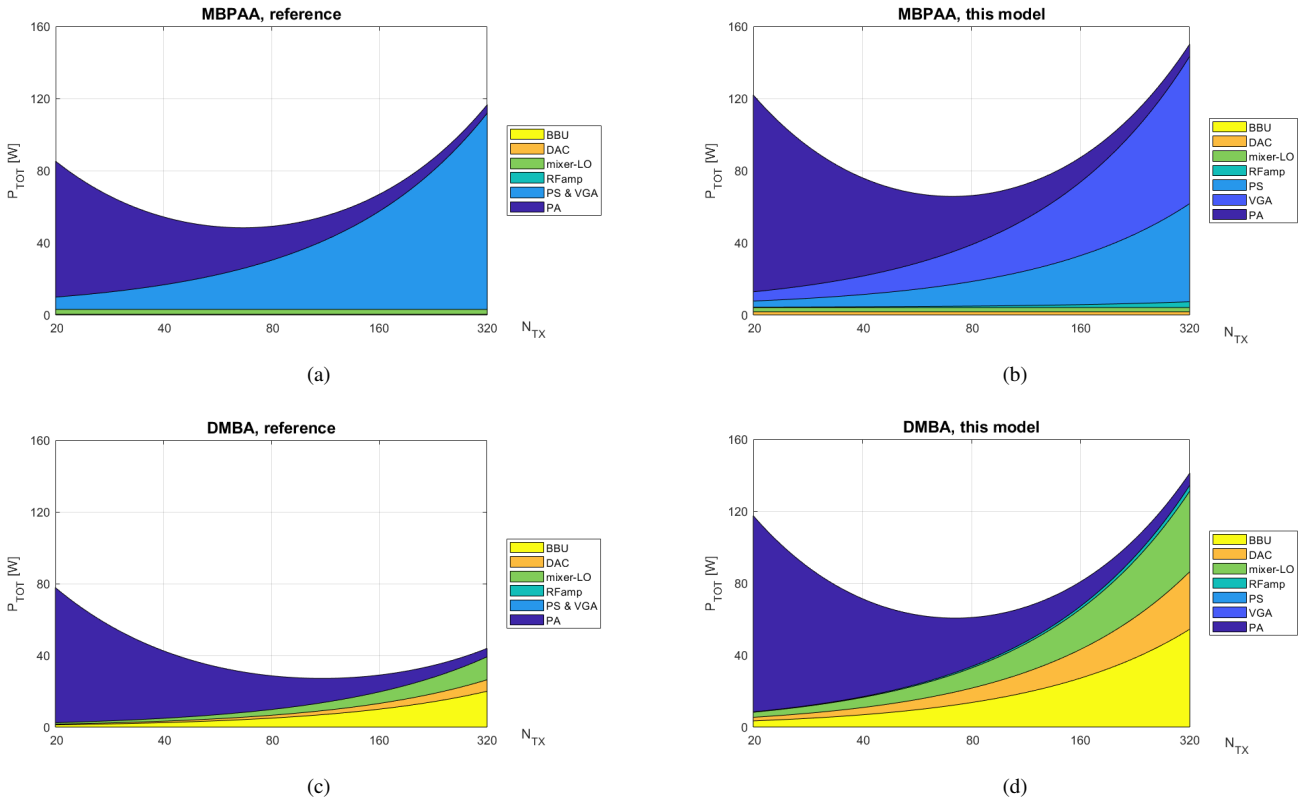

Fig. 4. Component contribution to total power consumption with varying number of antenna elements (17 users, 250 MHz bandwidth, 25% PAE). Since the reference model [2] does not differentiate between the power consumption of the PS and the VGA, it is shown as a combined value.

digital beamforming schemes. The estimated optimal power consumption exceeds the benchmark [2] by 37% for MBPAA and 126% for DMBA architectures, which underscores the need for more low-power and energy-efficient circuits within the telecommunications industry.

Future work will include the incorporation of hybrid beamforming architectures, additional use cases, and varying PA technologies. Open source code will also be provided with the future publication.

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