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Online Fault Detection and Diagnosis in RRAM

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***Abstract*—Resistive Random Access Memory (RRAM, or ReRAM) is a promising memory technology to replace Flash because of its low power consumption, high storage density, and simple integration in existing IC production processes. This has motivated many companies to invest in this technology. However, RRAM manufacturing introduces new failure mechanisms and faults that cause functional errors. These faults cannot all be detected by state-of-the-art test and diagnosis solutions, thus leading to slower product development and low-quality products. This paper introduces a design-for-test (DFT) based on a parallel-multi-reference read (PMRR) circuit that can detect all RRAM array faults. The PMRR circuit replaces the standard sense amplifier and compares the cell's state to multiple references during one read operation. Thus, it can be used as a DFT scheme and a normal read circuit at once. This allows for speeding up production testing and the online detection of faults. Furthermore, the circuit is extendable so that more references can be compared, which is required for efficient diagnosis. Finally, the references can be adjusted to maximize the production yield. The circuit outperforms state-of-the-art solutions because it can detect all RRAM faults during diagnosis, production testing, and during its application in the field while minimizing yield loss.**

***Index Terms*—RRAM, ReRAM, Fault, Test, Diagnosis, DFT**

I. INTRODUCTION

Resistive Random Access Memories (RRAMs) are a promising memory technology to replace Flash memories because of their low energy consumption, low latency, dense structure, and simple integration into existing production processes [1, 2]. RRAMs store data as resistance, rather than as charge and thus are non-volatile. Because of these benefits, many companies, such as TSMC, Weebit-Nano, and Fujitsu, are developing prototypes and products that use RRAMs. Besides these positive characteristics, there are also negative ones. RRAM devices suffer from resistive variations, even when employed in the field, which limit their reliability [3]. Furthermore, these devices suffer from new manufacturing defects and failure mechanisms that cannot be detected by standard memory test solutions [4–6]. Therefore, to guarantee high-quality, reliable RRAMs, new test solutions are required.

Several papers have addressed the testing of RRAMs. The proposed solutions can be divided into (simpler) march algorithms [7–9], and more specialized design-for-test (DFT) solutions [10–12]. Examples of march algorithms for RRAMs are: March-MOM [7], March-C*-1T1R [8], and March-W-1T1R [9]. These algorithms are able to detect conventional memory faults, but they are unable to detect unique RRAM faults, such as undefined state faults. To detect these unique faults, DFT schemes are employed, such as Weak Write operations [10], On-Chip Sensor [11], and DFT-HR-ET-NOR^N [12]. These DFTs are able to detect some unique RRAM faults, but they cannot guarantee the detection of all of them, or they can only do this at a high cost. For example, the intermittent undefined state fault (IUSF) [5] only occurs intermittently, and hence it cannot be guaranteed to be neither detected by the Weak Write, nor by the DFT-HR-ET-NOR^N DFTs. The On-chip sensor may detect it, but this DFT requires many transistors per cell in combination with multiple read operations, which is prohibitively expensive. Furthermore, it is important that DFTs can be calibrated after manufacturing, in order to guarantee the highest detection rates possible while minimizing yield loss. The above problems also limit the application of these DFTs for diagnosis purposes, since they cannot detect any fault at any time. Clearly, there is no test solution for RRAMs that detects all array faults in an efficiently.

This paper presents a novel, easily trimmable DFT based on a parallel-multi-reference read (PMRR) circuit to detect all RRAM array faults. The circuit replaces a standard sense amplifier (SA) that only compares one input against one reference at a time. Instead, the proposed DFT scheme compares the input against multiple references simultaneously and can thus detect the faults. The circuit can do this during diagnosis and yield learning, during manufacturing test, as well as online (i.e., in the field). Furthermore, the references can be tuned so that the circuit performs optimally with minimal yield loss. In short, the contributions of this paper are:

- Proposes an RRAM parallel-multi-reference read (PMRR) circuit that guarantees the detection of all RRAM array faults, both during diagnosis or manufacturing test and online.
- Implements the circuit, validates it, and shows that it outperforms the state of the art.
- Demonstrates that the circuit can be adjusted for high-quality diagnosis and to maximize yield.

The remainder of this paper is organized as follows. Section II presents background information on RRAMs. Section III discusses RRAM faults and existing test solutions to detect them. Section IV presents the proposed DFT. Section V validates the DFT and uses it to develop a test for RRAM. Section VI demonstrates how the DFT can be adjusted for optimal yield and high-quality diagnosis testing. Section VII discusses the work. Finally, Section VIII concludes the paper.

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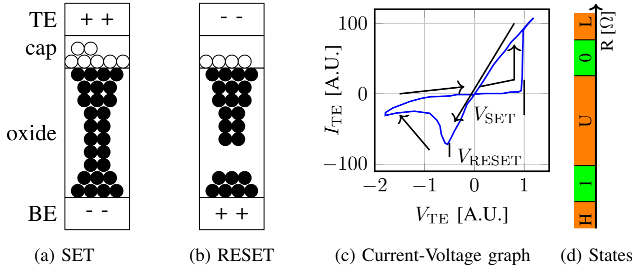
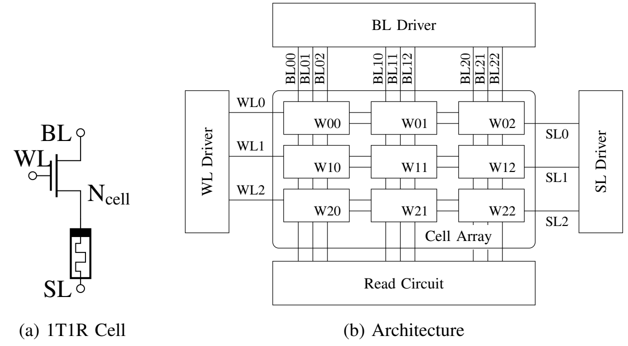


(a) SET (b) RESET (c) Current-Voltage graph (d) States

Fig. 1: RRAM CF and switching.



(a) 1T1R Cell (b) Architecture

Fig. 2: RRAM cell and architecture.

II. Background

This section introduces the RRAM devices and architecture.

A. RRAM Device

An RRAM device is a sandwich-like structure of an oxide (OxRAM) between two metallic electrodes (bottom (BE) and top (TE)), or between an electrode and a capping (cap) layer, as shown in Fig. 1a. When a positive voltage is applied to the TE with respect to the BE, the bond between the oxygen and metal ions can break [13–15]. The oxygen ions are then attracted towards the TE into the capping layer, leaving behind a chain of oxygen vacancies. This chain can conduct high currents and is called a conductive filament (CF). The CF does not dissolve when no voltage is present, making the device non-volatile. When a negative voltage is applied to the TE, the oxygen ions move back from the capping layer into the oxide and break the CF, as shown in Fig. 1b. In this case, less current can flow through the CF, and the resistance of the device increases. The low resistive state (LRS) is called the SET state or logical '1', while the high resistive state (HRS) is called the RESET state or logical '0'. This switching process is illustrated in Fig. 1c. The figure shows that when $V_{TE} > V_{SET}$, the CF forms and the resistance of the device decreases, while when $V_{TE} < V_{RESET}$, the CF is dissolved and the resistance increases again. The shape of the CF determines the device resistance, e.g., a long and wide CF will have a low resistance, while a short and thin CF will have a high resistance.

The CF will have a different shape every time that it is grown or dissolved, leading to cycle-to-cycle variations [16]. Furthermore, the CFs in different RRAM devices also behave differently, leading to device-to-device variations. Hence, the resistance of the RRAM device will vary in every cycle and in every device. For this reason, resistance ranges are determined that correspond to a certain logical value, as shown in Fig. 1d. The figure shows that there are three additional states next to '1' and '0', being: extreme high conductance ('H'), extreme low conductance ('L'), and the undefined state ('U') between '1' and '0'. These states are undesired, because it is difficult to switch back from them ('H' and 'L'), or because the difference between '1' and '0' cannot be reliably detected ('U').

B. RRAM Architecture

RRAMs use RRAM devices in a memory cell to store data. Fig. 2a shows a typical 1T1R memory cell that is comprised of one transistor (1T) and one RRAM device (1R). In this figure, BL, WL, and SL denote bit line, word line, and select line, respectively. The access transistor is used to control the access to the cell and prevents sneak paths that exist in 1R cells [17]. Three cells are grouped to form words (e.g., W12 in Fig. 2b) which are structured in an array to form a complete RRAM, as shown in Fig. 2b. The cells in the array can be written by applying the appropriate voltages through the WL, BL, and SL drivers, e.g., a '1' can be written to the cell by setting the BL and WL voltage to V_{DD}, and the SL voltage to GND. To read out the contents of a cell, additional read circuits, e.g., sense amplifiers (SAs), are needed that compare the current through a cell with a predefined reference current. If the cell current is higher than the reference, then the SA outputs '1', while it outputs '0' in the other case.

III. RRAM Faults and Test Solutions

This section details faults in RRAM arrays and the state-of-the-art in testing to detect them.

A. RRAM Faults

Manufacturing defects in RRAMs may sensitize many different array faults. Some of these are also seen in traditional memory technologies, such as static RAM (SRAM), and dynamic RAM (DRAM), while some other are unique to RRAM. SRAM and DRAM cells can only store data as '1' or '0', while RRAM cells can store more than that, as shown in Fig. 1d. Some conventional faults in RRAMs are transition faults where the cell fails to switch from '1' to '0' (or '0' to '1'), and incorrect read faults where the SA outputs a wrong value [18]. These faults can typically be easily detected using march algorithms that use regular read and write operations; i.e., the SA is used to determine the state of the cell. These faults are *easy-to-detect* (EtD). Unique RRAM faults are sensitized when the cell is in the 'L', 'U', or 'H' state, due to the analog nature of the CF. These faults cannot always be detected using a march algorithm, because reading a cell in these states may not result in a wrong output. For example, a defect causes a write '1' operation to fail, leading to the cell storing 'U'. When this cell is read, the current may still be high enough so that the SA outputs the expected value. However, the cell is storing a wrong value, which can lead to

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TABLE I: Guaranteed fault detection capabilities of existing tests for RRAM

Name	Type	Detected fault type			
		EtD	HtD U	HtD L/H	HtD NP
March-MOM [17]	March	Y	N	N	N
March-1T1R [20]	March	Y	N	N	N
March C*-1T1R [8]	March	Y	N	N	N
March W-1T1R [9]	March	Y	N	N	N
March-CMOL [21]	March	Y	N	N	N
Weak-write [10]	DFT	N	Y	Y	N
Sneak-path [17]	DFT	Y	Y	Y	N
Fast-write [22]	DFT	Y	N	N	N
Parallel March [23]	DFT	Y	N	Y	N
On-chip sensor [11]	DFT	Y	Y	N	N
Enhanced March [24]	DFT	Y	Y	Y	N
DFT-HR-ET-NOR^{N} [12]	DFT	Y	Y	Y	N

failure later in time. These faults are *hard-to-detect* (HtD) and require additional efforts to be detected. Defects that put the cell into 'L' or 'H' typically occur when the RRAM production process is still in development and thus are important for diagnosis, while defects that relate to the 'U' state also happen in mature processes and may cause *non-permanent* (NP) faults [19]. These faults either occur intermittently, such as the IUSF [5], or are caused by degradation or extreme cycle-to-cycle variations [3].

B. Existing Tests

Existing test solutions for RRAMs can be divided into two types: march algorithms, and a DFT schemes (sometimes combined with march algorithms). Table I lists all these in combination with the type of array faults that each one can guarantee to detect. Note that we have split the HtD faults based on the state of the cell and on its time dependency. From the table, it becomes clear that using a march algorithm without any DFT can never guarantee the detection of all array faults. Hence, they must be combined with a DFT. However, none of the existing DFT schemes can guarantee the detection of NP faults, because they do not monitor the cell states continuously. They may detect some HtD NP faults; for example, if a test is run during the startup of the device, but this approach still misses in-field failures when they occur.

From the above, we can conclude that high-quality RRAM test approaches are needed not only to detect EtD *and* HtD faults during manufacturing test of the device, but also during the operation.

IV. Proposed Parallel-Reference Read Circuit

This section proposes a the general concept of the DFT, and provides its implementation details.

A. Concept

From the previous section, it follows that a high-quality RRAM fault detection circuit must be able to detect cells that store an undesired 'L', 'U', or 'H' state. To detect aging degradation and IUSFs, the faults should also be detected during runtime of the chip.

With these requirements in mind, we propose to replace the standard SA read circuit that can only compare its input against a single reference at a time, with an alternative read circuit that compares its input against q references at once, called a *parallel-multi-reference read* (PMRR) circuit. In this way, $q+1$ different states can be detected using only one read operation. To illustrate this, consider Fig. 1d, when $q=2$ with $I_{\text{ref},1}$ between '1' and 'U', and $I_{\text{ref},2}$ between 'U' and '0', the circuit can distinguish the '1', 'U', and '0' states reliably. This allows the detection of all faults that relate to a cell going into the 'U' state. Furthermore, during diagnosis it is important to also detect the 'L', and 'H' states. Setting $q=4$ allows the detection of all these states. Hence, applying a simple march algorithm while enabling the PMRR DFT will allow easily detect faulty and unreliable RRAMs with final states in 'U', 'L', or 'H'.

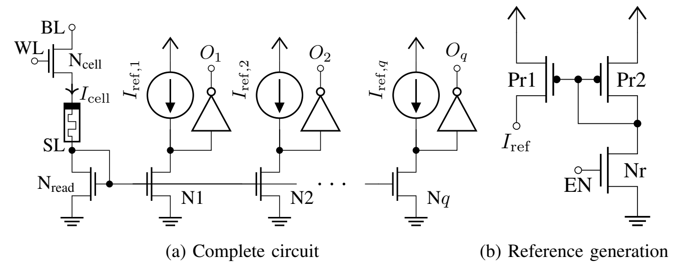

Fig. 3: Parallel-multi-reference read circuit acting as DFT.

B. Implementation

Fig. 3a shows the implementation of the proposed DFT. During a read operation, a current I_{cell} flows through the BL, via the access transistor through the RRAM device into the SL. The current through the SL is copied and it is compared to the references. This current is mirrored via transistor N_{read} to q different branches that each will compare the cell current to a specific reference current $I_{\text{ref},p}, p \in \{1,2,\ldots,q\}$. Each branch is connected to an inverter that drives an output signal O_p. When $I_{\text{ref},p} > I_{\text{cell}}$, the input of this inverter will be close to V_{DD}, so O_p will be set to '0'. Conversely, when $I_{\text{ref},p} < I_{\text{cell}}$, the input of this inverter will be close to GND, so O_p will be set to '1'. Now, the state of the cell can be determined by analyzing all outputs O. The references for all branches are generated using the circuit in Fig. 3b. It comprises a current mirror (Pr1 and Pr2) that mirrors the current through transistor Nr that is controlled by the signal EN. By tuning the length and width of Nr, we can generate the desired reference current.

V. Validation and Test Development

In this section, we validate the PMRR DFT and use it to develop a test for RRAMs.

A. Experimental Setup

To validate the PMRR DFT, we implement one 1T1R cell with write drivers and the proposed read circuit. We use the TSMC $40\,\text{nm}$ $2.5\,\text{V}$ transistor model, and the JART VCM v1b [25] RRAM device model to implement the circuit. The $2.5\,\text{V}$ transistor is required to allow for higher WL voltages during RESET and to allow for the initial CF forming. The circuit is

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TABLE II: Circuit specifications

Parameter	Value
V_{DD}	$1.5\,\mathrm{V}$
V_{read}	$750\,\mathrm{mV}$
$V_{WL,Set/Read}$	$1.8\,\mathrm{V}$
$V_{WL,\,Reset}$	$2.5\,\mathrm{V}$
‘H’	$[0\,\Omega; 1.3\,\mathrm{k}\Omega\rangle$
‘1’	$[1.3\,\mathrm{k}\Omega; 19\,\mathrm{k}\Omega\rangle$
‘U’	$[19\,\mathrm{k}\Omega; 32\,\mathrm{k}\Omega\rangle$
‘0’	$[32\,\mathrm{k}\Omega; 68\,\mathrm{k}\Omega\rangle$
‘L’	$[68\,\mathrm{k}\Omega; \infty\Omega\rangle$
Read time	$60\,\mathrm{ns}$
Set time	$40\,\mathrm{ns}$
Reset time	$7.2\,\mathrm{\mu s}$

TABLE III: Reference settings

Reference	‘H’/‘1’	‘1’/‘U’	‘U’/‘0’	‘0’/‘L’
$q = 2$	–	O_1	O_0	–
$q = 4$	O_3	O_2	O_1	O_0
Resistance [kΩ]	1.3	18.8	32.7	68

simulated in Cadence’s Spectre simulator. Table II lists all the circuit operating conditions.

We perform two experiments. *1) Distinguishing Different RRAM States*: to do this, the resistance of the RRAM device is swept through all states by changing the resistance in the RRAM device model and the resulting output of the DFT is observed. *2) Detecting Resistive Defects*: we validate the DFT’s defect-detecting capabilities by injecting defects into the netlist. We inject resistive defects in the memory cell, one defect at a time, and sweep their defect size (or defect strength) from $100\,\Omega$ up to $100\,\mathrm{M}\Omega$ in 101 logarithmically spaced steps. The injected defects are listed in Fig. 4. Here, an open (Rop) indicates a broken wire that increases the resistance, a bridge (Rbr) indicates a connection between two nodes, and a short (Rsh) indicates a connection between a node and V_{DD} or GND. Because faults in the circuit can only be detected by a read operation, we only apply sensitizing sequences that end in a read operation. We apply all applicable sensitizing sequences up to two operations [18], i.e., 0r0, 1r1, 0w0r0, 1w0r0, 0w1r1, 1w1r1, 0r0r0, and 1r1r1. We compare an ideal SA where the reference is set directly between the ‘1’ and ‘0’ states, with two configurations of the read circuit, i.e., for $q = 2$, and for $q = 4$. Table III lists the reference settings for both configurations. ‘Reference’ indicates the position of the reference, e.g., to distinguish between ‘H’ and ‘1’, the reference resistance needs to be set to $1.3\,\mathrm{k}\Omega$. Note that O_0 and O_1 for $q = 2$ correspond with O_1 and O_2 for $q = 4$, respectively.

B. Results

Next, we discuss the validation results.

1) Distinguishing Different RRAM States: Fig. 5 shows the output of the PMRR circuit for $q = 4$ for increasing cell resistance R_{mem}. The results for $q = 2$ are equal, if we only look at O_1 and O_2. The figure shows that the outputs of the circuit switch from V_{DD} to GND at the correct resistances and that every state can be uniquely identified. This proves that for $q = 2$, all RRAM faults related to the ‘U’ state can be detected and that for $q = 4$, all RRAM array faults can be detected.

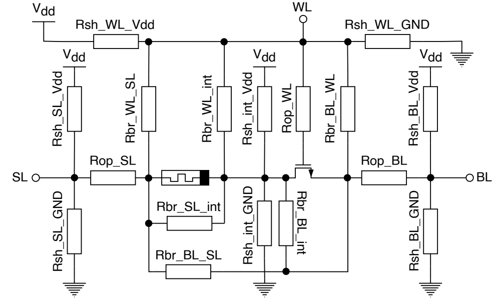

Fig. 4: Defects injected in 1T1R cell

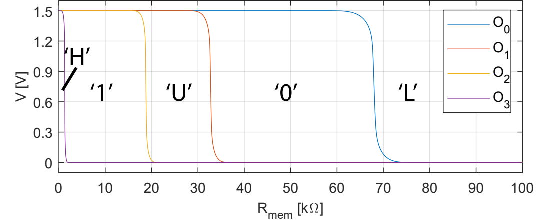

Fig. 5: Distinguishing different resistance states for $q = 4$

2) Detecting Resistive Defects: Table IV presents the results from the defect coverage comparison for the regular SA, the PMRR DFT with $q = 2$, and the PMRR DFT with $q = 4$. It lists the number of covered defect sizes per defect (i.e., the number of values from the range $100\,\Omega$ up to $100\,\mathrm{M}\Omega$) that can be detected, the sensitization sequences that are required to obtain that, and in the case of the proposed read circuit, the achieved improvement compared to the regular SA design. Note that the sensitization sequences may be grouped using an ‘;’ or an ‘&’ symbol. The former indicates that any of the sequences sensitizes faults for the listed number of defect sizes, and the latter indicates that all sensitizing sequences are needed to sensitize faults for all listed defect sizes.

We observe that both versions of the PMRR circuit are able to sensitize faults for more defect sizes than a regular SA; the PMRR DFT with $q = 2$ improves the defect coverage with $3.92\,\%$, while the PMRR DFT with $q = 4$ improves the defect coverage with $14.79\,\%$. This is due to the fact that the detection of every fault that puts the cell into the ‘U’ state is guaranteed. For example, the short defect Rsh_int_Vdd makes it harder to reset the cell (i.e., to write ‘0’ to the cell), thus resulting in many write failures where the cell ends up in ‘1’ or ‘U’ instead of ‘0’. For low resistances of the short, a subsequent read operation will result in more current flowing, leading to a wrong output value. However, when the resistance increases, the current from the defect decreases and the resulting read current falls into the ‘U’ state, but below the reference for a regular SA, thus leading to an escape of the defect. Now, the proposed PMRR circuit is able to detect that the current is in the ‘U’ range, and thus will detect it. Interestingly, the same defect sensitizes even more faults for $q = 4$ when the cell contains a ‘1’. In this case, the short adds additional current to the read operation, causing the read circuit to output ‘H’,

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TABLE IV: Comparison of defect coverage for a normal SA, the proposed PMRR DFT with $q = 2$, and the proposed PMRR DFT with $q = 4$.

Defect	Regular SA		Proposed PMRR DFT with $q = 2$			Proposed PMRR DFT with $q = 4$		
	#Defect sizes [–]	Sensitization	#Defect sizes [–]	Improvement [%]	Sensitization	#Defect sizes [–]	Improvement [%]	Sensitization
Rop_BL	83	1w0r0	84	1.20	1w0r0	84	1.20	1w0r0
Rop_SL	82	1w0r0	82	0.00	1w0r0	82	0.00	1w0r0
Rop_WL	53	0w1r1	54	1.89	0w1r1	54	1.89	0w1r1
Rbr_BL_int	0	–	0	–	–	36	∞	1w1r1; 0w1r1
Rbr_BL_SL	48	0r0; 1w0r0; 0r0r0	51	6.25	0r0; 1w0r0; 0r0r0	51	6.25	0r0; 1w0r0; 0r0r0
Rbr_BL_WL	35	0w1r1 & 1w0r0	38	8.57	0w1r1 & 1w0r0	38	8.57	0w1r1 & 1w0r0
Rbr_SL_int	47	1w0r0	51	8.51	1w0r0	51	8.51	1w0r0
Rbr_WL_int	50	1w0r0	52	4.00	1w0r0	53	6.00	1w1r1
Rbr_WL_SL	62	0r0; 1w0r0; 0r0r0	65	4.84	0r0; 1w0r0; 0r0r0	65	4.84	0r0; 1w0r0; 0r0r0
Rsh_BL_GND	25	1r1; 1w1r1; 0w1r1; 1r1r1	27	8.00	1r1; 1w1r1; 0w1r1; 1r1r1	42	68.00	0w0r0
Rsh_BL_Vdd	33	1w0r0	35	6.06	1w0r0	35	6.06	1w1r1
Rsh_int_GND	47	0w1r1	48	2.13	0w1r1	57	21.28	0w0r0
Rsh_int_Vdd	47	1w0r0	49	4.26	1w0r0	51	8.51	1w1r1; 0w1r1
Rsh_SL_GND	45	1r1; 1w1r1; 0w1r1; 1r1r1	47	4.44	1r1; 0w1r1; 1r1r1	70	55.56	0w0r0
Rsh_SL_Vdd	60	0r0; 1w0r0; 0r0r0	63	5.00	0r0; 1w0r0; 0r0r0	63	5.00	0r0; 1w0r0; 0r0r0
Rsh_WL_GND	45	0w1r1	46	2.22	0w1r1	46	2.22	0w1r1
Rsh_WL_Vdd	29	0w1r1	30	3.45	0w1r1	30	3.45	0w1r1
Total	791	–	822	3.92	–	908	14.79	–

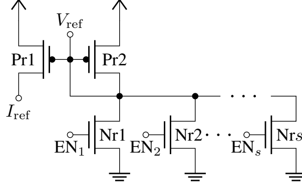

Fig. 6: Adjustable reference generation

instead of '1', which detects the defect.

C. Test Development

Next, we develop a test using both versions of the PMRR DFT that detects as many defect sizes as possible while minimizing test time. Note that to detect all defects for all sizes, every sensitization sequence in Table IV needs to be included in a test, unless multiple sequences sensitize the same faults. In that case, only one of the sequences needs to be included in the test. Based on this statement, we can observe that the following set of sensitizing sequences is required when $q = 2$: $\text{S}_{q=2} = \{1\text{w}0\text{r}0, 0\text{w}1\text{r}1\}$. These sequences can be combined in a march algorithm as follows:

$$\text{March-PMRR}_{q=2} = \Updownarrow(\text{w}0)\,; \Updownarrow(\text{w}1, \text{r}1)\,; \Updownarrow(\text{w}0, \text{r}0)\,; . \quad (1)$$

Here, $\Updownarrow$ indicates addressing in any order, wy, $y \in \{0, 1\}$ indicates a write operation, and ry, $y \in \{0, 1\}$ indicates a read operation. Similarly, when $q = 4$: $\text{S}_{q=4} = \{1\text{w}0\text{r}0, 0\text{w}1\text{r}1, 1\text{w}1\text{r}1, 0\text{w}0\text{r}0\}$. Note that this set is different from $\text{S}_{q=2}$, because different sensitizing sequences are required to sensitize all defect sizes, cf. Rsh_SL_GND. This results in the following march algorithm:

$$\begin{aligned}\text{March-PMRR}_{q=4} = &\Updownarrow(\text{w}0)\,; \Updownarrow(\text{w}0, \text{r}0)\,; \\ &\Updownarrow(\text{w}1, \text{r}1, \text{w}1, \text{r}1)\,; \Updownarrow(\text{w}0, \text{r}0)\,; .\end{aligned} \quad (2)$$

VI. Circuit Adjusting

From the previous section, it became clear that the PMRR is a suitable solution to detect all RRAM array faults. Unfortunately, variations in the production process may introduce a mismatch in the current mirrors, which reduces the accuracy of the circuit and may lead to yield loss. To mitigate the mismatch we propose to make the reference generator trimmable so that it can be adjusted and calibrated. This can be done by adding additional NMOS transistors in the reference generation circuit, as shown in Fig. 6. Here, s parallel transistors Nrr, $r \in \{1, 2, \ldots, s\}$ generate I_{ref}. Each of these can be controlled separately through signals ENs. The dimensions of every transistor are selected so that the current through every next transistor is doubled with respect to the previous one. This allows setting the reference current with a binary code with a precision of s bits. Now, the reference can be precisely trimmed (for every q), e.g., using a high-precision current source, and the binary code can be stored on the chip so that it can be used in every reference generation circuit on the chip. Note that this trimming needs to be done only once directly after manufacturing the RRAM.

The adjustability of the reference generation circuit is also useful for diagnosis purposes as it allows one to determine the exact resistance of a cell. To do this, a binary search can be performed over all s bits as follows. First, the cell is read while only the largest transistor Nrr ($r \in \{1, 2, \ldots, s\}$) is enabled. If the corresponding output O_q switches to V_{DD}, then the current through the RRAM device is higher than the reference current and thus Nrr needs to be enabled. In the other case, the current is lower and Nrr needs to be disabled. This process is repeated for the other transistors from the largest to the smallest transistor. When the search is completed, the resistance of the device can be determined with high precision.

VII. Discussion

Next, we compare the proposed PMRR DFT with other test solutions, elaborate on the application for other memory technologies, and discuss its drawbacks and limitations.

A. Comparison with the State of the Art

1) Detection Capabilities: Table V presents the detection capabilities of all RRAM tests and compares them with PMRR DFT. It can be seen that the proposed PMRR DFT is the only one that guarantees the detection of all RRAM array faults when $q = 4$. The circuit can read out all states in a single read operation, while the other DFTs cannot.

2) Cost: The last column of Table V lists the transistor usage of all test solutions. Here, R denotes the number of rows in the memory, and C denotes the number of columns.

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TABLE V: Comparison of the proposed PMRR DFT with state of the art

Name	Type	Detected fault type				Area overhead [transistors]
		EtD	HtD U	HtD L/H	HtD NP	
March-MOM [17]	March	Y	N	N	N	-
March-1T1R [20]	March	Y	N	N	N	-
March C*-1T1R [8]	March	Y	N	N	N	-
March W-1T1R [9]	March	Y	N	N	N	-
March-CMOL [21]	March	Y	N	N	N	-
Weak-write [10]	DFT	N	Y	Y	N	$24 + 18R$
Sneak-path [17]	DFT	Y	Y	Y	N	$28 + 26R$
Fast-write [22]	DFT	Y	Y	Y	N	$50 + 18R$
Parallel March [23]	DFT	Y	N	Y	N	-
On-chip sensor [11]	DFT	Y	Y	N	N	$20RC$
Enhanced March [24]	DFT	Y	Y	Y	N	26
DFT-HR-ET-NOR^N [12]	DFT	Y	Y	Y	N	$2\log_2 R + 96 + 4C$
PMRR ($q = 4$) [this work]	DFT	Y	Y	Y	Y	$13C$

The PMRR comprises 25 transistors per column for $q = 4$, but as it replaces the regular SA consisting of 12 transistors, its area overhead is only $13C$. From the table, it follows that only Parallel March and Enhanced March have a lower area overhead than the PMRR DFT.

B. Application to other Memory Technologies

The proposed PMRR DFT can also be applied to test other memory technologies. For example, it is shown that an intermediate state between '1' and '0' exists in spin-transfer torque magnetic RAM [26, 27]. The PMRR DFT can detect this state as well and thus is a suitable test solution.

C. Drawbacks and Limitations

The PMRR circuit also faces some drawbacks and limitations that relate to its design and operating conditions. To design the circuit, every transistor needs to be specifically designed. Conversely, in a regular SA, there is symmetry and many transistors can be equally sized. Hence, the design effort of the PMRR circuit is higher. Furthermore, the usage of current mirrors introduces a voltage loss over the copying transistors that requires increasing the operating voltages, and thus energy consumption. Finally, the performance of the current mirrors may degrade due to process variations and temperature shifting. This can be partially mitigated by adjusting the circuit, as described in Section VI.

VIII. Conclusion

This paper proposed a novel PMRR DFT that can guarantee the detection of all array faults that exist in RRAMs. It replaces a regular SA with a circuit that compares the stored state of a cell to multiple references at once. This allows for fast and efficient detection and diagnosis of faults not only during production testing but also in the field. We demonstrated the superiority of our solution compared to prior work. Furthermore, the circuit can be adjusted to compensate for process variations and to optimize the diagnosis process.

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