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A 6GHz Multi-Path Multi-Frequency Chopping CTΔΣ Modulator achieving 122dBFS SFDR from 150kHz to 120MHz BW

Sundeep Javvaji[1], Muhammed Bolatkale[1,2], Shagun Bajoria[2], Robert Rutten[2], Bert Oude Essink[3], Koen Beijens[2], Kofi Makinwa[1], Lucien Breems[1,2]

[1]Delft University of Technology, Delft, [2]NXP Semiconductors, Eindhoven, [3]NXP Semiconductors, Delft, The Netherlands

Abstract

Advances in CMOS technologies have led to the development of continuous-time ΔΣ modulators (CTDSMs) with GHz sampling rates that achieve better than -100dBc linearity and bandwidths above 100MHz. However, at low frequencies (below ~10 MHz), their SNDR is limited by 1/*f* noise, which limits their use in radio receivers intended to cover both the AM and the FM bands. In this work, a multi-path multi-frequency chopping scheme is proposed to suppress 1/*f* noise, while maintaining interferer robustness, noise, spurious, and linearity performance. Implemented in a CTDSM sampling at 6GHz, it reduces its 1/*f* noise corner frequency by 22x and achieves -98.3dBc THD, 122dBFS SFDR in 120MHz BW.

Introduction

Fig. 1 shows the simplified architecture of the proposed wideband CTDSM, which employs a 4th order loop filter based on two resonators in a CIFF architecture and a 2b quantizer. For high-linearity, DAC mismatch and quantizer offset are digitally calibrated [1]. To achieve the targeted 120MHz BW, the input devices of the input stage are quite small, and so suffer from significant 1/*f* noise. This can be mitigated by chopping the 1st stage, as shown in Fig. 2. Due to its finite gain, however, its input and output voltages will contain significant amounts of the quantization-noise (Q-noise) present in the DAC output. At each chopping transition, as shown in Fig. 3, the voltage across the parasitic capacitors C_g and C_p is inverted, causing impulsive charge transfer that effectively samples, and thus folds down, Q-noise at multiples of $2f_{ch}$ [3]. Since Q-noise has notches at multiples of f_s, such folding can be avoided by chopping at $f_s/2$ or f_s [2]. At GHz frequencies, however, the parasitic switched capacitor (SC) resistors formed by chopping C_g and C_p are a significant problem. The input SC resistor increases the inverter's input-referred voltage noise (by 3dB with f_s chopping), while the output SC resistor reduces its DC gain, by 15dB with f_s chopping), which degrades modulator linearity and causes NTF peaking. Alternatively, an N-tap FIR DAC can be used to creates Q-noise notches at multiples of f_s/N, thus allowing the input stage to be safely chopped at multiples of f_s/2N [3]. However, since these notches are only in the feedback path, chopping will still fold down interferers near multiples of f_s/2N, thus degrading interferer robustness.

Proposed Chopping Technique

As shown in fig. 4, multi-path chopping is an alternative way of reducing chopping artifacts [4]. For example, three input stages can be chopped by interleaved clocks at $f_s/6$ whose edges are delayed by $1/f_s$ with respect to each other. This ensures that each sampling period only contains *one* chopping clock edge. The sampled sequence Ve[n] due to chopping will then consist of identical samples at $f_s/2$, and thus, like chopping at $f_s/2$, will not cause Q-noise folding. Furthermore, the parasitic capacitance of each inverter, and thus, the associated artifacts, will now be 3x smaller than those of a single equivalent inverter. However, any mismatch between the paths, either due to parasitic capacitor mismatch or clock skew, will result in Q-noise sub-sampling and, thus, some residual noise folding. As shown in Fig. 4, one mismatched inverter, for example, will cause one out of every three samples to be different, resulting in the folding of quantization noise and interferers near multiples of f_s//3.

This work proposes a mismatch-robust multi-path chopping scheme based on the observation that Q-noise folding will not occur if only one chopping edge occurs in every sampling period; and that this edge can be in *any* of the paths. For example, noise folding will not occur if one inverter is chopped at $f_s/2$ while the other two are not. However, this will not mitigate the 1/*f* noise of the other two inverters. In this work, they are also chopped, but at a lower frequency ($f_s/26$) so that their 1/*f* noise is just modulated outside the signal band, where it can be removed by the decimation filter. As shown in Fig. 4, the remaining inverter is then chopped by a modified $f_s/2$ clock, which ensures that only one chopping edge occurs in every sampling period. As a result, most of the chopping edges, and thus the associated Q-noise sampling, occur in this path. Compared to a single frequency 3-path scheme, this significantly reduces the rate at which mismatch-related sampling errors occur. For example, mismatch in one of the slow-chopped inverters will now cause errors once every 13 samples, instead of once every 3 samples. This will then fold down noise near multiples of $f_s/13$, where there is much less Q-noise than at $f_s/3$.

Measurement Results and Performance Summary

The prototype CTDSM is designed and fabricated in a 28nm CMOS process (Fig. 5) with an active area of 0.15mm^2. Fig.6 shows the measured in-band PSD with chopper OFF and chopper ON, for different chopping modes. Without chopping, the 1/*f* noise corner is at 7.8MHz, which drops to 350kHz after 3-path chopping. Chopping at $f_s/2$ increases the thermal noise floor by 1.3dB due to the input SC resistor. Single-frequency 3-path chopping limits the SFDR to 113.4dBFS due to path mismatch and the associated Q-noise folding. The proposed multi-frequency 3-path chopping improves this significantly to 122dBFS in a BW from 150kHz to 120MHz, enabling high quality narrow-band radio reception over multiple frequency bands including AM.

Fig. 7 shows the level of the in-band folded tones caused by interferers at various frequencies with single-frequency and multi-frequency 3-path chopping. Mismatch in one of the paths will fold down interferers at multiples of $2f_{ch}$. With single-frequency 3-path chopping, this will occur at multiples of $f_s/3$, while with multi-frequency chopping, this will occur at multiples of $f_s/13$, although the associated folding level around ($f_s/13$) and 2*($f_s/13$) is now 19dB lower. Measurements show that, compared to single-frequency chopping, multi-frequency chopping reduces the worst-case folding levels by 9.4dB as shown in Fig. 8. Measurements over 6 different chips show an average improvement of 9dB, as shown in Fig.9.

The linearity of the CTDSM is measured with both single-tone (0dB at 38MHz) and two-tone (-6dB at 88 & 94MHz) input signals, as shown in Fig. 10 and 11. The overall power

consumption of the CTDSM is 115mW. The measurement results are summarized and compared in Table. I. The proposed multi-path multi-frequency chopping CTDSM achieves an SFDR of 122dBFS in the widest reported BW of 120MHz.

Acknowledgments: Paul Swinkles, NXP layout team.

References

[1] M. Bolatkale, *et.al., ISSSC*, 2023 [2] P. Cenci, *et.al., ESSCIRC, 2023.*
[3] S. Billa, *ISSCC, 2016.* [4] Y. Kusuda, *ISSCC, 2015.*

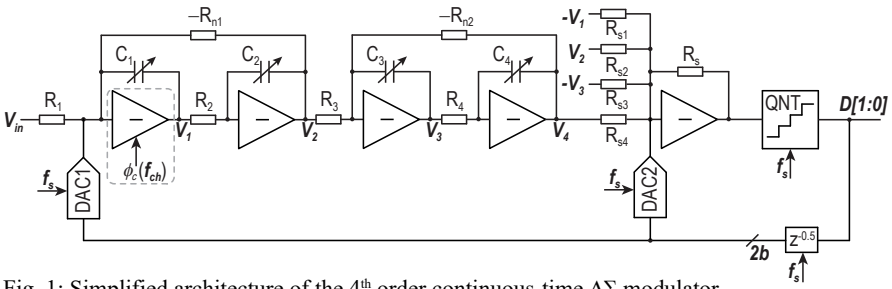

Fig. 1: Simplified architecture of the 4th order continuous-time ΔΣ modulator (input feed-ins are not shown).

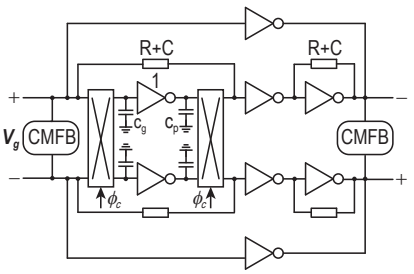

Fig. 2: First amplifier with chopped input stage.

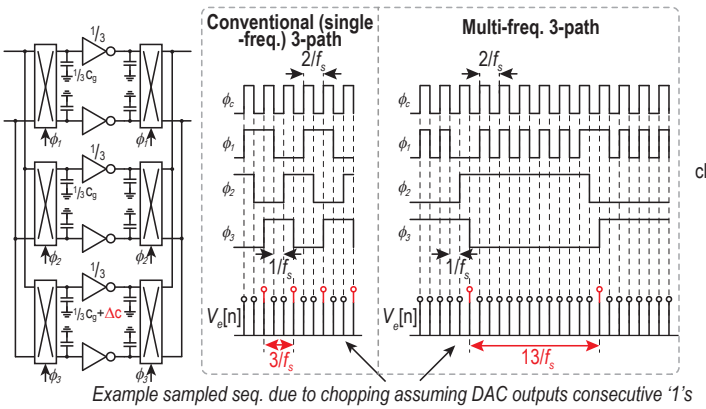

Fig. 4: Amplifier's first stage with a three path chopper. Conventional and proposed multi-frequency 3-path clocks.

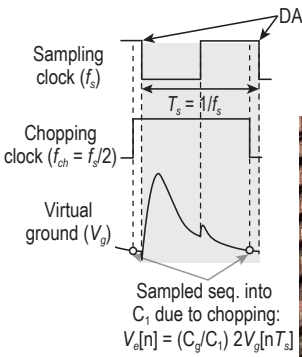

Fig. 3: Sampled sequence due to chopping.

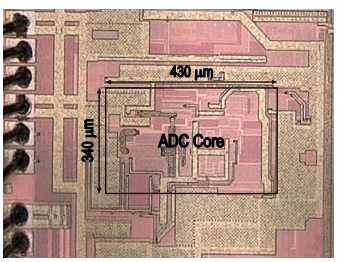

Fig. 5: Chip micrograph.

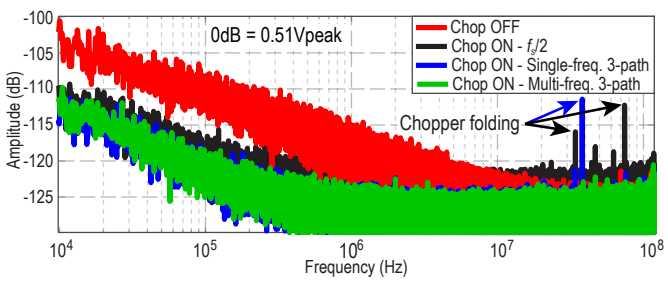

Fig. 6: Measured in-band spectra with chopper ON and OFF w/o input signal (RBW=53Hz).

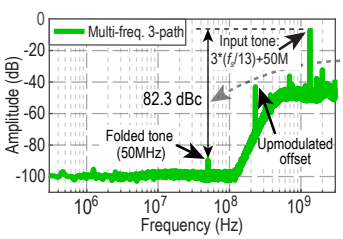

Fig. 7: Measured spectrum with out -of-band interferer (RBW=10kHz).

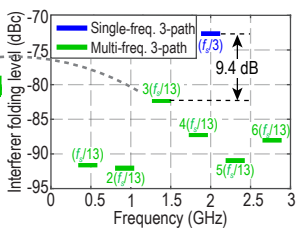

Fig. 8: Measured interferer folding level.

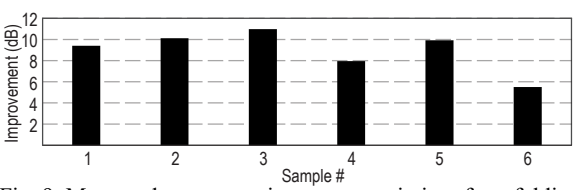

Fig. 9: Measured worst case improvement in interferer folding.

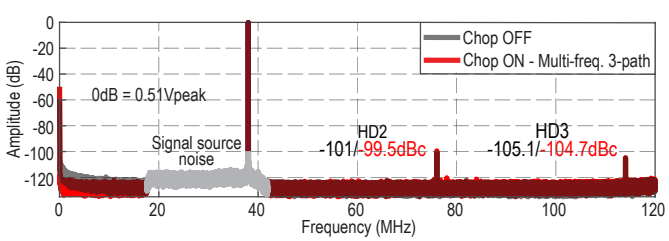

Fig. 10: Measured output spectrum of a 0.51V (-2dBFS), 38MHz input signal (RBW=53Hz).

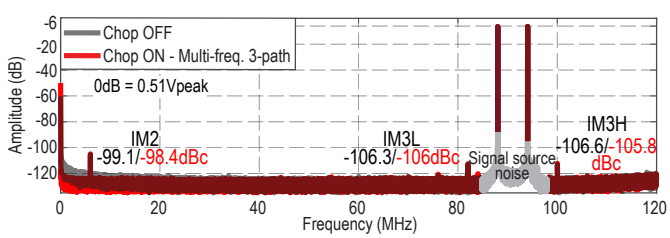

Fig. 11: Measured output spectrum of a two-tone input signal of -8dBFS (=-6dB) at 88MHz & 94MHz (RBW=53Hz).

	This work				[2]	[3]
Technology (nm)	28				28	180
Sampling freq. (MHz)	6000				2000	6.144
Quantizer bits	2				2	1
DAC	Dual RTO				Dual RTO	12-tap FIR
Bandwidth (MHz)	120				30	0.024
Chopping mode	Multi freq. 3-path	Single freq. 3-path	1-path	Chop OFF		
Chopping freq. (MHz)	$f_s/26, f_s/2$	$f_s/6$	$f_s/2$	-	f_s	$f_s/24$
Peak SNDR (dB)	72.8	72.7	69.4	71.8	78.5	98.5
SFDR (dBFS)	122.0(2)	113.4(2)	114.2(2)	112.0(2,3)	122.0	107.6
THD (dBc)	-98.3	-98.3	-97.0	-99.6	-104.7	-107.4
NSD (nV/√Hz)	11.0	11.1	12.9	13.0	9.7(1)	58.5(1)
SNDR in 30MHz AM band (dB)	78.9	78.8	75.7	75.5	-	-
DR (dB)	73.4	73.3	70.0	73.0	80.1	103.6
Power (mW)	115.0	115.0	117.2	113.3	61.4	0.28
FoM Schreier (dB)	163.0	162.9	159.5	162.1	165.4	177.8

[1]Calculated from the paper. [2] SFDR is excluding harmonic distortion in a BW from 150kHz to 120MHz.
[3] Limited by FFT resolution

Table I: Performance comparison.