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***Abstract*—For quantum computing modules using diamond color centers, we propose an integrated structure of a quantum chip with photonic circuits and an interposer with electric circuits. The chip and interposer are connected via gold stud bumps using flip-chip bonding technology. For evaluating the proposed integrated structure, we bonded a test chip of 15 × 15 mm^2, corresponding to the area that allows the allocation of color center qubits in the order of 10^2, with an interposer of 20 × 20 mm^2, including test measurement lines. We confirm all connections of 16 lines with two bumps for each line at 10 K. The resistance of the lines with two bumps at 10 K is ~3.5 Ω. These resistances are mainly attributed to the gold lines on the interposer, which is confirmed by simulations. The shear strength of the flip-chip bonded structure is ~67 g/bump. It is larger than that of previous reports where the chips passed the standard temperature cycle test. Moreover, we integrate the flip-chip bonded structure with a printed circuit board (PCB). We confirm a connection between the connector terminal of the PCB and the test chip at 80 K. It is shown that the integrated structure using gold stud bumps has a potentially highly reliable connection at cryogenic temperature. These results will lead to realizing large-scale diamond spin quantum processors.**

Keywords—Quantum computer, Diamond color center, Cryogenic integration, Flip-chip bonding

I. Introduction

Quantum computers can solve complex problems that classical computers cannot calculate efficiently. The solid-state color-center spin qubits in diamonds have attracted vast attention as a qubit platform because of their long coherent time that is sufficient for quantum gate operations and realizing long-range entanglement using optical photons [1]-[4]. The basic functions required for universal quantum computation have been demonstrated in a few color centers [5]. The spin qubits are controlled via optical photons, microwaves, and magnetic fields at cryogenic temperatures of 10 K or below.

However, a chip integration technology must be developed to scale up the diamond spin quantum system [6]. A photonic circuit layer with qubits and an electrical circuit layer for irradiating magnetic fields and microwaves must be integrated vertically for efficient field coupling. Furthermore, the chip size must be relatively large for a practical large-scale quantum system. A stable flip-chip integration technology compatible with such conditions must be developed instead of previously reported solder bumps [7], [8], which are unstable owing to the melting process of solders, with limited postprocessing for solid-state color centers spin qubits.

Herein, we investigated the flip-chip bonding for quantum chips operating at cryotemperatures. We reveal that gold (Au) stud bumps are suitable for this purpose in terms of uniformity and stability. We also demonstrate the integration of those chips with PCBs.

II. Cryogenic Integration for Color Center Spin Qubits in Diamonds

A schematic of the integration for the solid-state color center spin qubits is shown in Fig. 1. We propose an integrated structure for quantum processors using the color center qubits in diamond. A quantum photonic chip consists of spin qubits in a diamond and a photonic circuit layer chip with optical waveguides, photonic switches for routing, and beam splitters for photon entanglement. The photonic waveguides are connected to lensed fibers at the edge of the chip to control the optical transitions of the color centers and detect single-photon signals. The optical fibers are connected to excitation lasers or single-photon detectors at the external equipment. An interposer consisting of antennae for irradiating microwave, magnetic fields, and electrical fields is placed under each spin qubit for controlling spin qubit transitions independently. Electrical input

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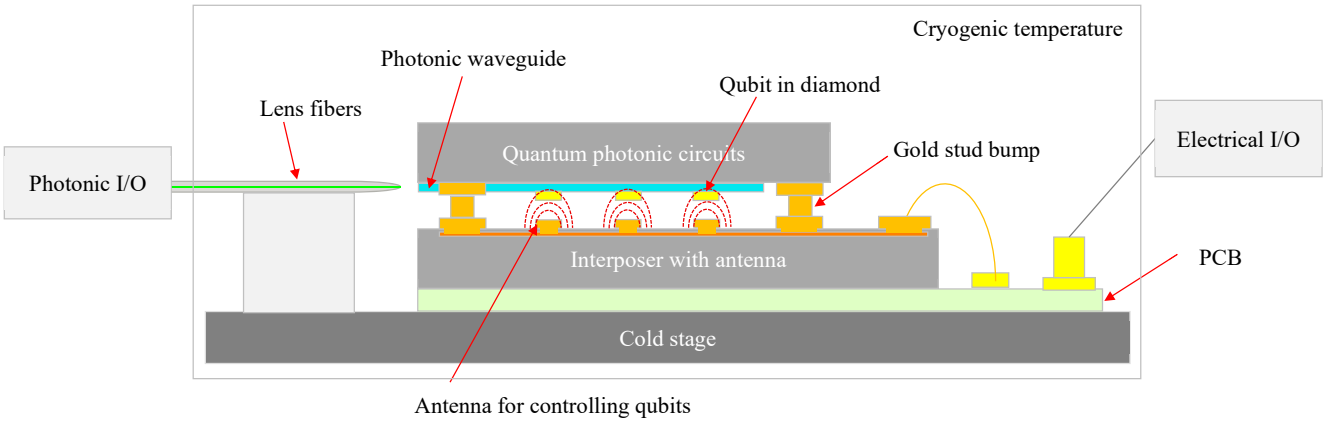


Fig. 1. Fabrication process of the test Si chip on the interposer.

and output between the external electrical controllers and the interposer are connected using a PCB with bonding wires.

The proposed layout allows us to inspect the quantum chip with photonic circuits and the interposer with electric circuits separately, which easily ensures the manufacturing yield of each component. Moreover, it has the potential for further integration of cryogenic-complementary metal oxide semiconductor (cryo-CMOS) circuits to the interposer side, which is suitable for a large-scale qubit system. From the point of view of the assembly process, a gold stud bump-based bonding process is used for flip-chip bonding. The formation of the gold stud bumps does not include any undesirable processes that introduce contamination on the quantum photonic chip side such as the exposure of organics, wet chemicals, and etching gasses. By forming the stud bumps on the quantum photonic chip side, damage-less chip handling can be achieved during bonding. Gold stud bumps and gold pads have potentially high reliability because it does not change the electrical characteristics by the temperature cycle test [9]-[11].

III. Method

A. Fabrication Process

The fabrication process is shown in Fig. 2. A test chip of 15 × 15 mm^2 and an interposer of 20 × 20 mm^2 were used in this work. Those sizes correspond to a chip with color centers in the order of 10^2, based on the current qubit chip technology of 1.0 × 1.0 mm^2 unit area for one color center. First, for the test chip and the interposer, 500 nm gold/100 nm nickel/30 nm titanium was sputtered on the silicon substrate using a two-layer left-off process. Then, the silicon was diced into 15 × 15 mm^2 and 20 × 20 mm^2 chips as the test chip and the interposer, respectively. Next, gold stud bumps on the test chip were fabricated using a wire bonder. Then, we performed thermocompression bonding between the test chip and the interposer using a flip-chip bonder. FCB-3 equipment made by Panasonic was used. The bonding condition of head temperature, pressure, and time were 350°C, 50 N, and 90 s, respectively.

B. Design of the Interposer and the PCB

The layout of the interposer is shown in Fig. 3. We measured 16 signal lines, including two gold stud bumps, and measured a line alone for extracting its resistivity. The width of the signal line on the test chip and the interposer is 30 µm. The width and length of the line for evaluating the resistivity of the line on the interposer are 100 µm and 10 mm, respectively. The pads of the resistivity line were designed for the 4-point probing measurement to exclude resistance components other than the line.

The layout of the PCB is shown in Fig. 4. The measurement line is highlighted in yellow. This measurement line is connected to the measurement line D of the interposer in Fig. 3 by wire bonding. The pads of the measurement point on the PCB are designed for 4-point probe measurements. The PCB allows us to measure the resistance of the entire path from the PCB through the interposer to the chip. A schematic measurement of the packaged chip on PCB is shown in Fig. 5. The packaging process was connected by a gold wire from the PCB to the interposer using a wire bonder after the integration of the test chip and the interposer. Finally, the measurement line from the terminal of the PCB to the test chip was completed via the wire bond, the interposer, and the gold stud bump.

C. Cryogenic Measurements

- The measurement of the test chip on the interposer

  The mechanical cryogenic prober station GRAIL10-305-4-LV-HT manufactured by Nagase Techno-Engineering and the semiconductor parameter analyzer 4156C made by Keysight Technology were used. Measuring points are 10 K and 50 K until 300 K at 50 K steps.

- The measurement of the packaged chip on the PCB

  The liquid N_2 prober SB-LN2P manufactured by Thermal block and the semiconductor parameter analyzer B1500A made by Keysight Technologies were used. The test chip on the interposer and the PCB were connected using a wire bond. The measuring point are 80 K.

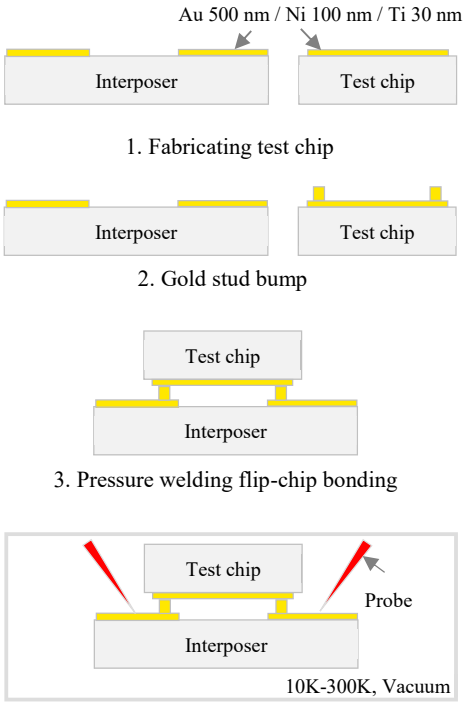


Fig. 2. Fabrication process of the test Si chip on the interposer.

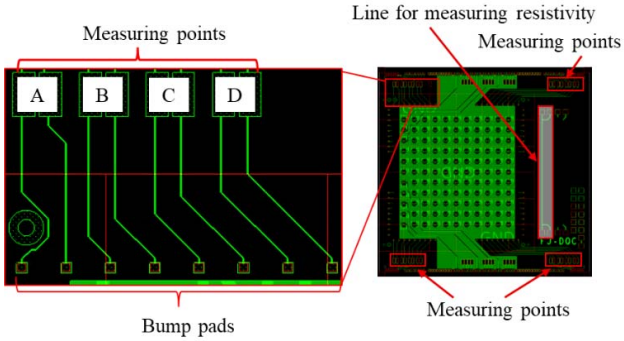


Fig. 3. The interposer layout and measuring points; 16 measuring points between the signal line and two bumps and a resistivity line of 10 mm with 4-point probe pads.

D. Chip Shear Strength Test

We measured the shear strength of the gold stud bumps with the chip shear strength tester for the flip-chip bonded structure of the chip and the interposer. Figure 6 shows a schematic of the shear strength test. The measurement speed was 50 μm/s at a shear height of 150 μm.

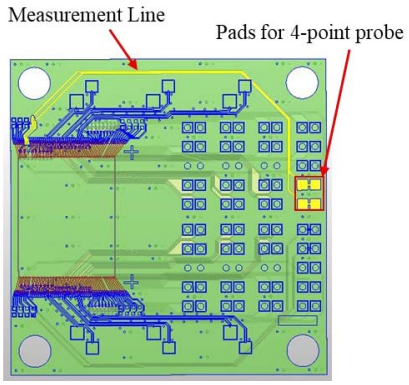


Fig. 4. The layout of the PCB and the measurement line.

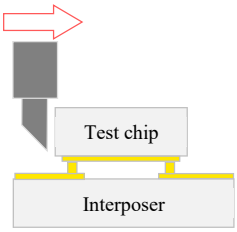


Fig. 5. Schematic of the chip shear strength test.

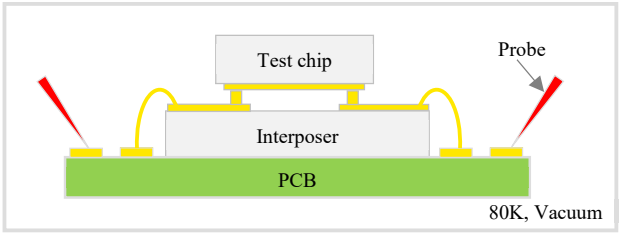
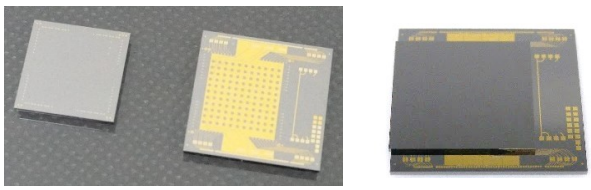


Fig. 6. Schematic image of measuring the test chip using the PCB.

IV. Results and Discussion

A. The msurement of The Test Chip on The Interposer

The photographs of the samples before and after flip-chip bonding are shown in Fig. 7. We successfully fabricated the test chip on the interposer using gold stud bumps. We measured 16 measurement lines in Fig. 7 (b) between 10 K and 300 K. All measurement lines in the test chip on the interposer maintained their connections up to 10 K. Temperature dependence of the resistance from 10 to 300 K for line A–D is shown in Fig. 8. The resistance range of these lines was 3.32–3.67 Ω at 10 K and 8.71–9.54 Ω at 300 K. The minimum resistance was in line B and increased in the order of line A, C, and D. This is simply because of the difference in the line lengths on the interposer. We measured the resistivity using the test line with a length of 10 mm and a width of 100 μm. The resistivities at 10 and 300 K were 1.17×10^{-8} and 3.08×10^{-8} Ω-m, respectively. The resistivity of gold is 2.44×10^{-8} Ω-m at 298 K [12]. Therefore, the measured resistivity on the interposer at room temperature is approximately 25% higher than that of the previous report [12]. The difference in resistivity between the measured sample and the value in the literature [12] is caused by the difference in the



(a) (b)

Fig. 7. The photographs of the test chip and the interposer; (a) before fabricating gold stud bumps and (b) after flip-chip bonding.

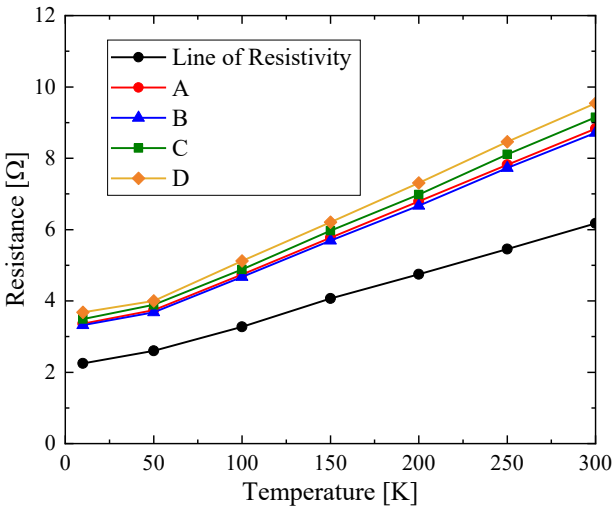


Fig. 8. Temperature-dependent resistance between the signal line and two bumps and the line of resistivity.

gold film thickness and/or the gold quality, depending on the deposition method. The temperature dependence of the resistivity from 10 to 300 K showed a similar trend with the characteristics of the 70-nm-thick gold film [13].

We simulated the DC electromagnetic simulation of measured lines from A to D at 10 K using the measured and calculated resistivity at 10 K. We used an electromagnetic simulator of SIwave made by Ansys. The simulated and measured values at 10 K are compared in Fig. 9. The simulated values ranged from 3.41 to 3.72 Ω, which is 1%–3% lower than the measured values.

B. *Structural Analysis of Flip-Chip Bonding using Gold Stud Bumps*

We observed the cross-section of gold stud bumps using a sample filled with resin and ground. Figure 10 shows a picture and scanning electron microscope (SEM) image of the cross-section of gold stud bumps. Fig. 10 (c) and (d) show the interface region of the thermocompression bonding. Fig. 10 (e) shows the surface of the ultrasonic bonding. The gold stud bumps are well-connected on both sides of the test chip and the interposer. No clear interface contrast can be observed between the sputtered gold layer and the gold stud bumps in Fig. 10 (c)–(e). It ensures the strong bonding between the stud bumps and the sputtered layer with high reliability. The average height of 18 gold stud bumps was 26.0 µm. Because the average diameter of the original gold stud bumps was 81.5 µm, the bumps were well-

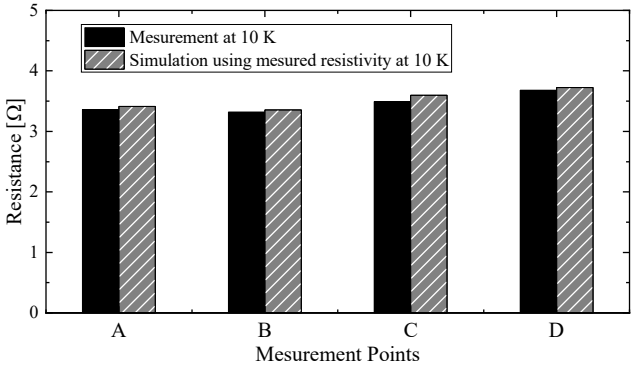


Fig. 9. The resistivity measurement results and the DC electromagnetic simulation of measurement lines at 10K.

deformed by the bonding process. The height variation of the stud bump was as small as 2 µm, and a uniform bonding was realized for a cm-order-size chip. For the quantum chip application, reducing the gap distance between the chip and the interposer is preferable because it can save the driving power of qubit control. The reduction of the gap distance can be realized using the low height of the gold stud bump that can be formed using thin seed wire and making a small gold ball at the ball bonding process.

C. *Chip Shear Strength*

We investigated the chip shear strength test of three samples. The test chip is the same, as shown in Fig. 7 (b). Table 1 shows the results of chip shear strength. The average shear strength of the chip was 4784.1 g, which corresponds to the shared strength of approximately 67.4 g per bump. The strength variation in the three samples was under 5%. The shear strength of all three samples is slightly larger than the previously reported values [13]. The ref. [13] reported that the gold stud bump passed the temperature cycle test, and there was no apparent change in the variation of the resistance and the shear strength of the gold stud bump. Therefore, the gold stud bumps are considered capable of robustness against temperature cycle tests. Hence, we will perform the cryogenic temperature cycle test between 4 and 300 K as the next step.

D. *Mesurement of the Packaged Test Chip on the PCB*

As shown in Fig. 11, the test chip on the interposer was mounted on the PCB to fabricate the measured packaged structure. The measurement line was connected between the terminal of the PCB and the interposer by wire bonding. The resistance of the measurement line is 12.63 Ω at 80 K. With comparing the results in Fig. 8, the resistance from wire bond to the connector terminal of the PCB is around 8 Ω because the resistance is around 5 Ω of line D on the test chip and the interposer. The measurement temperature was simply limited by the equipment, and the lower temperature measurements for the packaged chips will be demonstrated in the future.

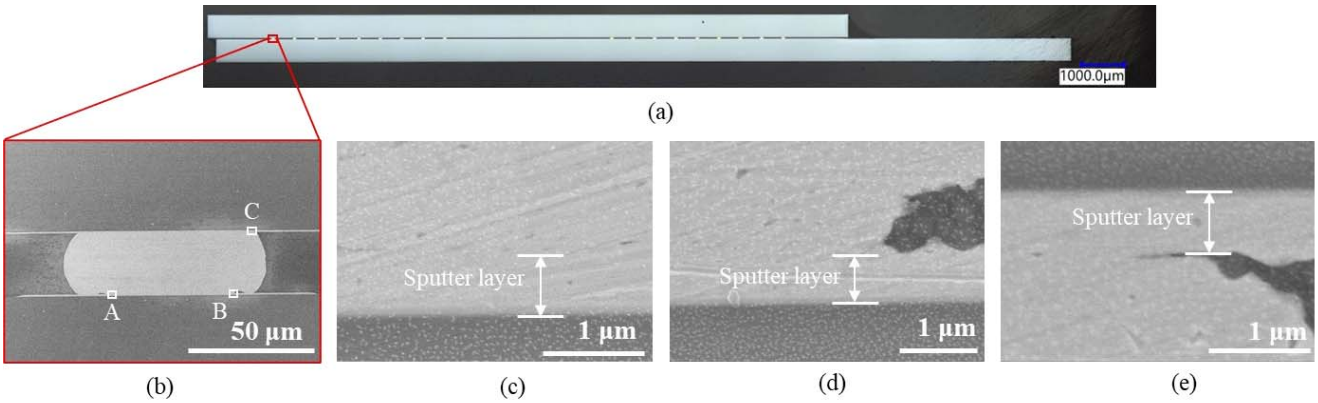


Fig. 10. A cross-sectional morphology analysis of the gold stud bumps in the flip-chip bonded sample; (a) picture of the test chip on the interposer, (b) SEM image of enlarged (a), (c) SEM image of pressure welding cross-section at A on (b), (d) SEM image of pressure welding cross-section of B at (b), (e) SEM image of ultrasonic wirebonding cross-section of C at (b).

TABLE I. CHIP SHEAR STRENGTH OF GOLD STUD BUMPS

	Shear strength [g]	
	Per chip	**Per bump**
No. 1	4677.6	65.9
No. 2	4968.0	70.0
No. 3	4706.8	66.3
Average	4784.1	67.4

CONCLUSION

We proposed integration using gold stud bumps for a quantum computer of color-center spin qubits in diamonds. We evaluated the connections of gold stud bumps between the 15 × 15 mm^2 test chip and the 20 × 20 mm^2 interposer. All connecting bumps between the test chip and the interposer were maintained at a low temperature of 10 K. The resistance between two bumps and the wiring pattern was 3.32–3.67 Ω at 10 K and 8.71–9.54 Ω at 300 K. Comparing the simulation results, the difference in resistance is mainly owing to the wiring pattern in the interposer. The resistance of gold stud bump connections was lower than the variation in fabrication or measurement error. We observed the cross-section of the gold stud bumps. Highly reliable connections between the sputtered layer and gold stud bumps were confirmed because no interfaces between the sputtered layer and gold stud bumps were observed. A sufficient shear strength of 67.4 g per bump was obtained, which means that the integrated chip has the potential to pass the temperature cycle test. Moreover, we fabricated the packaged test chip on the printed circuit board and demonstrated their connection of all routes from the PCB to the test chip. The resistance between the test chip and the printed circuit board was 12.63 Ω at 80 K. These results will realize large-scale diamond spin quantum processors.

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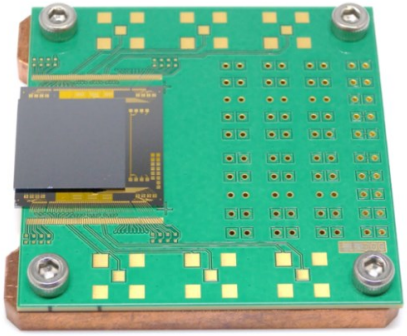

Fig. 11. Picture of the packaged test chip on the PCB.

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