IC–MEMS Co-Fabrication

Enabling smart–seamless microsystem integration for emerging biomedical technologies

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IC–MEMS CO-FABRICATION

ENABLING SMART–SEAMLESS MICROSYSTEM INTEGRATION FOR EMERGING BIOMEDICAL TECHNOLOGIES

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
by the authority of the Rector Magnificus, prof. dr. ir. T.H.J.J. van der Hagen,
chair of the Board for Doctorates
to be defended publicly on
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by

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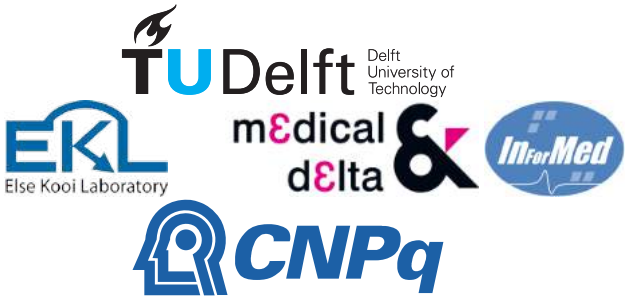

Keywords: monolithic fabrication, microsystem integration, integrated circuits, micro-electromechanical systems, organs-on-a-chip, optrodes, holistic co-design methodology

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To the memory of my beloved brother,
who unwittingly sparked my passion for scientific discoveries
at the tender age of five
when he dismantled an old radio box
to prove me wrong.

Sometimes a scream is better than a thesis.

—Ralph Waldo Emerson

CONTENTS

ACRONYMS

AC Alternating current.

ADC Analog-to-digital converter.

AFE Analog front-end.

AlSi Aluminium silicide.

ASIC Application-specific Integrated Circuit.

BEOL Back-end of line.

BiCMOS Bipolar CMOS.

BiFET Bipolar–and–FET technology.

BOX Buried oxide.

CD Critical dimension.

ChR2 Channelrhodopsin-2.

CM Common mode.

CMOS Complementary metal–oxide–semiconductor.

CMRR Common-mode rejection ratio.

CSD Cortical spreading depression.

CTAT Complementary to absolute temperature.

CVD Chemical vapor deposition.

DC Direct current.

DM Differential mode.

DRIE Deep Reactive Ion Etching.

DSP Double-sided polished.

EDL Electrical double layer.

EIS Electrochemical impedance spectrometry.

EKL Else Kooi Laboratory.

EMI Electromagnetic interference.

ESC Electrostatic clamping chuck.

FEOL Front-end of line.

FET Field-effect transistor.

FS Full scale.

G1 Gap 1 phase, or growth 1 phase.

GND Ground.

HNO_3 Nitric acid.

IC Integrated circuit.

InGaN Indium Galium Nitride.

iPSC Human induced pluripotent stem cell.

IPTAT Inversely proportional to the absolute temperature.

IRN Input-referred noise.

ISA Infraslow brain activity.

JFET Junction-gate field-effect transistor.

LDO Low-dropout regulator.

LED Light-emitting diode.

LFP Local field potential.

LOC Lab-on-a-chip.

LP Loop-gain-Poles product.

LSB Least significant bit.

MCM Multi-chip module.

MEMS Micro-electromechanical systems.

MiM Metal–insulator–metal.

MUAP Multi-unit action potential.

NTC Negative temperature coefficient.

OOC Organ-on-a-chip.

OPAMP Operational amplifier.

OPC Optical proximity correction.

PBS Phosphate buffered saline.

PCB Printed circuit board.

PDK Process design kit.

PDMS Polydimethylsiloxane.

PECVD Plasma-enhanced chemical vapor deposition.

PES Phosporic/Acetic/Nitric acid.

PoP Package-on-package.

PSD Power spectral density.

PSRR Power-suppy rejection ratio.

PT-100 "PT" is the symbol for platinum, "100" for the resistance in ohms at 0 °C.

PTAT Proportional to absolute temperature.

RCA Radio Corporation of America.

RDL Redistribution layer.

RH Relative humidity.

RLD Right Leg Driving.

RMS Root mean square.

SEM Scanning electron microscope.

SF_6 Sulfur hexafluoride.

SiO_2 Silicon dioxide.

SiP System-in-package.

SNR Signal-to-noise ratio.

SOI Silicon-on-insulator.

Specs Specifications.

SPICE Simulation program with integrated circuit emphasis.

SSP Single-sided polished.

STI Shallow trench isolation.

TEOS Tetraethyl orthosilicate.

THD Total harmonic distortion.

TiN Titanium nitride.

TSV Through-silicon via.

TTV Total thickness variation.

UI User interface.

VLL Ventral Lateral Nucleus.

WEB Washed-emitter-base.

ZIF Zero insertion force.

SUMMARY

The development of personalized healthcare solutions is a complex and multifaceted challenge that requires synergistic collaboration and cross-fertilization between multiple disciplines, including microelectronics, nanotechnology, materials science, and biotechnology. As numerous biomedical applications necessitate the precise regulation and observation of various biological systems at the microscale, developing integrated microsystems with functionalities that span diverse domains, such as electrical, mechanical, and optical, has become imperative in paving the way for next-generation biomedical devices.

Nevertheless, as the number of microsystems within a biomedical device escalates, a pressing need emerges to interconnect these independent microsystems using an approach that meets the constraints imposed per each particular context. Wire bonding, for instance, is one of the most widely known and used methods to establish electrical connections between chips and packages. However, wire-bonded microsystems may be inadequate to fit in applications confined by the available physical space and whereby aspects such as reliability and biocompatibility are paramount. Specifically deserving attention is the increased footprint and the introduction of protrusions that may jeopardize an effective interface of biomedical devices with biological systems. Therefore, it becomes essential to devise seamless connections between these microsystems for enhanced robustness, electrical performance, compactness, and improved physical conformability to biological structures.

This doctoral research was driven by the increasing demand for microsystem integration alternatives in the biomedical field and the need to develop advanced biomedical devices with improved functionality and performance. Monolithic fabrication was the principal method of establishing a seamless integration between distinct microsystems: integrated circuits—essential for the signal conditioning of transducers—and micro-electromechanical systems—excellent for implementing functionalities at the microscale via precise micromachining delicate structures on high-quality materials. Two novel biomedical devices were devised to achieve this objective: an organ-on-a-chip system for cell-culture experimentation equipped with an analog-compatible, cost-effective, BiCMOS-based temperature sensor and a stretchable polydimethylsiloxane membrane; and an artifact-resilient optrode optimized for ultralow-noise measurements of infraslow brain activity. The latter benefited from dual-gate, low-noise, p-channel JFETs based on a BiFET technology and deep reactive ion etching on a silicon-on-insulator wafer for micromachining nonrectilinear features on the probe—essential for creating application-oriented solutions that interface better with biological structures.

Both devices were designed based on a unique awareness-oriented co-design methodology that aids the device architect in undertaking design decisions of various process-related hurdles entailing co-fabrication. This methodology, namely “holistic

iterative co-design thinking", offers an iterative co-design process that facilitates the early identification of integration obstacles related to the manufacturing process. One of the key procedures in this methodology refers to functionally decomposing a multidimensional complex design problem into a set of individual one-dimensional problems that are less complex to solve. As a result, the (co)-design is iteratively readjusted, significantly saving time and resources.

This dissertation also takes a new standpoint into the existing monolithic fabrication modalities, proposes a new taxonomy, clarifies terminologies, and addresses a novel co-fabrication technique: IC-interlaced-MEMS, employed for cost-effectively co-fabricating the organ-on-a-chip system described in Chapter 4. The IC-interlaced-MEMS is similar to its "sibling" IC-interleaved-MEMS. The distinction lies primarily in their degree of process orthogonality. While the IC-interleaved-MEMS benefits from fully orthogonalizing process steps between the IC and MEMS domains, the IC-interlaced-MEMS trades orthogonality for process simplification and enhanced lithographic pipeline workflow. These benefits promise to leverage the construction of next-generation biomedical devices that interact with biological systems via specialized, large-area transducers.

SAMENVATTING

De ontwikkeling van gepersonaliseerde oplossingen voor de gezondheidszorg is een complexe en veelzijdige uitdaging die synergetische samenwerking en kruisbestuiving vereist tussen meerdere disciplines, waaronder micro-elektronica, nanotechnologie, materiaalkunde en biotechnologie. Aangezien tal van biomedische toepassingen de nauwkeurige regulering en observatie van verschillende biologische systemen op microschaal vereisen, is de ontwikkeling van geïntegreerde microsystemen met functionaliteiten die zich uitstrekken over diverse domeinen, zoals elektrisch, mechanisch en optisch, noodzakelijk geworden om de weg vrij te maken voor de toekomstige generatie biomedische apparaten.

Desalniettemin, naarmate het aantal microsystemen binnen een biomedisch apparaat toeneemt, ontstaat er een dringende behoefte om deze onafhankelijke microsystemen met elkaar te verbinden met behulp van een aanpak die voldoet aan de beperkingen die per specifieke context worden opgelegd. Wire bonding is bijvoorbeeld een van de meest bekende en gebruikte methoden om elektrische verbindingen tussen chips en pakketten tot stand te brengen. Microsystemen die verbonden zijn middels wire bonding kunnen echter ontoereikend zijn om te passen in toepassingen die beperkt zijn door de beschikbare fysieke ruimte en waarbij aspecten als betrouwbaarheid en biocompatibiliteit van het grootste belang zijn. Specifiek aandacht verdienen de toegenomen voetafdruk en de introductie van uitsteeksels die een effectieve interface van biomedische apparaten met biologische systemen in gevaar kunnen brengen. Daarom wordt het essentieel om naadloze verbindingen tussen deze microsystemen te bedenken voor verbeterde robuustheid, elektrische prestaties, compactheid en verbeterde fysieke conformiteit met biologische structuren.

Dit doctoraatsonderzoek werd gedreven door de toenemende vraag naar alternatieven voor microsysteemintegratie op biomedisch gebied en de noodzaak om geavanceerde biomedische apparaten te ontwikkelen met verbeterde functionaliteit en prestaties. Monolithische fabricage was de belangrijkste methode om een naadloze integratie tussen verschillende microsystemen te bewerkstelligen: geïntegreerde schakelingen—essentieel voor de signaalconditionering van transducenten—en microelektromechanische systemen— uitstekend geschikt voor het implementeren van functionaliteiten op microschaal via nauwkeurige microbewerking van delicate structuren op hoogwaardige materialen. Twee nieuwe biomedische apparaten werden bedacht om dit doel te bereiken: een orgaan-op-een-chip-systeem voor celkweekexperimenten uitgerust met een analoog-compatibele, kosteneffectieve, op BiCMOS gebaseerde temperatuursensor en een rekbaar polydimethylsiloxaanmembraan; en een artefact-veerkrachtige optrode die is geoptimaliseerd voor ultralage-ruis metingen van infraslow-hersenactiviteit. De laatstgenoemde profiteerde van dual-gate, lage-ruis, p-kanaal JFET's op basis van een BiFET-technologie en diepe reactieve ion-etsing op een silicium-op-isolator-wafel voor microbewerking van niet-rechtlijnige kenmerken

op de sonde—essentieel voor het creëren van toepassingsgerichte oplossingen die beter aansluiten bij biologische structuren.

Beide apparaten zijn ontworpen op basis van een unieke op bewustzijn gerichte co-ontwerpmethodologie die de apparaatarchitect helpt bij het nemen van ontwerpbeslissingen over verschillende procesgerelateerde hindernissen die co-fabricage met zich meebrengen. Deze methodologie, namelijk "holistisch iteratief co-ontwerp denken", biedt een iteratief co-ontwerpproces dat de vroege identificatie van integratieobstakels met betrekking tot het fabricageproces vergemakkelijkt. Een van de belangrijkste procedures in deze methodologie verwijst naar het functioneel ontleden van een multidimensionaal complex ontwerpprobleem in een reeks individuele eendimensionale problemen die minder complex zijn om op te lossen. Hierdoor wordt het (co)-ontwerp iteratief bijgestuurd, wat een aanzienlijke tijd- en middelenbesparing oplevert.

Dit proefschrift neemt ook een nieuw standpunt in over de bestaande monolithische fabricagemodaliteiten, stelt een nieuwe taxonomie voor, verduidelijkt terminologieën en behandelt een nieuwe co-fabricagetechniek: IC-interlaced-MEMS, gebruikt voor het kosteneffectief co-fabriceren van het orgaan-op-een-chipsysteem beschreven in hoofdstuk 4. De IC-interlaced-MEMS is vergelijkbaar met de "verwante" IC-interleaved-MEMS. Het onderscheid ligt voornamelijk in hun mate van orthogonaliteit van het proces. Terwijl de IC-interleaved-MEMS profiteert van volledig orthogonaliserende processtappen tussen de IC- en MEMS-domeinen, ruilt de IC-interlaced-MEMS orthogonaliteit in voor procesvereenvoudiging en verbeterde lithografische pijplijnwerkstroom. Deze voordelen beloven te profiteren van de constructie van dragen de belofte in zich biomedische apparaten die interageren met biologische systemen via gespecialiseerde transducenten met een groot oppervlak.

1

INTRODUCTION

If we knew what it was we were doing, it would not be called research, would it?

Often attributed to Albert Einstein
(1879–1955)

1

1.1. MOTIVATION

Research in the field of bioelectronics has elicited remarkable strides in developing next-generation biomedical devices with multiple functionalities and exceptional performance. The high level of sophistication achieved cost-effectively has made biomedical devices ubiquitous, and their transformative potential to enhance healthcare and improve the well-being of millions is increasingly evident. The rapid progress in this field is generating innovative diagnostic, therapeutic, and healthcare delivery solutions, which hold great promise for addressing the most pressing health challenges of our time.

One example is lab-on-a-chip (LOC). LOC technology integrates multiple laboratory functions, such as DNA analysis, disease diagnosis, and drug testing, onto a single chip with dimensions typically limited to a few square millimeters. Recently, these devices have garnered significant attention in light of the COVID-19 pandemic caused by the SARS-CoV-2 virus [1–3]. This attention stems from their capability to enable faster, more precise, and more cost-effective diagnostic results, surpassing conventional laboratory-based techniques. Besides COVID-19 testing, LOC technology has also been employed to develop portable diagnostic devices suitable for resource-constrained environments. These devices are designed to be user-friendly and do not necessitate specialized equipment or trained staff, making them ideal for deployment in regions with inadequate healthcare infrastructure.

Another example of biomedical devices that have undergone remarkable technological advancements is neural implants. Neural implants offer a promising avenue for treating neurological disorders such as Parkinson's, epilepsy, and chronic pain [4–6]. Early interventions for these conditions involved electrical stimulation regulating neural activity, resulting in symptom relief and enhanced patient outcomes. However, these approaches have been met with certain limitations, including the inability to target specific groups of neurons and potential damage to surrounding tissue [7, 8]. Therefore, alternative stimulation modalities, such as optogenetics and ultrasound, are being explored more recently to overcome these limitations and pave the way for more effective and precise treatment strategies [9, 10].

Like the examples above, numerous next-generation biomedical devices result from the synergistic collaboration between microelectronics, nanotechnology, materials science, and biotechnology. This interdisciplinary synergy has led to the development of novel materials and fabrication methods to facilitate their microsystem integration. By cross-fertilizing the strengths of each field, researchers have designed and manufactured complex integrated systems capable of real-time monitoring, diagnosis, and therapy.

1.1.1. THE ROLE OF MICROSYSTEM INTEGRATION IN BIOMEDICAL DEVICES

Microsystem integration has been instrumental in the development of next-generation biomedical devices: it has facilitated the miniaturization and integration of various components, such as sensors, actuators, and fluidic systems, leading to improved device functionality and performance.

Several approaches have been employed for the successful integration of microsys-

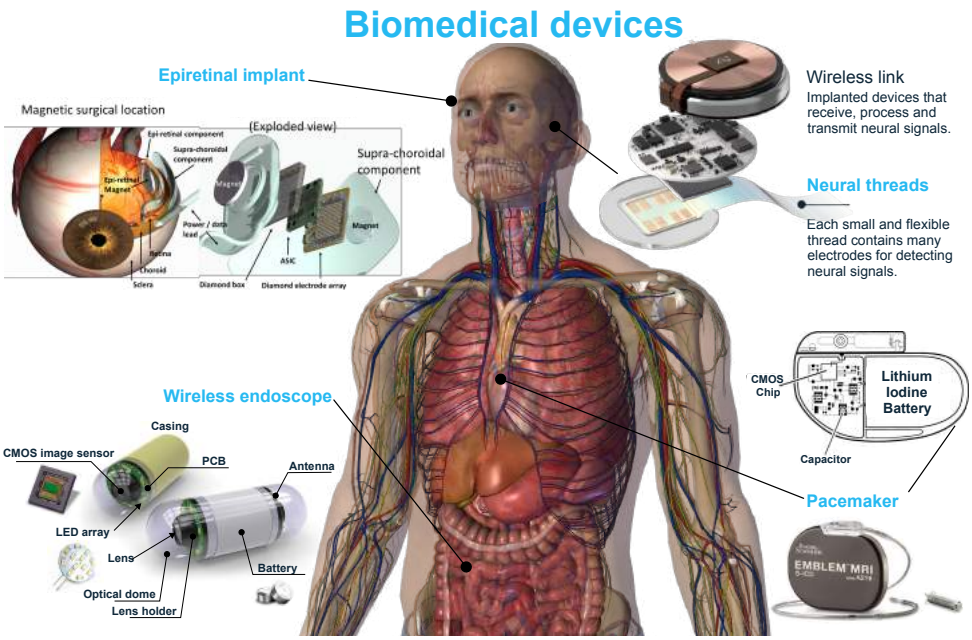

Figure 1.1: Artistic impression highlighting various biomedical devices and their microsystems distributed in a 3D anatomy of a human body. The illustration features an example of an epiretinal implant on the right eye [11], a neural implant on the left temporal lobe [12], a wireless endoscope in the digestive tract [13], and a pacemaker in the chest cavity [14]. Artwork created by the author of this thesis. Copyrights to reuse certain parts of [11] were granted by John Wiley & Sons, Inc.

tems [15–22], mainly:

- **Monolithic integration**, which involves fabricating all the microsystem components on a single substrate, typically silicon. This approach offers high precision, compactness, and scalability. By monolithically integrating multiple functions on a single chip, the size and weight of the device can be reduced—which is highly beneficial in numerous applications. Monolithic integration may substantially reduce the device footprint by incorporating multiple functionalities onto a single chip. The potential for miniaturization allows for implantation in smaller anatomical regions, facilitating minimally invasive procedures. Miniaturization could also improve system performance by reducing parasitics from interconnects, thereby reducing the signal propagation delay and improving the signal's integrity. However, achieving the desired functionality using monolithic integration can be challenging. This approach is limited to a single substrate material and fabrication technology, which can result in higher costs due to the increased number of photomasks and processes.

- **Hybrid integration**, which involves combining at the packaging stage multiple microsystem components, each fabricated using a different technology or substrate, into a single package. This approach can enhance the system's overall functional-

ity and reduce costs by leveraging existing commercial components and fabrication technologies. However, hybrid integration can result in more complex interconnects and packaging, potentially increasing the device's footprint and reducing yield and reliability.

- **Heterogeneous integration**[1], which involves combining, at the fabrication stage, different materials such as metals, ceramics, polymers, and semiconductors with varied technologies such as microelectronics, photonics, and microfluidics. This integration approach offers a broad range of materials and processes to undertake, which can lead to better performance and compatibility with biological systems. However, achieving a reliable interface between the different materials can take time. Thus, this approach can result in more complex fabrication and packaging processes, potentially leading to higher costs than hybrid integration. Moreover, the final package footprint achieved with heterogeneous integration is usually smaller than the hybrid but larger than the monolithic.

Table 1.1: Pros and cons of different microsystem integration approaches for biomedical devices

Approach	**Pros**	**Cons**
Monolithic	• Higher minituarization and reduced footprint • High integration density • High reliability • Scalability	• Limited functionalities • Limited materials and processes • Often leads to high costs
Hybrid	• Increased functionality • Design versatility • Cost savings	• Complex assembly and testing • Poor yield and reliability
Heterogeneous	• Increased functionality • Miniaturization • Versatility	• Complex design and fabrication processes • Integration challenges • Reliability issues • Achieving high yields

[1] The terms "hybrid integration" and "heterogeneous integration" are not always clearly distinguished in the literature. Some scholarly works may even refer to these terms interchangeably. The reader may refer to the academic work presented in [23] for further clarification on the differences between both integration methods.

Furthermore, various methods and techniques are accessible for the execution of microsystem integration approaches at different hierarchical levels, ranging from package and wafer levels to component levels (Fig. 1.2).

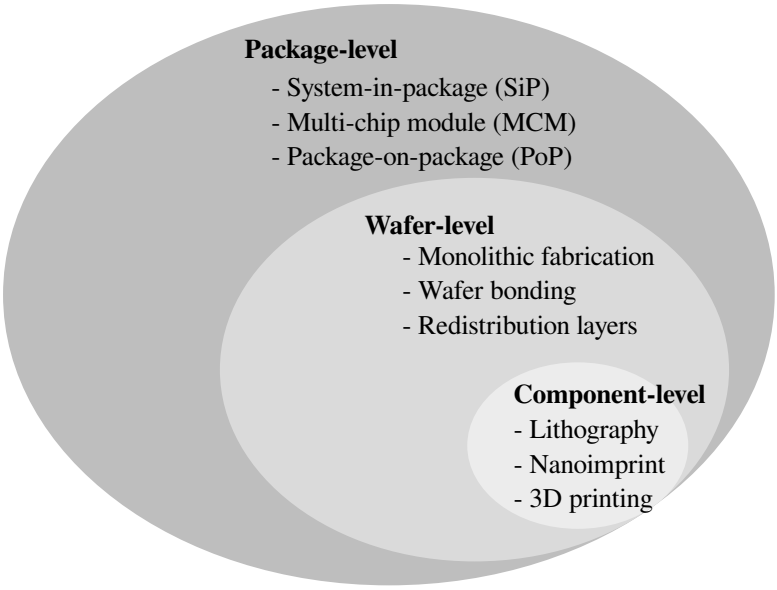

Figure 1.2: Implementing microsystem integration approaches at distinct hierarchical levels: a comparative analysis of package, wafer, and component levels.

At the package level, discrete components, microsystems, and other packages are merged to form a higher-level assembly known as a system-in-package (SiP). Flip-chip bonding, wire bonding, and through-silicon vias (TSVs) are some techniques employed at this stage. Likewise, multi-chip modules (MCM) and package-on-package (PoP) are two popular advanced packaging technologies commonly used at the package level. MCM integrates multiple chips or dies on a single substrate or package, whereas PoP creates a stacked package arrangement, i.e., one package on top of another.

On the other hand, at the wafer level, multiple microsystem components are integrated into a single silicon wafer before packaging. This integration level employs standard semiconductor processes such as lithography, etching, and thin-film deposition to manufacture complex functions at the microscale. Other techniques utilized at this level include redistribution layers (RDL) and wafer bonding. Wafer-level integration is commonly used for mass-producing integrated circuits (ICs) and micro-electromechanical systems (MEMS).

Microsystem integration at the component level refers to integrating individual components with specific functionalities that are subsequently assembled into a single microsystem. It aims to create a functional microsystem with minimal complexity. The components used in this level of integration can be fabricated using a wide range of materials and processes, such as silicon, polymers, metals, elastomers, and ceramics. These components can be assembled using techniques such as bonding, adhesives, and

soldering. Moreover, fabrication techniques at this level include, but are not limited to, MEMS technology, soft lithography, 3D printing, and nanoimprint lithography. At the component level, the integration process is relatively simple compared to higher levels of integration. Nonetheless, the selection and compatibility of materials and processes used in the fabrication and assembly of the components require careful consideration to ensure optimal performance and reliability of the microsystem.

Table 1.1 outlines the microsystem integration approaches previously mentioned, delineating their unique advantages and disadvantages, whereas Fig. 1.2 illustrates the possible hierarchy levels to accomplish them in a nested-like fashion.

ADDRESSING CONSTRAINTS AND CHALLENGES OF SPECIFIC MICROSYSTEM INTEGRATION TECHNOLOGIES FOR BIOMEDICAL APPLICATIONS

Naturally, selecting an appropriate integration approach depends on the specific context of the application in question. Multiple factors must be considered when making this decision. For instance, wire bonding is a widely used process in the semiconductor industry to establish electrical connections between a semiconductor chip and a package. However, due to the distinct requirements of the medical field, wire bonding may not be suitable for certain biomedical applications in terms of:

1. **Electrical performance:** wire bonds and bond pads introduce additional resistance, capacitance, and inductance into a circuit, which can affect the electrical performance of a biomedical device. Specifically, it can reduce the amplitude of weak electronic signals, resulting in elevated noise levels and heightened susceptibility to electromagnetic interference (EMI), thereby limiting the signal's fidelity.

2. **Miniaturization:** wire-bonded systems entail multiple chips (or chiplets) arranged laterally or vertically. Such configurations inevitably increase the package footprint due to the chip dimensions and the extra physical space used for the wire bonds.

3. **Reliability:** wire bonds are susceptible to mechanical and thermal stresses, which may cause them to deteriorate or fracture over time. Moreover, as bond-pad and wire dimensions decrease, ensuring reliable wire bonds becomes increasingly challenging while the likelihood of wire breakage or other failures escalates. In the context of biomedical devices, where reliability is of utmost importance, this can be a particularly significant concern.

4. **Biocompatibility:** the alloys employed in wire bonds may form loops or "stitches," thereby introducing unwanted protrusions into the final device. Such protrusions may introduce additional challenges in interfacing the device with biological structures, such as cells, tissues, organs, or the nervous system. Moreover, the materials employed in wire bonding may interact with biological tissues or fluids, resulting in adverse reactions or performance discrepancies. Hence, ensuring biocompatibility is critical when designing biomedical devices utilizing wire bonding.

Additionally, wire-bonded microsystems suffer from constrained versatility. The singulation process, which involves sawing the wafer into rectangular chips, considerably restricts the design freedom for mechanical characteristics, physical shapes, and configurations better suited for effectively interfacing with the nonrectilinear structures of the human body and biological systems.

INVESTIGATING MICROSYSTEM INTEGRATION ALTERNATIVES FOR WIRE BONDS

The caveats of establishing electrical connections with wire bonds in certain biomedical applications have become apparent. Specifically deserving attention is the increased footprint and the introduction of protrusions that may jeopardize an effective interface of biomedical devices with biological systems. Therefore, seamless connections between different system components are desired in numerous biomedical applications. A seamless biomedical microsystem provides several benefits, including tighter integration between components, improved electrical performance, compactness, reduced package footprint, robustness, and smoother physical shapes, enabling biomedical devices to interface effectively with biological structures. To this end, it is imperative to investigate integration approaches that minimize the device footprint and eliminate protrusions introduced by wire bonds.

Likewise, it is crucial to investigate a process technology that allows the construction of essential functionalities demanded in biomedical applications, such as sensing, actuation, and microfluidics. Preferably, the process technology must permit the implementation of these functionalities across diverse domains, including mechanical, electrical, and optical, to facilitate the precise regulation and observation of various biological systems at the microscale. A viable solution is MEMS because this process includes the abovementioned functionalities into a single device while providing scalability, reproducibility, and cost-effectiveness features. Furthermore, this approach allows for the monolithic fabrication of integrated circuits, which is essential for the signal conditioning of transducers. Hence, this solution not only obviates the need for wire bonds but also enables the development of complex and sophisticated **smart–seamless biomedical devices** with enhanced functionalities and performance.

Finally, it is of utmost importance to thoroughly investigate the foundational stages and optimal methodologies involved in co-fabricating integrated circuits with MEMS. This inquiry is crucial in determining how this process can yield optimal integration performance, reliability, and functionality, essential for developing next-generation biomedical devices. Such advancement has far-reaching implications in biomedical technology, making this area of research a critical component of future advancements in healthcare.

1

1.2. RESEARCH OBJECTIVES AND FURTHER MICROSYSTEM INTEGRATION CHALLENGES

The present thesis explores the design and construction of seamless biomedical devices by co-fabricating ICs with MEMS. Traditionally, one standard route for co-fabricating MEMS with ICs involves purchasing state-of-the-art complementary metal-oxide-semiconductor (CMOS) wafers and micromachining structures on top of them. However, this approach presents several challenges:

1. The melting point of metals employed in the CMOS interconnects severely constrains the maximum thermal budget allowed by the MEMS process.

2. This integration strategy may increase the possibility of dopant redistribution within diffusion layers, thereby posing detrimental consequences to the operational efficiency of the device.

3. The economic viability of this approach is limited in the context of emerging technologies that interact with biological systems via specialized, large-area transducers[2].

The principal factor that underlies the insufficient economic viability of this approach is the proportion of wafer expenses that arise from the restricted throughput of lithography. In modern CMOS wafers, this fraction of wafer expenses may account for up to 50 % of the overall costs [24–27]. Consequently, the cost-per-unit area assumes greater importance, which can prove especially onerous for emerging biomedical technology that incorporates large-area transducers.

This doctoral thesis proposes a novel awareness-oriented co-design methodology to overcome the constraints of traditional co-fabrication methods. This methodology involves an iterative co-design process that can identify process-related integration hurdles upfront and readjust the design accordingly, significantly saving time and resources. Moreover, to enable the fabrication of monolithic ICs and MEMS cost-effectively, two proprietary IC technologies were employed to streamline lithographic processing and enhance integration compatibility with additional MEMS-based processing modules. These technological advancements have the potential to facilitate the creation of seamless microsystems that could serve as essential components of the next generation of biomedical technology.

The first IC process technology, BiCMOS7, was developed as a research tool by Van Zeijl, H. W., and colleagues [28, 29] to address the high process complexity and costs associated with many BiCMOS technologies. The BiCMOS7 process is a submicron, double-metal BiCMOS technology compatible with analog applications and economically viable. It features a vertical NPN bipolar junction transistor, NMOS and PMOS transistors, diffusion resistors, diodes, and metal-insulator-metal (MiM) capacitors. Importantly, all these devices can be produced in only five mask steps, and circuits utilizing these components can be completed in just seven steps.

[2] Sensors, actuators, displays, imagers, and biointerfaces (e.g., DNA, protein, lab-on-a-chip, and neural interfaces)

The second IC process technology, DIMES03, was initially proposed by Nanver, L. K. and colleagues [30] and is predicated upon a BiFET approach that integrates bipolar transistors and low-noise junction-gate field-effect transistors (JFETs) within a single process line. A salient characteristic of this technology is the enhanced performance of the NPN devices due to implementing a washed-emitter-base processing scheme. This methodology preserves the low process complexity necessary for creating a cost-effective IC technology that seamlessly integrates with additional processing modules.

To that end, this research endeavors to create two distinct biomedical microsystems that address disparate applications: an organ-on-chip system featuring an in-situ BiCMOS-based temperature sensor with a stretchable polydimethylsiloxane (PDMS) membrane for in-vitro applications and an artifact-resilient optrode for ultralow-noise measurements of infraslow brain activity for in-vivo applications.

1.3. THESIS ORGANIZATION

This doctoral thesis is organized into five main chapters, each of which contributes to the overall goal of developing novel IC–MEMS co-fabrication techniques for biomedical applications.

Chapter 2 aims to structure, organize, and elucidate knowledge about IC–MEMS monolithic fabrication techniques. Through a rigorous examination of relevant literature, this chapter clarifies the terminologies of "integration" and "fabrication". Additionally, it explores possible foundry business model strategies that enable monolithic fabrication and introduces a novel nomenclature that employs a strict criterion to classify such techniques. By providing clear guidelines for classification, this criterion effectively resolves disputes surrounding the categorization of works. Furthermore, this chapter presents a new classification branching of the IC-inter-MEMS technique and offers a detailed analysis of the advantages and disadvantages of each technique.

Chapter 3 presents a novel methodology for designing and co-fabricating ICs with MEMS, called "IC–MEMS holistic iterative co-design thinking." This methodology aims to equip designers with the necessary tools to overcome the challenges and obstacles commonly encountered during the co-fabrication phase. To this end, the methodology involves collecting relevant information beforehand to anticipate and accommodate potential uncertainties. The process is iterative, with designers refining their models until they meet the desired performance specifications (specs). Moreover, the methodology includes a functional decomposition method, which enables designers to tackle complex, multidimensional problems in a structured manner. The methodology facilitates a more efficient and effective co-design process by breaking down complex problems into smaller, more manageable ones. Overall, this methodology represents an innovative approach to IC–MEMS co-design, which promises to streamline the co-fabrication process and improve the overall performance of these integrated systems.

Chapter 4 focuses on the monolithic fabrication of a BiCMOS-based temperature sensor on a MEMS-based organ-on-chip device. Based on the methodology proposed in Chapter 3, Chapter 4 tests the approach using a novel IC-inter-MEMS fabrication technique that enables the monolithic fabrication of circuits with micromachining processes. In particular, the process involves fabricating a customized stretchable PDMS

membrane to host a cell culture. The chapter presents the time constants associated with the convection–cooling mechanism inside each microplate well after conducting wafer-level and chip-level measurements. The results provide practitioners with valuable information about how long cells can be outside the incubator for inspection and may even be used in a closed-loop manner in the future. Overall, Chapter 4 represents a contribution to the field of IC–MEMS co-fabrication, as it demonstrates the successful integration of complex circuits with MEMS-based structures, thereby paving the way for future developments in organ-on-chip devices and related technologies.

Chapter 5 applies the "IC–MEMS holistic iterative co-design thinking" methodology to design artifact-resilient optrodes with in-situ direct-coupled low-noise amplifiers for infraslow brain activity recordings in optogenetic experimentation. The optrodes are equipped with commercial in-situ μLEDs mounted on the shaft to emit light at 460 nm. Additionally, low-noise p-channel JFETs configured in a fully-differential mode and employing common-mode feedback enable high-quality measurements of infraslow brain activity. The photomasks are designed to accommodate six different designs for multiple studies. However, the microfabrication progress was halted due to the inactivation of the epitaxy machine and the ion-beam implanter. Despite this setback, Chapter 5 represents a contribution to optogenetic experimentation. It demonstrates the successful application of the IC–MEMS co-design methodology to design artifact-resilient optrodes with in-situ DC-coupled low-noise amplifiers. Furthermore, the multiple design options provided by the photomasks highlight the potential for this technology to facilitate a wide range of future studies.

Chapter 6 serves as the conclusion and the future work of this doctoral thesis, summarizing the main scientific contributions and findings presented in the previous chapters.

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2

IC AND MEMS FABRICATION TECHNIQUES

We adore chaos because we love to produce order.

M.C. Escher
(1898–1972)

2.1. INTRODUCTION

This chapter describes possible techniques and their associated logistic foundry models used to fabricate, on wafer level, MEMS and IC components monolithically.

The fabrication methods are categorized into three basic techniques: IC-before-MEMS, IC-inter-MEMS, and IC-after-MEMS. The foundry models determine whether the ICs and MEMS processes can be carried out in one unified IC–MEMS foundry or in two different IC and MEMS foundries. The technique of choice strongly depends on the device, the application, and the commercial requirements.

According to various estimations, it is reported that nearly half of the current market value of MEMS products is attributed to the utilization of ICs fabricated monolithically on the same substrate [1]. Examples include digital mirror devices, infrared bolometer arrays, inkjet printheads, gyroscopes, accelerometers, and pressure sensors. Many of these products consist of large transducer arrays in which each transducer operates individually. Thus, integrating each MEMS transducer and its associated IC on a single chip is the only practical way to implement these microsystems.

Further benefits of monolithic integration include reduced parasitics, greater sensitivity, increased reliability, and reduced package complexity. Challenges to such integration approach include MEMS layer deposition and annealing temperatures, passivation of CMOS during MEMS etching and release steps, surface topography of MEMS, materials incompatibilities, and yield losses.

2.2. IC–MEMS MONOLITHIC FABRICATION TECHNIQUES

Before diving into the IC–MEMS monolithic fabrication techniques, it is essential to clarify the author's standpoint regarding the etymology and use of the terms "monolithic fabrication" and "monolithic integration" throughout the text. Their use interchangeably often creates inaccuracy in the literature.

When broken into its roots mono and lithic, monolithic means simply "one stone". Hence, "monolithic fabrication" naturally means all fabrication steps are carried out and completed on the same substrate—before its singulation. On the other hand, "monolithic integration" refers to any wafer-level or chip-level approach that incorporates materials, components, or complete systems, such that everything is unified on the same substrate material at the end. Consequently, monolithic fabrication refers to the method; monolithic integration, to the approach.

Such distinction rectifies erroneous claims of monolithic fabrication found in the literature [2]. For instance, when high-performance CMOS and MEMS wafers are fabricated in separated foundries and later integrated into a single substrate via direct wafer bonding [3]. In this scenario, the approach is monolithic integration; the method, however, is direct wafer bonding. Akin cases must be distinguished from genuinely monolithic fabrication because they differ in terms of technological challenges, limitations, and the range of possible techniques [4, 5].

The classification proposed here refers exclusively to the various techniques covered by monolithic fabrication methods. Even though there is already literature classifying monolithic IC–MEMS techniques using unlike terminologies [1, 6–8], the lack of

a rigorous benchmark to define them often creates classification inconsistencies. Consequently, different authors may classify the same work into distinguished categories, which is confusing. The classification suggested here adopts the thermal budget as the principal decisive player in differentiating the monolithic IC–MEMS categories. In summary, the process technology that contains the highest thermal budget is the one that rules the fabrication sequence: if the IC technology, then the IC-before-MEMS is the most natural technique of choice; else, the IC-after-MEMS. The IC-inter-MEMS technique mixes or shares the order of processes from both technologies to avert specific thermal budgets along the fabrication or other fabrication challenges.

2.2.1. IC-BEFORE-MEMS

Monolithic IC and MEMS integration using the IC-before-MEMS processing means that the MEMS structures are fabricated after the entire IC fabrication is completed until the back-end of line (BEOL). Other nomenclatures found in the literature for this technique include MEMS-last, Post-CMOS, and MEMS-after-CMOS fabrication [1, 7]. Fabricating the IC before the MEMS means that the total thermal budget from the MEMS steps must be limited ($< 450\,^{\circ}C$) not to undermine the metallization layers used for the IC interconnection or to avoid dopant re-distribution. The IC fabrication, consequently, holds the highest thermal budget in the manufacturing process.

The IC-before-MEMS technique enables using state-of-art CMOS wafers from a pure-play semiconductor foundry, while the MEMS processing can be realized on a dedicated MEMS foundry. Despite the technical possibility of utilizing a unified IC–MEMS foundry concept, it is pertinent to consider that the probability of cross-contamination on the CMOS streamlines reduces when the integration happens with a separated IC–MEMS logistic model. However, the foundries must ensure equipment compatibility—meaning, for instance, that the process wafers are of the same diameter and operate under similar conditions.

Both surface and bulk micromachining are possible for processing the MEMS structures. Additionally, the MEMS structures can be fabricated on top of or abutted to the CMOS circuit.

Fig. 2.1 shows the steps to fabricate a CMOS-based neural probe, the Neuropixels probe [9], using the IC-before-MEMS technique with a separated foundry logistic model. The IC was implemented with the TSMC 0.18 µm standard CMOS technology, using a five-metal-layer aluminum BEOL stack without dielectric passivation covering the top metal layer (M5). The MEMS post-processing was carried out in a dedicated MEMS foundry using a 200 mm wafer. The CMOS post-processing created TiN electrodes and used micromachining steps to define and release the probes.

The MEMS process starts with depositing a low-stress SiO_2 on top of the CMOS wafer and planarization with chemical mechanical polishing (CMP). Reactive ion etching (RIE) opens the vias, TiN is sputtered on the wafer, and the electrodes are patterned with RIE. Then, the bond-pads are exposed through the SiO_2 using RIE, and deep RIE (DRIE) etches the silicon down to 80 µm. After laminating a grinding tape on the wafer's front side, the wafer is thinned down and singulated across the whole surface. Finally, the wafers are mounted on UV tape, and the grinding tape is removed. The most significant

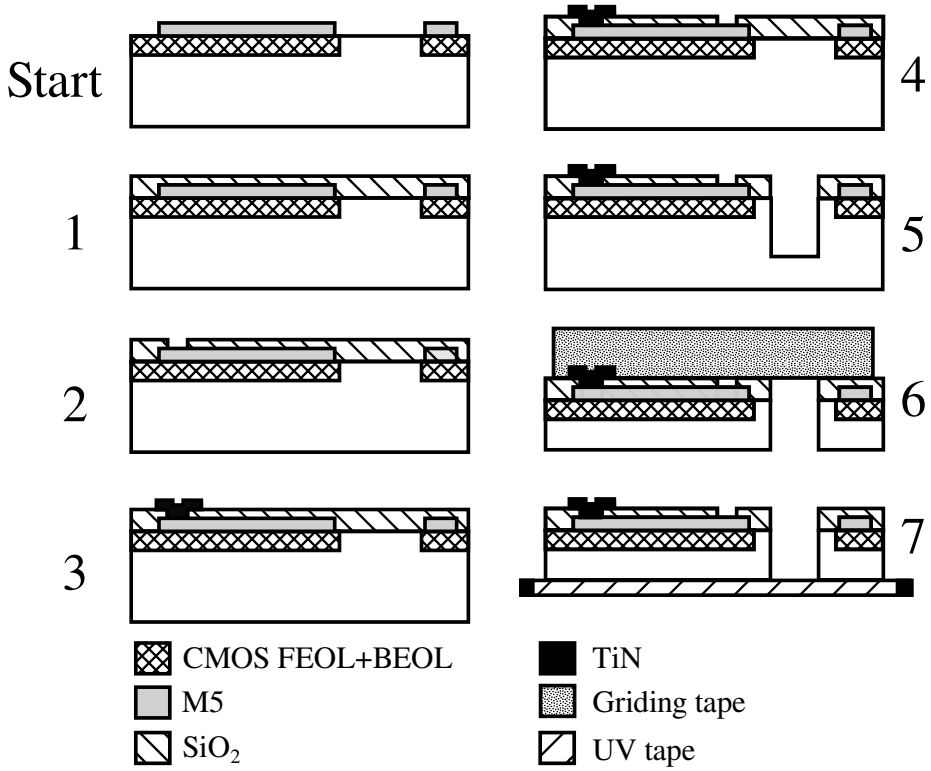

Figure 2.1: Schematic cross-sectional view of the main post-processing fabrication steps performed on top of 200 mm Si wafers with a five-metal-layer Al BEOL process. The fabrication steps use the IC-before-MEMS technique with a separated foundry logistic model. Adapted from [9].

advantage of such a technique is the possibility of incorporating high-performance ICs on a MEMS device.

On the other hand, besides the restricted thermal budget allowed for the MEMS steps, disadvantages of the IC-before-MEMS include the limited design freedom for the MEMS materials and structures. Furthermore, achieving the appropriate etching time to prevent damage to the underlying IC after completing all micromachining processes can be challenging.

Moreover, challenges in post-processing CMOS wafers include constraints related to the increased bow and wafer curvature due to the stress associated with stacking many thin-film layers. Such factors may create additional challenges during the optical lithography, and, if possible, stress-relief annealing should be performed.

2.2.2. IC-AFTER-MEMS

In the IC-after-MEMS fabrication, all required steps for a complete MEMS device are performed prior to the IC processing, typically including substrate planarization to enable subsequent IC fabrication. Planarization at the sub-micro scale is often a critical step in IC-after-MEMS fabrication as the defect density plays a significant role during IC processing.

Other nomenclatures found in the literature for this technique include MEMS-first, Pre-CMOS, and MEMS-before-CMOS fabrication. One of the motivations for fabricating the IC after the MEMS is the high thermal budget associated with the MEMS manufacturing steps. The IC-after-MEMS fabrication technique allows thermal budgets from the MEMS processes greater than 1100 °C, which enables the use of high-temperature processes to obtain high-performance epitaxial films or to release stress in thick layers. The MEMS devices can be protected with passivation layers (e.g., TEOS oxide) such that they will not be adversely affected by the hundreds of process steps required to complete the IC.

However, the IC process temperatures severely limit the selection of materials for the IC-after-MEMS integration: silicon, polysilicon, oxide, and nitride are the only candidates. Polymers, metals, carbon-based materials, and contaminating materials in the IC processing line are prohibited. Contacting the MEMS part to the IC part is preferably done by diffusions because metal-silicon interfaces cannot be made until reasonably late. Typically, this integration is less common in a separated foundry logistic model because pre-processed wafers are not allowed to be brought into standard CMOS fabs. Therefore, such integration is more common when access to a dedicated CMOS fab exists. Likewise, this integration is also impractical in fabless business models.

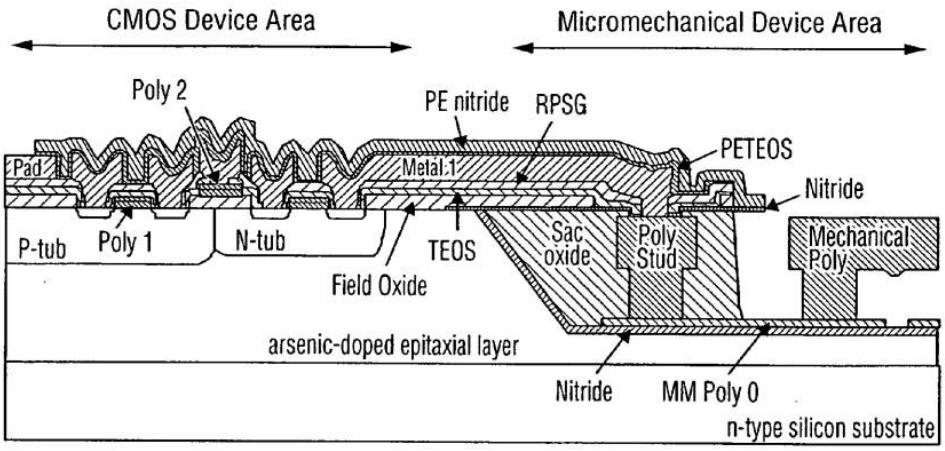

Figure 2.2: Schematic cross-section of the IC-after-MEMS fabrication process used to monolithically integrated polysilicon microstructures with CMOS technology for constructing inertial sensors. The technology was developed by Sandia National Laboratories. Picture taken from [10].

Fig. 2.2 shows a cross-section used to fabricate an inertial sensor developed by San-

dia National Laboratories. This work was one of the first demonstrations of the IC-after-MEMS fabrication. In this technique, the polysilicon microstructure is built in a trench and etched into the bulk silicon with anisotropic wet silicon etching. After the formation of the polysilicon microstructures, the trench is refilled with LPCVD oxide and planarized with a CMP step. Subsequently, the wafers with embedded microstructures are used as starting material in an entire CMOS process, fabricating CMOS circuitry in areas adjacent to the MEMS areas. The metallization is used to interconnect the ICs with the MEMS. The backend of the process requires additional masks to open the protective silicon nitride cap over the MEMS areas prior to the release of the polysilicon structures by silicon oxide sacrificial layer HF etching.

The fact that the polysilicon beams were released after the completion of the CMOS circuitry induced some literature to classify this work as IC-interleaved-MEMS instead of IC-after-MEMS [1]. On the other hand, there is no practical way to release the polysilicon structures before the CMOS completion. The high thermal budget used in the MEMS devices rules the fabrication order. Therefore, the IC-after-MEMS seems to be a more logical category for this fabrication technique [7, 8].

2.2.3. IC-INTER-MEMS

The IC-inter-MEMS fabrication uses a combination of IC and MEMS steps between the front-end (FEOL) and back-end of line. Other nomenclatures in the literature include Intra-CMOS micromachining, mixed IC–MEMS, and interleaved MEMS-and-IC processing [6]. Often this integration means a significant increase in mask count and process complexity, increasing overall costs.

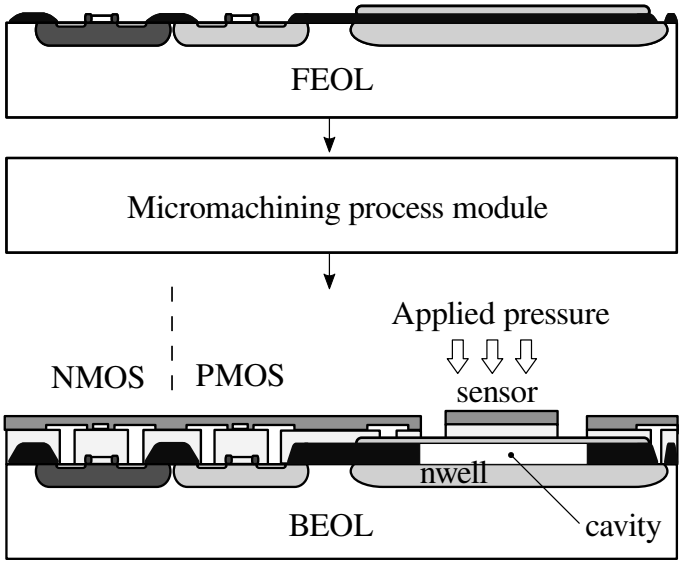

Figure 2.3: Schematic cross-section of Infineons' integrated MEMS technology for the fabrication of pressure sensors. Adapted from [11]

Commercially available examples of such integration, such as Infineons' integrated pressure sensors, use CMOS/BiCMOS processes with intermediate micromachining (Fig. 2.3) [11]. The fact that Infineon's has access to a unified in-house foundry facilitates the IC-inter-MEMS fabrication. Such access allows fine-tuning of the overall process sequence to minimize degradation in electronic and mechanical components. Business models based on complete outsourcing of the IC-inter-MEMS fabrication are impractical because a CMOS fab will probably not accept wafers back into their line after several micromachining steps have been performed elsewhere. Moreover, the overall costs become prohibitively expensive.

The fabrication sequence of the pressure sensor uses a 16-mask BiCMOS process that is stopped before the BEOL to insert a single-mask micromachining module. The primary pressure sensor structure is formed within the course of the BiCMOS process sequence. The n-well forms the lower electrode, a 600 nm field oxide serves as the sacrificial layer, and a 400 nm capacitor polysilicon serves as the structural layer and top electrode. The polysilicon membranes are released within the micromachining module by sacrificial layer etching, and the cavities are sealed. After perforating the membranes with a dry etching step, the sacrificial layer is etched using HF in a vapor state. Finally, the cavities are sealed with a process optimized for the vertical etch channels, yielding a typical cavity pressure of 300 mbar. After completion of the micromachining module, the regular BiCMOS aluminum-based BEOL is performed for the circuit interconnections.

PROPOSED CLASSIFICATION UNFOLDING

The study and implementation of the IC-inter-MEMS fabrication in this thesis motivated the author to distinguish between two possible versions and to unfold the IC-inter-MEMS into two different subcategories: the IC-interleaved-MEMS and the IC-interlaced-MEMS. The essential difference is how the IC and MEMS processes are combined or shared.

The IC-interleaved-MEMS often uses micromachining modules between the FEOL and BEOL steps, such that all micromachining processes are orthogonally defined to facilitate the fabrication of MEMS devices without impacting the optimal performance of the end product. The pressure sensor of Infineon [11] presented in the previous section is an example of such a technique. Despite being constructed from the same materials and processes utilized in the standard BiCMOS run, the pressure sensor structure was optimized to attain peak performance[1] without compromising the pre-existing ICs. This strategy offers a better optimization of the MEMS and the IC because the processes are orthogonal and, thus, minimally interfere with each other, either on the design or fabrication levels.

On the other hand, the IC-interlaced-MEMS sacrifices orthogonalization to favor sharing some fabrication processes between the IC and the MEMS devices. Suppose

[1] The work in [11] has not addressed performance tradeoffs or (co-)design parameter contradictions resulting from leveraging the pressure sensor fabrication from an unmodified BiCMOS process. Consequently, the author of this thesis assumes that there is no (significant) loss in performance based on the absence of discussion by the authors.

Infineon would have traded the peak performance of its pressure sensor structure for adhering to an unmodified BiCMOS process—thereby streamlining its fabrication—it could be considered an instance of utilizing an IC-interlaced-MEMS technique. This strategy brings other benefits, such as relaxing the fabrication complexity, often implying a reduced mask count, abbreviating the processing time, and decreasing the overall costs. An example of this strategy with a detailed fabrication process can be found in Chapter 4 of this thesis.

The diagram of Fig. 2.4 proposes a taxonomy for the IC–MEMS monolithic fabrication techniques in which the IC-interleaved-MEMS and the IC-interlaced-MEMS are subcategories of the IC-inter-MEMS.

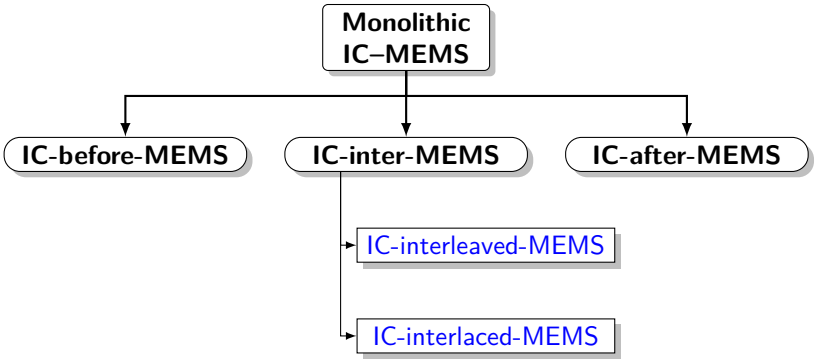

Figure 2.4: Proposed taxonomy for the IC–MEMS monolithic fabrication techniques. The IC-interleaved-MEMS and IC-interlaced-MEMS are new nomenclatures proposed in this chapter.

2.3. DISCUSSION

The integration of IC and MEMS through monolithic fabrication necessitates the utilization of diverse concepts, schemes, and strategies based on the application at hand. Familiarity with each technique's advantages, disadvantages, and challenges is crucial to making informed decisions regarding their selection, thus avoiding any potential process rectifications and additional fabrication costs. The integration process can be optimized by selecting the appropriate technique, ultimately leading to enhanced device performance and functionality.

For instance, if the MEMS device requires a thermal budget exceeding 450 °C, the IC-before-MEMS approach must be excluded from the fabrication process. In this case, the options are narrowed down to IC-inter-MEMS or the IC-after-MEMS. Additional factors, such as process complexity, should be considered to determine the optimal technique. The example highlights the importance of the thermal budget in establishing the sequence of process steps. It underscores the significance of assessing the thermal budget to select the most appropriate fabrication technique, which can enhance the quality of the resulting integrated device.

Applying the thermal budget as a criterion for categorizing distinct monolithic fabrication techniques is an endeavor to resolve conflicting categorizations in the litera-

ture. This approach aims to provide a unified parameter to address some divergences, thus facilitating the standardization and differentiation of various techniques. Likewise, creating novel terminologies to describe monolithic fabrication techniques is an effort to introduce a more clear, consistent, and unified language within the scientific community. Developing a standardized lexicon can resolve the ambiguities and disparities among existing terminologies, allowing for improved communication and understanding across different fields and disciplines.

2.4. CONCLUSION

This chapter suggested a taxonomy of IC–MEMS monolithic fabrication techniques. Literature covering such techniques was addressed to illustrate the main differences, pros, and cons.

A distinction between the terms “monolithic fabrication” and “monolithic integration” settled the difference between the method and the approach. In this chapter, only literature covering truly IC–MEMS monolithic fabrication techniques was addressed.

Even though prior literature has already classified different monolithic IC–MEMS techniques, the lack of a rigorous criterion engendered some inconsistencies. This chapter proposed the “thermal budget” as a criterion to order the process sequence and, thus, the technique of choice.

Finally, a new branching of IC-inter-MEMS was proposed. The subcategories consist of IC-interleaved-MEMS and IC-interlaced-MEMS. The latter shares some fabrication processes between the IC and MEMS to simplify the manufacturing, which usually implies finding the best performance trade-off on the design level. The former offers a better optimization of the MEMS and the IC because the processes are orthogonal and, thus, decoupled, which minimizes process interference.

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3

IC–MEMS CO-DESIGN: A HOLISTIC APPROACH

In nature, there is no separation between design, engineering, and fabrication; all constitute the same framework intended to build a functional, seamless, and cohesive whole.

Proposition created by the author of this thesis and inspired by the ideas of architect, designer, and professor Neri Oxman.

3.1. INTRODUCTION

The various intermeshed challenges associated with the monolithic fabrication of integrated circuits (ICs) and micro-electromechanical systems (MEMS) encourage the development of a design methodology that can systematically dissociate the problems into sub-problems that are simpler to solve. Moreover, thinking about a design strategy that can minimize the costs and the number of product iterations is a crucial task to be performed before starting any microfabrication process in the cleanroom.

Prior knowledge of the relations between the different materials, deposition methods, equipment capability, and the various parameters (temperature, contamination, stresses between deposited layers, among others) substantially aids the co-design phase. Therefore, the design strategy to be adopted shall use a bird's eye view into the whole envisioned system (holistic) such that the designer may anticipate, extract, and adequately compensate for the processes interplay during the IC–MEMS co-design phase. This design methodology is termed here as holistic iterative co-design thinking.

3.2. HOLISTIC ITERATIVE CO-DESIGN THINKING METHODOLOGY

The IC–MEMS holistic iterative co-design thinking exploits splitting, combining, adding, or removing process steps and reiterating this information into the co-design step. Subsequently, different device attributes can be revised, adjusted, and properly accommodated over the design domain. This iterative process runs until the designer finds a solution that meets the performance specifications (specs) (Fig. 3.1).

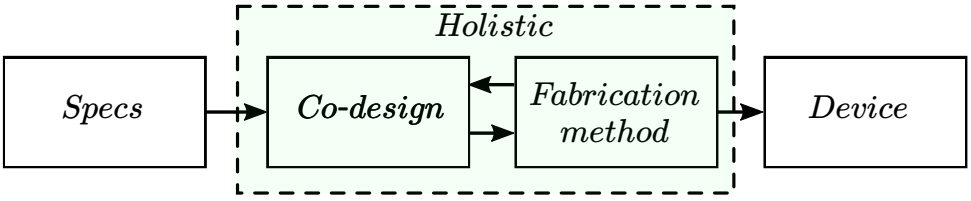


Figure 3.1: Block diagram representing the holistic iterative co-design thinking methodology.

3.3. SPECIFICATIONS

Specifications refer to the set of requirements to be satisfied by the device. There are three types of specifications: functional, performance, and operational.

The functional specification defines the functions that a system or component must perform. A function is any specific task, behavior, action, or process that describes the relationship between the input and output of the system—for instance, a signal amplification that happens in the electrical domain or a mechanical actuation that happens in the mechanical domain.

The performance specification describes the performance of the system or component. In other words, it sets in quantitative terms the qualitative metrics that each function must perform—for instance, the expected signal-to-noise ratio of an electrical signal or a mechanical actuator's driving capability (i.e., mechanical force).

The operational specification delineates the conditions (temperature, humidity, pressure, radiation, among others) in which the device or system must operate. The operational specifications play an important role in biomedical devices as the environmental conditions may drastically change depending on the application (e.g., wearable, implantable, disposable, degradable) and the placement of the device in the body (e.g., cortex, heart, bladder, skin).

The design uses all combined specifications, including functions belonging to a multidimensional design domain. Usually, a multidimensional design domain entails the combination and interaction of multiple variables (e.g., electrical signals or material attributes) in a rather complex manner.

3.4. FUNCTIONAL DECOMPOSITION OF DESIGN DOMAINS

In order to find a better way to explore the design space, a multidimensional complex design problem is decomposed into a set of individual one-dimensional problems that are less complex to solve [1, 2]. This decomposition can be achieved by firstly arranging and mapping the various functional requirements of the device into their respective set of one-dimensional design domains.

This method is called functional decomposition. Its primary purpose is to find design domains that are easier to solve and whose parameters are entirely (or strongly decoupled) from other design domains. The one-dimensional design domain is categorized into a unique branch of knowledge to which the function itself belongs. The main classification used for these design domains is mechanical, electrical, optical, chemical, magnetic, and physical domains.

Once the design domain is decomposed into individual functional groups, one can optimize each function to meet the performance requirements. The challenge here is finding and keeping the design domains orthogonal, meaning that the optimization of functions in different design domains does not interfere (or minimally interfere) with each other.

Likewise, this orthogonality approach helps order subsequent microfabrication processes used to construct such functions. When IC and MEMS microfabrication processes are organized such that there is zero or minimum process interference between each other, a process orthogonalization is found (Fig. 3.2) [3].

Hence, it is crucial to identify which aspects shall be used to describe the central process interplay during the fabrication of IC and MEMS processes. Section 3.6.1 of this chapter further elaborates on the IC–MEMS process interplay.

Before getting there, the following section explores the methods used in the co-design phase.

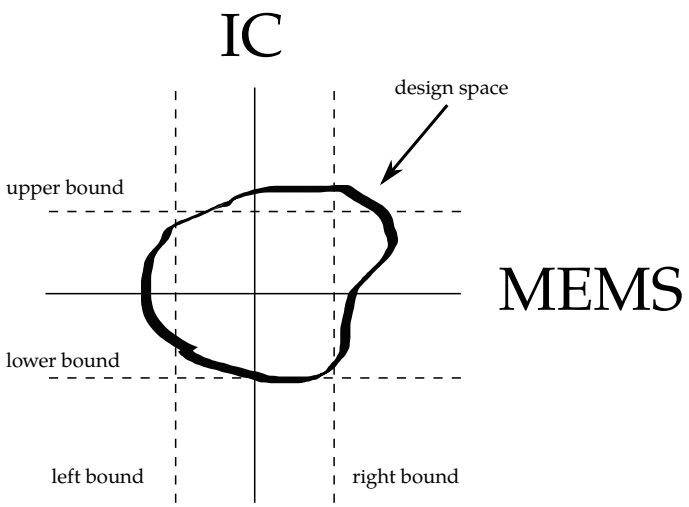


Figure 3.2: IC–MEMS design domain illustrating design orthogonalization. Adapted from [3]

3.5. CO-DESIGN PHASE

After extracting the device's functional and performance requirements, the specs feed the co-design phase. Co-designing involves finding solutions that comply with the performance specifications of each particular one-dimensional domain while solving for possible trade-offs between each adjoined domain.

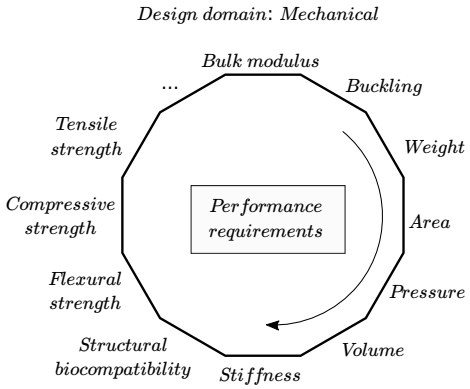
For instance, in the mechanical design domain of Fig. 3.3a, a list of important physical features are firstly identified and subsequently used as the basis to design the various structures of the device. Suppose the device comprises a beam structure such as a cantilever or a probe. One shall identify the range of thickness, length, width, weight, among other parameters, ensuring the device's proper operation under specific environmental conditions.

As an exemplification, the range of axial and shear load forces applied to the beam may cause buckling or excessive bending, leading to a catastrophic failure. Hence, functional design calculations shall be used in order to solve and find an optimal design solution.

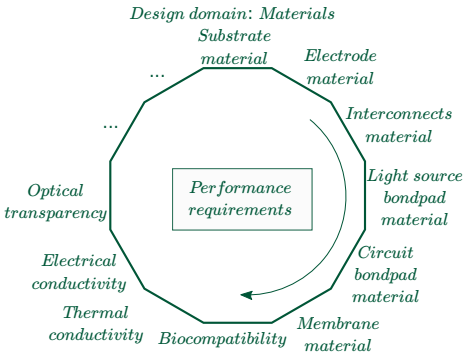
After concluding the design in the mechanical domain, one can run similar procedures in the next design domain (Fig. 3.3c) and so forth (Fig. 3.3e). Eventually, an initial global solution (Fig. 3.4) is met, and possible design interfaces between adjoined domains (mechanical, electrical, optical, etc.) still need to be solved.

For example, the physical dimensions of the light source (optical domain) on the probe may override the minimum possible width (physical domain) allowed to be used. This information is exploited to refine specific physical features of the device, such as the range of thickness that prevents device buckling (mechanical domain).

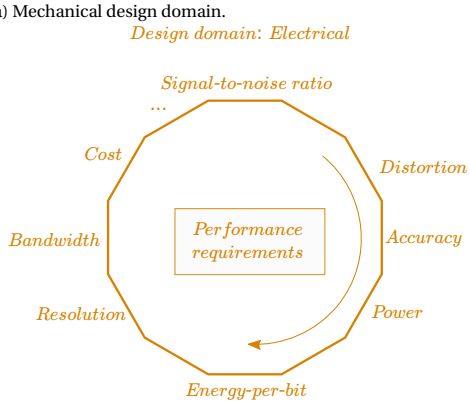
Moreover, if the design uses the minimum beam width, the maximum number of interconnects (at a given minimum width and spacing) is also set by this constraint. Solv-



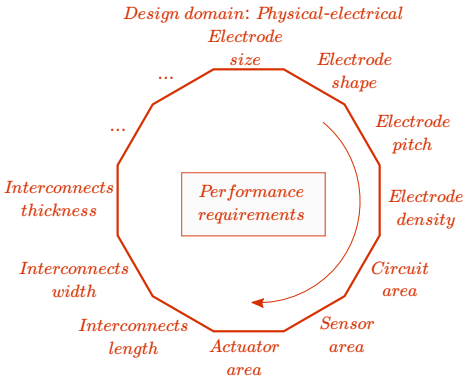
(a) Mechanical design domain.



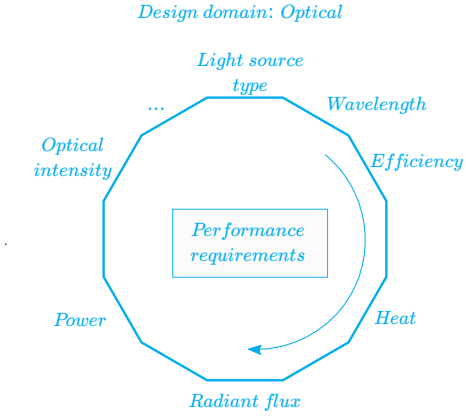
(b) Materials design domain.



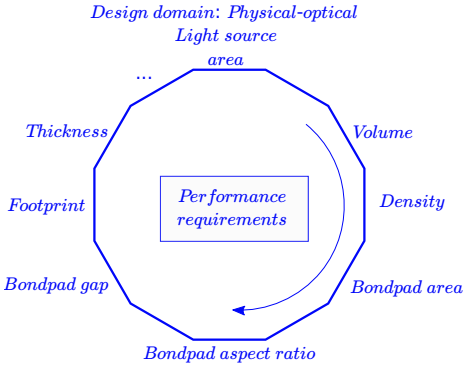
(c) Electrical design domain.



(d) Physical domain associated with the electrical design.



(e) Optical design domain.



(f) Physical domain associated with the optical design.

Figure 3.3: Set of possible IC–MEMS design domains. Other domains may be included as per the application.

ing such interfaces is not always straightforward and requires a holistic view from the designer to cope with various multidisciplinary aspects and design conflicts.

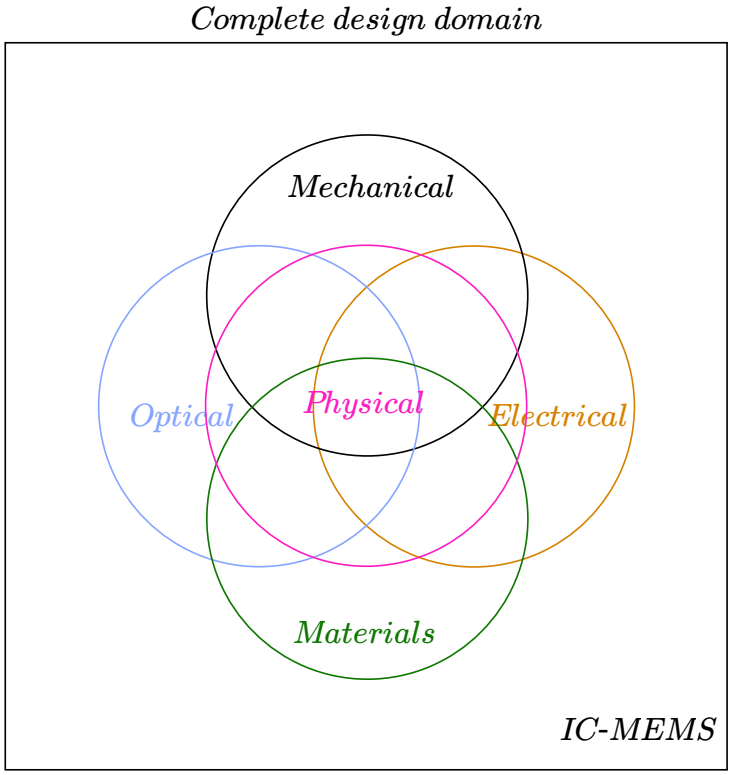


Figure 3.4: Complete IC–MEMS design domains outlining the design interplay among different domains.

3.5.1. WAFER LEVEL DESIGN CONSIDERATIONS

The wafer is the carrier of all microfabrication process steps. Therefore, wafer-level design is a must because all decisions on the device level inevitably take place at the wafer level first. Deposition of layers, for instance, affects the global topography of the wafer. Hence, process corrections might be vital to preventing the wafer's warp and bow beyond its operational limits.

Furthermore, electrostatic forces dramatically increase as feature sizes scale down into the sub-micron level, and these features form sharp edges and notches. If not properly considered, it can impact the wafer's whole structure, especially if thin-film membranes are already patterned or the process equipment uses the electrostatic clamping chuck (ESC).

Likewise, capillarity forces applied on thin features (e.g., microchannels in microfluidics) may affect the wafer. These capillarity forces may happen, for instance, during wet-etching or cleaning procedures due to the surface tension created by the solid-liquid interface.

Understanding what is happening at the wafer level due to a design choice at the device level plays a central role in semiconductor processing for high yield rates and

reliability.

3.6. FABRICATION METHOD

In Chapter 2, the different fabrication strategies (IC-before-MEMS, IC-inter-MEMS, and IC-after-MEMS) used in monolithic IC–MEMS were addressed. As discussed, the fundamental difference among them, as the name suggests, refers to the fabrication order of the IC and MEMS processes.

The order of the process steps (as will be explained later) is essential to define the fabrication protocol and to detect important parameters that eventually need to be compensated or fine-tuned during the co-design phase to facilitate the microfabrication phase. This iterative design process runs until a valid design domain is found under the boundary conditions set by the specifications.

3.6.1. FUNCTIONAL DECOMPOSITION OF IC–MEMS FABRICATION

This section describes how to use the functional decomposition method again to segregate the complex multidimensional problems associated with the IC–MEMS monolithic fabrication into one-dimensional subproblems, which are more manageable. Otherwise stated, a problem on a macroscale level partitions into multiple subproblems on a mesoscale level and is subsequently scaled further down into micro-level units (Fig. 3.5) [4].

The meso-level hierarchy includes eight different functional groups (or dimensional groups) identified and classified with some dedicated literature on microfabrication processes [5]. The microscale level includes pivotal questions used as guidelines to anticipate and solve more specific microfabrication challenges. With the general macro problem decomposed into individual questions, an optimum solution that meets orthogonality is easier to find.

The first functional group on the mesoscale refers to selecting a wafer that meets the required specifications. The subsequent functional group, entitled 'materials compatibility', deals with how to process materials and prevent deleterious outcomes by understanding the interplay among the materials.

In the functional group entitled 'process–device interactions', it is investigated how processes may interfere with already constructed devices. The functional group 'foundry and equipment capability' aims to consider specific equipment conditions or limitations prior to wafer loading.

The functional group 'design rules' sets good practices to account during the design phase and the layout. The subsequent functional group, entitled 'photomasks considerations', addresses requirements for the photomasks specifications. The sequence of process steps aids in ordering the microfabrication protocol. Finally, the functional group entitled 'reliability' covers aspects related to the production yield of the device.

Below, one may find the specific questions related to each functional group. Naturally, the following questions can never cover all fabrication problems and conflicts thoroughly. The reader must explore these canonical questions as the basis to elaborate on more tailored and refined questions on one's specific problems.

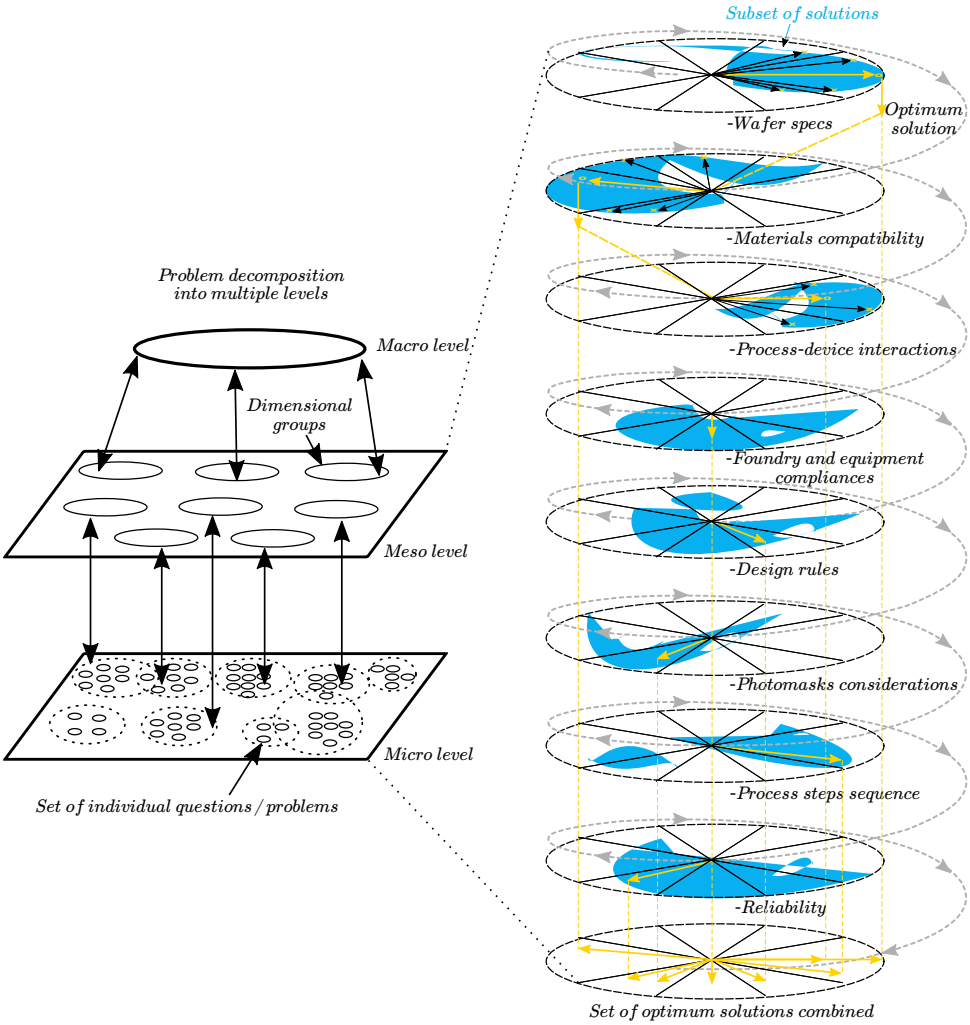


Figure 3.5: Application of the problem decomposition and optimum solution synthesis for the microfabrication process interplay.

- Wafer specifications:
  - What are the important wafer properties to be combined? Mechanical, electrical (p-type or n-type), crystallographic orientation, substrate material (silicon, silicon carbide, sapphire, quartz, among others), optical, and so forth.
  - What is the surface polishing type needed for the application? Single-sided polished (SSP) or double-sided polished (DSP)?
  - Is silicon-on-insulator (SOI) needed for the application?
  - Any other important wafer specifications? For instance, growth method

(Czochralski or Flat zone), doping type, resistivity, warp, total thickness variation (TTV), handle and device thickness, micro-roughness, flatness, bow, surface defectivity, etc.

- Materials compatibility:
  - How to prevent interference or catastrophic failure by material contamination?
  - What is the maximum temperature allowed at each processing step?
  - Are there any mismatches in the thermal expansion coefficient of the different films?
  - How to process and clean substrates with polymeric layers?
  - Can lift-off processes be used?
  - How important is the adhesion of different materials and layers?
- Process–device interactions:
  - How to minimize or prevent process interactions with already constructed devices or materials?
  - How to handle different thermal budgets? Do the thermal treatments add to diffusion profiles?
  - Does the stress-relief anneal affect structures already fabricated?
  - Does the process have any collateral thermal budget that can be transferred to the wafer and affect already fabricated structures?
- Foundry and equipment capabilities, constraints and compliances:
  - What processes are allowed and what is not allowed?
  - At which conditions can the wafers be loaded in the equipment? Are polymers allowed? Must RCA[1] cleaning be performed prior to loading?
  - What is the typical wafer dimension used by the foundry? Are the wafer dimensions compatible with the semiconductor foundry or equipment (diameter, thickness)?
- Design rules:
  - What is the impact of curvilinear structures on the process?
  - What is the critical dimension (CD) of the lithographic feature at the wafer level?
  - What is the minimum allowed spacing between lines?

[1] RCA stands for Radio Corporation of America. RCA cleaning is a standard set of wafer cleaning steps which need to be performed before high-temperature processing steps (oxidation, diffusion, CVD) of silicon wafers.

  - Are dummy fillings needed for chemical mechanical polishing (CMP)? How does it affect the device's operation? [2]

- Photomask considerations:
  - What are the minimum specs to be considered on each photomask?
  - Which photomasks are critical, which are non-critical?
  - Is etch undercutting compensation or optical proximity correction (OPC) required?

- Process steps sequence:
  - Which order of processes minimizes or prevents interactions?
  - Should front-side processing be completed before back-side processing? How to protect the side that is in contact with the chuck?
  - Is fence removal necessary, for instance, in the context of back-side processing following the conclusion of front-side processing?
  - What processes can be done after through-wafer etching?
  - Can any steps be done after thin-membrane formation? How to handle vacuum chucking and wafer singulation?

- Reliability:
  - What is the production yield?
  - How do stresses build up when more layers are deposited?
  - How to solve for the mechanical stresses built after successive thin-film deposition?
  - What are the breakdown voltages of thin oxides?
  - Is wafer handling critical? Which type of tweezers must be used to handle the wafers?
  - Are there any requirements for adjusting or calibrating process-dependent variables? For instance, is it necessary to include isofocus bias to account for variations in the width of lithographic features resulting from changes in focus and exposure parameters?

The right side of Fig. 3.5 illustrates a top-down plan on how to use this method [7, 8]. First, the functional groups classify problems that are ideally orthogonal to each other. Specific subproblems under each functional group discern a set of questions that describe the problem more accurately. A pool of answers builds a subset of possible solutions (i.e., black arrows) that includes an optimum point (i.e., yellow arrows). This screw-like procedure runs on the following functional groups until the last one is solved. Lastly, the designer may combine all optimum solutions into a unique orthogonalized solution set arising from each functional group.

[2] For instance, traditional squared dummy metal fillings may cause hybrid modes in nearby waveguides, causing the power to disperse across different frequencies. Moreover, since the dummies are floating (not connected to ground potential), they can get coupled with parasitic capacitances to the signal path—especially when operating at higher frequencies [6].

3.7. DISCUSSION

Likely, the eight functional groups offered in the previous section may not be enough or may not cover all microfabrication challenges and details thoroughly.

Nevertheless, it may provide a first step to orient and fragment the problems into different subproblems and individual problems. Consequently, it becomes easier to find the set of subsolutions and optimum solutions of each functional group (Fig. 3.5).

Additionally, the answers can provide the designer a means to:

1. Look upfront into specific microfabrication impediments or hindrances.
2. Invent new solutions or procedures to such specific microfabrication challenges.
3. Readjust parameters or variables in the co-design phase.
4. Order the process steps orthogonally.

For example, one could find specific microfabrication impediments associated with wafer-equipment compatibility, materials compatibility, or thermal budget compatibility.

In wafer-equipment compatibility, the process equipment may not load specific wafer sizes or wafers with specific properties, such as transparent wafers. Materials and thermal budget compatibility refer to limitations or restrictions in using specific materials or temperatures. Eventually, such challenges could provide means for creating new ideas or breaking paradigms on how to process wafers.

Furthermore, specific materials attributes (e.g., layer thickness, coverage area, materials type, and others) can be revised in the co-design phase to compensate for specific process interactions in the microfabrication stage. As a result, one may find solutions based on alternative or non-orthodox materials. Ideally, the materials selection and the order of the process steps are defined to meet process orthogonality.

3.8. CONCLUSIONS

This chapter presented a design methodology for the monolithic fabrication of ICs and MEMS. This methodology is named here as holistic iterative co-design thinking.

The design strategy uses a holistic approach comprising a co-design and microfabrication phase that exchanges mutual design information iteratively. This lateral design approach is essential to account for the interplay between IC–MEMS during semiconductor microfabrication. Accordingly, the co-design phase uses predictive information from microfabrication processes to reorganize or adjust specific design information in a synergic-like manner.

Moreover, the methodology uses functional decomposition to break down complex multidimensional design problems into orthogonal functional groups that are more manageable. As a result, interference among the various microfabrication processes is nullified or minimized.

The methodology presented in this chapter may equip the designer with tools to solve various problems that are usually complex or present a high level of interdependence. Additionally, it can provide the designer with a means to look into specific micro-

fabrication problems ahead of time, invent new solutions, readjust parameters or variables in the co-design phase, and order the process steps orthogonally.

The next chapter presents the integration of a BiCMOS smart sensor with a silicon-based organ-on-a-chip device (OOC) using the design methodology elaborated in this chapter. This integration allowed *in situ* temperature measurements of the cell culture with a resolution of less than ± 0.2 °C with a time response ten times faster than the time constant of the convection-cooling mechanism found in the culture medium.

Chapter 5 elaborates on designing a smart optrode using custom BiFET technology to enable the readout of infra-slow local field potentials in the central nervous system of animal subjects utilizing optogenetics.

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4

Monolithic Integration of a Temperature Sensor on a Silicon-based Organ-on-a-chip (OOC)

Parts of this chapter have been published in IEEE Biomedical Circuits and Systems Conference (BioCAS), 2018, pp. 1-4, doi: 10.1109/BIOCAS.2018.8584834 and in Sensors and Actuators A: Physical, Volume 317, 2021, 112439,ISSN 0924-4247 [1, 2].

4.1. BRIEFING OF THIS CHAPTER

This chapter's contents are divided and based on two publications that reported the monolithic integration of a temperature sensor on a silicon-based organ-on-chip platform—the Cytostretch.

In the first part, the work focused on the circuit design and the microfabrication of a temperature sensor using an enabling BiCMOS technology. This endeavor mainly aimed to explore and characterize the semiconductor technology employed to construct the circuit and assess its performance considering a future co-fabrication with the Cytostretch platform.

The second part describes the processes carried out for the monolithic fabrication of the temperature sensor with the Cytostretch. In doing so, the design methodology benefited from some of the techniques elaborated in Chapter 3. Specifically, the co-design phase exploited the information from the through-wafer etching step of the Cytostretch to find a more cost-effective solution regarding area usage and process complexity.

The through-wafer microfabrication step utilizes Bosch deep reactive-ion etching (DRIE), and it requires a stop mask for landing on the PDMS membrane. Silicon dioxide (SiO_2) is an excellent stop mask material due to its high selectivity (400:1) against the Sulfur hexafluoride (SF_6) attack that occurs in the Bosch process. Moreover, it can also function as a dielectric for the metal-insulator-metal (MiM) capacitor included in the signal generation unit of the temperature sensor. Hence, a single SiO_2 deposition implemented two different functions across different design domains in an interlaced-like style: a stop mask in the Bosch process, which implements its functionality in the physical domain, and a dielectric in the MiM capacitor, which implements its functionality in the electrical domain.

However, a design parameter contradiction exists because, on the one hand, it is advantageous to minimize the oxide thickness to maximize the capacitance-per-area, whereas its increase improves the Bosch process reliability.

To solve this problem, a minimum thickness ($2\,\mu m \pm 20\%$) ensured the safe landing on the PDMS membrane, whereas an increase in the capacitor area around the available silicon area ($2\,mm \times 7\,mm$) counteracted the capacitance loss.

This solution enabled the combination of a single deposition step in both the IC and the MEMS design domains while saving lithographic costs and process complexity. As a result, the circuit integration expended more silicon area.

PART I: DESIGN AND CUSTOM FABRICATION OF A SMART TEMPERATURE SENSOR FOR AN ORGAN-ON-A-CHIP PLATFORM [1]

4.2. ABSTRACT

This part reports on the design and fabrication of a time-mode signal-processing *in situ* temperature sensor customized for an organ-on-a-chip (OOC) application. The circuit was fabricated using an in-house integrated circuit (IC) technology that requires only seven lithographic steps and is compatible with the OOC MEMS fabrication process. The proposed circuit is developed to provide the first out-of-incubator temperature monitoring of cell cultures on an OOC platform employing a monolithic fabrication. On-wafer measurements reveal a temperature resolution of less than $\pm 0.2\,^{\circ}\mathrm{C}$ (3σ) and a maximum nonlinearity error of less than 0.3% across a temperature range from $25\,^{\circ}\mathrm{C}$ to $100\,^{\circ}\mathrm{C}$.

4.3. INTRODUCTION

Incubators for cell cultures are used to grow and maintain cells under optimal temperature alongside other key variables, such as pH, humidity, atmospheric conditions etc. As enzymatic activity and protein synthesis proceed optimally at $37.5\,^{\circ}\mathrm{C}$, a temperature rise can cause protein denaturation, whereas a drop in temperature can slow down catalysis and polypeptide initiation [3].

The temperature inside the incubator is gauged according to a sensing element that does not undergo physical contact with the cell culture. Therefore, the incubator's temperature readout aligns better with the temperature of the moisture inside the incubator, which does not necessarily capture the local fluctuations in temperature experienced by the cells. An even more critical aspect is that molecular and cellular biologists often need to inspect the cells under an optical microscope outside the incubator, thereby exposing the culture to a dramatic change in temperature. As many molecular processes are temperature-dependent, time outside the incubator can significantly impact cell health. In fact, out-of-incubator temperature and its change over time are unknown variables to clinicians and researchers, while a considerable number of cell culture losses are attributed to this reason [4–7]. To accurately monitor the temperature of the culture throughout cell growth, an *in situ* temperature sensor with at least $\pm 0.5\,^{\circ}\mathrm{C}$ of resolution is of paramount importance. This allows the growth of the cultured cells to be optimized.

To the author's best knowledge, no *in situ* temperature-sensing fully integrated on an organ-on-a-chip (OOC) platform exists to date. This is the first time such integration is being performed using a custom-designed circuit fabricated on the same silicon substrate as that of the OOC. For a better visualization of the system, the reader is referred to Fig. 4.1.

The simple, robust, and custom IC technology used for the sensor fabrication grants a very cost-effective integrated solution in virtue of the reduced cost per wafer along

[1] Part I is based on the publication "Design and Custom Fabrication of a Smart Temperature Sensor for an Organ-on-a-chip Platform", 2018 IEEE Biomedical Circuits and Systems Conference (BioCAS), 2018, pp. 1-4, doi: 10.1109/BIOCAS.2018.8584834.

with the large silicon area available on the platform [8]. Moreover, no further complicated assembly and subsequent protection of the pre-fabricated components is required. This minimizes the number of extra processing steps, along with the related handling risks, leading to higher yields. Finally, the freedom enjoyed by the MEMS-electronics co-design offers a large degree of versatility to accommodate electronics in a range of different OOC shapes and structures.

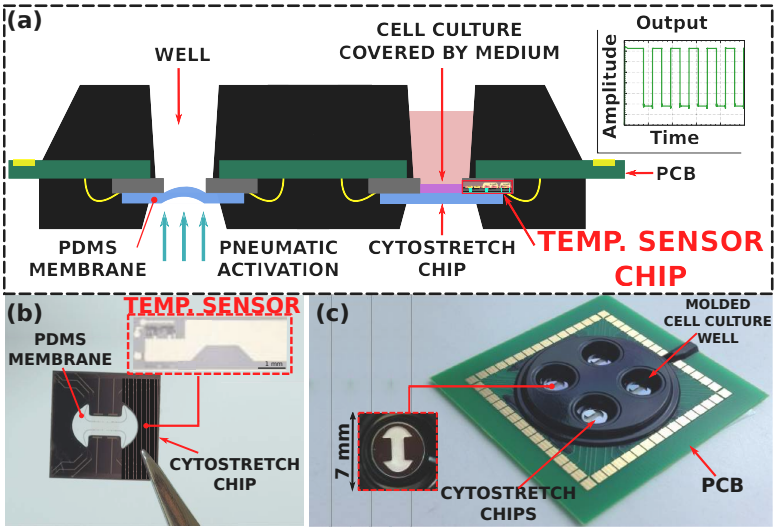


Figure 4.1: The OOC platform (cytostrech device [9]) used to integrate the temperature sensor chip: a) cross-section of the system, b) top-view detailing the silicon die comprised of a PDMS membrane and the monolithically integrated temperature sensor, c) optical image of the multi-well plate including four cytostretch chips. Reproduced with permission of the authors.

4.4. BLOCK DIAGRAM OF THE INFORMATION PROCESSING TASKS

The smart sensing module was designed to detect the *in situ* temperature of the culture and convert it into a periodic binary electronic signal, which carries the temperature information encoded in the time domain (Fig. 4.2). The main functional block of the smart sensing module is a temperature-to-time converter (TTC) that implements the conversion of the temperature information into a time-domain representation. In this way, the overall system level is more energy efficient because the data transfer is carried out through one wire only. As a result, the energy per sample is reduced compared to that required by conventional digital designs [10]. In addition, the conditioned signal becomes more robust against noise and interference.

To realize this time-domain functionality, the system consists of two main blocks: a

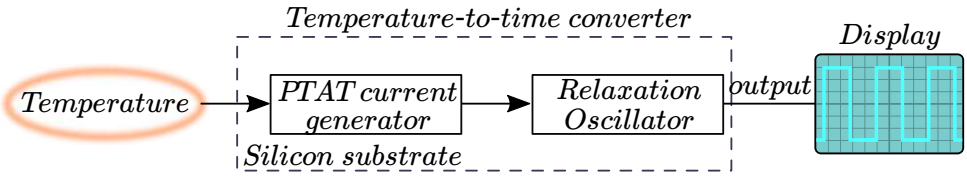


Figure 4.2: Main blocks of the smart BiCMOS temperature sensor: a PTAT current generator and a relaxation oscillator.

proportional to absolute temperature (PTAT) current generator (employing NPN bipolar transistors to sense the temperature information) and a relaxation oscillator.

4.5. SYSTEM DESIGN

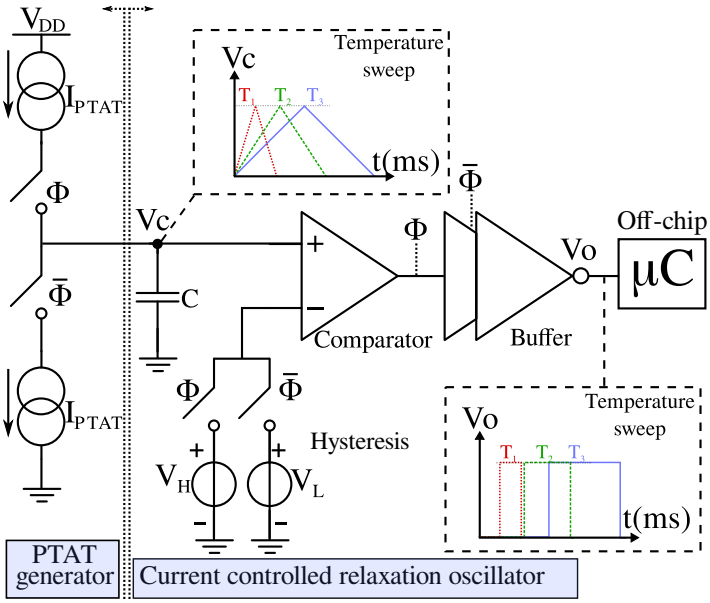
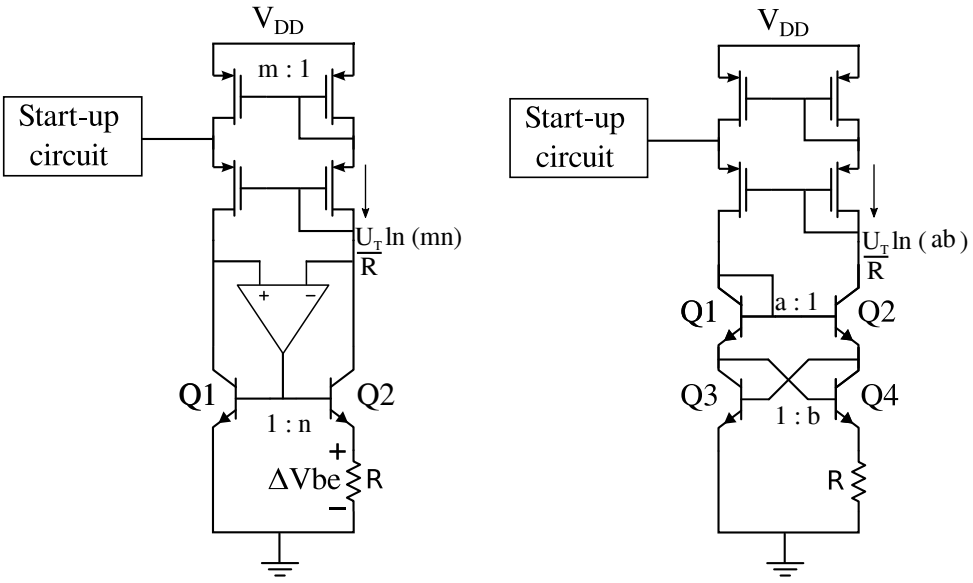


Figure 4.3: System-level design detailing the main blocks: a PTAT generator and a current-controlled relaxation oscillator

The circuit operation can be understood through an inspection of Fig 4.3. After start-up, the output of the comparator is set to a logic “0”, the current source is switched on and the charging cycle takes place. During this cycle, the PTAT current generated is integrated on the capacitor (C), forcing the voltage (V_C) to ramp up. This voltage is compared to two different voltage references that are produced by the hysteresis block: the high and low thresholds (V_H and V_L) associated with the end of the charging and discharging cycles, respectively.



(a) Design 1: OTA for the base current feedback

(b) Design 2: cross-quad translinear loop

Figure 4.4: Different designs used to implemtent the PTAT circuit using the EKL BiCMOS technology.

When V_C equals V_H, the output of the comparator switches its logical state and the discharging cycle takes place, discharging the capacitor through the PTAT current sink. When V_C reaches V_L, the discharging cycle ends and the whole process repeats itself again, indefinitely. The comparator outputs a signal, the period of which is IPTAT (inversely proportional to the absolute temperature) according to the following equation:

$$T = \frac{2 \cdot C \cdot \Delta V}{I_{\text{PTAT}}}, \tag{4.1}$$

where ΔV is the difference between the two threshold voltages V_H and V_L.

4.5.1. PTAT GENERATORS

For the PTAT current source and sink generators, two different designs were constructed (Fig. 4.4).

The first PTAT current generator (Fig. 4.4a) yields a current according to the voltage drop across resistor R: $\Delta V_{\text{BE}} = V_{\text{BE1}} - V_{\text{BE2}}$. Since this voltage is the difference of the two V_{BE} voltages, the current produced, $I = \Delta V_{\text{BE}}/R$, is PTAT. Cascode current mirrors with a m:1 ratio send a copy of the current to the integrator. The opamp acts as a nullor to keep the collector voltages the same, regardless of variations in the power supply or in the temperature, as well as providing the necessary base currents to the bipolar transistors. An expression of the current is:

$$I = \frac{U_T}{R} \ln\left(\frac{I_{C2} I_{S1}}{I_{S2} I_{C1}}\right) = \frac{U_T}{R} \ln(mn), \tag{4.2}$$

where U_T is the thermal voltage, I_S is the saturation current (which is dependent on the emitter area), m is the current mirror ratio and n is the bipolar emitter area ratio. Therefore, the responsivity of this cell is mainly determined by the current mirror and emitter-area ratios. For this design, values of five and four for m and n, respectively, were chosen. In addition, because of the self-biasing mechanism involved in this PTAT cell, this generator shows a second operating point when all currents are equal to zero. Hence, a start-up circuit is of paramount importance to guarantee the proper operation of the circuit.

The second PTAT generator (Fig. 4.4b) uses a translinear cross-quad as a PTAT cell [11]. Following the translinear network [11, 12], the voltage drop ΔV_{BE} across the resistor is now computed as:

$$\Delta V_{BE} = V_{BE3} + V_{BE2} - V_{BE4} - V_{BE1}. \tag{4.3}$$

The expression for the current thus becomes:

$$I = \frac{U_T}{R} \ln\left(\frac{A_1 A_4}{A_2 A_3}\right). \tag{4.4}$$

The responsivity here is determined by the emitter areas of the four bipolar transistors, A_1–A_4. Hence, this topology is less sensitive to any mismatch in the cascode current mirror. However, the circuit is slightly sensitive to the finite current gain of the bipolar transistors. For this design, A_1 and A_4 were chosen to be four times larger than A_2 and A_3.

4.5.2. RELAXATION OSCILLATOR

The relaxation oscillator is realized by a feedback control performed by the current integrator, the comparator, and the hysteresis circuit.

The current integrator performs the time integration of the PTAT current across the MIM capacitor, thus measuring the total electric charge. Alternative pathways for the PTAT current were implemented to ensure that there is always a route for the current to flow to ground when the main path is blocked by switches M1 and M2 (Fig. 4.5a).

The comparator (Fig. 4.5b) consists of a differential input, single-ended output stage and a CMOS inverter as a gain stage. The CMOS inverter ensures that the final comparator output reaches both rail values (GND and V_{DD}).

The hysteresis circuit was implemented with nine stacked diode-connected bipolar devices biased with a copy of the PTAT current so as to produce the voltages V_H and V_L, at 37 °C, of 6 V and 3.5 V, respectively. Through the use of diodes (instead of, e.g., resistors), the voltage ΔV of the hysteresis circuit was made inversely proportional to the absolute temperature (IPTAT) to increase the circuit responsivity with respect to the period.

4.6. SIMULATIONS

Circuit simulation results of both PTAT cells as a function of the temperature are shown in Fig. 4.7.

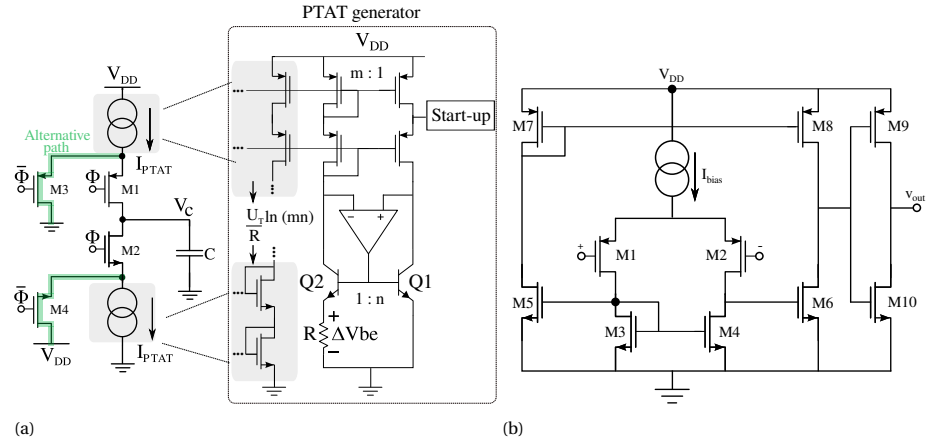


Figure 4.5: Circuits used to implement the relaxation oscillator: a) integrator detailing the implementation used to provide an alternative path to the currents, and b) comparator using a differential input, single-ended output stage.

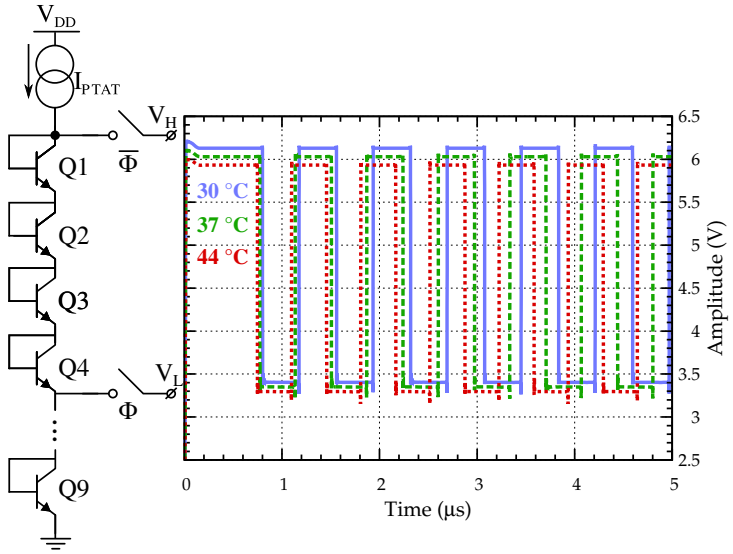


Figure 4.6: Hysteresis circuit used to yield the threshold voltages for the comparator operation, V_H and V_L, and simulated output waveform generated.

Considering the value of resistance R used of 300 Ω, the expected responsitivities for the cross-quad and opamp-based PTAT generators are 797 nA/°C and 860 nA/°C, respectively. The simulation results reveal a responsitivity of 745 nA/°C and 885 nA/°C for the cross-quad and opamp-based PTAT generators, which are in good agreement with the expected values. Further, simulations disclose less than 0.3% of maximum nonlinearity error across the range from 0 °C to 100 °C.

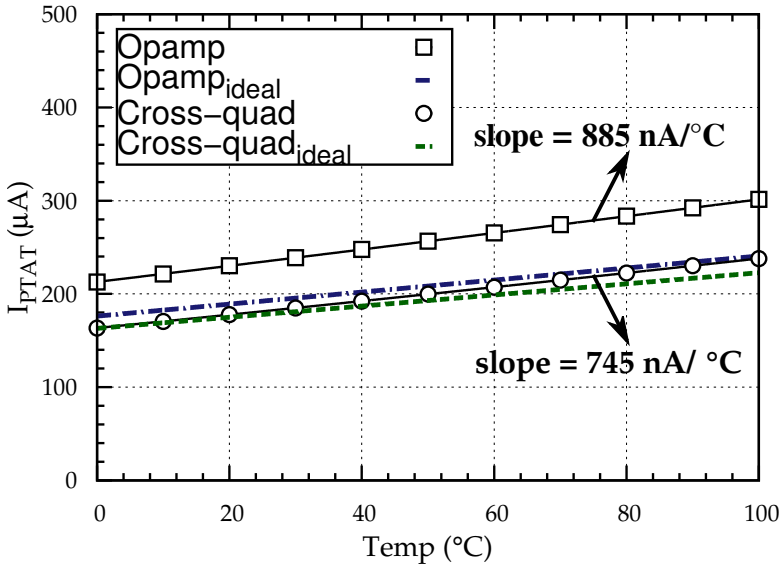


Figure 4.7: Simulation results of the output currents of both PTAT generators (opamp-based and cross-quad) as a function of the temperature and their respective ideal theoretical curves as per Eq. 4.2. Deviations in value from their ideal characteristics are mainly explained by high-level injection effects in the base region and non-zero emitter resistances both present in the SPICE model.

The difference in the value of the opamp-based generator from its ideal theoretical characteristic denoted by Eq. 4.2, as shown in Fig. 4.7, is mainly due to the value of the reverse beta high current roll-off (I_{KF}) included in the SPICE model. As a result, high-level injection effects in the base region modify the ideality factor (η) of the collector current, causing it to deviate from its theoretical exponential behaviour.

On the other hand, the difference in the cross-quad output from its ideal characteristic is mainly due to the higher sensitivity of this topology to non-zero emitter resistances that are also included in the SPICE model.

4.7. FABRICATION

A planar BiCMOS IC technology that requires only seven masking steps is used to fabricate the three main devices in the circuit: bipolar transistors (NPN), NMOS and PMOS transistors (Fig. 4.8) with a resolution down to 500 nm [2].

The process starts with a double-polished p-type silicon wafer with <100> of crystolographic orientation and $5\,\Omega\cdot$cm of resistivity. A p-type epitaxial film with thickness of 2 µm, and with a boron doping of 1e16 ions/cm^3 at 1050 °C is grown on the polished side. The first mask (Fig. 4.8.a) is used to define the n-well and the collector area of the bipolar transistor using a dose of 5e12 ions/cm^2 of phosphorus, and followed by 415 minutes of annealing.

[2] Using an i-line automatic wafer stepper with a numerical aperture of 0.48.

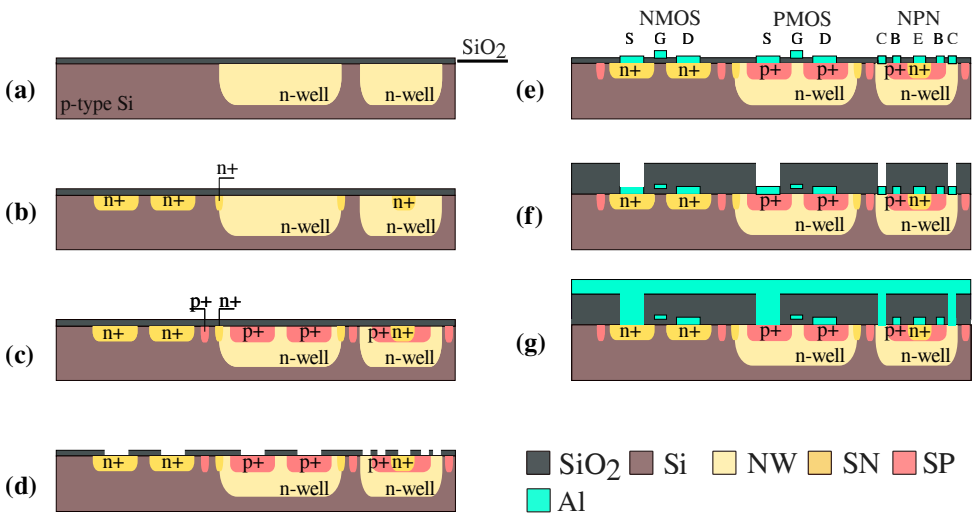


Figure 4.8: Cross-sections of the custom-made BiCMOS technology used in TU Delft's EKL (Else Kooi Lab).

The second and third masks (Figs. 4.8.b and c, respectively) define the n/p-type diffusion areas for the CMOS and the emitter/base area for the bipolar device using arsenic and boron as dopants, respectively. After this step, another boron implantation is carried out to adjust the threshold voltages in four different quadrants of the wafer, followed by 115 minutes of oxidation to activate the dopants.

After the doping adjustment, the threshold voltages of the NMOS and PMOS transistors change to about 2.0 V and −2.5 V, respectively. As a result, the circuit is operated from a 10 V power supply in order to provide enough headroom for saturation of the FET transistors.

Contact openings are wet-etched with a BHF (buffered hydrofluoric acid) solution after the patterning of the fourth mask (Fig. 4.8.d), while the fifth mask (Fig. 4.8.e) is used to pattern the interconnect and gate material via the deposition of AlSi (1%).

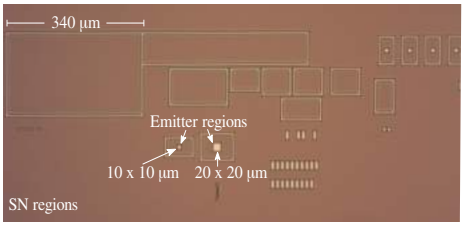
The process continues with a deposition of 2 µm of SiO_2 using PECVD (plasma-enhanced chemical vapor deposition) on the front and back of the wafer to create the dielectric of the MIM (metal-insulator-metal) capacitor.

Masks 6 and 7 (Figs. 4.8.f and g) are used to open the vias using dry etching, before depositing the second layer of metal.

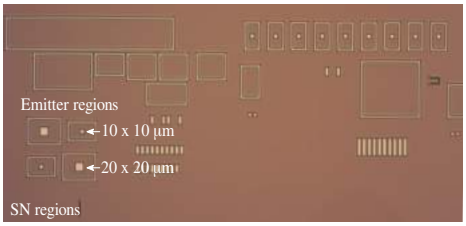
The microfabrication result of each photolithographic mask is shown in Fig. 4.9. The result of the chip fabrication, with the main building blocks highlighted, is shown in Fig. 4.10. The total chip area used, including the MIM capacitor, is about 10.88 mm^2.

4.8. RESULTS

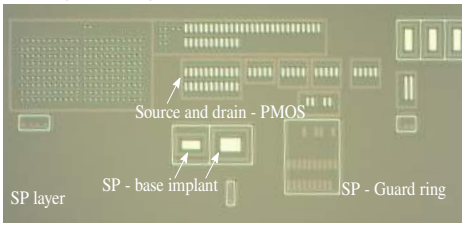
Measurements were carried out through a wafer microprobe station that includes a thermal chuck for sweeping the temperature across the desired range. The time-domain output of the circuit was probed using a digital oscilloscope (Fig. 4.11) at the reference temperature (37.5 °C).



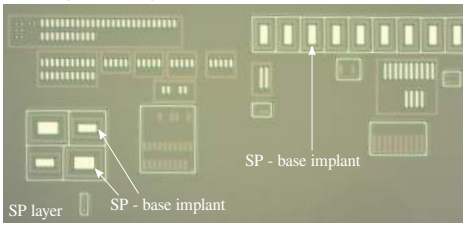
(a) Design 1: SN regions after arsenic implantation



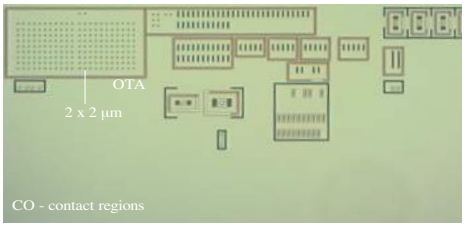
(b) Design 2: SN regions after arsenic implantation



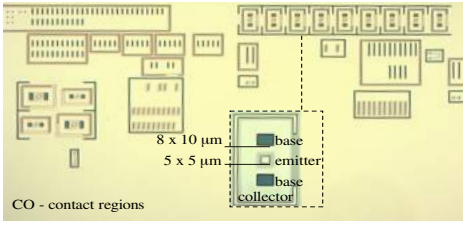
(c) Design 1: SP regions after boron implantation



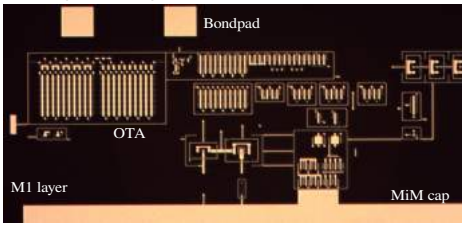
(d) Design 2: SP regions after boron implantation



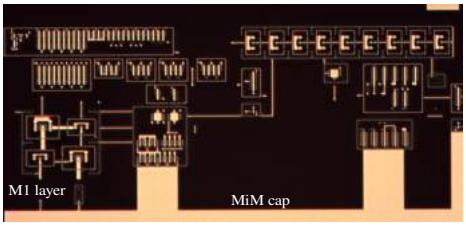
(e) Design 1: CO regions after BHF



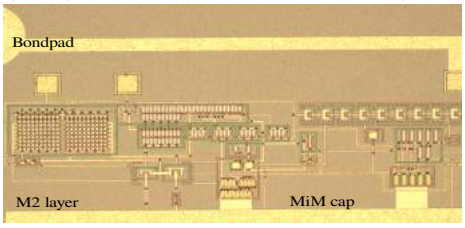
(f) Design 2: CO regions after BHF



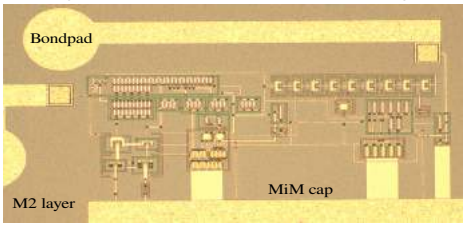
(g) Design 1: First metallization after plasma etching



(h) Design 2: First metallization after plasma etching



(i) Design 1: Second metallization after plasma etching



(j) Design 2: Second metallization after plasma etching

Figure 4.9: Microfabrication results of the seven photolithographic masking steps.

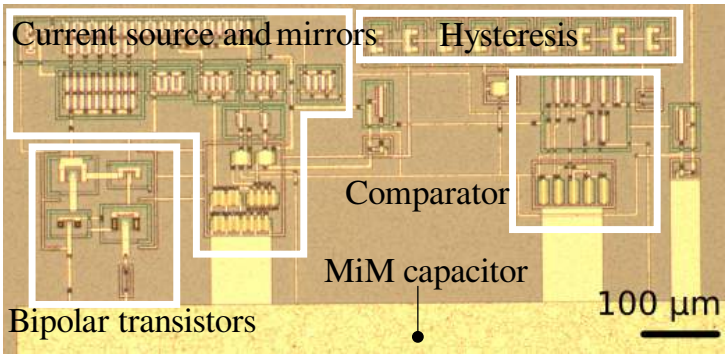


Figure 4.10: The result of the fabricated chip using the in-house EKL technology with the: PTAT current source, current sink and current mirrors, bipolar transistors, capacitor, hysteresis block and comparator.

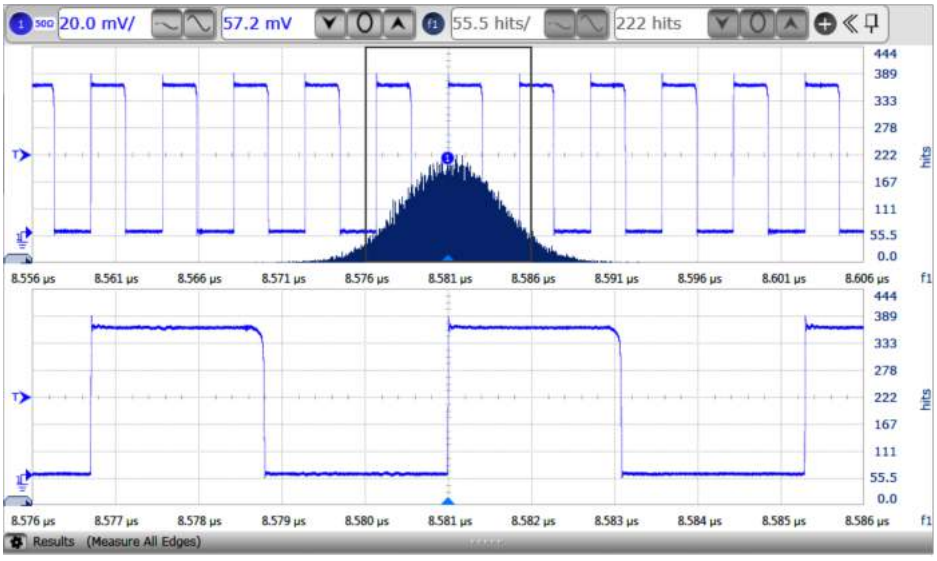


Figure 4.11: Transient result of the temperature sensor at the reference temperature of 37.5 °C for the opamp-based PTAT generator. The standard deviation over 50,000 random samples of the measured period reveals a jitter of 2.78 ns.

To calculate the resolution, the total root mean square (rms) period jitter was measured by tracing the histogram of the period over 10,000 random samples for each temperature point, from 25 °C to 100 °C, and computing the standard deviation. The result of this temperature sweep is shown in Fig. 4.12.

The difference in slopes shown in this figure stems from the different responsitivities of both PTAT generators, as well as from non-idealities present in both circuits: high-level injection and emitter resistances. Further, the measurement results reveal a maximum nonlinearity error of 0.26% and 0.75% for the opamp and cross-quad circuits, respectively.

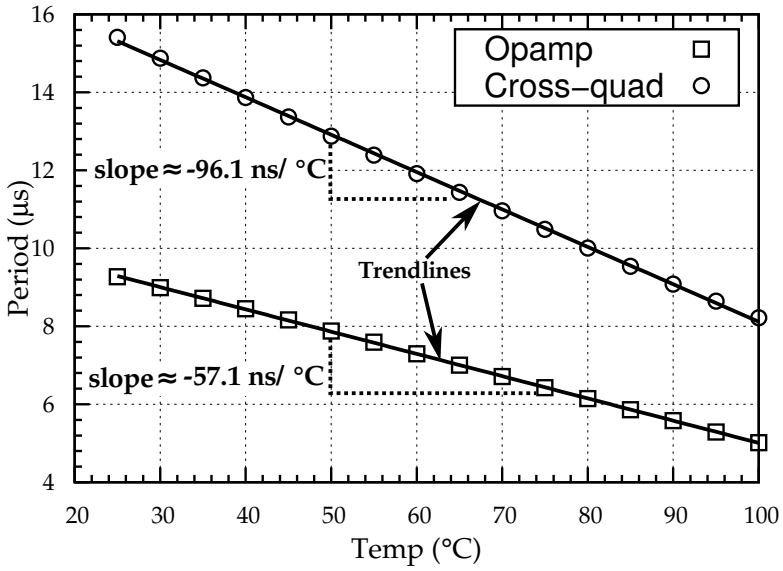


Figure 4.12: Temperature conversion of the smart temperature sensor. The least-squares polynomial regression reveals a responsivity of 57.1 ns and 96.1 ns for the opamp-based and cross-quad PTAT generators, respectively.

At 37.5 °C, the total rms jitter was measured for more than 50,000 random samples and is equal to 2.78 ns and 5.98 ns for the opamp-based and cross-quad sensor, respectively.

Two main reasons account for this difference: firstly, the large open loop gain of the opamp provides additional robustness against power supply variations; secondly, the current drawn by the opamp-based PTAT generator core is slightly higher than the current drawn in the cross-quad, thus, its total rms period jitter is lower. The resolution (ϕ) is calculated as the ratio of the jitter for 3σ and the responsivity, and equals:

$$\phi_{\text{opamp}} = \frac{3 \times 2.78 \text{ ns}}{57.1 \text{ ns/°C}} = 0.15 \text{ °C } (3\sigma), \tag{4.5}$$

$$\phi_{\text{cross-quad}} = \frac{3 \times 5.98 \text{ ns}}{96.1 \text{ ns/°C}} = 0.19 \text{ °C } (3\sigma). \tag{4.6}$$

The measured resolutions are about three times better than the initial intended resolution (±0.5 °C). As a result, we will undertake the co-fabrication with the OOC platform as a follow-up to this work, and the opamp-based PTAT cell to be used at the final integration due to its better resolution. For a practical use on the OOC, the circuit is anticipated to have a 2-point calibration to correct for offset and non-idealities in the slope of the temperature-period curve.

4.9. CONCLUSIONS

A smart temperature sensor for an OOC platform, which produces the temperature information in the time domain, was designed and fabricated using an in-house IC technology that requires only seven lithographic steps and is compatible with our in-house MEMS fabrication process.

The measurement results reveal a responsitivity of 57.1 ns and a total rms period jitter of 2.78 ns, yielding a resolution of less than $\pm 0.2\,^{\circ}\mathrm{C}$ (3σ), from $25\,^{\circ}\mathrm{C}$ to $100\,^{\circ}\mathrm{C}$. The maximum nonlinearity error found is less than 0.3%. When operating from a 12 V power supply, the circuit consumes about 36 mW.

PART II: MONOLITHIC INTEGRATION OF A SMART TEMPERATURE SENSOR ON A MODULAR SILICON-BASED ORGAN-ON-A-CHIP DEVICE [3]

4.10. ABSTRACT

One of the many applications of organ-on-a-chip (OOC) technology is the study of biological processes in human induced pluripotent stem cells (iPSCs) during pharmacological drug screening. It is of paramount importance to construct OOCs equipped with highly compact *in situ* sensors that can accurately monitor, in real time, the extracellular fluid environment and anticipate any vital physiological changes of the culture. In this paper, we report the co-fabrication of a CMOS smart sensor on the same substrate as our silicon-based OOC for real-time *in situ* temperature measurement of the cell culture. The proposed CMOS circuit is developed to provide the first monolithically integrated *in situ* smart temperature-sensing system on a micromachined silicon-based OOC device. Measurement results on wafer reveal a resolution of less than $\pm 0.2\,^{\circ}$C and a nonlinearity error of less than 0.05% across a temperature range from $30\,^{\circ}$C to $40\,^{\circ}$C. The sensor's time response is more than 10 times faster than the time constant of the convection–cooling mechanism found for a medium containing 0.4 mL of PBS solution. All in all, this work is the first step towards realising OOCs with seamlessly integrated CMOS-based sensors capable of measuring, in real time, multiple physical quantities found in cell-culture experiments. It is expected that commercial foundry CMOS processes may enable OOCs with very large-scale integration, incorporating multi-sensing and actuation systems in a closed-loop manner.

4.11. INTRODUCTION

Organ-on-a-chip (OOC) is an emergent technology in which a microfluidic perfusion platform for culturing human iPSCs is used to mimic a minituarized version of an explicit organ anatomy and physiology. This technology has been developed to substitute traditional *in vitro* and animal models that are often inaccurate to predict the human physiology [13, 14]. Studies indicate that OOCs can play a transformative role in the drug development cycle by bridging the gap between preclinical studies and human trials, while reducing the pharmaceutical R&D costs to 10–26% [15].

For the construction of these OOC systems, various micro- and nano-fabrication technologies have been used, including soft lithography on elastomeric materials. The simplicity, fast turnaround time, and relatively low cost of this technique affords quick experimentation of new designs. Examples of such designs include OOCs for the heart [16], the liver [17], the kidney [18], the lung [19], and tumors [20]. On the other hand, shortcomings of such methods include limited device throughput which is a crucial fea-

[3] Part II is based on the publication "Monolithic integration of a smart temperature sensor on a modular silicon-based organ-on-a-chip device", Sensors and Actuators A: Physical, Volume 317, 2021, 112439, ISSN 0924-4247 [2]

ture for high-volume manufacturing.

To overcome the limited device throughput, MEMS (Microelectromechanical Systems) technology based on silicon-wafer-level processing proves to be a very efficient option for micromachining high-aspect ratio structures with submicrometer resolution, and over a wide range of materials [21]. Although dependent on highly specialized and expensive equipment, the high initial costs are counteracted when a large production volume is anticipated. Additionally, MEMS processes often are compatible with CMOS (Complementary Metal Oxide Semiconductor) technology which allows monolithic integration of dedicated interface electronics for thermal, optical, pH, and label-free sensing necesssary to design compact cell culture systems [22]. Furthermore, the *in situ* real-time analysis offered by these microelectronic systems could reveal new insights into intra- and inter-cellular signalling pathways.

Currently, the aforementioned analysis assumes that the pH, temperature (~ 37 °C), humidity (~ 95% RH) and gaseous atmosphere (CO_2/O_2 levels) around the cell culture medium are regulated by incubators. These parameters should be kept constant since they play a pivotal role in the optimal growth and maximum productivity of the cell culture [23]. However, variations do occur, which cause stress in the cells that can respond in various ways ranging from the activation of survival pathways to the initiation of senescence.

Especially, recurrent temperature variations in the cell culture should be carefully monitored as they may severely affect the experiments. Causes for such variations can be due to deviations between the incubator's temperature setpoint and the temperature of the cells, the frequency and duration of the incubator's door opening, and the duration the cells are outside the incubator for inspection [24]. Above all, time spent outside the incubator represents a larger, more variable, factor that is likely to impact cell health. A drop of the culture temperature to room temperature results in a considerable decrease in cell growth along with the accumulation of cells in the G1 [4] phase [3, 25]. In fact, the rate at which the temperature of the cell culture decreases outside the incubator is unknown to life science researchers. This has motivated us to construct a real-time BiCMOS temperature sensor to monitor the *in situ* temperature of the culture throughout the cell-division cycle.

A variety of electrical cell culture temperature sensing methods has been presented in previous literature: commercial T-type thermocouples made of copper and constantan wires [26], NTC (negative temperature coefficient) thermistors [27] or commercial PT-100 RTDs (resistance thermometer detectors) [28]. A common drawback of the aforementioned solutions manifests itself when interfacing the sensor's output with readout systems that are outside the culturing environment. In this scenario, with the sensor remote from readout electronics, various sources of errors (noise, interference, distortion, crosstalk, etc.) may be introduced over the channel and impair the measurement. Moreover, such commercial sensors are not very compact for OOC applications.

Non-electrical temperature sensing methods have also been reported, such as liquid crystal displays [29], fluorescent polymeric thermometers [30], and optoacoustic methods [31]. These solutions, however, are not very compact because they depend on expensive and bulky instrumentation laboratory equipment [32] to optically map the tem-

[4] G1 is the first of four phases of the cell cycle that takes place in eukaryotic cell division.

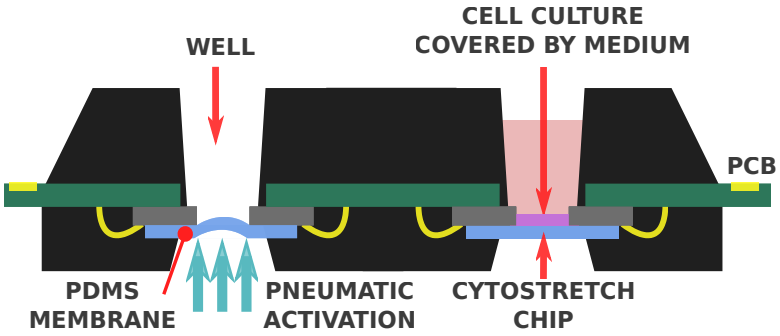


Figure 4.13: Artistic impression of the Cytostrech system.

perature of the culture. Moreover, these systems have poor resolution (~ 1 °C), do not easily allow the integration of closed-loop systems and do not offer the high throughput of silicon-based microsystems.

To tackle these shortcomings, we have fabricated a smart temperature sensor on the same silicon substrate used to construct our custom micromachined organ-on-a-chip device. As a consequence, the system is made more compact and the robustness to various sources of errors is enhanced. To accomplish this, we used a simple, robust, and custom in-house integrated circuit (IC) technology [8]. We have previously used this technology to design and characterise a suitable temperature sensor [1]. In this paper, we are presenting a complete, seamlessly integrated *in situ* smart temperature-sensing system on an OOC. To the best of the authors' knowledge this is the first time such integration is performed using a custom-designed sensing and conditioning circuit fabricated on the same silicon substrate as that of the OOC.

As opposed to a System-in-Package (SiP) approach, in which an outsourced ASIC (Application-specific Integrated Circuit) is heterogeneously integrated on the OOC device, our solution avoids the use of chip mounting technology (e.g. wire and die bonding) that usually requires extra packaging protection of the assembled components. In contrast, our seamless integration minimizes the extra processing steps and precludes potential mechanical stresses caused by mismatches in the thermal expansion coefficient of the various dissimilar components and materials to be used in a SiP scenario. Finally, the holistic CMOS-MEMS co-design approach offers the possibility to conform and better accommodate the inclusion of CMOS electronics over various MEMS topologies.

4.12. MATERIALS AND METHODS

Our OOC platform, presented here as Cytostretch [33], is modular, customizable, silicon-based and microfabricated with cleanroom-compatible processes. The main components of the system are depicted in Fig. 4.13, where the Cytostretch chips are bonded to a PCB that includes a molded multi-well plate for culturing the cells.

The chips include a pneumatically-activated freestanding dog-bone-shaped PDMS

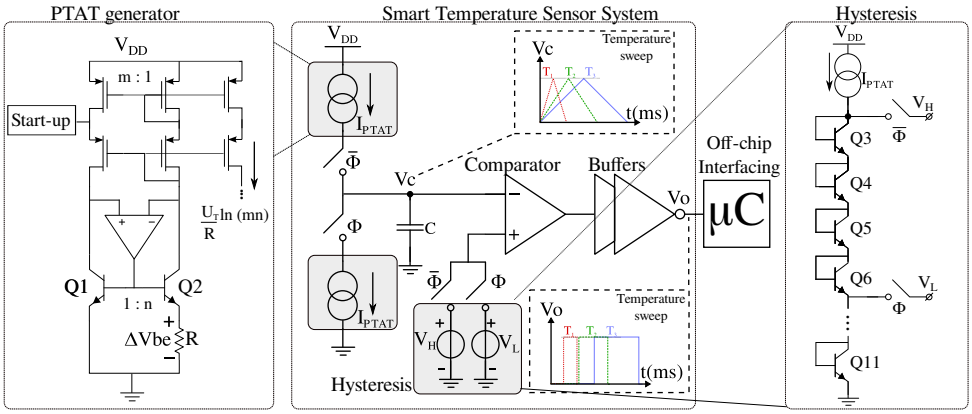


Figure 4.14: Main blocks of the smart BiCMOS temperature sensor: a PTAT generator and a relaxation oscillator.

membrane to accommodate the cell culture (Module 1) while delivering mechanical stimuli to the cells in various in-vitro studies, additional features, such as through-membrane micro-pores for biological signal exchange (Module 2), on-membrane grooves for cell alignment (Module 3), in-membrane titanium nitride (TiN) microelectrodes for monitoring activity from electrically active cells (Module 4), and titanium (Ti) strain gauges to measure the deformation of the PDMS membrane during inflation (Module 5). More details on these specific modules can be found in [34]. The smart temperature sensor presented in this paper is the sixth module of this OOC platform.

This module was accomplished thanks to the monolithic integration of this smart sensor on the backside of our OOC device. The temperature of the cells is sensed as a result of the heat transferred from the culture medium to the crystalline silicon through thermal conduction mechanisms associated with elastic vibrations of the lattice (i.e. phonons transport).

THE SMART TEMPERATURE SENSING MODULE

The smart sensing module was designed to detect the *in situ* temperature of the culture and convert it into a periodic binary electronic signal, which carries the temperature information encoded in the time domain. To realize this, the system consists of two main blocks: a proportional to absolute temperature (PTAT) current generator (employing NPN bipolar transistors to sense the temperature information) and a relaxation oscillator (Fig. 4.14).

The circuit operation can be understood from the system diagram of Fig. 4.14. During start-up, the output of the comparator is set to a logic "0" which turns the CMOS switches ($\overline{\Phi}$) on for the comparison phase. As a result, a PTAT current is integrated in the capacitor and its voltage (V_C) is ramped up. When V_C equals voltage V_H, the output of the comparator toggles and turns the other pair of CMOS switches (Φ) on. The voltage V_C is now ramped down via the PTAT current sink until it reaches V_L ending the discharging cycle. Once started, this process continues indefinitely to yield a signal in which the

period is IPTAT (inversely proportional to the absolute temperature) according to the equation $T = (2 \cdot C \cdot \Delta V)/I_{\mathrm{PTAT}}$, where ΔV is the difference between the threshold voltages V_{H} and V_{L}, C is the capacitance and I_{PTAT} is the PTAT current generated.

PTAT GENERATOR

The PTAT current generator yields a current that is proportional to the voltage drop (ΔV_{BE}) across the resistor R. Since this voltage is the difference of two base-emitter voltages, the current produced, $I = \Delta V_{\mathrm{BE}}/R$, is PTAT. Current mirrors with a m:1 ratio convey a copy of this PTAT current to the capacitor. The collector voltages are forced to be equal, regardless of variations in the power supply or in the temperature, via the negative feedback loop that includes the operational amplifier (opamp), the bipolar devices (Q_1 and Q_2) and the resistor.

The expression of the current through resistor R is:

$$I_{\mathrm{PTAT}} = \frac{U_{\mathrm{T}}}{R} \ln(mn), \tag{4.7}$$

where U_{T} is the thermal voltage (~26 mV at room temperature), m is the current mirror ratio and n is the bipolar emitter area ratio. Hence, the responsivity of this block is mostly determined by the current mirror and emitter area ratios. In the design, values of 5 and 4 for m and n, respectively, were chosen. In addition, a start-up circuit for this PTAT cell was implemented to ensure its correct operating point.

RELAXATION OSCILLATOR

The relaxation oscillator is realized by a feedback control performed by the comparator, the PTAT current source and the hysteresis circuit. The hysteresis circuit was implemented with nine stacked diode-connected bipolar devices biased with a copy of the PTAT current so as to produce the voltages V_{H} and V_{L}, which, at 37 °C, are about 6 V and 3.5 V, respectively. The hysteresis was made inversely proportional to the absolute temperature (IPTAT) to increase the circuit responsivity with respect to the period.

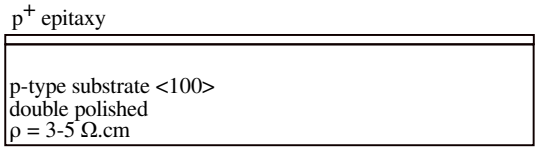
4.12.1. MICROFABRICATION ON SILICON SUBSTRATE

The co-fabrication of MEMS and BiCMOS on a single silicon substrate is typically adverse in terms of costs. This problem exacerbates in more advanced BiCMOS technologies due to the increased number of masks and processing steps required. For instance, adding high-performance vertical bipolar devices to a standard 0.18 µm CMOS technology can add up to 10–20 extra photolithographic masks and increase the costs by 20–30 % [35].

Using a simpler BiCMOS process with fewer photomasks and process steps is more attractive. Our in-house BiCMOS process comprises seven photomasks which yields a more cost-effective solution (Fig. 4.14a-h.) while offering a holistic CMOS-MEMS co-design. The co-fabrication procedure uses the IC-interlaced-MEMS processing strategy. In this approach, CMOS and MEMS processes are mixed such that one or more process steps are shared or reused in both the IC and the MEMS domains.

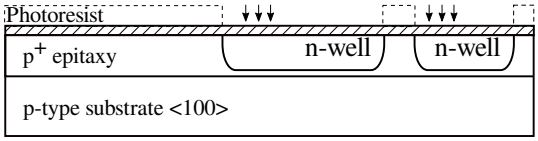
PROCESS FLOW

(a)



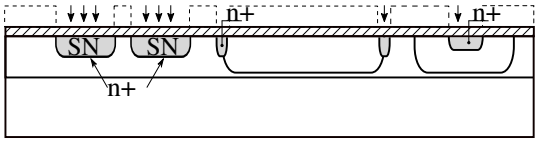
Epitaxy growth:
2 μm of p-type epitaxial film
Boron: 1e16 atoms/cm^3

(b)



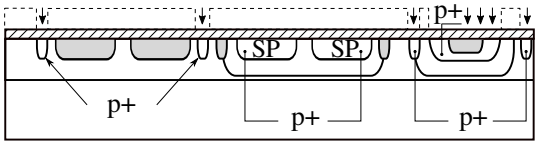
N-well implantation:
Thermal screen oxide formation
P$^-$ implanted through 20 nm of SiO_2
Dose: 5e12 ions/cm^2 at 150 keV
Annealing at 1150 °C for 415 min.
Oxide strip.

(c)



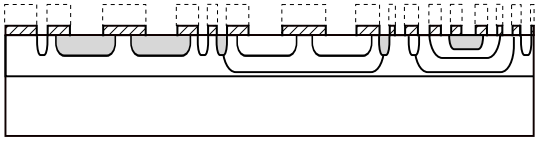
Shallow N-type implantation:
Thermal screen oxide formation
As$^-$ implanted through 20 nm of SiO_2
Dose: 5e15 ions/cm^2 at 40 keV

(d)



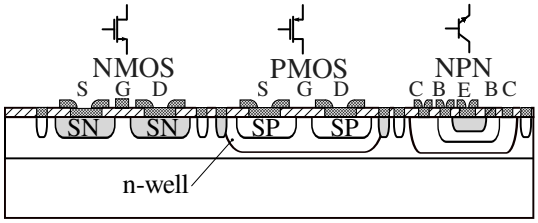
Shallow P-type implantation:
B$^+$
Dose: 4e15 ions/cm^2 at 20 keV

(e)



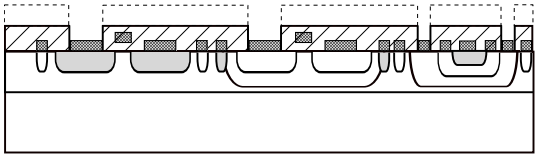
Contact openings:
BHF 1:7 SiO_2

(f)



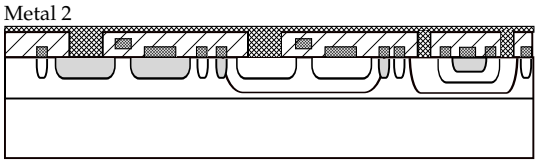
First metallization and RIE:
200 nm of sputtered AlSi (1%)
Plasma etching using RIE
30 s in wet etchant bath for Al fence removal

(g)



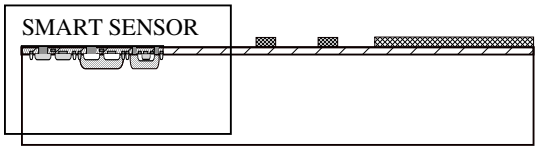
PECVD deposition and VIAs:
2 μm of SiO_2
Opening of VIAs using dry etching with soft landing (100 W)

(h)



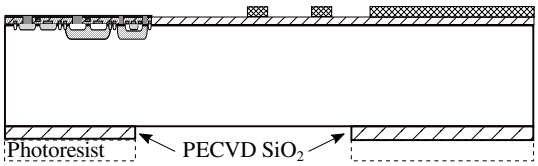
Second metallization:
3.1 μm of sputtered AlSi (1%)
Plasma etching using RIE
30 s in wet etchant bath for Al fence removal

(i)

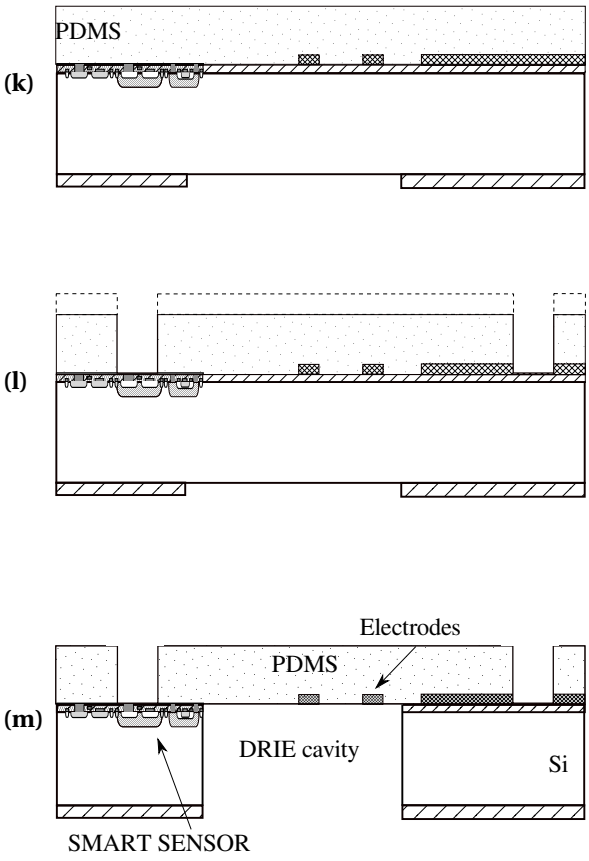


SMART sensor with electrodes and interconnects

(j)



PECVD deposition on the back
5 μm of SiO_2
Openings through SiO_2 on the back using dry etching



PDMS deposition on the front: 15-μm-thick PDMS layer spin-coated at 3500 rpm for 30 s and cured for 1 hour at 90 °C

PDMS openings

DRIE on the back
SiO_2 landing

Figure 4.14: Fabrication steps in a custom BiCMOS-MEMS technology for the smart sensor device on the Cytostretch platform. Not to scale.

CMOS FABRICATION

A double-polished p-type silicon wafer with <100> of crystallographic orientation and $5\,\Omega\cdot$cm of resistivity is used to start the alignment layer (zero layer) definition. A 2 µm thick of p-type epitaxial layer was grown on the top of the silicon wafer with 1e16 ions/cm^3 of boron doping in order to obtain a precise p-dopant concentration required to include NPN bipolar transistors in the BiCMOS process.

A 20 nm barrier was formed using wet oxidation to screen co-implanted particles. The n-well and the collector area of the NPN bipolar transistor are patterned using the first photomask (Fig. 4.14.a) with a 3.1 µm of photoresist thickness. A dose of 5e12 ions/cm^2 of phosphorus was implanted at 150.0 keV of energy, and following a 415 minutes of annealing for doping redistribution. A 230 nm of thick oxide is created as a result. An oxide stripping is performed using a buffered hydrofluoric acid (BHF)

solution with 1:7 of selectivity. Another dirt barrier oxide layer is grown to process the subsequent steps.

The second photomask is used to define the n-type diffusion areas for the CMOS transistors and the emitter area for the bipolar transistors (Fig.4.14.b) using an arsenic dose of 5.0e15 ions/cm^2 at 40.0 keV of energy. The third photomask defines the p-type diffusion areas for the CMOS as well as the base area of the bipolar transistors (Fig.4.14.c) using a boron dose of 4.0e14 ions/cm^2 at 20.0 keV of energy. An optimal dose implantation should be investigated here due to the trade-off between the intrinsic current gain of the NPN bipolar devices and the current drive capacity of the PMOS devices. Notice that the implantation doses of the n-well/collector, n-type diffusion/emitter, and p-type diffusion/base are strapped, creating an interlaced fabrication strategy for the BiCMOS devices that saves lithography costs and fabrication time.

Next, a threshold voltage adjustment is carried out using a net dose of 20e11 ions/cm^2 at 25.0 keV in the fourth quadrant of the wafer. Subsequently, the dirt barrier oxide is removed using a 1:7 BHF solution, followed by nine minutes of wet oxidation for dopant activation and to create the 100 nm thick of gate oxide. After this step, the threshold voltages for the NMOS and PMOS transistors, in the fourth quadrant, are set to about 2.0 V and −2.5 V, respectively.

In the next step (fourth mask), the contact openings are patterned and wet-etched with a 1:7 BHF solution (Fig. 4.14.d). The interconnects and the gate material are created by sputtering 200 nm of AlSi (1%) and patterning with the fifth photomask (Fig. 4.14.e). The 1% of silicon composition in the aluminum avoids spikes in the shallow metal-diffusion interfaces.

The process follows with a deposition of 2 µm of SiO_2 using PECVD (plasma-enhanced chemical vapor deposition) at the frontside of the wafer to create at the same time the MIM (metal-insulator-metal) capacitor dielectrics and the stopping mask for the DRIE (Deep Reactive Ion Etching) step that defines the PDMS membrane area, in an interlaced-like manner. To share this process step, a clear trade-off is to be made in the co-design phase. Ideally, the thinner the dielectric of the MIM capacitor the bigger the capacitance, thus, the higher the total capacitance-per-area. This results in a more area-saving solution. On the other hand, enough oxide thickness headroom should be provided in the DRIE step to ensure a reliable hard mask landing. As a consequence, during the co-design phase, a larger silicon area was used to compensate for the reduced capacitance-per-area of the MIM capacitor.

The vias are opened using plasma etching after patterning the sixth photomask (Fig. 4.14.f) with photoresist. The second metallization (Fig. 4.14.g) uses a 3.1 µm thickness of sputtered AlSi (1%). This step simultaneously patterns the second level of interconnects of the smart sensor together with the contact pads and the electrical interconnects outside the membrane area of the Cytostrech (Fig. 4.14.h).

MEMS BULK MICROMACHING

Following the last step of the smart sensor microfabrication (Fig. 4.14.h), 5 µm of PECVD SiO_2 is deposited on the backside of the wafer to prepare the substrate for the DRIE step. The Cytostretch membrane area is then patterned on the same backside by dry etching

(Fig. 4.14.j).

Subsequently, a 15 µm-thick PDMS layer is spun onto the front of the wafer at 3500 rpm for 30 s and cured for 1 hour at 90 °C (Fig. 4.14.j). Next, 300 nm of AlSi (1%) is sputtered at room temperature on top of the PDMS film created. The Al is masked with 4 µm of photoresist (PR) (AZ ECI 3027) and dry-etched (Fig. 4.14.k). The lithography and etching processes used are optimized to circumvent issues caused by the difference between the expansion coefficients of the PDMS and the PR. Besides serving as a hard mask to later expose the electrical contacts, the Al layer reduces the effects of the differences in expansion coefficients by acting as a buffer layer between the PDMS and the PR.

Subsequently, the membrane is released after removing the Si and the SiO_2 layers from underneath the membrane using DRIE and BHF, respectively (Fig. 4.14.l). Finally, an etch mixture of Phosphoric/Acetic/Nitric acid (PES 77-19-04) is used to remove the aluminium on the top of PDMS and make the membrane fully transparent. This does not remove the Si from the AlSi (1%), though. To that end, a 15 µm thick photoresist deposited on the front side with the spray coater acts as passivation for the interconnects made of aluminum.

4.13. EXPERIMENTAL RESULTS

A photograph taken from the top of the microfabricated device is shown in Fig. 4.15. In this figure, the PDMS membrane, the electrodes and the temperature sensor circuitry can be visualized. Notice that the circuitry takes only a small fraction of the total chip area. The total chip size is 7x7 mm^2 and less than 15 % of this area was used for the smart sensor.

Another photograph of the chip was taken using a scanning electron microscope (SEM) (Fig. 4.16). In this photograph, the cavity formed with the Bosch DRIE process can be visualized better.

Static and dynamic response measurements were carried out to characterize the sensor's performance. The resolution and linearity were extracted by means of a series of static response measurements in which the temperature was kept constant over time. The dynamic response measurement was used to characterize the sensor's response speed by applying a brief temperature pulse by means of a pre-heated PBS solution. By exciting the system with a brief pulse with finite duration, the output follows the transfer function of the system asymptotically[5].

STATIC RESPONSE: DRY MEASUREMENTS

The static response measurements were carried out with a microprobe station that includes a thermal chuck to sweep the temperature of the wafer over the desired range. A commercial PT-100 temperature sensor was attached to the thermal chuck to set a well-calibrated reference and the 4-point probes method was used to measure its resistance changes (Fig. 4.17).

A temperature sweep from 25 °C to 100 °C with 5 °C increment was carried out in or-

[5] The convolution of an impulse input with a function outputs the function itself.

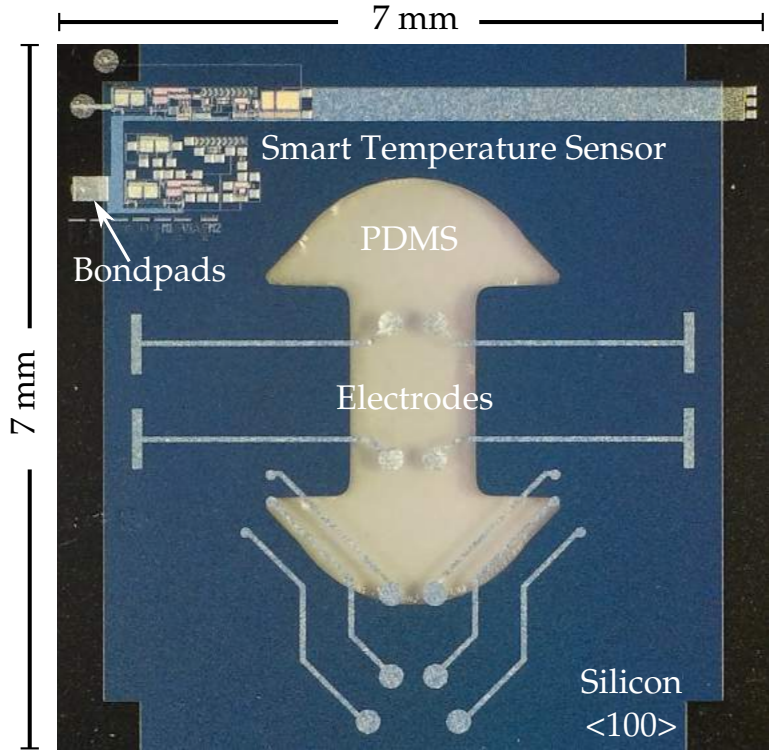


Figure 4.15: Smart temperature sensor monolithically integrated on the Cytostretch chip.

der to measure the responsivity and the nonlinearity of the temperature-to-time conversion. The responsivity and the maximum nonlinearity error obtained from this measurement was 57.1 ns/°C and 0.26 %, respectively (Fig. 4.18). A temperature measurement over a shorter range (30 °C to 40 °C with 1 °C increment) was also performed in order to characterize the sensor's linearity within a temperature span that is closer to the cell culture application. A simple linear regression of the data over this temperature range reveals a 99.988 % fit with the linear model. Hence, a 0.05 % of maximum nonlinearity error was found over this range.

The jitter is a measure of the deviation of the periodic signal from its true periodicity and it affects the resolution that the sensor can achieve. The total root mean square (rms) jitter was measured at 37 °C for more than 50.000 samples and is equal to 2.78 ns. The sensor's resolution (ϕ) is calculated as the ratio of the jitter for 3σ and the responsivity, and equals:

$$\phi = \frac{3 \times 2.78\,\text{ns}}{57.1\,\text{ns}/^{\circ}\text{C}} = 0.15\,^{\circ}\text{C}\ (3\sigma), \tag{4.8}$$

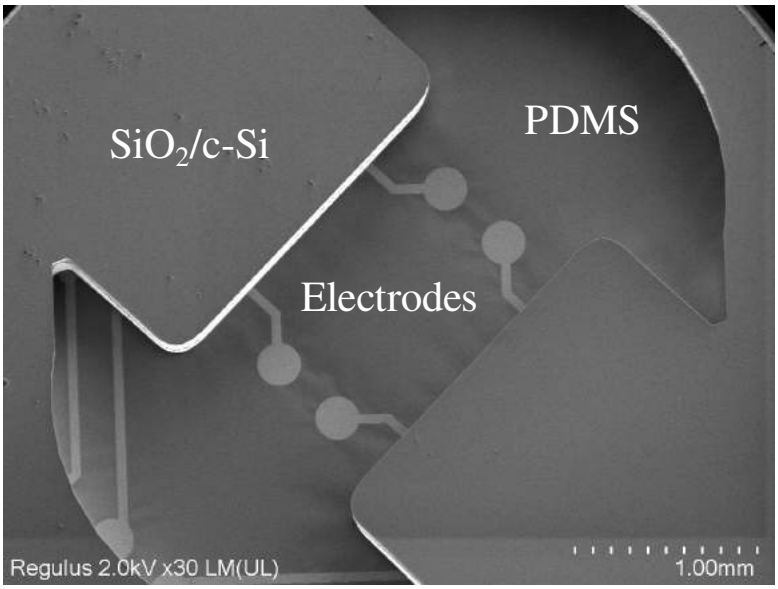


Figure 4.16: Photograph of the Cytostretch chip taken using a scanning electron microscope.

DYNAMIC RESPONSE: WET MEASUREMENTS

To measure the sensor's dynamic response, the wafers were diced and four different dice were assembled on a semi-flexible PCB containing four different wells intended for cell culture experimentation (Fig. 4.19).

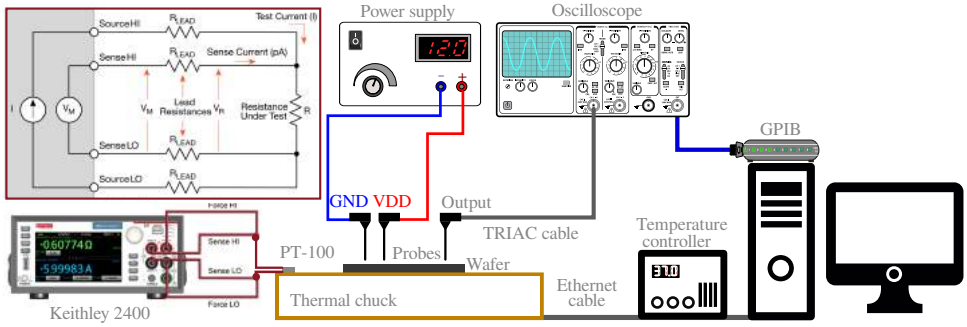


Figure 4.17: Schematic representation of the wafer-level measurement using the microprobe station.

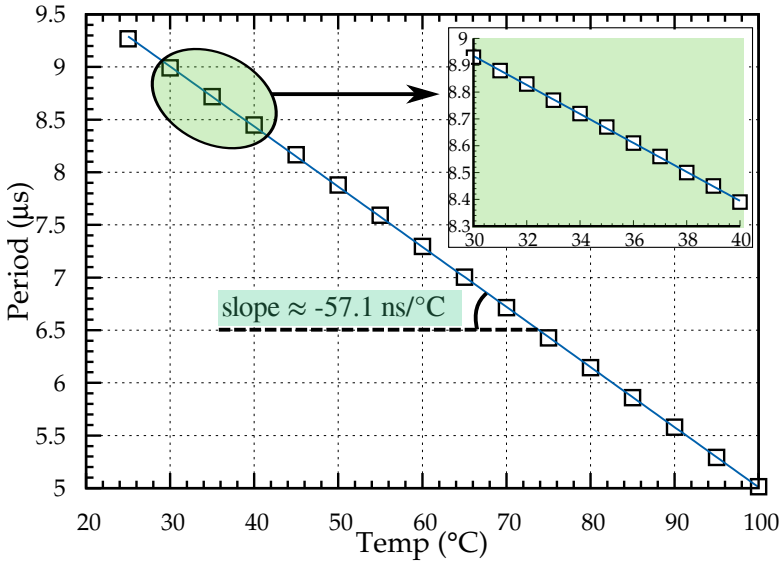


Figure 4.18: Temperature-to-time conversion of the smart temperature sensor. The least-squares polynomial regression reveals a 57.1 ns/°C of responsivity.

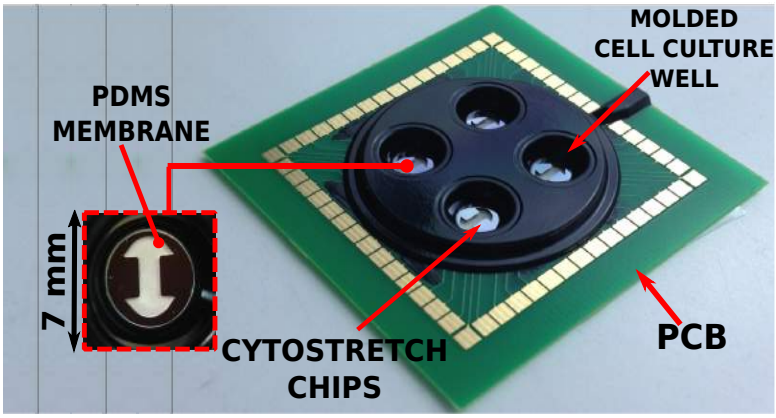


Figure 4.19: Cytostrech chips mounted on a PCB containing wells for cell culture experiments.

The measurements were initiated with the ambient temperature at 28 °C (±0.5 °C) and after approximately 15 s the wells were filled with 0.4 mL of PBS (Phosphate-buffered saline) solution pre-heated to a temperature of 32 °C. A PT-100 sensor configured under a four-wire sensing measurement was placed inside the wells to set a temperature reference. The changes in the output's signal period, resulting from the thermal equilibrium between the temperature of the PBS inside the wells and the room temperature, were measured and stored with a digital oscilloscope (Fig. 4.20).

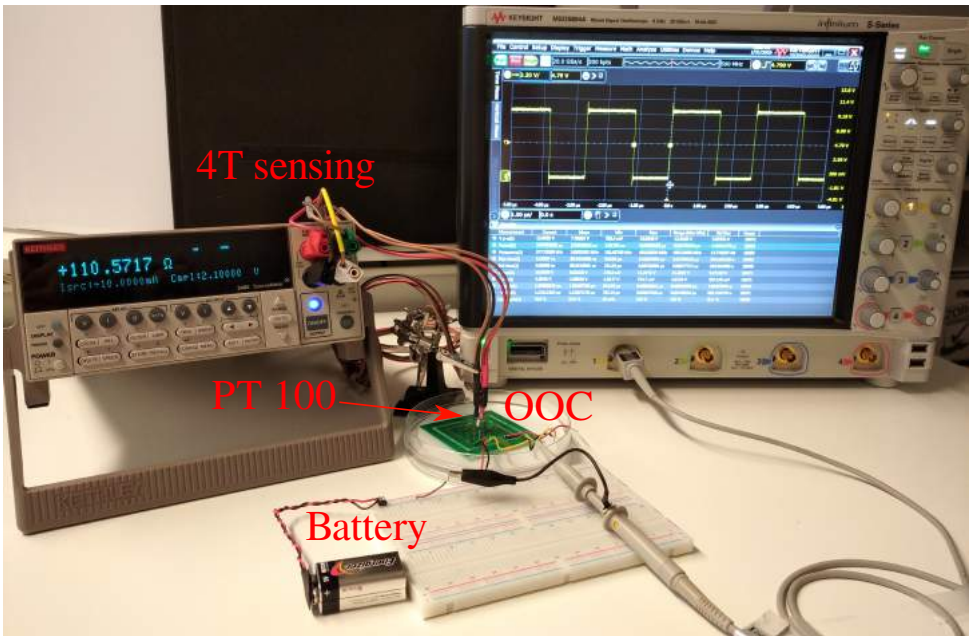


Figure 4.20: Measurement setup used for characterizing the dynamic response of the system. The PT-100 was used as reference, and a digital oscilloscope measured the period variation over the experimentation.

Here, three different time constants are involved in the heat transfer exchange (Fig. 4.21): (1) the time constant associated with the convection–cooling mechanisms between the medium and the ambient temperature (τ_1), (2) the time constant associated with the thermal conduction happening at the interface between the medium bulk and the silicon crystal lattice (τ_2), (3) and the time constant associated with the intrinsic delay between the silicon lattice and the sensor itself (τ_3).

The results of this measurement are plotted in Fig. 4.22 for ten different measurements (dark green lines) taken at different times within a day. The pink line on this curve indicates the mean value calculated for these ten samples, whereas the shaded light green regions encompass the $\pm 3\sigma$ confidence level around the mean.

An exponential curve is also fitted on the data to indicate the tendency of the samples. From this curve, the time constant associated with the heat loss between the medium and the ambient (τ_1) has been extracted and it is roughly 50 s. The cumulative time constant ($\tau_2 + \tau_3$) associated with thermal conduction in the silicon and the sensor's response has also been derived from the slope in the curve around t = 15 s, and it is on average 1.5 s.

The ratio of the thermal resistances due to conduction between the medium and the silicon surface compared to the thermal resistance due to the heat loss mechanisms give an indication of the Biot number. This dimensionless quantity was calculated to be about 0.03 and it implies that the heat conduction inside the medium is much faster than the heat convection away from its surface, and temperature gradients are negligible inside of it. Having a Biot number smaller than 0.1 labels a substance as "thermally thin",

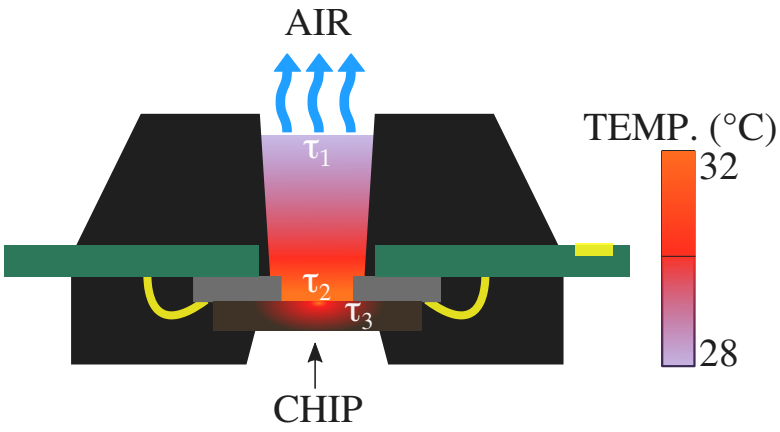


Figure 4.21: Different time constants involved on the heat transfer of the system. Time constant τ_1 happens between the medium and the ambient temperature, τ_2 between the medium and the silicon lattice and, τ_3, between the silicon and the sensor.

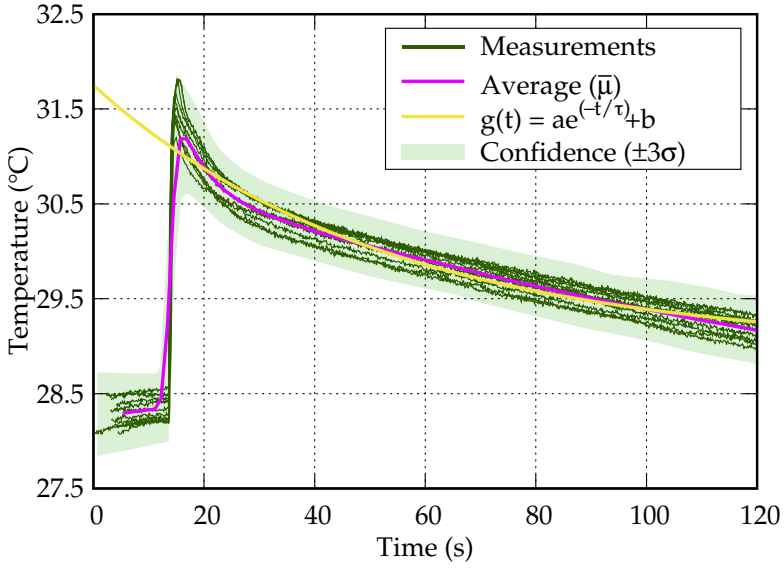


Figure 4.22: Dynamic response of the sensor to a brief temperature pulse.

and temperature can be assumed to be constant throughout the material's volume.

4.14. RESULTS AND DISCUSSION

The results presented in the previous section demonstrate the capability of monolithically integrating electronic functionality in silicon-based OOC devices for real-time in-situ temperature measurements of the cell culture. Our in-house BiCMOS technology has been used as a research tool for the proof of concept. This has been the first step to realise OOCs with integrated electronic functionality for multi-sensing many other different physical quantities (pH, glucose, glutamate, growth factors, etc) in the cell culture. As the number of sensors in the platform increases, more correlations can be performed for stoichiometric optimizations of the culture.

Previous literature has extensively used commercial sensors for this purpose, which are not compact, not scalable, potentially lack an effective seamless interface for the cells, and do not allow for high-density multi-sensing integration. We expect that more advanced CMOS technological nodes may enable higher integration of sensing and actuation functionalities in a closed-loop manner, albeit this progress is accompanied by a corresponding rise in financial costs due to the increased number of photomasks required and the process complexity. To achieve higher integration in a closed-loop manner, the sensors shall yield the necessary accuracy and respond fast enough for the application. For instance, the results obtained with the dynamic response measurements indicate that the sensor's response (~1.5 s) is much faster than the time it takes to elapse one time constant (~50 s) of the convection–cooling mechanism. In this case, the sensor could be incorporated in a closed-loop configuration with local heaters to keep the *in situ* temperature as close as possible to its reference for the time that the cell culture is outside the incubator.

In addition, the curve obtained from the cooling mechanism 4.22 indicates that the rate of heat loss in the medium where the cells are cultured tends to follow an exponential decay and this rate is proportional to the temperature difference between the medium and its surroundings. Such result is also a relevant information to the biologists during the time the culture is outside the incubator for inspection.

With respect to the results found in the static measurements, the sensor's resolution (0.15 °C) and linearity suggest that the sensor can potentially monitor temperature increments of the culture that could give an indication of the metabolic growth rate as a result of the heat dissipated due to enthalpy changes [36].

It is important to notice that the sensor's circuit design is not optimized for best performance. Therefore, circuit improvements can be made to achieve better resolution or responsitivity, if needed. Regarding the microfabrication challenges, care must be taken when processing materials such as PDMS. After etching, residues may still remain at the surface which can hamper further system-level integration processes such as wire bonding. Non-selective over-etching, on the other hand, might partially or completely remove the materials beneath. Hence, process optimization during the etching phases is of paramount importance for the reliability and reproducibility of the end product.

SELF-HEATING ERRORS

Despite the fact that the self-heating mechanism of the smart temperature sensor exhibits a negligible effect on its resolution, it has the potential to produce a slight temperature offset in the readout during the system's steady-state operation.

If one assumes that conduction is the main heat transfer mechanism happening between the circuitry and the silicon lattice boundary, the energy balance may be calculated with the aid of the heat transfer equation described in Eq. 4.9:

$$\dot{Q} = kA\frac{\Delta T}{\Delta x} \tag{4.9}$$

In which $\dot{Q}$ is the heat transfer rate, the constant of proportionality k is the thermal conductivity of the silicon and equals 148 W/(m °C), A is the area normal to the heat gradient and equals 49 mm^2, ΔT is the temperature difference, and Δx the thickness of the material and equals 400 µm. Therefore, assuming that all power, which equals 36 mW, is converted into heat, the expected error introduced by the self-heating mechanism is only 0.002 °C, and is two orders of magnitude smaller than the 0.2 °C of resolution measured.

FAILURE AFTER ETCHING WITH PES 77-19-04

Unfortunately, many chips (more than 60% of the wafer batch) failed after the aluminum etching step using PES. This may be because the PES etchant also partially attacked the interconnects. The principal hypothesis for this attack was an ingress of the etchant through some of the PDMS membranes that could have been damaged by the vacuum chuck clamping system of the microprobe station during the electrical measurements. The etchant could have diffused through the photoresist-silicon interface and non-uniformly consumed specific locations of the interconnects.

However, if one considers an etch rate of 50 nm/min at room temperature and a total etching time of approximately 20 min, the amount of aluminum consumed should be approximately 1 µm. In other words, the etching time should be enough to remove the 300 nm aluminum from the PDMS but insufficient to etch an interconnect with a thickness of 3.1 µm. A possible explanation for this paradox assumes a localized progressive increase in the etch rate of the solution with temperature due to the highly exothermic reactions involving aluminum oxidation and dissolution.

For this reason, it is crucial to ensure that the PDMS membranes are not damaged and to consider an appropriate etch rate model for a more accurate etch time estimation.

FAILURE AFTER WET MEASUREMENTS

Following the experimental procedure of filling the wells using pre-heated PBS, some chips failed. Although the definitive cause is not determined, three reasons for such failure are possible.

The first one relies upon moisture ingress through the silicon substrate until it reaches the electronics on the front side. This situation is rather implausible because the very thick 5 µm of SiO_2 passivation conjointly with 400 µm of crystalline silicon

should be sufficient to prevent any moisture ingress along the time frame used for the measurements.

The second cause surmises that the moisture seeped out to the front side of the chip through ruptures on the PDMS membrane, due to the vacuum clamping system, or through a detachement at the PDMS–SiO_2 interface. However, no ruptures were found after inspection with an optical microscope. Additionally, PDMS commonly has good adhesion to SiO_2 mainly due to the covalent bonds created with the free hydroxyl (–OH) groups of the SiO_2. An SEM photograph taken at the interface between the PDMS and the SiO_2 showed no evident detachment of the membrane (Fig. 4.23).

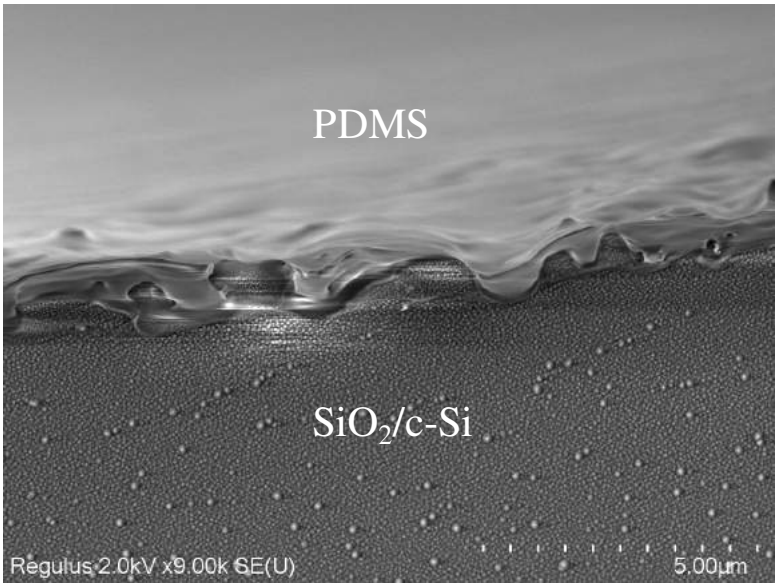


Figure 4.23: Photograph detailing the interface between the PDMS and the SiO_2 using a scanning electron microscope.

The third hypothesis assumes the bond wires have been disjointed from the bond pads due to a poor welding. Figs. 4.24–4.26 show x-ray photographs of the failing PCB samples. Highlighted, one may notice footprints on the bond pads that suggest the exact locations where the wire bonds contacts used to be. The disconnection of the wire bonds to the bond pads is, in principle, the most probable cause for the failure of the chips after repetitive wet measurements.

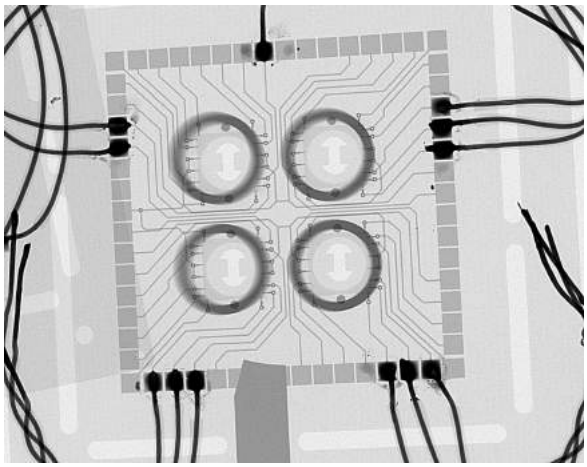


Figure 4.24: X-ray of the PCB from the top view detailing the four wells and the chips.

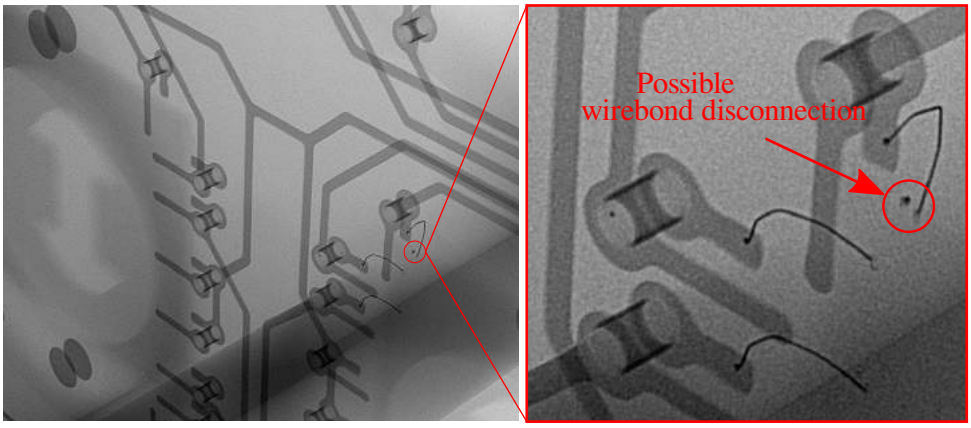


Figure 4.25: X-ray with a tilted view detailing a possible wire bond disconnection.

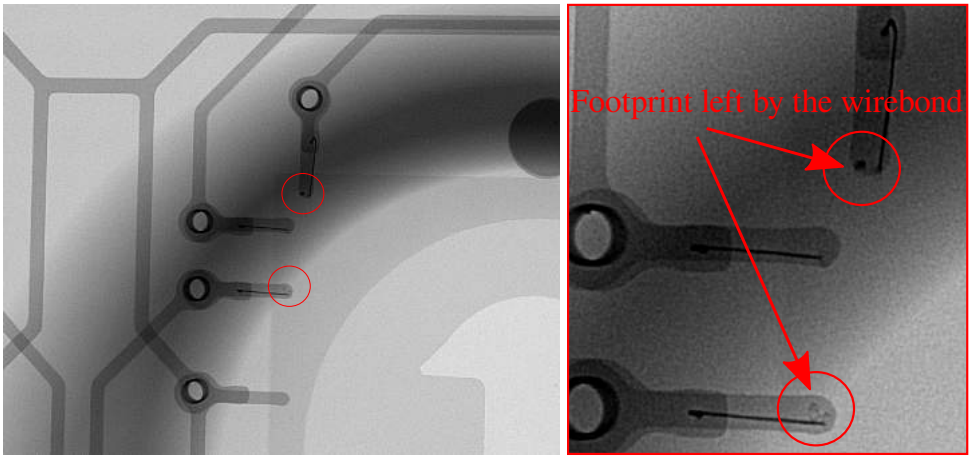


Figure 4.26: X-ray detailing the wire bond footprint left on the bond pads.

4.15. CONCLUSIONS

Cell cultures are maintained at an appropriate temperature and gas mixture inside a cell incubator. Because the *in situ* culture conditions may vary, especially when the culture is outside the incubator, it is advantageous to construct OOCs that are equipped with sensors that can accurately measure in real-time the *in situ* conditions of the cells.

In this work, we investigated the monolithic integration of a BiCMOS smart temperature sensor in our MEMS OOC device. Our in-house large-area BiCMOS technology has been used as a research vehicle for the proof of concept. Advantages of using such process technology include reducing the process complexity and costs often encountered in many BiCMOS technologies. Additionally, the process line is made more flexible, improving the integration compatibility with alien process modules. Ergo, it facilitates the monolithic fabrication of ICs and MEMS for emerging technologies that use large-area smart sensors. By combining BiCMOS and MEMS technology monolithically, it is possible to create OOCs to accommodate the cells over different MEMS structures while integrating high-density electronics for very compact systems that can measure *in situ* physical quantities in the culture medium. The BiCMOS-MEMS co-fabrication method employed a novel IC-interlaced-MEMS fabrication strategy and yielded, for the first time, an OOC device with integrated CMOS sensing functionality for a real-time *in situ* temperature measurement of the cell culture.

Measurement results of our smart temperature sensor indicate that temperature increments of 0.2 $^{\circ}$C can be accurately monitored. This could potentially be used to give an indication of the metabolic growth rate when the culture is inside the incubator. The sensor's time response found was approximately 1.5 s, which is much faster than the time it takes for the temperature of a 0.4 mL medium to drop by 1 $^{\circ}$C.

This work is the first step towards constructing OOCs with integrated large-area BiCMOS electronics for multi-sensing relevant information in the cell culture (O_2, CO_2, pH, glucose, glutamate, grow factors, etc). It is expected that the use of more advanced CMOS

nodes may enable powerful OOCs with a very large degree of multi-sensing integration and actuation in a closed-loop system manner.

Moreover, as a result of sharing common process steps and by minimizing the number of BiCMOS masks used, a more cost-effective and scalable solution is obtained. In order to meet specific requirements of both technologies, a holistic co-design phase has been followed so the trade-offs between circuit performance and micromaching reliability were taken into consideration.

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5

IC-MEMS MONOLITHIC INTEGRATION FOR ARTIFACT-RESILIENT OPTRODES

5.1. MOTIVATION

Studies interested in infraslow brain activity (ISA) fluctuations have recently elicited special attention across the fields of neuroscience and medicine [1–3]. Such signals occur below 0.1 Hz and may reveal specific brain states such as sleep, anesthesia, coma, and wakefulness [4]. Likewise, ISA may reveal signatures of some brain diseases such as migraine aura, which denote sensory disturbances that usually precede a migraine attack. ISA in brain aura is commonly known as cortical spreading depression (CSD), a slow wave of sustained depolarization moving through intact brain tissue [5].

Neuroscientific methods to study migraine include optogenetics [6]. Optogenetics is a neuromodulation technique that allows the control and monitoring of well-defined biological events in excitable cells with high spatial and temporal resolution. This method uses genetic tools to express light-sensitive ion channels, pumps, or enzymes in the target cells [7, 8]. Thereupon, the expressed cells can modulate signaling events during an optical stimulus under specific optical intensity and wavelength requirements.

Experimental setups used in optogenetic studies are usually cumbersome, and the combination of optical and recording units in a single compact device (i.e., an optrode) involves various engineering challenges [9, 10]. Laser-based setups use optical fibers, mechanical shutters, dichroic mirrors, objective lenses, optical modulators, collimators, mixers, emission filters, and other mechanical parts and accessories that are challenging to downsize. A more compact approach uses submillimeter light-emitting diodes (μLEDs) directly mounted on a custom micromachined silicon-based probe. This solution not only evades optical fibers or waveguides but also offers an improved potential for constructing wireless closed-loop optrodes required in the behavioral experimentation of untethered animal subjects.

Recording the electrical activity of infraslow signals with passive microelectrodes is also particularly demanding [11]. Oftentimes, optrodes designed for deep-brain studies require long wires to interface the microelectrodes to general-purpose amplifiers. These passive solutions are vulnerable to low-frequency noise and common-mode interference, which, in turn, impairs the signal quality of the recordings. Moreover, general-purpose amplifiers contain a bandpass filter nature which is inadequate for measuring ISA.

Another modality of interference in optogenetics is the so-called photo-induced artifact [12, 13], which occurs when photons illuminate electrodes in an electrolyte medium with sufficient energy to emit electrons from its surface. Although there is ambiguity on the detailed mechanism behind its cause, the literature primarily ascribes it to the Becquerel effect [14, 15]. Most importantly, some works reported that photo-induced artifacts in silicon probes have the time-domain appearance and spectral features of genuine local field potentials (LFPs) [16]. Such conclusions imply that photo-induced artifacts may play a decisive role during signal discrimination due to false positives. Controlling artifacts with an in-situ solution is more promising than post-processing techniques because it relaxes the signal bandwidth and power without transmitting unnecessary information. Lastly, photo-induced artifacts may saturate the recording amplifiers, blanking out any neural activity information.

Therefore, it is essential to fabricate optrodes with in-situ μLEDs and an in-situ DC-

coupled low-noise amplifier to enable a robust measurement of infraslow brain activity under optogenetic experimentation, while mitigating any source of interference.

Fig. 5.1 shows an artistic impression of the envisioned optrode that includes the μLEDs and electrodes. For visualization purposes, the figure also details a photograph of a passive optrode previously fabricated and the in-situ electronics on the layout level.

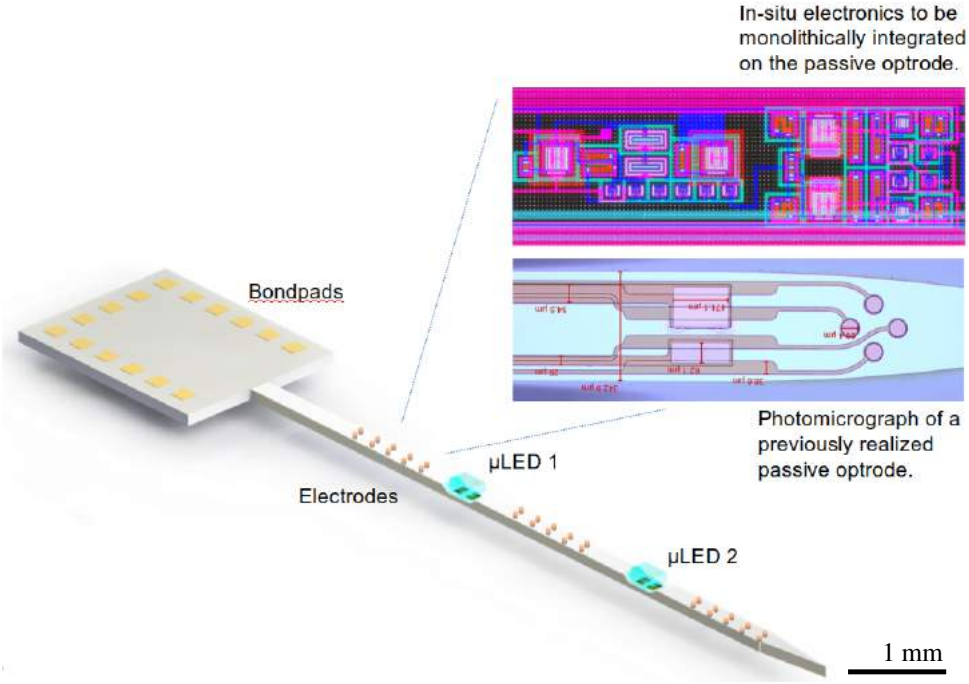


Figure 5.1: Artistic impression of the envisioned silicon-based optrode detailing the recording units and two μLEDs along the shaft. The bondpads on the optrode's head interface to a printed circuit board (PCB). The zoomed images show a photomicrograph of a passive optrode previously fabricated and the layout of the electronics to be placed in-situ along the optrode's shaft. Artwork created by the author of this thesis.

A top-level hierarchy of the whole system is shown in Fig. 5.2. A printed circuit board (PCB) assembles the optrode and is used to fan out the signals from the optrode's bond pads. A flexible zero insertion force (ZIF) cable transfers the signals to an Arduino board that converts them to the digital domain. Further, it transmits them to a user interface (UI) via a Bluetooth link. A commercial low-noise, low-dropout regulator (LDO) ensures all voltages used for powering meet the specifications while mitigating any disturbances coupled to the power lines.

This chapter focuses on the design process used in the IC-MEMS monolithic fabrication of artifact-resilient optrodes for measuring infraslow signals.

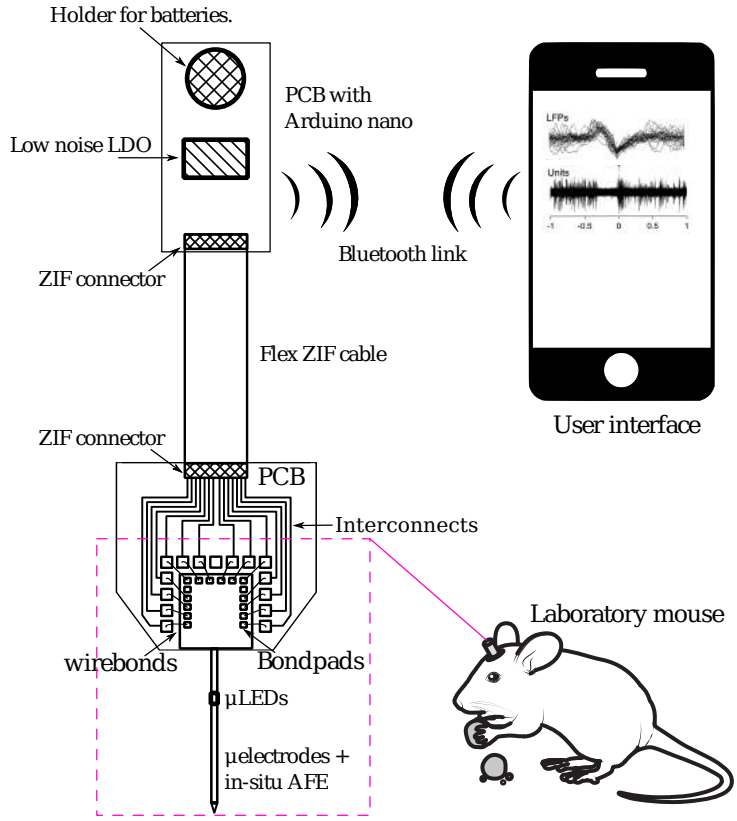


Figure 5.2: Sketch of the envisioned top-level hierarchy for the optrode system. AFE stands for analog front-end. Artwork created by the author of this thesis.

5.2. SPECIFICATIONS

Preceding the optrode's design, requirements that satisfy the device's correct operation according to its function, performance, and operational conditions shall be prepared.

5.2.1. FUNCTIONAL SPECS

The optrode's design shall incorporate specific functional features to perform tasks such as the perforation and penetration into the brain tissue, narrow-band light emission for stimulation, sensing, filtering, amplification, and transportation of the electrophysiological recordings. The minimum tasks that the optrode shall execute according to its design domains are listed in Table 5.1.

Perforation and penetration are mechanical tasks that the probe executes to puncture the dura and enter the brain matter. Narrow-band light emission is an optical task performed by µLEDs. The use of an in-situ µLED precludes the inclusion of extra accessories required in laser-based setups and, thus, it is simple in terms of system-level in-

Table 5.1: Minimum functional requirements for the optrode.

Functional domains			
Physical	**Mechanical**	**Electrical**	**Optical**
Depth	Perforation	Sensing	Narrow-band emission
Width	Penetration	Filtering	Light modulation
		Amplification	
		Transportation	

tegration. Microelectrodes sense the electrophysiological signals and are the easiest option to fabricate on a silicon wafer using deposition methods. In-situ monolithic single-pole amplifiers carry out filtering and amplification roles, while electrical wires interface the signals from the amplifier's output to the load. Table 5.2 shows the desired minimal functions to be performed by the objects.

Table 5.2: Assignment of the required functions with their objects.

Functions \ **Objects**	Sharp tip	Rigid probe	Electrode	Amplifier	Wires	µLED
Perforation	**x**					
Penetration		**x**				
Sensing			**x**			
Filtering [1]				**x**		
Amplification				**x**		
Transportation					**x**	
Narrow-band emission						**x**
Light modulation						**x**

5.2.2. PERFORMANCE SPECS

OPTICAL

In optogenetics, the light source shall deliver an optical intensity higher than the minimum threshold required to activate the light-sensitive proteins (opsins) expressed in the target cells. The specific optical intensity required may vary depending on the type of opsin used, the location and density of the opsin expression in the target cells, and other experimental parameters. For example, for the commonly used opsin channelrhodopsin-2 (ChR2), a typical threshold intensity is around $1\,\mathrm{mW/mm^2}$ at a

[1] In reality, the amplifier's single pole performs the desired active low-pass filtering characteristic.

nominal wavelength of 460 nm, but this can vary depending on the specific application and experimental conditions [17]. Naturally, it is important to optimize the light intensity to ensure that the desired level of opsin activation is achieved without causing unwanted cellular damage or other side effects [18].

Silicon's 1.1 eV bandgap energy restricts the material's ability to emit photons in the blue spectrum, making blue light sources directly from silicon impractical. Accordingly, a non-monolithic solution[2] was chosen to integrate light sources on the silicon probes.

The µLED model DA1530 manufactured by Cree™ combines InGaN materials on a silicon-carbide substrate to emit photons at a dominant wavelength of 460 nm, under a radiant flux of 23– 27 mW and 20 mA of nominal current consumption. The bond pad's bottom design allows eutectic die attach, which eliminates the use of wire bonds while improving the device thermal management.

Additionally, its compact design (i.e., 150×300×80 µm) enables integration on the optrode's shaft without jeopardizing the footprint. Fig. 5.3 sketches the µLED's physical dimensions in bottom and side views.

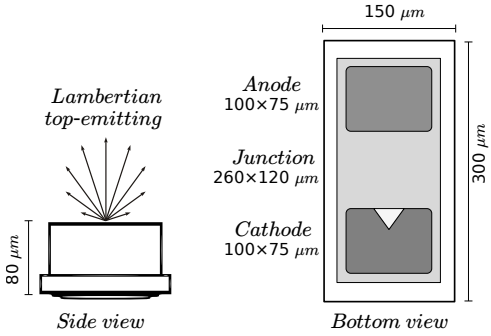


Figure 5.3: Physical specifications of the commercial light source to be used. Adapted from [19].

Information on the µLED's dimensions also feeds the optrode's physical specifications. Hence, there is an interplay between the optical and physical design domains to be solved by co-design.

PHYSICAL

Physical specifications refer to the optrode's dimensions and include its length, width, thickness, shape, profile, or any other spatial attribute relevant to its physical design. Laboratory mice are often the animal subject used in optogenetic experimentation. The mouse's brain is tiny, and studies have estimated that the average brain volume of an adult male mouse is around 400 mm^3, while the average brain volume of an adult female mouse is around 350 mm^3 [20, 21].

The probe insertion causes injury and displacement of the brain matter, which may be vital to the animal if not adequately minimized. Minimizing injuries and displacement of the brain matter are crucial in animal experimentation. Thereby, the probe's de-

[2] Specifically, hybrid integration.

sign shall minimize the footprint and allow for a maximum brain matter displacement up to 0.1 % [3] of the total brain volume.

The µLED's physical dimensions, alongside the required space for interconnects and the in-situ AFE, specify the minimum width feasible for the optrode's shaft. An estimation of this metric yields a range from 170 to 240 µm.

The shaft's length depends on how deep the brain layers under study are. An anatomic atlas with a stereotaxic coordinate system (Fig. 5.4) supplies the information for estimating the minimum probe's depth required to reach specific anatomic regions.

The cortex, hippocampus, and thalamus are the principal cerebral regions of experimental interest, ordered by depth, from superficial to deep. Therefore, considering the distance between the Ventral Lateral Nucleus (VLL), which is a nucleus located in the thalamus, and the Layer I of the cerebral cortex (~4 mm) plus the headroom length required to exceed meninges and the saline well (~1 mm), a minimum shaft length of 5 mm shall be created.

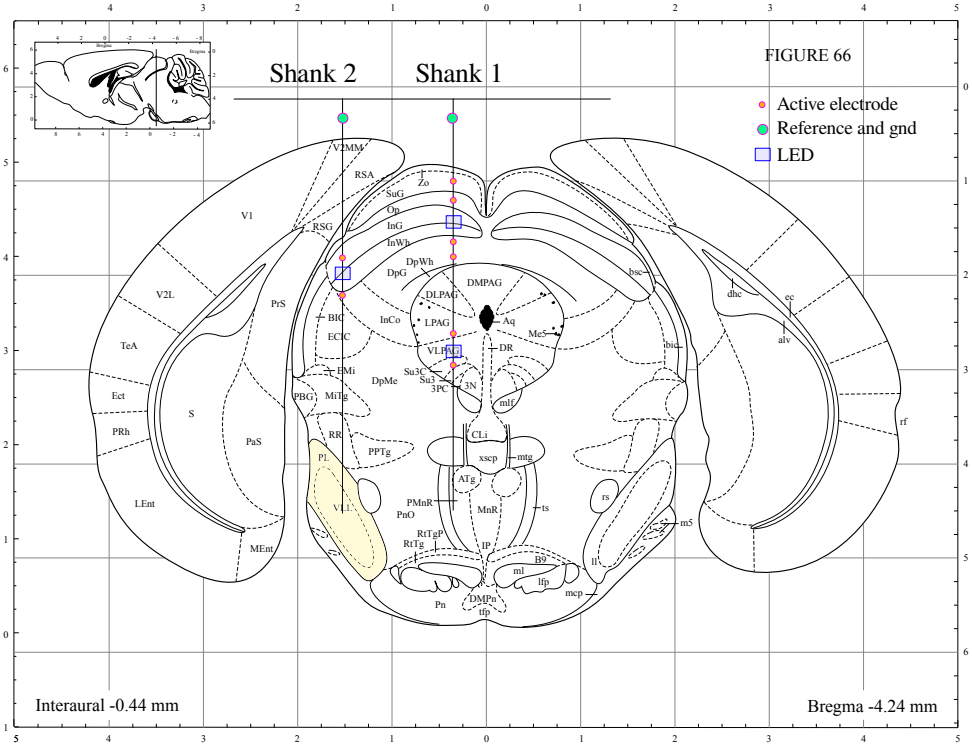


Figure 5.4: Anatomic cross-sections of the mouse's brain under the stereotaxic coordinate system detailing the position where the electrodes and µLEDs shall be inserted. Coordinates are in millimeters. Adapted from [22].

[3] No universally accepted maximum brain matter displacement exists for an adult mouse during experimentation, as the acceptable amount of displacement may depend on the aim of the experimental studies. A 0.1 % displacement of the total cerebral volume is an educated guess used by the author of this thesis to allow for a design that can accommodate various experiments.

Given that this research project involves collaborators from various research institutions with distinct experimentation needs, the author of this thesis developed six different designs to suit the requirements of each individual study. The number of shafts, electrodes, and LEDs, in conjunction with their coordinates and spacings on the optrode, are some variables that can be adapted as long as the technological constraints are not exceeded. Fig. 5.5 shows an example of a floorplan used to conceive the multiple designs. For additional details, please refer to Appendix C.

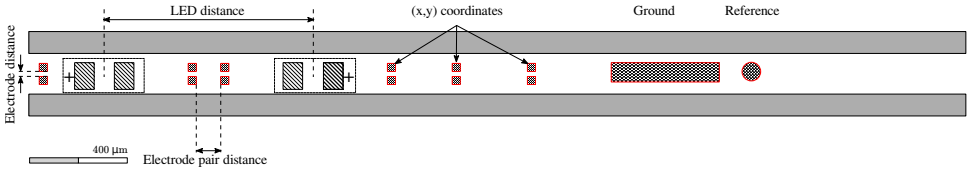


Figure 5.5: Optrode's floorplan. The (x,y)–coordinates of the elecrodes, µLEDs, and the distances between each pair of electrode and µLED are examples of physical specs that feeds the optrode's physical design.

Different electrode types (i.e., working, reference, and ground) and configurations were also considered—for instance, in pairs or in a tetrode configuration. The latter enables electrophysiological recordings with single-cell signal discrimination.

MECHANICAL

The optrode's physical design shall also consider how forces affect its compliance. The minimum force applied to the probe that penetrates the dura and pia mater typically ranges between 1–30 mN [23, 24]. The generated thrust includes radial and axial compression forces, frictional forces, and clamping forces (Fig. 5.6).

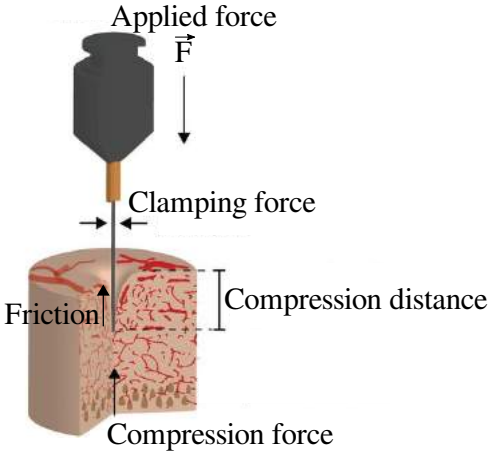


Figure 5.6: Insertion of the probe creates reaction forces that contributes to buckling. Adapted from [24]

There is a high risk of buckling the probe during the perforation of the dura mater. Ideally, the optrode's physical design should minimize the buckling effect with the probe

penetrating straight down into the brain. The maximal force that the optrode's shaft withstands without buckling is:

$$F_{\text{buckling}} = \frac{\pi^2 \cdot E \cdot I}{(K \cdot L)^2}, \text{ with } I = \frac{W \cdot h^3}{12} \tag{5.1}$$

In Eq. 5.1, ***E*** is the Young's modulus of the probe's material, ***I*** the moment of inertia defined by the cross-section, ***K*** is the effective length factor, and equals 0.7 for a fixed probe at one side, ***L*** is the length, ***W*** the width, and ***h*** is the thickness of the probe tip.

With the aid of Table 5.3 and the physical specs derived in the previous subsection, one can determine the minimum thickness until buckling, which equals 50 µm. In this research project, a more solid value of 100 µm was used for the probe thickness.

Table 5.3: Parameters used for the determination of the minimum shaft thickness.

Symbol	Description	Value used	Units
E	Young's modulus of silicon	179	GPa
F	Insertion force	0.3	N
K	Effective length factor for a fixed-free probe	0.7	–
L	Length	6	mm
W	Width	0.3	mm

ELECTRICAL

Electrical specifications for the amplifier design include details from the source, the load, and the transfer type.

Signals produced by the source and sensed by the electrodes are extra-cellular potentials and thus in the voltage domain. Specifications from such signals include the voltage swing, noise, offset, bandwidth, and source impedance.

There are two types of load to consider: the first one refers to the load associated with the setup used for wafer-level measurements under a microprobe station; the second refers to the system-level implementation employing an analog-to-digital converter (ADC). Analyzing both scenarios is necessary because each one demands different specifications.

Specifications from the transfer include the signal-to-noise ratio (SNR), bandwidth, and the amount of distortion that does not seriously hinder the interpretation of the studies.

THE SOURCE: NATURE OF THE INFORMATION

The electrophysiological signals of interest can be categorized according to their importance to the experimentation.

The primary (most significant) information is infraslow signals, including cortical spreading depression. Such signals consist of a negative potential difference with an amplitude range of 10–30 mV and a bandwidth from 0.01 Hz to 0.1 Hz [6, 25–27].

The secondary information is local field potentials consisting of 100 µV–1 mV in amplitude and 1–300 Hz in bandwidth [28, 29].

The tertiary information is multi-unit action potentials (MUAP) with an amplitude range from 50 µV to 500 µV and bandwidth from 100 Hz to 10 kHz [30] [4]. Table 5.4 lists the specifications from the source.

Table 5.4: Electrophysiological signals of interest according to their degree of significance to the experiments.

Specs	**Primary**	**Secondary**	**Tertiary**
	CSD	**LFP**	**MUAP**
Domain	Voltage	Voltage	Voltage
Amplitude	10–30 mV	100 µV–1 mV	50–500 µV
Bandwidth	0.01–0.1 Hz	1–300 Hz	100 Hz–10 kHz

THE SOURCE: DISTURBANCES AFFECTING THE READOUT

Noise and interference are disturbances that degrade the quality of the electrophysiological signals. Thus, their effect must be limited.

Sources of noise include thermal and flicker noise coming from the electrodes and the amplifier. The noise contribution from the electrodes is better estimated with the knowledge of the source-impedance model detailed in the next subsection.

Sources of interference may come from electrostatic coupling, also known as capacitive coupling; magnetostatic coupling, also known as inductive coupling; or electromagnetic coupling, also known as radio-frequency interference. Additionally, disturbances may be introduced into the system due to motion artifacts or the light source. The former stems from axial micromotions of the probe due to swelling or blood pumping, causing local ion concentration changes and resulting in half-cell potential fluctuations. The latter arises from photo-induced artifacts or electrostatic coupling from the µLEDs' interconnects.

THE SOURCE-IMPEDANCE MODEL

An electrode immersed in an electrolyte solution affects the distribution of free charges at the electrode–electrolyte interface building the so-called electrical double layer (EDL).

The EDL refers to two parallel layers of ions surrounding the electrode. The first layer consists of ions adsorbed onto the electrode's surface due to electrochemical reactions; the second of ions attracted via Coulomb forces. More information about the theory behind the electrical double layer can be found in [31, 32].

Fig. 5.7 details a lumped-element model that simplifies the behavior of spatially distributed charges at the electrode–electrolyte interface. Such a model is convenient for

[4] It's also worth noting that the amplitude of electrophysiological signals can depend on the distance of the recording electrode from the source of the signal, as well as the materials and placement of the electrode. Thus, these values are just rough estimates.

estimating the source impedance and the amount of thermal noise generated by the electrode.

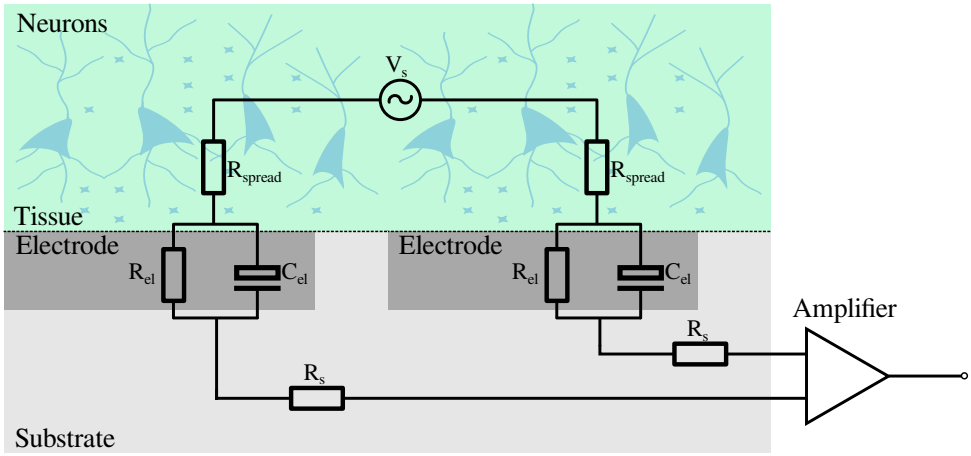


Figure 5.7: Source-impedance model of a pair of electrodes for a differential mode measurement.

In this model, V_s is a voltage source that characterizes the electrophysiological signal, R_{spread} accounts for the resistance that describes the extracellular space, C_{el} is the capacitance associated with the EDL, R_{el} models any leakage current happening at the electrode–electrolyte interface and R_s is the equivalent resistance of the interconnects to the in-situ amplifier.

Electrochemical impedance spectrometry (EIS) results of the electrodes from a test optrode previously fabricated, in conjunction with the formulas presented in [33], were used to estimate the values from each element in the model (Table 5.5).

Table 5.5: Values estimated for each element in the source impedance lumped model.

Element	Value	Unit
R_{spread}	30	kΩ
C_{el}	0.5	nF
R_{el}	2.5	MΩ
R_s	420	mΩ

From Table 5.5 one can estimate the spectral noise density created by the source impedance, which equals approximately 290 $nV/\sqrt{Hz}$.

THE ELECTRODE OFFSET

Electrode offset is a drift mechanism that results from the half-cell potential between a pair of mismatched electrodes and manifests itself as a DC signal.

Mismatches occur due to variance in the material's properties such as porosity, chemical species, surface area, and electrode size. The DC offsets are usually in the

submillivolt range when recording between two microelectrodes fabricated under cleanroom-based deposition methods [34]. Unfortunately, there is no explicit formula to estimate the offset in electrodes, and quantitative studies measured during recordings are generally lacking in the literature.

THE LOAD SCENARIOS

Before prototyping the optrode's chips on a PCB, wafer-level characterization under a microprobe station is used to assess the circuit's performance. The total load impedance (Z_L) must be estimated to ensure that the AFE's output stage transfers enough power to the measurement setup. An impedance estimation of 1 MΩ|| 300 pF includes the interconnects' and bond pads capacitance, wafer microprobe impedance, oscilloscope's probe impedance, and approximately three meters of coaxial cable. Fig. 5.8 shows a plan of the wafer-level measurement setup.

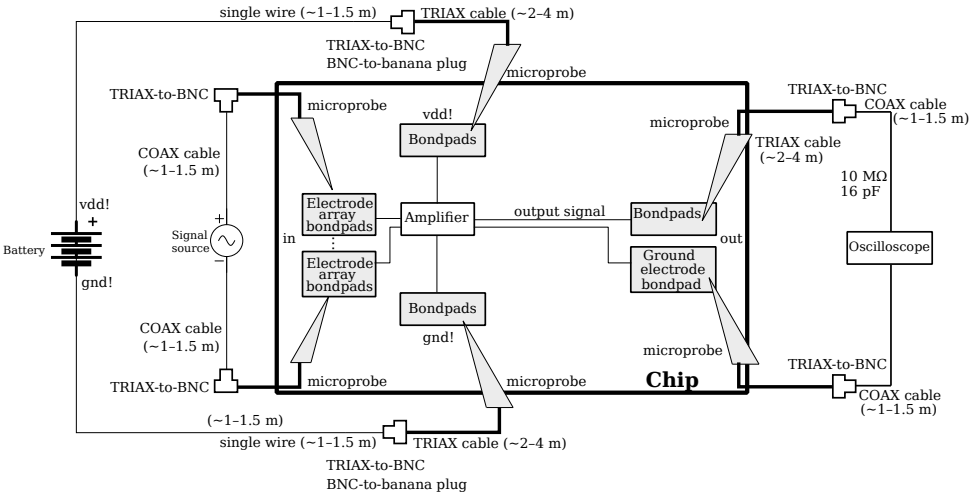


Figure 5.8: Planned measurement setup for the chips under a wafer microprobe station.

The second load scenario refers to the system-level implementation that uses a differential successive-approximation (SAR) ADC included in the Arduino Nano 33 BLE Sense. This ADC supports up to 14-bit resolution with oversampling. Furthermore, the 45×18 mm form factor in five grams of weight, along with the Bluetooth capabilities offered by this board, make it favorable for system-level integration. Based on information from the Arduino datasheet [35, 36], the ADC's input capacitance is 10 pF, corresponding to the total load estimated on the amplifier's output stage.

The amplifier's output voltage excursion (V_L) must be limited to the ADC's full-scale (FS) range from 0 V to 3.3 V to minimize errors from signal clipping in the analog-to-digital conversion. Table 5.6 summarizes the main specifications of the load.

The quantization noise generated by the ADC is a by-product added to the AFE's output and, consequently, adds to the AFE's input-referred noise (IRN). Since the quantization noise amplitude is a random variable uniformly distributed between ±LSB/2 with a

Table 5.6: The specifications of the load.

Parameter	Description	Value			Notes
		Min.	Nom.	Max.	
V_L	AC output voltage across the load	0 V	–	3.3 V	
Z_L	Impedance	10 pF	–	1 MΩ$\|\|$ 300 pF	

zero mean value, the RMS value is the standard deviation of this distribution and equals LSB/$\sqrt{12}$. Since FS equals 3.3 V and assuming a digital output encoded in 14 bits, the LSB equals

$$\text{LSB} = \frac{\text{FS}}{2^{N_{\text{bits}}}} \approx 200\,\mu\text{V}. \tag{5.2}$$

Hence, the quantization noise (σ_{QN}) added to the AFE's output equals

$$\sigma_{\text{QN}} = \frac{\text{LSB}}{\sqrt{12}} \approx 60\,\mu\text{V}_{\text{rms}}. \tag{5.3}$$

5

THE TRANSFER: AFE'S SPECS

The peak-to-peak quantization noise voltage is approximately six times its RMS value assuming a 99.7% confidence level. Based on this observation, a minimum gain higher than seven is required to ensure that the AFE can detect the weakest signal, with a peak-to-peak magnitude of 50 µV, at its input. This conclusion derives from $(6 \times 60\,\mu\text{V}_{\text{rms}})/50\,\mu\text{V}_{\text{pp}}$, which yields a result of 7.2.

Based upon an expected largest voltage magnitude of 30 mV_{pp} from the input signal[5], an ideal gain of 110 would be required because the quotient between the FS (3.3 V) and the expected largest voltage magnitude (30 mV_{pp}) equals 110. However, it is worth remarking that the total voltage error at the amplifier's input port—which includes the source offset, the amplifier's input-referred offset, and voltage errors resulting from random mismatches in the feedback network—appears in series with the input signal, thereby contributing to a shift in its DC level. Therefore, by estimating an unfavourable DC voltage error of 35 mV in series with the amplifier's input port, the largest resulting peak-to-peak voltage across the amplifier's input port is 65 mV. Consequently, the upper limit for the amplifier's gain that specifies the onset of clipping distortion in the signal is 50. The derivation of this upper limit results from the quotient between the FS (3.3 V) and the peak-to-peak voltage (65 mV_{pp}), which yields a result approximately equal to 50. Since the fraction of this voltage error mainly comes from the source offset, a maximum input-referred offset of 5 mV was set as a goal for the amplifier.

Another pertinent specification related to the transfer is the frequency response. In light of the information in Table 5.4, the highest frequency component expected from the signal is 10 kHz. Hence, the bandwidth resulting from the maximally flat magnitude response equals 10 kHz. Additionally, based on the premise that the amplifier exhibits a

[5] For simplification purposes, the calculations presented herein assume that the signal under consideration is unipolar.

single-pole characteristic, and assuming a gain of 50, it can be deduced that a unity-gain bandwidth of 0.5 MHz is desired. This conclusion results from the fact that there are 1.7 decades up from the 10 kHz bandwidth before the magnitude response of the amplifier drops to unity.

Following the transfer's specification, the SNR represents the relationship between the signal to be processed and the noise introduced by the processing chain. Assuming that the noise introduced by the processing chain is just marginally smaller than the minimum discernable signal, the maximum SNR becomes the ratio of the smallest and largest signal that can be processed simultaneously. According to this definition, the maximum SNR equals the dynamic range in a linear system without a programmable-gain amplifier, PGA. In other words,

$$\mathrm{SNR}_{\mathrm{max}} = \mathrm{DR} = 20\log_{10}\frac{30\,\mathrm{mV_{pp}}}{50\,\mu\mathrm{V_{pp}}} = 55.5\,\mathrm{dB}. \tag{5.4}$$

Another relevant specification for the transfer refers to the highest degree of distortion the input signal may experience without significantly losing its information quality. The non-linear nature of amplifiers contributes to the total distortion added to the signal. The amount of tolerable distortion that does not compromise the signal's interpretation quality mainly depends on the subjective experience of the neuroscientist. For a more objective assessment, the state-of-the-art literature provides a better estimate for the amount of distortion often tolerated in neural amplifiers for electrophysiological recordings. Table 5.7 presents typical values of the Total Harmonic Distortion (THD) found in the literature for neural amplifier systems.

Table 5.7: Typical values for the total harmonic distortion in neural amplifiers found in the state-of-art literature.

Parameter	[37]	[38]	[39]	[34]
Process	65 nm	65 nm	65 nm	180 nm
Supply voltage	0.5 V	0.5 V	1 V	1 V
THD	2 %	0.1 %	1 %	2 %

As shown in Table 5.7, the values for the THD range from 0.1–2 %. Hence, a THD metric of less than 0.1 % was set for this project. The main specifications for the transfer are summarized in Table 5.8.

Table 5.8: The specifications of the transfer.

Parameter	Description	Value			Notes
		Min.	Nom.	Max.	
SNR	Signal-to-noise ratio	55.5 dB	–	–	
Input offset	V_{os}	–	–	< 5 mV	
BW	Bandwidth	–	10 kHz	–	
THD	Total harmonic distortion	–	–	< 0.1 %	

5.2.3. OPERATIONAL SPECS

The optrode shall be inside the brain of a mouse for chronic studies.

The mouse's body temperature is 37 °C and must not deviate more than 1 °C over the experimentation period.

The immune response, among other stress factors, often contributes to the degradation of the probe's performance in measuring signals. Therefore, passivation layers are essential features to be considered. Some studies show that silicon oxide, silicon nitride, and silicon act as barriers against moisture ingress [40, 41]. Hence, deposition of such materials shall be considered. The investigation of the probe's reliability due to moisture ingress, however, was kept out of the scope of this research.

5.3. CO-DESIGN: OPTICAL, PHYSICAL, MECHANICAL AND ELECTRICAL DOMAINS

Co-designing is a task that usually follows the derivation of the specifications. Nevertheless, extracting, organizing, and interpreting specifications are procedures that may overlap with co-designing because the specs of one design domain may overrule solutions of other domains.

For instance, the physical dimensions of the µLED might take precedence over the intended design specifications for the shaft width embodied within the optrode. Likewise, the minimum spacings between different layers that comply with the circuit design layout rules, circuit topology compactness, and particularities of the built-in technology[6] influence the shaft's width design and area usage. Since it is not evident how and which specs from which domain affect or overrule design decisions in other domains, the co-design strategy may involve some heuristics such as educated guesses and trial-and-error methods to identify a solution.

All in all, finding solutions to minimize the optrode's footprint is a co-design endeavor that involves multiple domains; the specification from one may instruct the design choice of others.

Another co-design example involved finding physical attributes to solve the optrode's mechanical performance, as in the case of the minimum shaft thickness calculation before buckling. Notice that the device's length and width information derived from other design domains was used for that calculation.

5.4. SEMICONDUCTOR TECHNOLOGY ASSESSMENT AND CONSTRAINTS: THE DIMES03 IC PROCESS

Assessment of the semiconductor technology is a valuable task for estimating the physical space available to fabricate the electronics.

DIMES03 is a double metal baseline BIFET process for smart-sensor experimentation designed to optimize the NPN transistor performance using a washed-emitter-base

[6] For instance, the device isolation type such as guard-rings, LOCOS, or shallow trench isolation (STI).

(WEB) structure. The process design kit (PDK) contains resistors, capacitors, diodes, vertical NPN and lateral PNP bipolar transistors, and joined- or separated-gate p-channel JFETs. The latter is a low-noise device with a 15 GHz transit frequency (f_T), a pinch-off voltage of −2.33 V, and a breakdown voltage of 15 V.

Table 5.9: DIMES03 process library. Notice the resistance tolerance in the column "Parameters".

Cell	Device type	Parameters	Total area usage
npn2x1	npn	emitter area = 2 μm^2	30.6×26.8 μm^2
npn4x1	npn	emitter area = 4 μm^2	30.6×28.8 μm^2
npn8x1	npn	emitter area = 8 μm^2	30.6×32.8 μm^2
npn16x1	npn	emitter area = 16 μm^2	30.6×40.8 μm^2
npn32x1	npn	emitter area = 32 μm^2	36.6×40.8 μm^2
spnp2x6	substrate pnp	emitter area = 12 μm^2	20×24 μm^2
spnp2x15	substrate pnp	emitter area = 34 μm^2	26×24 μm^2
spnp2x30	substrate pnp	emitter area = 60 μm^2	32×26 μm^2
lpnp30x2	lateral pnp	emitter area = 60 μm^2	34.8×62.6 μm^2
pjfw2l1	p-jfet	w = 2 µm l = 1 µm	31×26 μm^2
pjfw4l1	p-jfet	w = 4 µm l = 1 µm	37×26 μm^2
pjfw20l1	p-jfet	w = 20 µm l = 1 µm	37×35.5 μm^2
jfet02	p-jfet	w = 100 µm l = 1 µm	63×64.5 μm^2
res25lp	resistor	r = 25 Ω±5 %	34×44 μm^2
res50lp	resistor	r = 50 Ω±5 %	32×32 μm^2
res100lp	resistor	r = 100 Ω±5 %	36×30 μm^2
res250lp	resistor	r = 250 Ω±5 %	43×28 μm^2
res500lp	resistor	r = 500 Ω±5 %	60×28 μm^2
res1k0lb	resistor	r = 1000 Ω±10 %	35.5×29 μm^2
res2k5lb	resistor	r = 2500 Ω±10 %	40.5×28 μm^2
res5k0lb	resistor	r = 5000 Ω±10 %	51×28 μm^2
res10klb	resistor	r = 10 kΩ±10 %	72×28 μm^2
res20klb	resistor	r = 20 kΩ±10 %	114×28 μm^2
res40klb	resistor	r = 40 kΩ±10 %	81×44 μm^2
res80klb	resistor	r = 80 kΩ±10 %	72.5×76 μm^2
res100k	resistor	r = 100 kΩ±10 %	56.5×55 μm^2
res400k	resistor	r = 400 kΩ±10 %	87×91.5 μm^2
pad	bonding pad	c = 508 fF	104×104 μm^2
padHF	bonding pad	c = 137 fF	54×54 μm^2

5.5. BLOCK DIAGRAM OF THE INFORMATION-PROCESSING TASKS

With the electrical specs extracted and the semiconductor technology assessed, the design of an integrated circuit is viable. Firstly, it is useful to construct the block diagram that describes the information-processing tasks (Fig. 5.9).

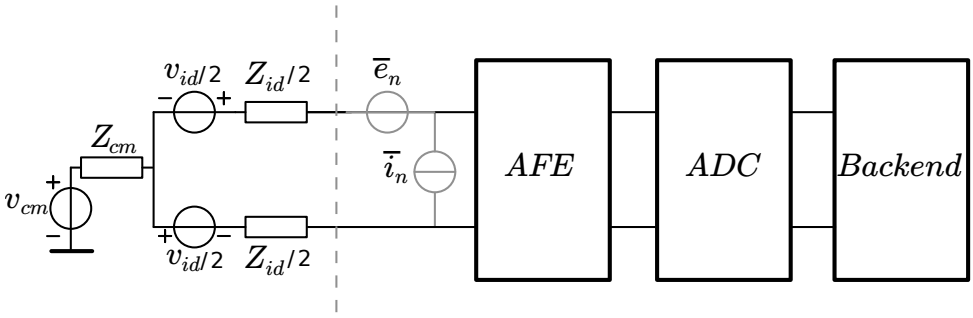


Figure 5.9: Functional blocks to perform the information-processing tasks.

In Fig. 5.9, v_{cm} and v_{id} represent the common-mode and differential-mode source voltages, Z_{cm} and Z_{id} refer to the common-mode and differential-mode source impedances, and $\overline{e}_{\text{n}}$ and $\overline{i}_{\text{n}}$ the input-referred noise voltage and current, respectively. The backend refers to any user interface that follows the ADC.

MEASUREMENT STRATEGY: THE 'RIGHT LEG DRIVING' TECHNIQUE

The AFE amplifies the biosignals measured differentially, viz. differential-mode (DM) signals, between a pair of electrodes. The amplitude levels presented in Table 5.4 show that these biosignals are electrically weak, and common-mode (CM) interferences frequently hampers their detection. A measurement strategy used to mitigate interferences in the recordings involves negative feedback of the CM signal into the amplifier's input. This feedback mechanism is achieved by sensing the common mode at the AFE's output and returning the amplified and inverted error difference to a third lead, which imposes a CM bias on the brain tissue (Fig. 5.10). As a consequence, the CM interference is substantially reduced at its source. This technique is known as the "Right Leg Driving" (RLD) technique, and along with a high common-mode rejection ratio (CMRR) of the amplifier, it offers very high-quality biopotential measurements [42, 43].

5.6. AFE DESIGN

The methodology used for the AFE synthesis was divided into two parts: 1) the DM, and 2) the CM synthesis.

The design sequence benefited from noise optimization of the input stage, reduction of nonlinear distortion in the amplifier's output stage, and bandwidth maximization by

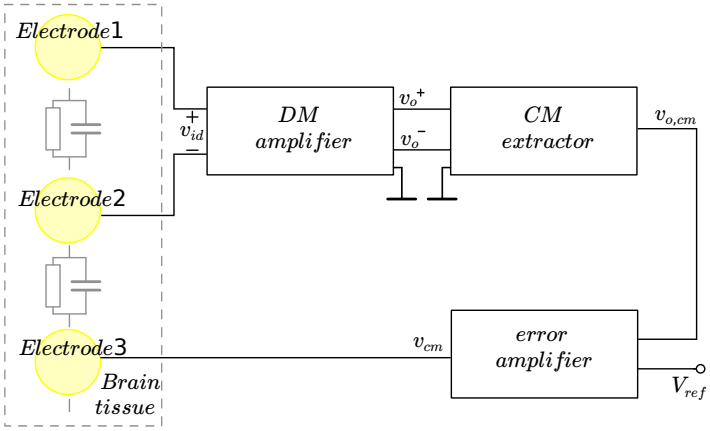


Figure 5.10: Measurement strategy based on the RLD technique. The AFE amplifies the differential-mode signal, v_{id}, whereas a feedback mechanism to a third electrode sets the common-mode bias, v_{cm}, imposed on the brain tissue.

5

the intermediate stage. Subsequently, biasing of the DM circuit was arranged.

After conclusion of the DM design, the CM stage was designed to provide CM measurement, comparison with a reference, and correction via negative feedback.

THE ASYMPTOTIC GAIN MODEL

The asymptotic gain model (Fig. 5.11) was used for the AFE synthesis because it completely characterizes feedback amplifiers, including loading effects and the bilateral properties of active devices and feedback networks.

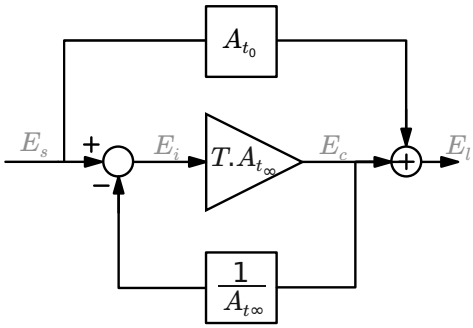


Figure 5.11: Block diagram of the asymptotic-gain model used to characterize negative-feedback systems.

In Fig. 5.11, the term $A_{\mathrm{t_0}}$ represents the direct transmission between the signal source, E_{s}, and the load, E_{l}, $A_{\mathrm{t_\infty}}$ represents the amplifier's ideal gain, and T is the return ratio with the input source disabled and equals the negative of the loop gain (L) in the case of a single-loop system composed of unilateral blocks. For simplification purposes, the term loop gain will be used interchangeably.

The source-to-load transfer, E_l/E_s, of the feedback system is given by:

$$A_t = A_{t_\infty} \frac{T}{1+T} + A_{t_0} \frac{1}{1+T}. \tag{5.5}$$

From Eq. 5.5, one may derive that:

$$\lim_{T \to \infty} A_t = A_{t_\infty}. \tag{5.6}$$

Eq. 5.6 suggests that when the loop gain is sufficiently large, the effect of A_{t_0} in the transfer is nullified and the closed-loop gain of the feedback system equals the ideal gain. From another perspective, the accuracy of the closed-loop gain improves by maximizing the loop gain—an essential metric to be considered when designing negative-feedback amplifiers.

The AFE's design involves two major parts: the feedback network and the nullor implementation (Fig. 5.12). The latter is a two-port network representing an ideal amplifier with all transmission parameters equal to zero; the former implements the transfer type by sensing the nullor's output and comparing it to the input.

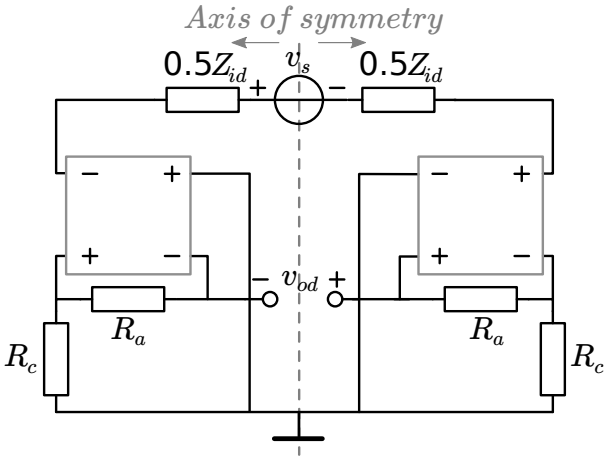


Figure 5.12: Balanced ideal amplifier implemented with a nullor and a feedback network. The signal source is represented by v_s and its impedance Z_{id}. The feedback network comprises the resistive elements R_a and R_c. The voltage v_{od} is the amplifiers's output quantity.

5.6.1. THE FEEDBACK NETWORK

The desired gain for the amplifier per the specifications in Tables 5.4 and 5.8 is 50, whereas a minimum of seven ensures that the AFE can detect the weakest signal at its input. In order to relax the power consumption, a two-stage amplification with a transfer equal to ten was chosen to better accommodate the area and power budgets while ensuring that the weakest signal at the amplifier's input port is further intelligible at its output. As a result, the required source-to-load transfer becomes:

$$A_{t_\infty} = 1 + \frac{R_a}{R_c} = 10 \tag{5.7}$$

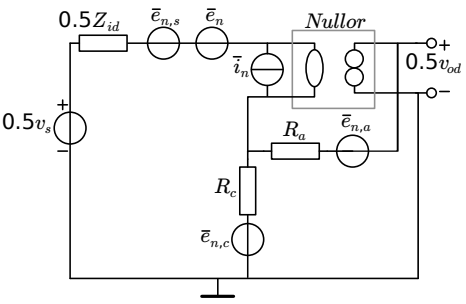
5.6.2. THE NULLOR IMPLEMENTATION

NOISE OPTIMIZATION

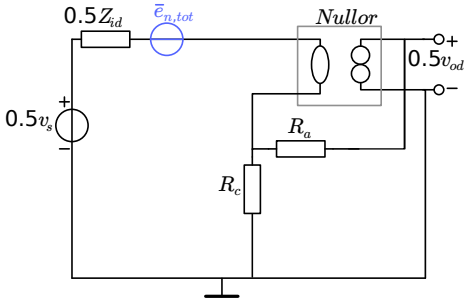
Including a dissipative feedback network into the signal path contributes to the SNR degradation, thus underscoring the importance of estimating its impact on the circuit performance. The inherent symmetry of the amplifier depicted in Fig. 5.12 enables the use of a half-circuit analysis for the sake of analytical conciseness. Fig. 5.13a illustrates the corresponding half-circuit configuration with the inclusion of the noise sources.

In Fig. 5.13a, $\overline{e}_{n,s}$ represents the noise voltage associated with the real part of half of the source impedance, $\overline{e}_{n,a}$ and $\overline{e}_{n,c}$ are the thermal noise from R_a and R_c, respectively, and $\overline{e}_n$ and $\overline{i}_n$ are the input-referred noise voltage and current of the nullor, respectively.

Fig 5.13b depicts the voltage amplifier when all noise sources are transformed and combined into one total equivalent input noise voltage source, $\overline{e}_{n,tot}$, in series with the signal source.



(a) Passive feedback voltage amplifier with noise sources included.



(b) Final result of the noise transformations to the amplifier's input port.

After such transformation, and assuming all noise sources are uncorrelated, it can be proven that the power spectral density (PSD) of the total equivalent input noise voltage source equals:

$$\overline{e_{n,tot}^2} = \overline{e_{n,s}^2} + \overline{e_n^2} + \overline{i_n^2}\left[Z_s + (R_a \parallel R_c)\right]^2 + (R_a \parallel R_c)^2\left(\overline{e_{n,a}^2}/R_a^2 + \overline{e_{n,c}^2}/R_c^2\right) \tag{5.8}$$

From the result of Eq. 5.8, one can conclude that the influence of the feedback network on the noise performance of the voltage amplifier is homologous to the parallel connection of R_a and R_c in series with the signal source.

Moreover, the third term in Eq. 5.8 suggests that a non-zero input-referred noise current of the nullor magnifies the total noise contribution substantially in case of large source impedances. For this reason, it is better to implement the nullor's first stage with Field-Effect Transistors (FETs) because they provide input currents of at least one order

of magnitude lower than their bipolar counterparts. In this project, a JFET was chosen for the input stage due to its lower 1/f noise corner than Metal–Oxide–Semiconductor Transistors (MOSTs), providing, thus, the lowest input-referred noise.

Fig. 5.14 is a general model representing the intrinsic contribution of all JFET's noise sources. In this model, $\overline{e}_{\mathrm{n,g}}$ represents the thermal noise contribution associated with the gate resistance R_{g}, $\overline{i}_{\mathrm{ig}}$ is the induced gate noise due to the capacitive coupling between the channel and the gate at frequencies around f_{T}, $\overline{i}_{\mathrm{g}}$ is the shot noise flowing from the reversed biased gate-channel, $\overline{i}_{\mathrm{df}}$ represents the 1/f noise flowing in the channel, and $\overline{i}_{\mathrm{d}}$ represents the thermal noise associated with the channel conductance.

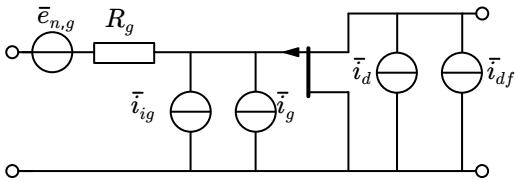


Figure 5.14: Noise model of a JFET.

The power spectral density of each noise source is given by:

$$\overline{i_{\mathrm{d}}^2} = 4kT\gamma g_{\mathrm{m}}\Delta f.^{7} \tag{5.9}$$

$$\overline{e_{\mathrm{n,g}}^2} = 4kTR_{\mathrm{g}}\Delta f, \tag{5.10}$$

$$\overline{i_{\mathrm{df}}^2} = 4kT\gamma g_{\mathrm{m}}\frac{f_{\mathrm{l}}}{f}\Delta f, \tag{5.11}$$

$$\overline{i_{\mathrm{ig}}^2} = 4kT\frac{(2\pi f)^2 C_{\mathrm{gs}}^2}{3g_{\mathrm{m}}}\Delta f, \tag{5.12}$$

$$\overline{i_{\mathrm{g}}^2} = 2qI_{\mathrm{g}}\Delta f, \tag{5.13}$$

In Eqs. 5.10–5.9, k is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, γ is a semi-empirical constant and equals 2/3 for long-channel devices in saturation, g_{m} is the transconductance, f_{l} is the corner frequency, I_{g} is the gate current, and C_{gs} is the gate-to-source capacitance.

When the noise sources $\overline{i}_{\mathrm{d}}$ and $\overline{i}_{\mathrm{df}}$ are referred to the JFET input using the two-port transform, the equivalent noise model of Fig. 5.15 is found.

The JFET chain parameters, B and D, in Fig. 5.15 are equal to:

$$B \approx -\frac{1}{g_{\mathrm{m}}}, \tag{5.14}$$

[7] This expression assumes a long-channel device operating in saturation. Otherwise, g_{m} reads g_{ds} with $V_{\mathrm{DS}} = 0$.

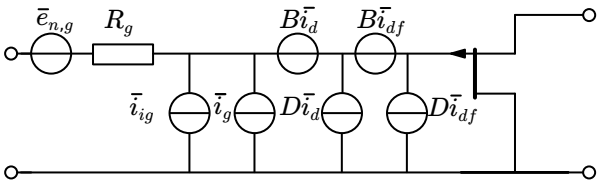


Figure 5.15: Noise model of a JFET with channel noise referred to its input.

$$D \approx -\frac{j2\pi f(C_{\mathrm{gs}}+C_{\mathrm{gd}})}{g_{\mathrm{m}}} = -j\frac{f}{f_{\mathrm{T}}}, \tag{5.15}$$

with C_{gd} the gate-to-drain capacitance and f_{T} the JFET's transit frequency.

If the PSD of the noise sources in Fig. 5.15 is substituted in Eq. 5.8, and assuming $\overline{e_{\mathrm{n,s}}^2} = 4kT\Re\mathrm{e}(Z_{\mathrm{s}})\Delta f$, the PSD of the total equivalent input noise voltage source can be expressed as:

$$\overline{e_{\mathrm{n,tot}}^2} = 4kT\left[\Re\mathrm{e}(Z_{\mathrm{s}})+R_{\mathrm{g}}+R_{\mathrm{a}} \parallel R_{\mathrm{c}}\right]+\left[\Re\mathrm{e}(Z_{\mathrm{s}})+R_{\mathrm{g}}+R_{\mathrm{a}} \parallel R_{\mathrm{c}}\right]^2\left[2qI_{\mathrm{g}}+4kT\frac{(2\pi f)^2C_{\mathrm{gs}}^2}{3g_{\mathrm{m}}}\right]+$$
$$+4kT\gamma g_{\mathrm{m}}\left\{\left[\Re\mathrm{e}(Z_{\mathrm{s}})+R_{\mathrm{g}}+R_{\mathrm{a}} \parallel R_{\mathrm{c}}\right]^2\left(\frac{f}{f_{\mathrm{T}}}\right)^2+\frac{1}{g_{\mathrm{m}}^2}\right\}\left(1+\frac{f_{\mathrm{l}}}{f}\right). \tag{5.16}$$

From the expression of Eq. 5.16, one may conclude that $\overline{e_{\mathrm{n,tot}}^2}$ can be minimized by:

- reducing the gate resistance, R_{g}, which can be achieved by increasing the JFET's area, WL;
- employing low resistances in the feedback, which costs power;
- nullifying the gate current, I_{g}, by forcing $V_{\mathrm{gs}} = 0$;
- increasing the transconductance, g_{m}, which usually goes at the expense of power, and;
- increasing the transit frequency, f_{T}.

The latter was optimized by Nanver, L. K. et al. [44] through the construction of JFETs with a lightly doped epi-channel in conjunction with separated top and bottom ring-gate structures. This gate separation allowed the reduction of the bulk and the sidewall parasitic capacitances while enabling the bottom-gate junction to be reversed biased for an optimum f_{T}. Additionally, the top-gate length was made sufficiently narrow, which is canonical for high-frequency operation.

Following the noise analysis, a second amplification stage was included in the nullor implementation to increase the loop gain and, thus, improve the transfer accuracy.

A NPN bipolar device with $2\,\mu m^2$ of emitter area was chosen for this task. As a result, the loop gain of the negative-feedback voltage amplifier is magnified by the NPN current gain, β, which typically lies around a value of 100. Fig. 5.16 shows the result of the implemented topology without inclusion of the biasing quantities.

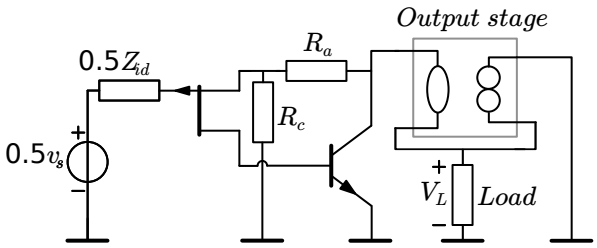


Figure 5.16: Implementation of the two-stage amplifier with a p-channel JFET as input and a NPN bipolar transistor as second stage. The biasing is not shown.

THE OUTPUT STAGE

After designing the previous pre-amplifiifcation stage for low-noise performance, one proceeds with the design of the output stage, which requires finding the desired quiescent point such that the signal does not experience harmonic distortion.

Using the microprobe station, a relatively low-frequency test signal can be applied for characterization purposes. In this scenario, the resistive component dominates the load impedance and approximately 1 MΩ. Thus, from specifications of Table 5.6, the output stage shall deliver a current to the load of 3.3 V/1 MΩ which equals 3.3 µA.

In the second load condition, the ADC's input capacitance is 10 pF. For a signal frequency of 10 kHz, the ADC's input impedance is 1.6 MΩ. Thus, the maximum output current to be delivered is approximately 2 µA. Therefore, the output stage shall deliver a maximum output current of 3.3 µA under an output voltage range of 3.3 V. An emitter follower circuit was used for the output stage (Fig. 5.17).

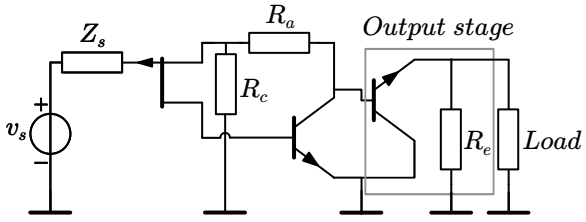


Figure 5.17: Emitter follower used for the output stage. The biasing is not shown.

BANDWIDTH

After completing the output stage design, the subsequent analysis ascertains whether the bandwidth requirement can be satisfied utilizing two stages.

The amplifier's maximum bandwidth capability can be assessed by estimating the Loop-gain-Poles product, or LP product for short, as described in Eq. 5.17:

$$\omega_{n_{max}} = \sqrt[n]{LP_n(s)} = \sqrt[n]{[1 - L(0)] \cdot \prod_{i=1}^{n} |p_{l,i}|}. \tag{5.17}$$

The terms L(0) and $p_{l,i}$ are the DC loop-gain and the (dominant) loop poles, respectively.

For estimation of the DC loop-gain and the loop poles, the small-signal circuit of Fig. 5.18 [8] was used.

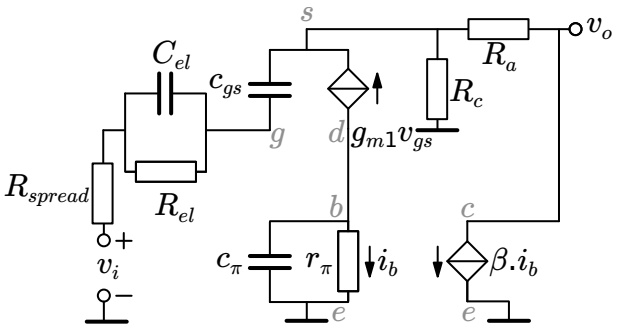


Figure 5.18: Small-signal circuit of the two-stage amplifier for computation of the loop gain.

The static small-signal analysis of the circuit in Fig. 5.18 finds a DC loop-gain of $\beta \cdot g_{m1}(r_c \parallel r_{m1})$, in which r_{m1} is the reciprocal of the JFET's transconductance, g_{m1}. Likewise, c_{gs} represents the small-signal source-to-gate capacitance, and $c_{\pi 2}$ and $r_{\pi 2}$ are the BJT's base-to-emitter small-signal capacitance and resistance, respectively.

Considering that the unilateral transfer of the controlled sources in Fig. 5.18 prevents charge exchange between c_{gs} and c_π, the number of poles can be estimated by the number of independent capacitor voltages. Since $C_{el} \gg c_{gs}$, its impedance is effectively seen as a short relative to c_{gs} and, thus, it is ignored from the loop poles calculation. Likewise, the DC port impedance seen from c_{gs} equals $R_c + r_{spread}$. Hence, an intuitive first-order approximation [9] for the loop poles can be found as:

$$\begin{aligned} p_{l,1} &= -\frac{1}{(r_c + r_{spread})c_{gs}} = -\frac{1}{40\,k\Omega \cdot 500\,fF} \approx -80 \times 10^6\ rad/s, \\ p_{l,2} &= -\frac{1}{r_\pi c_\pi} = -\frac{1}{21\,k\Omega \cdot 100\,fF} \approx -0.5 \times 10^9\ rad/s. \end{aligned} \tag{5.18}$$

The values of c_{gs}, r_π, and c_π in Eq. 5.18 were estimated with the available SPICE models (Appendix D). Calculation of the amplifier's maximum bandwidth yields:

[8] The small-signal output impedances, and the gate-to-drain and the base-to-collector capacitances were not considered in the circuit to simplify the analysis.

[9] In practice, the presence of feedback around the controlled sources may effectively add, move or remove the loop poles in a more elaborated manner.

$$\omega_{n_{max}} = \sqrt[2]{LP_2(s)} = \sqrt[2]{26 \cdot 80 \times 10^6 \,\mathrm{rad/s} \cdot 0.5 \times 10^9 \,\mathrm{rad/s}} \approx 1 \times 10^9 \,\mathrm{rad/s} = 160\,\mathrm{MHz} \tag{5.19}$$

Considering that the amplifier's relative frequency behaviour follows the Butterworth characteristic, the dominant poles are the largest set of poles for which holds:

$$\sum_{i=1}^{n} p_{l,i} \geqslant \sum_{i=1}^{n} p_{s,i} \tag{5.20}$$

in which $p_{s,i}$ is the system poles in Butterworth position. Accordingly,

$$p_{s,1} + p_{s,2} = -2 \cdot \frac{1}{2}\sqrt{2} \cdot 1 \times 10^9 \,\mathrm{rad/s} \approx -1.4 \times 10^9 \,\mathrm{rad/s}. \tag{5.21}$$

And the sum of the loop poles equals:

$$p_{l,1} + p_{l,2} \approx -0.58 \times 10^9 \,\mathrm{rad/s}. \tag{5.22}$$

Because $p_{l,1} + p_{l,2} > p_{s,1} + p_{s,2}$, both poles are dominant.

Since the amplifier's maximum bandwidth, which equals 160 MHz, is much larger than the signal's bandwidth, which equals 10 kHz, there is no need to design more than two stages for bandwidth purposes.

BIASING

With the amplifier's transfer defined by the small-signal behavior, the devices' input signal shall be translated to the correct operating point by adding bias sources. Biasing a nonlinear resistive device requires inserting voltage sources in series and current sources in parallel to the device's input and output port. Since the output port quantities are dependent on the input port quantities, two out of the four sources are selected by design to control the remaining two. Fig. 5.19 indicates how this biasing scheme was implemented for the balanced circuit.

In Fig. 5.19, the ideal source I_{ee} sets the tail current for biasing the NPN differential pair, whereas I_d defines the drain current I_{ds} that flows into the channel of the JFET's input pair. Consequently, satisfying KCL at nodes S and $S^{'}$ yields a current of $I_d + 0.5I_{ee}$.

Because the output voltages v_o^+ and v_o^- are undefined, a control loop was designed to establish them. It works as follows: the impedances R_c measure the output common-mode voltage which is subsequently compared to a reference V_{ref}. The difference is converted into a common-mode error signal that is amplified and fed into the nodes g and $g^{'}$; the gates of the JFET's input pair. If the absolute value of the common-mode loop gain is much larger than one (for DC), then the error signal is nullified and the complete amplifier is biased correctly.

Next, the ideal sources are converted into practical ones as shown in Fig. 5.20.

Due to the balanced configuration of the NPN differential pair, the DC voltage at the emitter's node is constant. Therefore, the resistor R_{ee} placed in series to that node sets the desired tail current I_{ee}. The current source I_d was replaced by a JFET of which its

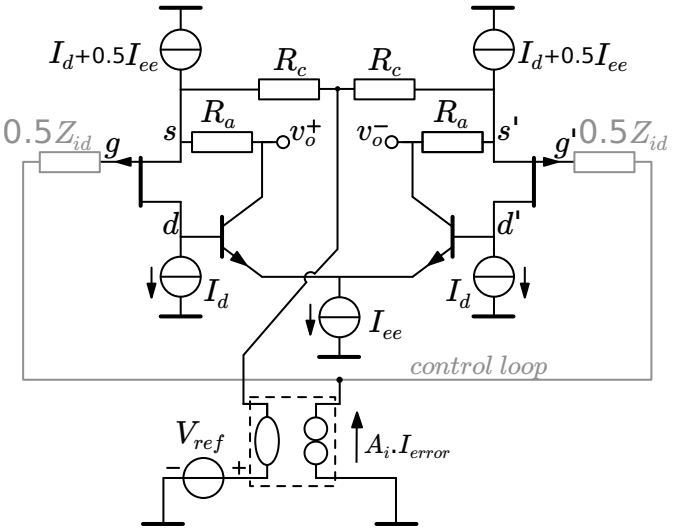


Figure 5.19: Biasing of the balanced circuit with ideal sources.

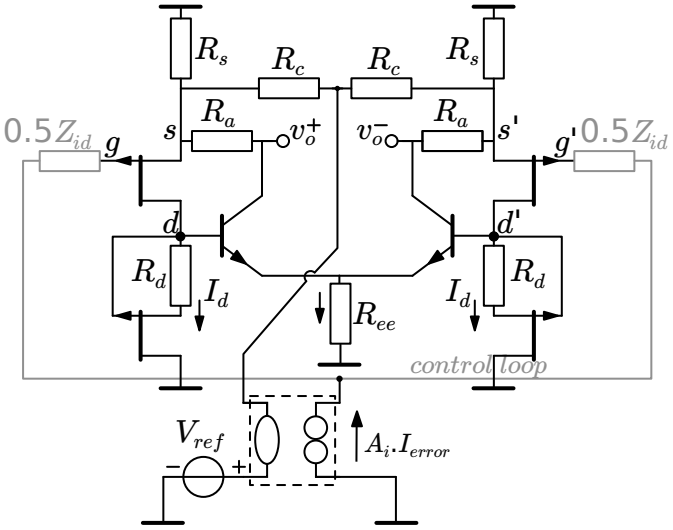


Figure 5.20: Practical biasing implementation for the differential-mode circuit. A nullor and an ideal voltage reference implement the common-mode feedback biasing scheme.

current is set by the voltage drop V_{GS} across the resistor R_d. Finally, the current source $I_d + 0.5I_{ee}$ has been implemented using a resistor R_s.

THE COMMON-MODE AMPLIFIER

The last remaining block refers to the implementation of the ideal transfer shown in Fig. 5.19 for the common-mode amplifier. Fig. 5.21 shows the circuit that fulfills such task.

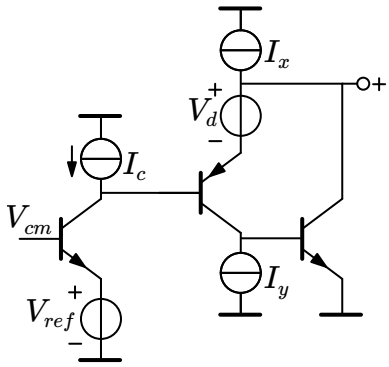


Figure 5.21: Common-mode amplifier biased with ideal sources.

In Fig. 5.21, the common-mode voltage, v_{cm}, is compared to a reference, V_{ref}, that was designed to be approximately half of the power supply for maximum signal excursion. A common-emitter stage amplifies the error signal, and a complementary-feedback emitter follower implements a current-gain stage for the CM amplifier. Thereby, the output of the CM amplifier uses the resulting amplified error signal to drive an electrode that connects the brain tissue[10] with the working electrodes attached to the JFET input pair. Fig. 5.22 details the practical biasing scheme.

In Fig. 5.22, a JFET with a resistor connected between the gate and source implements the current sources I_{c} and I_{x}. Even though this implementation suffers from a modest output impedance, it offers an optimal performance in terms of area usage.

A stack of four diode-connected NPN transistors realizes the voltage V_{ref}. Consequently, the reference voltage is inversely proportional to the absolute temperature, thus satisfying a hysteresis implementation concerning temperature variations in the circuit. The voltage V_{d} is a level shifter realized with a diode-connected PNP transistor.

5.7. VERIFICATION VIA SIMULATIONS

The complete fully-differential amplifier was simulated for verification purposes using the SPICE models available from the DIMES03 process.

AC SIMULATION

The complete circuit draws approximately 1 mA of DC current from a 6.5 V source. With the operating point of all devices set, the small-signal AC simulation (Fig. 5.23) reveals a gain of 21 dB at low frequencies, which is sufficient for the application.

[10] More precisely, the cerebrospinal fluid that surrounds the brain tissue.

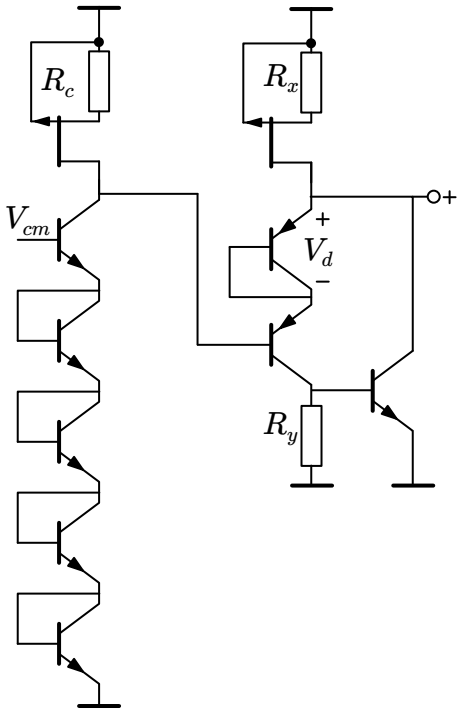


Figure 5.22: Practical biasing scheme of the common-mode amplifier replacing all ideal sources by practical ones.

One can notice from the result of Fig. 5.23 that the signal's bandwidth, which equals 10 kHz, is more than three orders of magnitude lower than the circuit's cut-off frequency, which equals 18.9 MHz. Hence, all frequency components from the source signal are preserved and no information is lost due to the roll-off of the amplifier's transfer. The simulation also reveals a unity-gain bandwidth of 142 MHz.

In a practical situation, the small-signal gain will be inevitably affected by process variations and device mismatches due to the finite resolution of lithography. Therefore, it is essential to ensure that the circuit has a DC loop gain much greater than one such that innacuracies from process variations are properly attenuated. Fig. 5.24 shows the result of the magnitude transfer as a function of frequency for the loop gain of the differential- and common-mode circuits.

The result of Fig. 5.24 reveals a DC loop gain of 28 dB and 30 dB for the differential- and common-mode circuits, respectively. Since both loop gains are much greater than one, the closed-loop transfer becomes less sensitive to process variations. Indeed, the sensitivity is the reciprocal of the loop gain, which means that deviations of the closed-loop transfer from its nominal value lie approximately within 4 % of tolerance.

A worst-case simulation analysis (Fig. 5.25) using the resistors' tolerance values of Table 5.9[11] provides more information on how much the process variations affect the

[11] For the transistors, variations in 10 % for the JFET's threshold voltage and the current gain of the bipolars

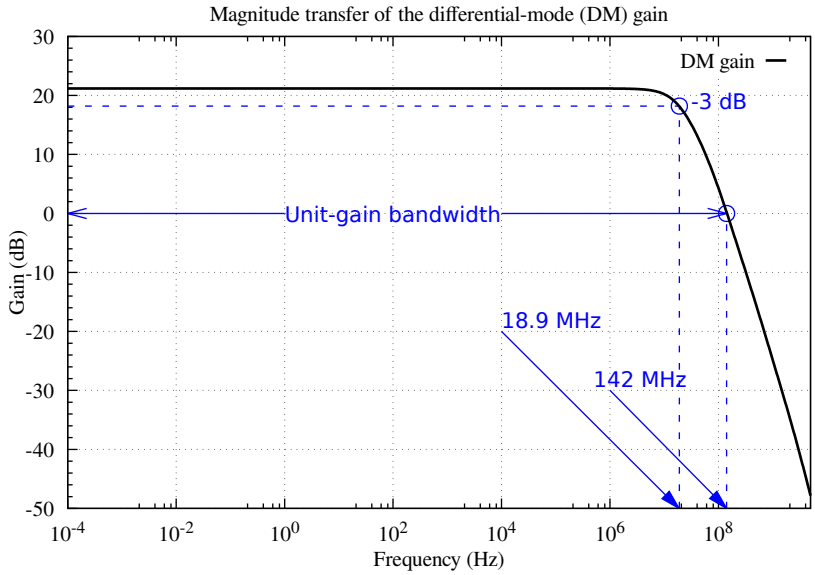


Figure 5.23: Result of the magnitude transfer as a function of frequency for the AC simulation illustrating how the small-signal differential gain rolls off at higher frequencies. Notice that the amplifier's bandwidth is much larger than the signal bandwidth.

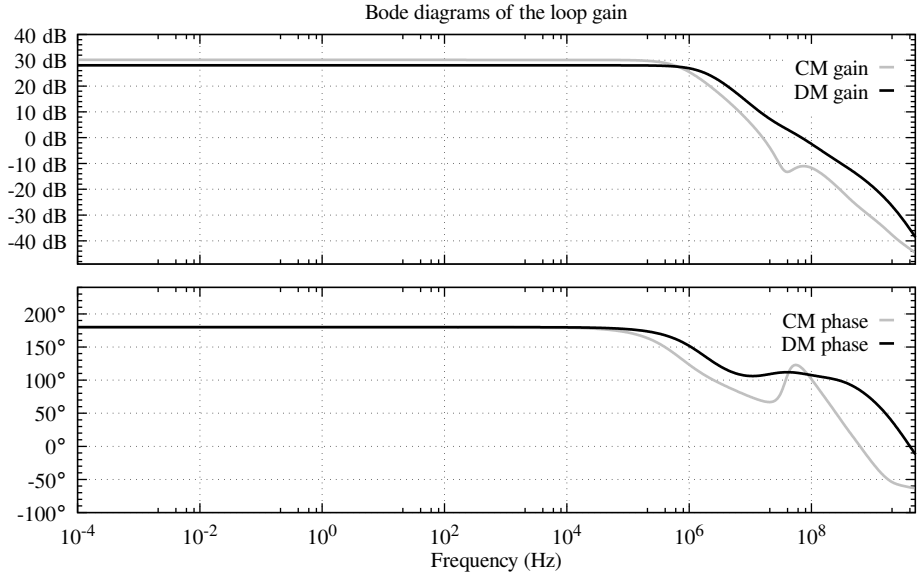


Figure 5.24: Bode diagrams illustrating how the differential- and common-mode loop gain of the negative-feedback amplifier rolls off at higher frequencies. The DC loop gain for the differential- and common-mode circuits are 28 dB and 30 dB, respectively.

were also taken into consideration for the referred analysis.

nominal value of the closed-loop gain.

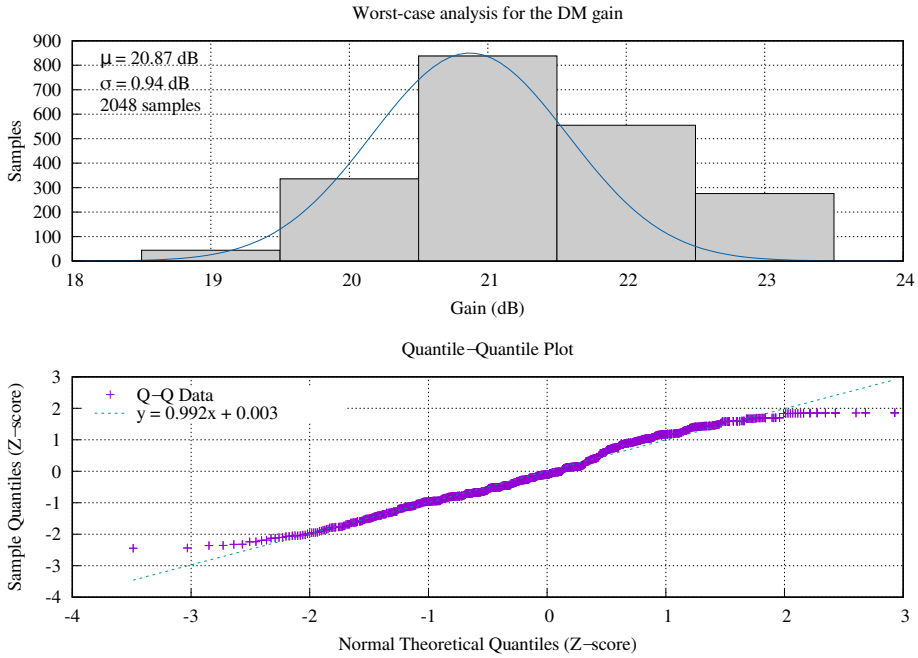


Figure 5.25: Top plot: sensitivity simulation for the small-signal differential gain. The simulation included a run of 2048 samples. The distribution follows a Gaussian curve with a mean value of 20.87 dB and standard deviation of 0.94 dB. Bottom plot: quantile–quantile (Q–Q) plot comparing the probability distribution of the worst-case analysis for the DM gain with its theoretical Gaussian distribution.

The results shown in the top plot of Fig. 5.25 indicate a mean value of 20.87 dB with a standard deviation of 0.84 dB which is in accordance with the previous sensitivity analysis. Therefore, the circuit is expected to be sufficiently robust against various sources of innacuracies. It is worth commenting that the mean and standard deviation values were computed after fitting the dataset to a theoretical Gaussian (Normal) distribution. The degree of goodness-of-fit between the dataset and its theoretical Gaussian distribution can be further examined with a quantile–quantile (Q–Q) plot.[12]

The bottom plot of Fig. 5.25 presents the Q–Q dataset, enabling a comparative evaluation of the goodness-of-fit between the probability distribution associated with the worst-case analysis for the DM gain and its corresponding theoretical Gaussian distribution. Typically, a Q–Q plot demonstrates a linear relationship between the sample and the theoretical quantiles when the data conforms to a Gaussian distribution.

[12] A Q–Q plot is a graphical tool used to examine the goodness-of-fit between two distributions. This visual representation facilitates a comparative assessment of the probability distribution, including evaluating properties such as location, scale, and skewness.

NOISE SIMULATION

Another performance to be verified is the RMS noise generated by the circuit. Fig. 5.26 shows the simulation results of the voltage and current amplitude spectral densities from 0.0001 Hz to 100 MHz for the input-referred noise. As expected, the voltage noise dominates at low frequencies and becomes flat at frequencies higher than the corner frequency, f_c. Simulations revealed a corner frequency about 400 Hz and a RMS integrated noise voltage of 1.2 µV over the signal's bandwidth, which is much lower than the weakest signal at the amplifier's input.

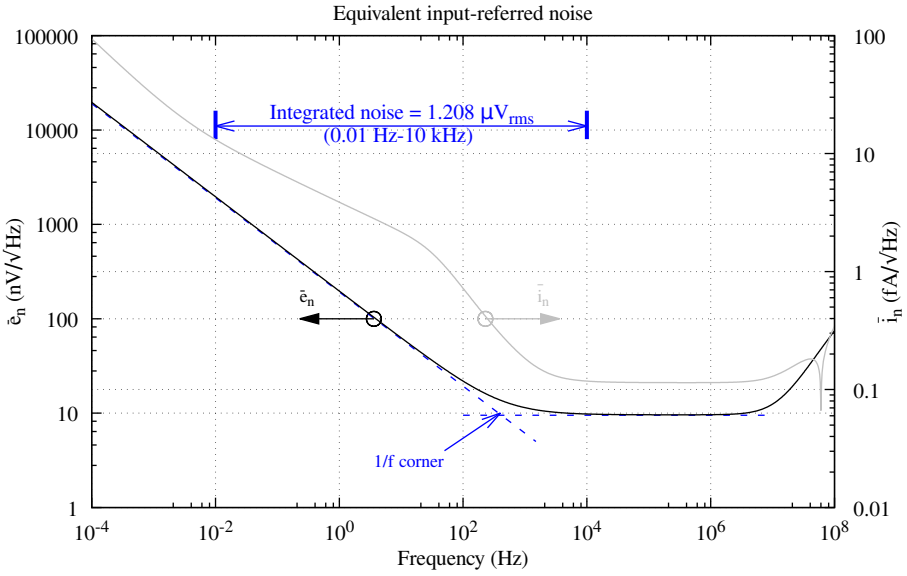


Figure 5.26: Simulation result for the equivalent input-referred voltage and current noise. The integrated noise across the signal's bandwidth is approximately 1.2 µV and the 1/f corner frequency is approximately 400 Hz.

THD SIMULATION

One of the benefits of a differential design is its symmetry. This symmetry ideally cancels any even-order harmonic terms at the amplifier's output port, which in turn contributes to a lower total harmonic distortion (THD). A Fourier analysis of the output signal reveals a THD less than 0.01 % for amplitudes ranging from 10 mV up to 100 mV. Fig. 5.27 shows a plot of the simulated THD values as a function of the amplitude of the input signal applied to the input port.

TRANSIENT SIMULATION

The circuit's output response in the time domain can be evaluated using transient simulations as shown in Fig. 5.28. The simulation setup used sinusoidal signals applied to

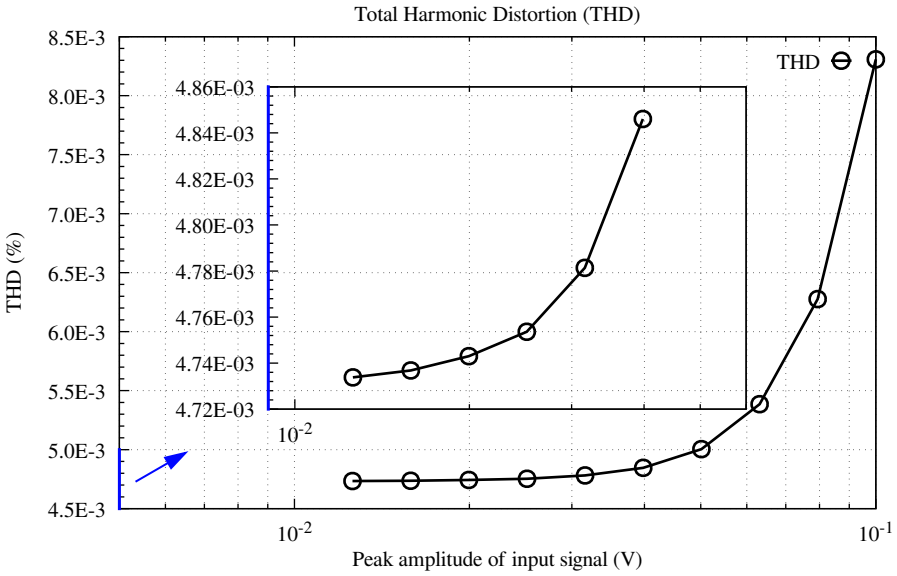


Figure 5.27: Total harmonic distortion simulation results for various excitation's amplitude. Notice that the THD is less than 0.01 % for all amplitudes applied. The subplot illustrates the initial six data points within the dataset, offering a zoomed glimpse of the total harmonic distortion into the observed range.

the amplifier's differential input superimposed on a common-mode interference so that it is possible to investigate the circuit's resilience to disturbances.

In Fig. 5.28, the common-mode interference is modeled as a train of pulses with very short duration and an amplitude of 10 mV, which is much larger than the sinusoidal input of 0.5 mV in amplitude. This train of pulses was used to mimic the photo-induced artifacts. As expected, the large common-mode loop gain provided by the negative-feedback amplifier substantially attenuates the common-mode interference at the source, and its traces can only be noticed when zoomed in.

One can notice from the zoomed image that the original 10 mV of amplitude interference is reduced to less than 20 µV at the source, an attenuation factor of more than five hundred. Most importantly, the DM output signal is spurious-free which indicates the amplifier has completely removed the common-mode interference due to its differential nature.

The next step was to replace the sinusoidal signals with raw intra-cortical signals taken from a public database used for collaborative research in computational neuroscience [13]. Using more enriched and realistic signals in the transient simulation provides a more accurate prediction of the final circuit behavior. One can notice from Fig. 5.29, that the output signal is an amplified copy of the source. Therefore, the circuit works as expected.

[13] Available in crcns.org

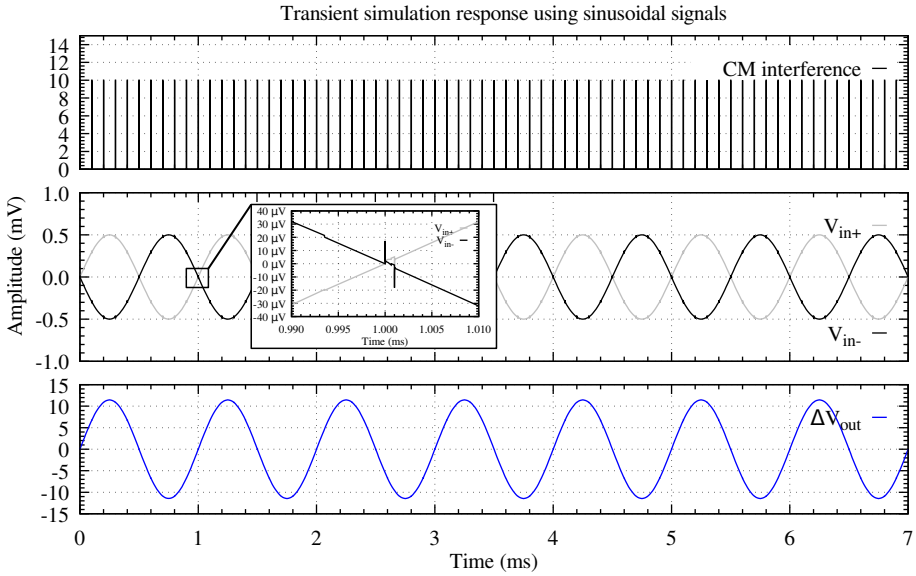


Figure 5.28: Transient simulation result showing the circuit's time-domain response. The first plot refers to a train of short pulses with 10 mV in amplitude as the common-mode interference signal applied to the amplifier's input. The pulses are 1 µs long with 1 ns of rise and fall times, and repetition rate of ten pulses per millisecond. The second plot shows the sinusoidal signals applied at the amplifier's input port, and a zoomed in version detailing the attenuation of the common-mode interference. The third plot shows the output signal, amplified, and without traces of interference.

STABILITY AND THE STEP RESPONSE

As any feedback system has the potential for instability, the design of negative-feedback circuits must follow stability rules to ensure that every bounded input produces a bounded output. A system is unstable if, in a closed-loop control with sinusoidal excitation, the feedback signal from the controlled variable is in phase and equal or greater in magnitude than the reference input at any frequency.

The circuit so far designed has two main closed-loops that have the potential to cause system instability: the differential-mode and the common-mode feedback loops. Therefore, both loops must yield a bounded output when excited by any bounded input.

Formally, the step response of a dynamical system gives information on the stability and on its ability to reach a stationary state. Fig. 5.30 shows the differential-mode output signal when a voltage step is applied to the differential-mode input port.

The circuit's step response to this test yields a bounded signal with settling times of 70.3 ns and 40 ns for the rising and falling edges, respectively. For the common-mode control loop, the step response was verified by injecting a voltage step into the common-mode input port or a current pulse into the common-mode output node. No oscillations in both tests were observed, which indicates that the system is stable.

In practice, however, the circuit's step response is insufficient to guarantee the feedback system's robustness. Moreover, it does not provide information to which degree the

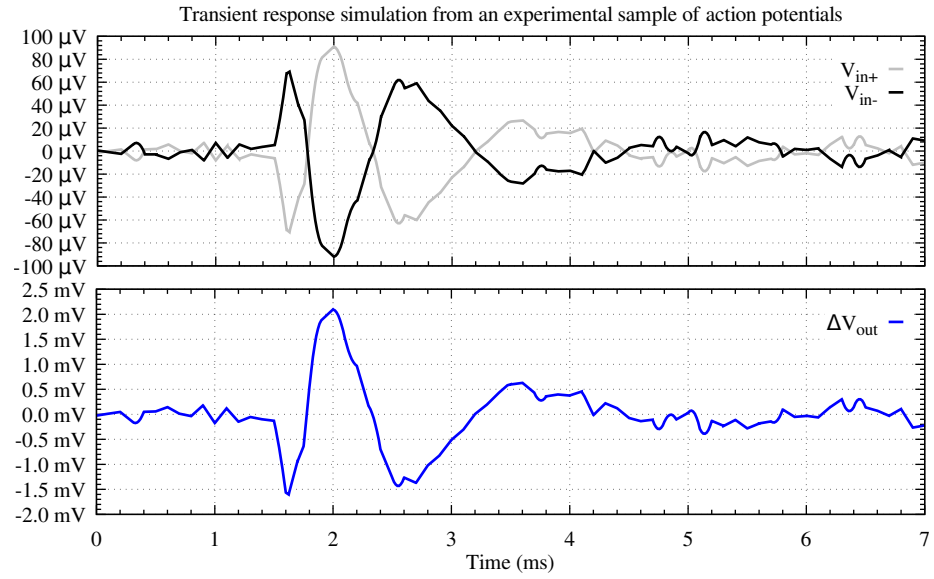


Figure 5.29: Transient simulation result using intra-cortical signals recorded from the thalamus using a multi-electrode array. The raw data was extracted from crcns.org.

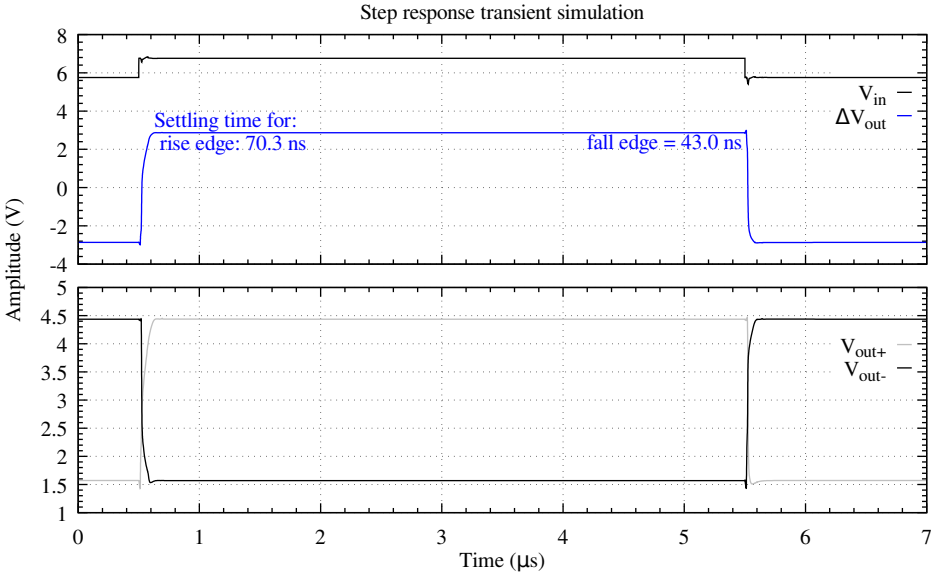


Figure 5.30: Step response of the circuit for the differential-mode path. Both rise and fall edges were applied and no ringings nor oscillations were observed around the loop. The ability of the circuit to reach steady state can be verified by the time the output stays within 1 % of its final value.

system is stable. The degree of stability can be better evaluated by inspecting the phase and gain margins of the loop gain [14]. In general, the gain and phase margins must be large enough to accomodate all anticipated variations in the magnitude and phase of the loop gain. Typically, phase margin values between 30°–70° and gain margins values between 2 dB–5 dB are satisfactory to ensure stability. The phase and gain margin results for the differential-mode and common-mode loop gain are summarized in Table 5.10.

Table 5.10: Stability simulation summary for the differential-mode and the common-mode open-loop gains. The phase and gain margins were computed after breaking the loop into the path between the differential-mode ports, to simulate the differential-mode loop gain, and between the common-mode ports, to simulate the loop gain of the common-mode regulation. The phase and gain margins indicate that both loops have enough headroom for variations in the magnitude and phase of the loop gain.

	Stability summary			
	Phase margin	**Freq.**	**Gain margin**	**Freq.**
DM	110°	68.91 MHz	35.5 dB	4.079 GHz
CM	68.63°	16.44 MHz	26.89 dB	613 MHz

The results indicate that the circuit's loop gain has enough headroom for phase and gain changes before instability.

Generally, an inspection of the circuit's step response and the loop gain offers complementary information on the system's stability. Often, such tests are sufficient to guarantee that signals do not oscillate around the feedback loops.

COMMON-MODE GAIN, COMMON-MODE REJECTION RATIO (CMRR), AND POWER-SUPPY REJECTION RATIO (PSRR)

The common-mode gain of an ideal fully differential amplifier is zero and, consequently, the common-mode rejection ratio (CMRR) is infinite. In practice, device mismatches introduce errors that contributes to deviations from such values. Fig. 5.31 shows a Monte Carlo histogram for the common-mode gain at frequencies below 100 Hz when device mismatches following a Gaussian distribution with 10 % of tolerance and $\pm 3\sigma$ are introduced.

The histogram of Fig. 5.31 reveals a mean value of -48.5 dB for the common-mode gain with 9.93 dB of standard deviation. Notice, however, that this Monte Carlo simulation does not include the correlation of random variables; thus, it leads to a more pessimistic result [15]. This bias can be noticed from the accentuated left skewness of the histogram, which indicates that the outliers have a tendency to fall in the direction of a more negative common-mode gain.

When a correlated worst-case simulation is run in lieu of the Monte Carlo analysis described above, a different result (Fig. 5.32) is found. The new histogram now reveals a

[14] The phase margin is the negative phase perturbation that makes the system marginally stable. Its value is the difference between the loop gain phase and -180°, when the magnitude of the loop gain is at zero dB. The gain margin is the gain perturbation that makes the system marginally stable. Its value is the difference between zero dB and the gain at the phase cross-over frequency that gives a phase of -180°.

[15] Owing to the symmetry of the amplifier, devices mirrored from the axis of symmetry in the layout faces the same process variation gradient; thus, their values are correlated.

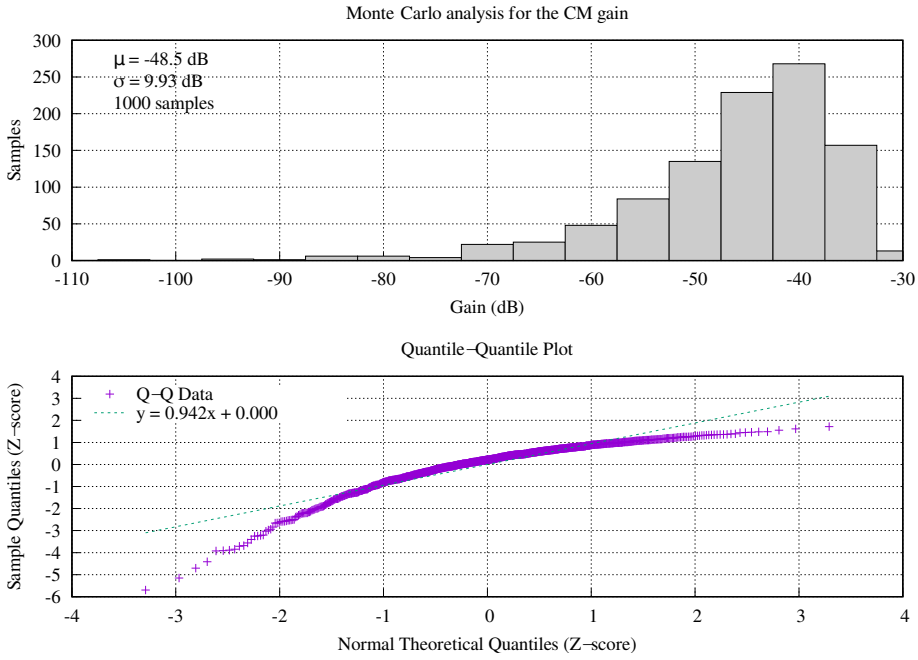


Figure 5.31: Top plot: Monte Carlo simulation for the small-signal common-mode gain. The simulation included a run of 1000 samples in which the tolerance value used for the components were based from Table 5.9. The distribution suggests a tendency to follow a Gaussian curve with a mean value of −48.5 dB and standard deviation of 9.93 dB. The left skewness indicates a bias produced by the uncorrelated random variables used in the Gaussian distribution, and it yields a more pessimistic estimation for the common-mode gain. Bottom plot: Q–Q plot comparing the probability distribution of Monte Carlo simulation for the small-signal CM gain with its theoretical Gaussian distribution. Notice that the distinctive concave curvature observed in the Q–Q plot provides supporting evidence for the presence of left-skewed data.

mean value of −265.8 dB for the common-mode gain with 3.17 dB of standard deviation, suggesting a more optimistic value when correlated variables are taken into account. However, since the worst-case model includes the same extreme values for each correlated component, there is less "randomness" in this analysis, which biases the results in direction of the ideal case. Nevertheless, both analyses provide an useful insight in what to expect from the experimental context.

Simulations of the power-suppy rejection ratio (PSRR) [16] were also performed and the results reveal 141 dB of suppression in the power supply variations to the output. Otherwise stated, with a differential gain of 21 dB, 1 V variation in the power supply would result in only 8 nV at the amplifier's input port; which is negligible when compared to the weakest signal of 50 μV.

[16] The PSRR definition used is: $PSRR = (dV_{dd}/dV_{out}) \times (V_{out}/V_{dd})$

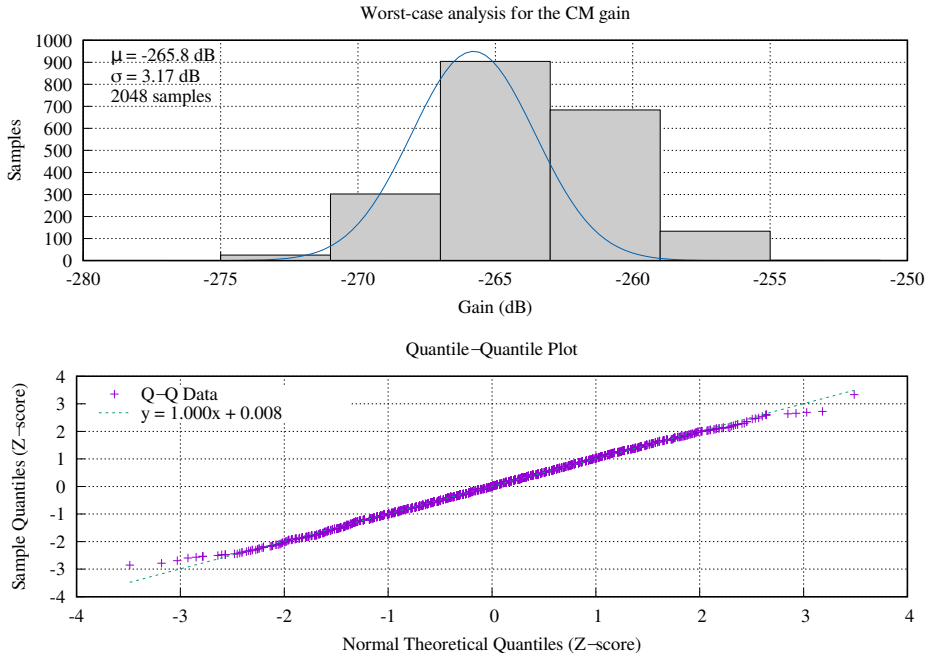


Figure 5.32: Top plot: sensitivity simulation for the small-signal common-mode gain. The simulation included a run of 2048 samples in which the tolerance value used for the components were based from Table 5.9. The distribution follows a Gaussian curve with a mean value of −165.8 dB and standard deviation of 3.17 dB. Bottom plot: Q–Q plot comparing the probability distribution of the worst-case analysis for the CM gain with its theoretical Gaussian distribution.

5.8. ERROR BUDGETS

The previous section analyzed and simulated the performance of various metrics when some mismatches were introduced on the nominal components of the amplifier. Other sources of errors might be introduced when mismatches occur in the source impedances, such as the electrode offset and the common-mode to differential-mode conversion.

OFFSET

The source offset, due to mismatches in the electrodes and the tissue surrounding the electrodes, plus the amplifier's input offset, due to component mismatch, shall not shift the amplifier's operating point out of its linear range. Otherwise, clipping distortion may occur.

The solution used to solve this problem involved the incorporation of the source offset as a DC component of the input signal during the amplifier design phase. Hence, the ADC's full-scale range divided by the amplitude range of the input signal limits the maximum amplifier's gain before saturation. Considering a maximum electrode offset

of 100 mV, and the largest input signal of 30 mV, the maximum possible AFE gain is:

$$A_{\mathrm{dm}_{\mathrm{max}}} = \frac{\mathrm{FS}}{V_{\mathrm{in}}} = \frac{3.3\,\mathrm{V}}{130\,\mathrm{mV}} \approx 25. \tag{5.23}$$

Fig. 5.33 shows the simulation results from the amplifier's linear operating region, which is 400 mV. Therefore, it is expected that the AFE has enough voltage headroom for its linear operation.

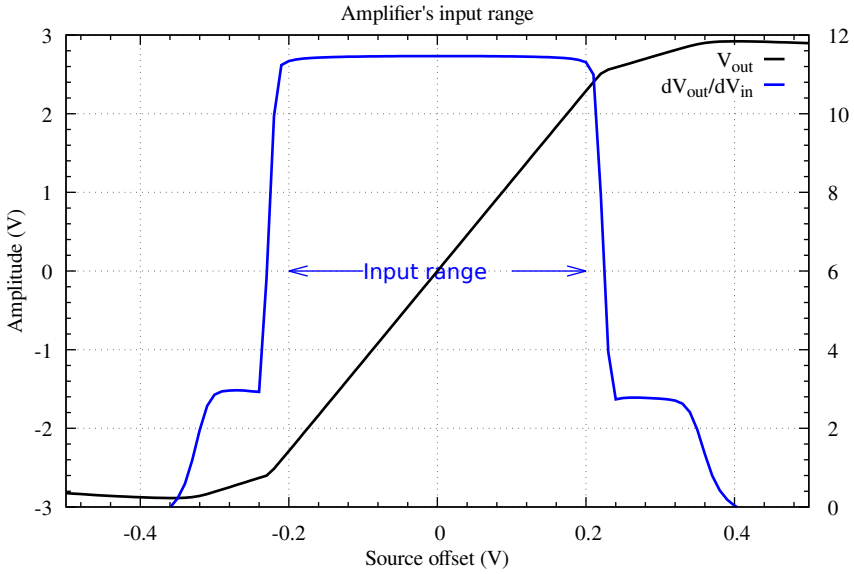


Figure 5.33: Simulation result of the amplifier's linear range. The simulation test involved modeling the electrode offset with a DC voltage source in series with the amplifier's input port and sweeping its value from −0.5 V to 0.5 V. The output, and its derivative, reveals the range in which the amplifier is operating in its linear range.

Besides the electrode offset, there is also the amplifier's offset which can be divided into systematic and random. The systematic offset is zero due to the topological symmetry of the amplifier. The random offset stems from component mismatch and it can be estimated with a Monte Carlo run. Fig. 5.34 shows the Monte Carlo histogram of the amplifier's random offset. The result reveals a mean offset of 278.79 µV with 13.72 mV of standard deviation, which is much smaller than the estimated electrode's offset. All things considered, the electrode and amplifier's offset are expected to not interfere in the linear operation of the amplifier.

5.8.1. COMMON-MODE TO DIFFERENTIAL-MODE CONVERSION

Another source of error created by unbalances in the electrode impedance is the so-called common-mode to differential-mode conversion.

This error occurs because the mismatch in the impedance of the electrodes generates two unequal partitions of the common-mode voltage at the amplifier's input port.

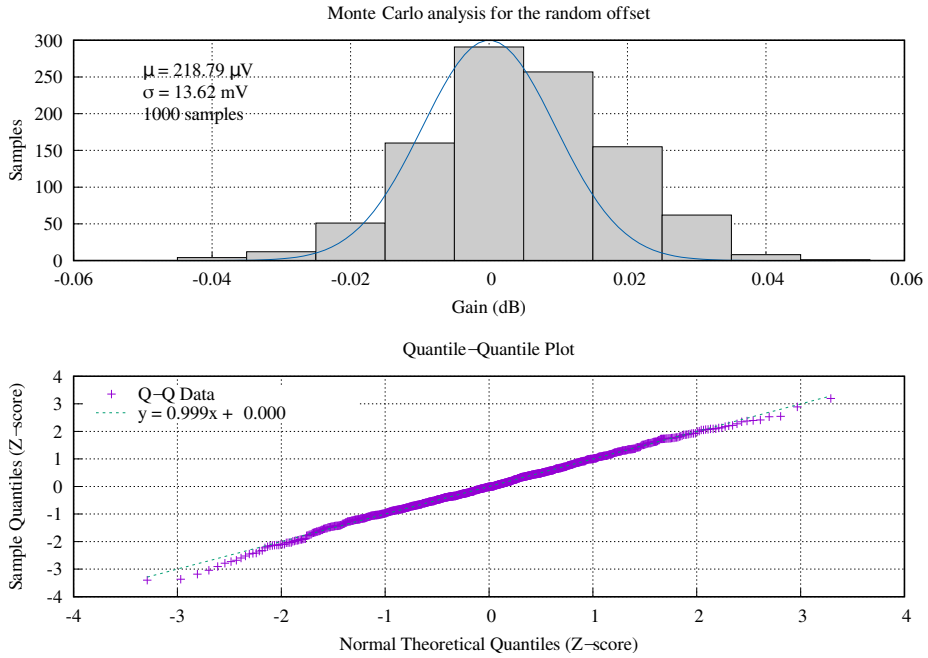


Figure 5.34: Top plot: Monte Carlo run, using 1000 samples, for estimation of the AFE's random offset. The result reveals a mean offset of 278.79 μV with 13.72 mV of standard deviation. Bottom plot: Q–Q plot comparing the probability distribution of the Monte Carlo analysis for the random offset with its theoretical Gaussian distribution.

The unequal partitions are undistinguished from a differential signal, thus, introducing a source of error in the amplifier.

Once the common-mode to differential-mode conversion happens, nothing is left to fix it. Therefore, mitigating this error typically involves minimizing the electrode mismatch [17] and attenuating sources of common-mode interference during the experimentation [18].

5.9. LAYOUT CONSIDERATIONS

The shape and placement of every polygon in the layout require a thorough understanding of device-physics principles, semiconductor fabrication, and circuit theory. For this reason, it is essential to understand how to minimize undesirable effects that may degrade the overall performance of the integrated circuit during semiconductor processing.

[17] Through a proper electrode layout and employing high-quality films.

[18] For instance, employing a Faraday shield during the experimentation, powering the circuit with batteries and a high power-supply rejection ratio (PSRR) low-dropout regulator, filtering, etc.

SYMMETRY AND COMMON-MODE CENTROID

Preserving the full circuit symmetry in the layout is a sine qua non of optimal common-mode rejection performance. Likewise, common-centroid layouts make the circuit more resilient to process variations; hence, there is less component mismatch.

On the other hand, given the extra complexity in routing and area usage added by common-centroid layouts, the use of this technique was limited to devices more prone to suffer from process variations. Fig. 5.35 shows the result of the circuit layout for the differential-gain stage configured for a tetrode measurement. In this particular layout,

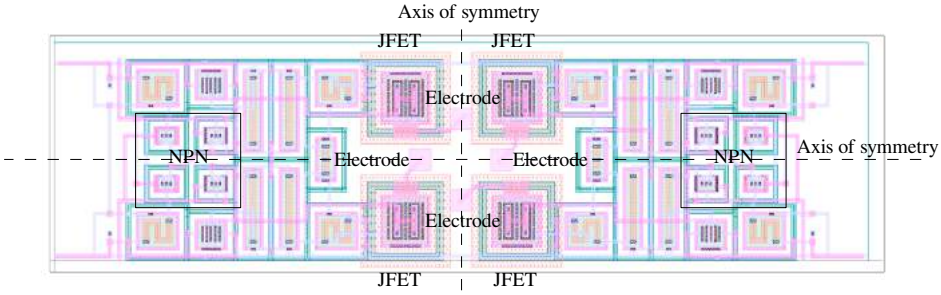


Figure 5.35: Layout result of the differential-mode stage highlighting the full symmetry around the X-axis and Y-axis, and the common-centroid technique used for the NPN differential pair.

the full circuit symmetry was preserved around both the X-axis and the Y-axis, and a common-centroid layout was used for the NPN differential pair. The common-mode centroid was not applied to the JFET-input pair because it would increase the area usage and routing complexity to a degree at which the circuit symmetry would be compromised.

THERMAL EFFECTS, PHOTO-INDUCED ARTIFACTS AND COMMON-MODE INTERFERENCE

Power dissipation from the µLEDs may cause thermal gradients across the silicon that impacts the AFE performance. Additionally, the µLEDs are sources of photo-induced artifacts and common-mode interference from the power lines.

The main layout measure used to mitigate such effects was the placement of diametrically opposed differential-mode stages around the µLED, such that each unit is placed on the same isothermal line. If the thermal gradients and photo-induced artifacts affect both AFEs equally, the result would be the cancellation of this common-mode signal by the differential nature of the circuit.

COMMON-MODE FEEDBACK CONTROL: LOCAL OR GLOBAL?

The implementation of the common-mode feedback during the layout phase posed a question on how many control loops there shall be if multiple differential-mode units are consired.

Imagine, for instance, there are six differential-mode units equally spaced along the shaft. If one control loop is used for each unit, how does the common-mode control of one unit affect the others? Will there be a common-mode biasing conflict? And what happens if there is only one global common-mode control for all units? Will the electrical conductivity of the cerebrospinal fluid (CSF) and surrounding tissues ensure that all units find their correct common-mode biasing? Or will the bias of some units be floating?

These questions urged the implementation of designs with different common-mode configurations such that more studies can be conducted to answer such inquiries.

DIFFERENT DESIGNS FOR MULTIPLE STUDIES

Fig. 5.36 shows an example of two versions implemented to investigate the action of the common-mode control loops. The first version uses two common-mode control loops diametrically opposed to each other around the Y-axis of symmetry. The ground electrode of each control unit extends until the center of the shaft surrounding the left and right differential-mode units similarly to a guard-ring structure.

This version aims to understand whether there will be a common-mode conflict between the two diametrically opposed control loops and whether the differential-mode units at the center will be correctly biased.

The second version uses a global common-mode control loop. There is only one ground electrode that extends until the probe tip and surrounds all differential-mode units across the entire shaft. This version will clarify whether a global common-mode control loop is sufficient to bias all units and whether there will be a floating bias across some units.

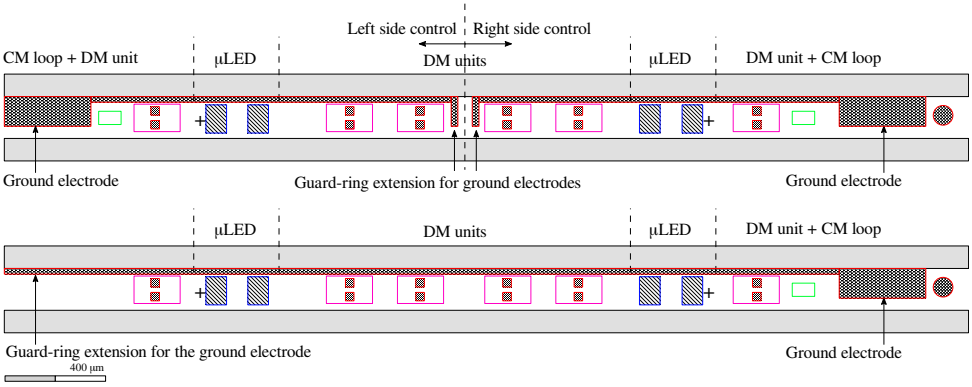


Figure 5.36: Different versions for the common-mode control loop. In the first version (top figure), two common-mode control loops diametrically opposed form the common-mode biasing of differential-mode units. This version aims to understand common-mode biasing conflicts among different units. In the second version (bottom figure), there is a global common-mode control loop covering all differential-mode units. This version will help understanding whether one global loop is sufficient to bias all units.

In addition to the designs aimed at studying the impact of the common-mode control loop, other designs were developed to meet the experimental requirements of our

collaborators. The particularities of each design include electrode pairs with different sizes and spacings, electrodes configured in a tetrode setup, different numbers and locations of μLEDs, different numbers of shafts per probe, different shaft lengths, among others (Appendix C).

5.9.1. WAFER LEVEL CONSIDERATIONS

Since there are multiple designs on the wafer, it is essential to ascertain that the silicon substrate will not collapse with the use of deep reactive ion etching (DRIE) meant to detach the optrodes.

Measures used to prevent such failure included providing enough sideroom spacing between adjacent designs and a clamping mechanism devised to keep the optrode safely attached to the wafer after the DRIE.

Moreover, because thin membranes are formed, it is crucial to minimize any processes that can potentially damage the wafer such as vaccuum chucking mechanisms or baths that can increase the tension or the upthrust on the thin membranes.

The next subsection elaborates on the main measures used during the functional decomposition to segregate the multidimensional difficulties associated with the IC-MEMS monolithic fabrication.

5.9.2. FUNCTIONAL DECOMPOSITION

The typical thickness of a 100-millimeter silicon wafer is 525 μm, which is not ideal for the application because the required optrode's thickness is 100 μm. Silicon wafers with a thickness of 100 μm require the use of a wafer carrier to prevent the wafer bowing beyond its limits during handling, transportation and thin-film deposition. A more convenient option is to use silicon-on-insulator wafers (SOI).

A commercially available p-type SOI wafer with 100 μm of device layer, 350 μm of handling layer, and 2 μm of buried oxide (BOX) was found and selected for this process. Alas, such SOI wafers contain an electrical resistivity between 0.01–0.02 $\Omega \cdot$ cm, which is much lower than the range of 2–5 $\Omega \cdot$ cm required to process the original BIFET microfabrication protocol, i.e., the DIMES03. Therefore, an additional epitaxy growth must be devised to tune the dopant concentration on the device layer to the required level.

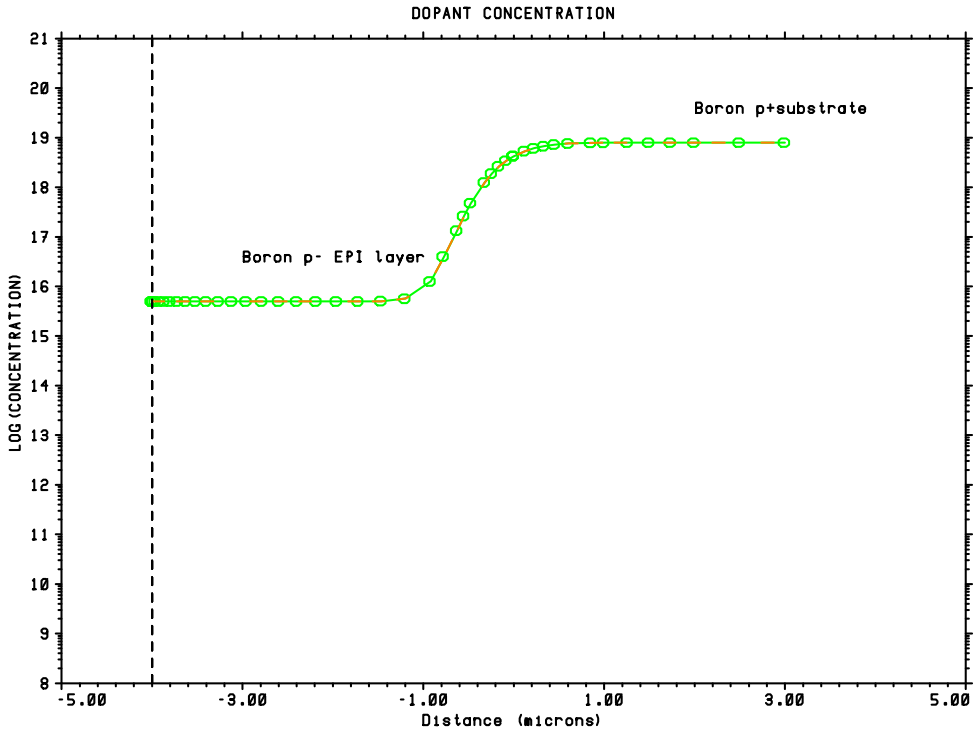


Figure 5.37: TSUPREM-4 simulation used to estimate the thickness of the epitaxial film required to change the dopant concentration of the device layer to approximately 5E15 atoms/cm^3. The x-axis refers to the thickness with the surface of the SOI wafer positioned at the zero coordinate. The vertical dashed line represents the surface boundary of the epitaxial film.

Simulations using the Taurus TSUPREM-4 (Fig. 5.37) reveal that a 4 µm-thickness of an epitaxial film is sufficient to change the boron dopant concentration accordingly while ensuring that there is enough penetration depth for the Arsenic implantation that defines the buried layer. Next, another epitaxial film is grown to change the Arsenic dopant concentration to 1E16 atoms/cm^3, which is the concentration required to construct the devices as per the DIMES03 protocol.

Fig. 5.37 shows the results from the TSUPREM-4 simulation used to estimate the epitaxial film thickness to be grown on the SOI wafers. The y-axis refers to the dopant concentration (atoms/cm^3) in log-scale; the x-axis, to the device thickness in which the surface of the SOI substrate is set as the reference and is positioned at the zero coordinate. The epitaxial film grows along the negative x-axis direction and the simulations reveal that it takes almost 2 µm of silicon before the dopant concentration depletes and stabilizes it to appoximately 5E15 atoms/cm^3.

Fig. 5.38 shows the dopant concentration profile and the penetration depth of the Arsenic implantation after the drive-in[19]. Notice that the buried layer regions remains

[19]The dopants segregate and diffuse on the silicon after the thermal annealing. It is essential to ascertain that the diffusion of dopants does not reach the surface of the SOI wafer.

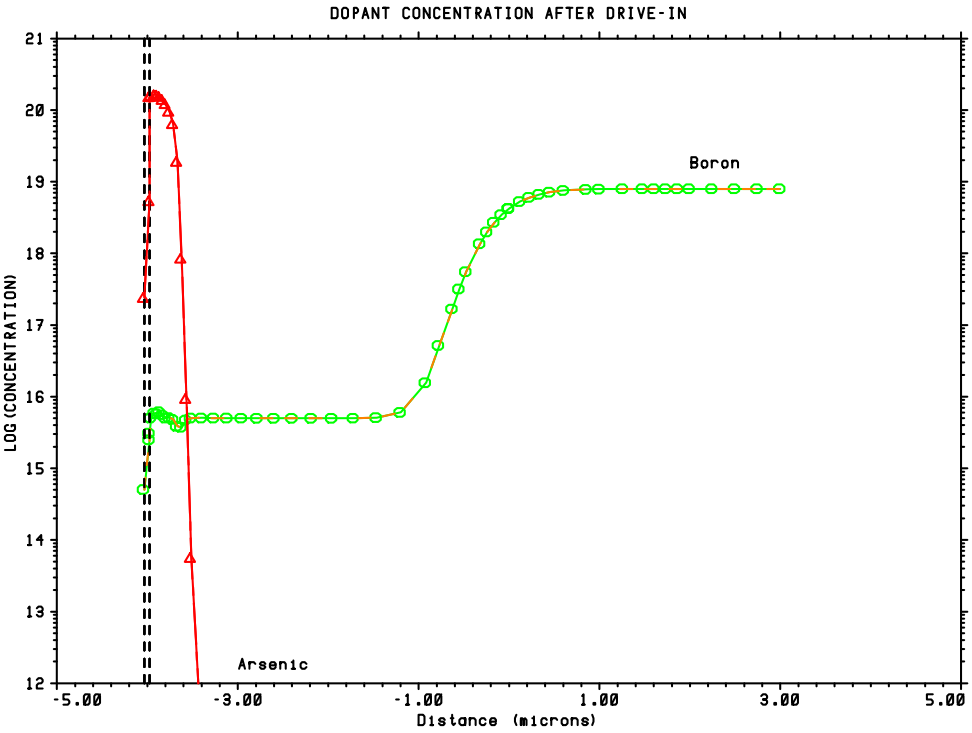


Figure 5.38: TSUPREM-4 simulation result used to estimate the As^+ dopant concentration and the penetration depth of dopants after drive-in. Notice the depletion in the As^+ concentration and the enough depth headroom from the surface of the SOI substrate.

inside the epitaxial film and that there is enough depth headroom from the surface of the SOI wafer.

Lastly, it is essential to ascertain that the dopant concentration remains under specification when another epitaxial film grows after the Arsenic drive-in. Fig. 5.39 reveals the dopant concentration profile when a 1 µm of epitaxial film grows to tune the dopant concentration to 1E16 atoms/cm^3. Notice that the Arsenic also diffuses inside the epitaxial film in the positive x-axis direction. The depth headroom provided avoids the dopants to reach the surface of the SOI substrate.

5.9.3. FABRICATION

The process starts with a p-type, boron-doped SOI wafer with <100> of crystallographic orientation, 100 µm of device layer, 350 µm of handling layer, 2 µm of buried silicon dioxide (SiO_2), frontside polished, 2 µm of SiO_2 on the back, and an electrical resistivity between 0.01 and 0.02 $\Omega \cdot$ cm (Fig. 5.40).

A p-type epitaxial film of silicon with a thickness of 4.5 µm[20] is grown on the

[20] An extra 0.5 µm of headroom thickness accounted for the silicon consumed during the oxidation used to

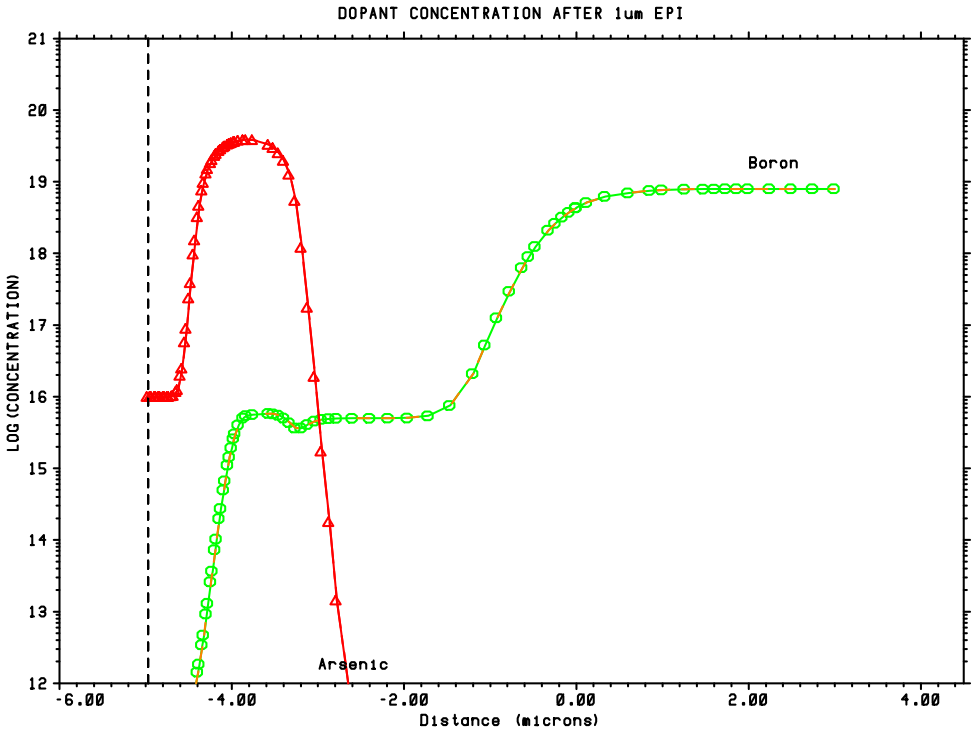


Figure 5.39: TSUPREM-4 simulation result used to verify the dopant concentration when an epitaxial film of 1 µm grows after the Arsenic drive-in. The dopant concentration at the surface of the epitaxial film is 1E16 atoms/cm^3, which is the required level to process the devices from the DIMES-03 protocol.

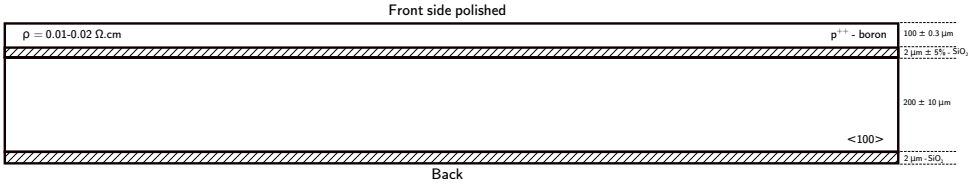


Figure 5.40: The substrate is a p-type, boron-doped SOI wafer with <100> of crystallographic orientation, 100 µm of device layer, 350 µm of handling layer, 2 µm of buried silicon dioxide (SiO_2), frontside polished, 2 µm of SiO_2 on the back, and electrical resistivity between 0.01–0.02 Ω · cm

polished frontside to tune the boron dopant concentration at the device surface to 5E15 atoms/cm^3 (Fig. 5.41).

After defining the fiducial markers through thermal oxidation, the buried n^+ (BN) regions are defined with a lithographic step through a BN mask. The purpose of the BN regions is to create a low-ohmic path between the contacts and the active regions of the NPNs and PNPs, plus create the bottom gate for the p-channel JFETs.

The patterned regions are etched with Buffered Hydrofluoric Acid (BHF) and a 200 Å

define the fiducial markers.

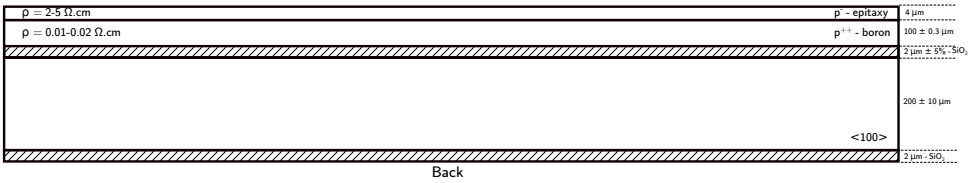


Figure 5.41: A 4.5 µm layer of an epitaxial film grows on the silicon to adjust the dopant concentration at the device surface.

of thermal oxide is grown to collect co-implanted particles during the Arsenic (As^+) implantation (i.e., a screen oxide). The implantation dose is 5E15 ions/cm^2 at 180 keV of energy (Fig. 5.42).

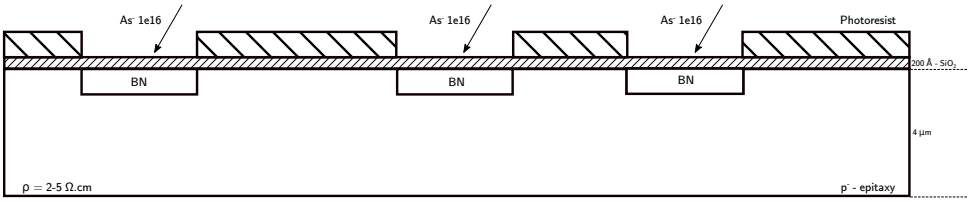


Figure 5.42: The buried n^+ regions provide a low-ohmic collector contact for the NPN devices, a bottom gate for the p-channel JFET, and a low-ohmic base contact for the PNP devices.

Next, a Hydrofluoric Acid (HF) bath removes the screen oxide and the wafers follow a thermal annealing for dopant activation. A 650 Å of SiO_2 grows during the thermal annealing, which is subsequently removed with a BHF for the second epitaxy growth.

The epitaxy uses 300 Å of intrinsic silicon plus 700 Å of As^+ with a dose of 1E16 atoms/cm^2 at 1050 °C. Then, a wet oxidation step grows 300 Å of SiO_2 and a thin photoresist film is patterned with a DP mask to create deep plugs (DP) used for the p^+ isolation. The implantation uses boron, with a dose of 5E15 ions/cm^2 at 180 keV of energy (Fig. 5.43).

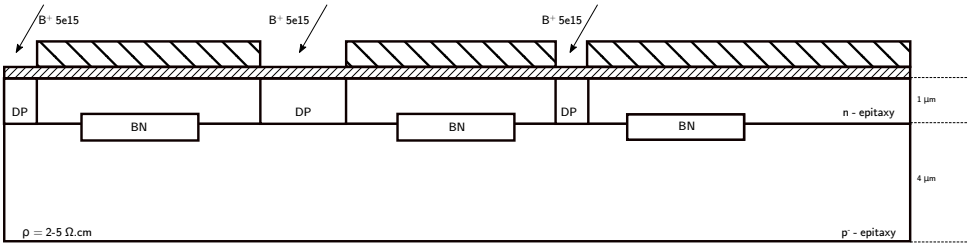


Figure 5.43: The process uses the DP (deep plug) p^+ regions to isolate the devices from each other.

After RCA cleaning[21], another thin-film photoresist is patterned with a DN mask to

[21] RCA cleaning is a multi-step cleaning process that is commonly used in semiconductor device fabrication to remove organic and inorganic contaminants from silicon wafers. The process is named after the Radio Corporation of America (RCA), where it was first developed in the 1960s.

define: the n^+ collector plug of the NPN devices, the bottom-gate plug of the p-channel JFET, and the base plug for the PNPs. The implantation uses phosphorus (P^+), with a dose of 5E15 ions/cm^2 at 180 keV of energy (Fig. 5.44).

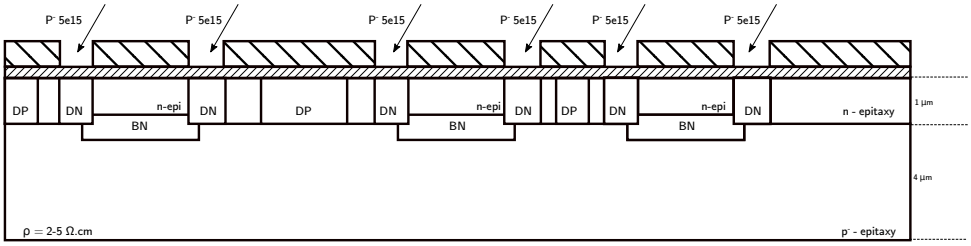


Figure 5.44: The DN regions serve as the n^+ collector plug for the NPN devices, the bottom-gate plug for the p-channel JFET, and the base plug for the PNPs.

After another RCA cleaning, a lithographic step via an LP mask defines the regions to create: a heavily-doped extrinsic base for the NPN devices, the drain and source regions of the p-channel JFETs, and an emitter region for the PNP devices (Fig. 5.45). A boron dose of 3E15 ions/cm^2 at 15 keV of energy is used for the implantation.

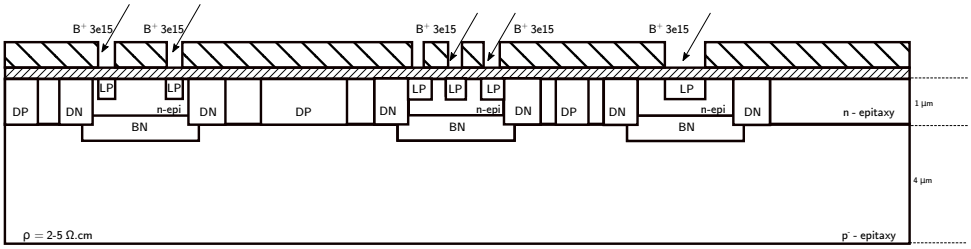


Figure 5.45: The process employs an LP mask to create a heavily-doped extrinsic base for the NPN devices, drain and source regions of the p-channel JFETs, and an emitter region for the PNP devices.

Then, an LB1 mask serves to pattern regions for the base-link implantation. A boron dose of 11E14 ions/cm^2 at 11 keV of energy is used (Fig. 5.46). The base-link regions contact the heavily-doped extrinsic base region to the lightly-doped intrinsic base region.

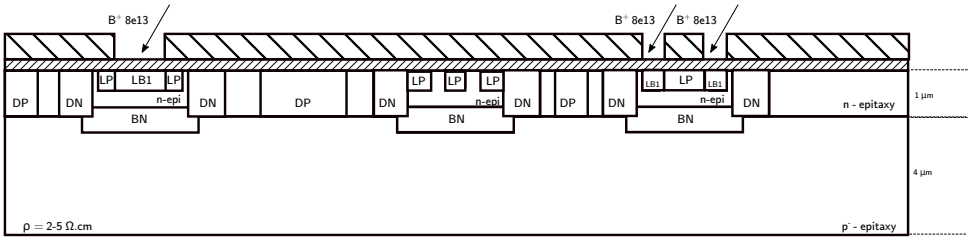


Figure 5.46: The process uses an LB1 mask to link the extrinsic and intrinsic base regions of the NPNs and to serve as collector regions for the PNPs.

An LB2 mask is used to implant a more lightly doped link-channel region on the low-noise p-channel JFETs (Fig. 5.47). The implantation happens with a dose of 4.5E12 ions/cm^2 of boron at 40 keV of energy.

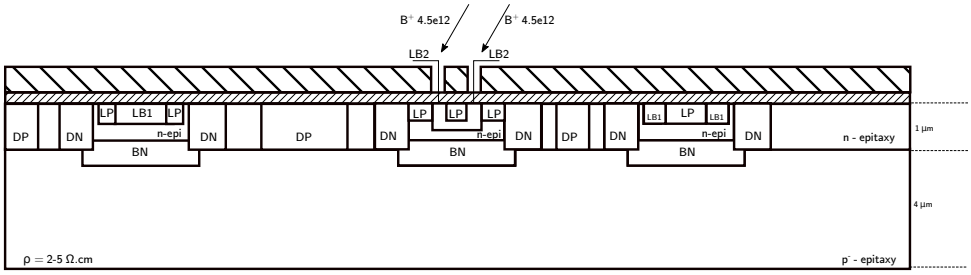


Figure 5.47: The process uses an LB2 mask to implant a lightly doped p-type channel for the low-noise p-channel JFETs.

Thereafter, a 300 nm of low-stress silicon nitride deposited by LPCVD (low pressure chemical vapour deposition) is used as a surface isolation layer. A plasma etching step opens the contact windows patterned by a CO mask for the emitter and collector regions of the NPNs, the top and bottom gates of the PJFETs, and the base contact of the PNPs. An As$^+$ dose of 7.5E15 ions/cm^2 at 40 keV of energy is used (Fig. 5.48). The nitride layer serves as the actual masking layer for this implantation and only the contact windows are implanted, i.e. the emitter implant is self-aligned to the emitter contact window.

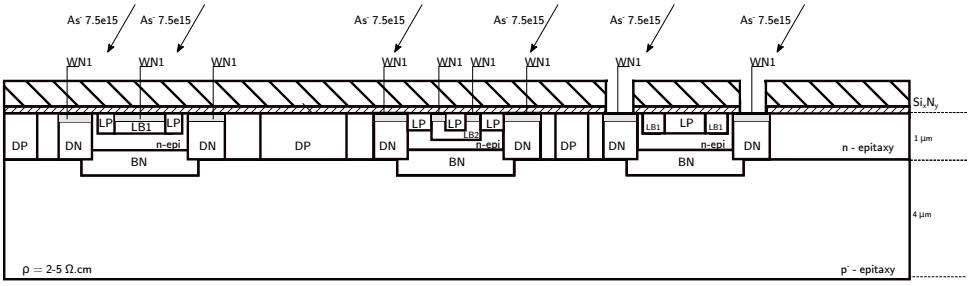


Figure 5.48: Using a WN1 mask, the process defines the emitter and collector regions of the NPNs, the top and bottom gates of the PJFETs, and the base contact of the PNPs.

The process uses an NWP mask to define the regions where no intrinsic base implant is desired (Fig. 5.49). Again the nitride serves as the actual masking layer and all contact windows outside the NWP regions receive a light boron implant of 1.4E14 ions/cm^2 at 20 keV of energy. It does not affect the quality of the n-type contacts. After completing all implantations, a single thermal annealing at 950 °C activates the dopants.

A Marangoni step removes the native oxide in the contact windows and a 650 nm layer of aluminum silicide (Al1%Si) at 350 °C is sputtered for the first metallization (Fig. 5.50). An IC mask defines the first layer of interconnects using RIE (reactive ion etching). An aluminum fence removal step is performed using a mixture of concentrated phos-

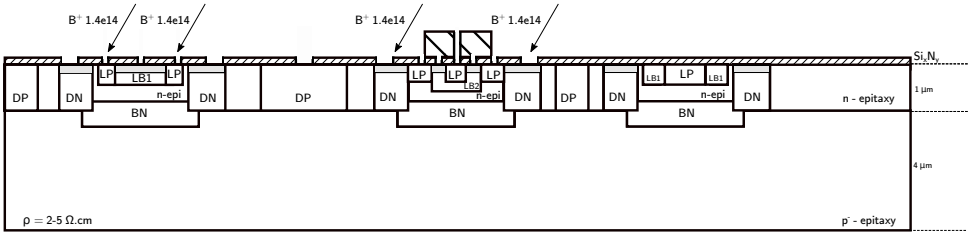


Figure 5.49: An NWP mask prevents the low-noise JFETs to receive an intrinsic base implant.

phorus acid (H_3PO_4 85%), concentrated nitric acid (HNO_3 65%), concentrated acetic acid (CH_3COOH 100%), and deionized water for 30 s.

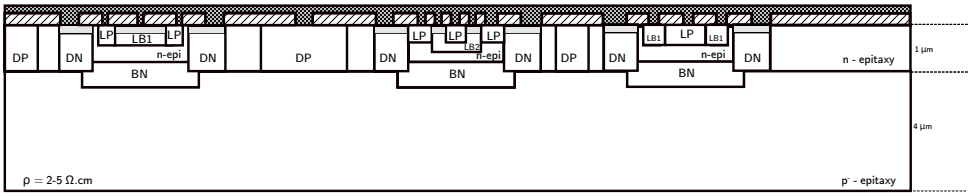


Figure 5.50: The process utilizes an IC mask to pattern the first metallization, composed of a thin layer of aluminum containing 1 % silicon.

The process follows with a deposition of 800 nm of SiO_2 using PECVD (plasma enhanced chemical vapor deposition) for surface isolation. A plasma etch is used to etch back 600 nm of oxide for spacer formation, and a 600 nm of SiO_2 is deposited using PECVD.

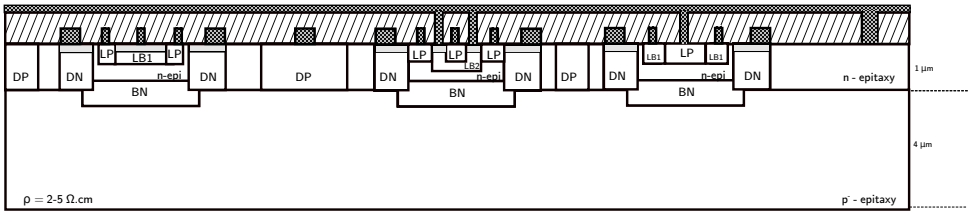


Figure 5.51: The process involves opening contact windows using a CT mask, sputtering a thin layer of aluminum containing 1 % silicon, and defining the second metallization using an IN mask.

The process utilizes a CT mask to pattern the regions where the contact windows for the second metallization layer must be opened. A plasma etches the oxide and softly lands on the aluminum layer. Then, a thin-film layer of aluminum containing 1 % silicon is deposited using RF sputtering at a temperature of 350 °C. The process uses an IN mask to pattern a second layer of interconnects using RIE (Fig. 5.51), and an aluminum fence removal step is performed.

Then, a 800 nm-thick silicon nitride film is passivated through PECVD to isolate the second and third metallization electrically. Next, the process utilizes a CT2 mask to pat-

tern regions where contact windows are open using a plasma etcher (Fig. 5.52).

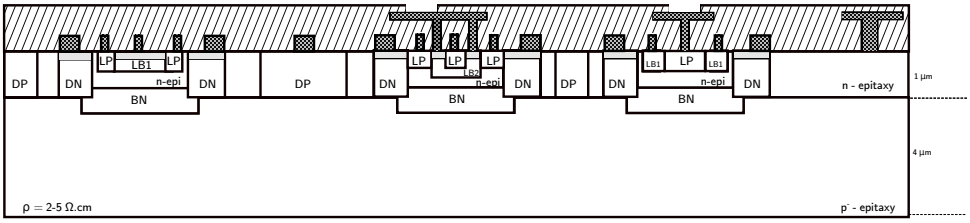


Figure 5.52: A CT2 mask defines the regions where windows are open with RIE.

For the third metallization, a single sputtering process deposits a 1475 nm-thick of aluminum film plus a 375 nm-thick of titanium nitride (TiN) film. The aluminum fills the vias while the TiN forms the electrodes. The TiN mask followed by a RIE step defines the regions for the electrodes (Fig. 5.53). Thereafter, the process utilizes an AL mask to pattern the aluminum bond pads where the µLEDs will be integrated, and to pattern the bond pads used for the PCB interfacing.

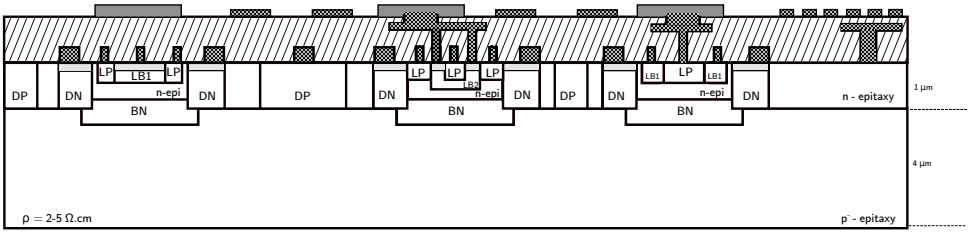


Figure 5.53: The third metallization uses a single sputtering of aluminum and TiN for creation of aluminum bondpads and electrodes, respectively.

Next, a 800 nm-thick silicon nitride layer deposited by PECVD passivates the exposed sidewalls of the aluminum, leaving only the TiN layer exposed[22]. The process then simultaneously utilizes masks AL and TiN to pattern regions where the silicon nitride film that covers the bond pads and the electrodes is selectively removed through an RIE step. Subsequently, the wafers are subjected to an alloying process at a temperature of 400 °C for a duration of 20 min to form a metallurgical bond between the first aluminum metallization and its underlying diffusion layers.

After alloying, the frontside processing has finished, and the backside processing starts. The backside processing comprises the micromaching steps used to release the optrodes from the wafers.

The process starts by spraying a 12 µm-thick of positive photoresist film onto the 2 µm-thick SiO_2 layer. After a 30 min rehydration period, the photoresist is exposed through an RIE mask (Fig. 5.55) and followed by a 30 min photoreaction time. Subsequently, the photoresist is manually developed using a diluted, sodium-free solution.

[22] This step ensures that TiN is the only electrode material in contact with the brain tissue.

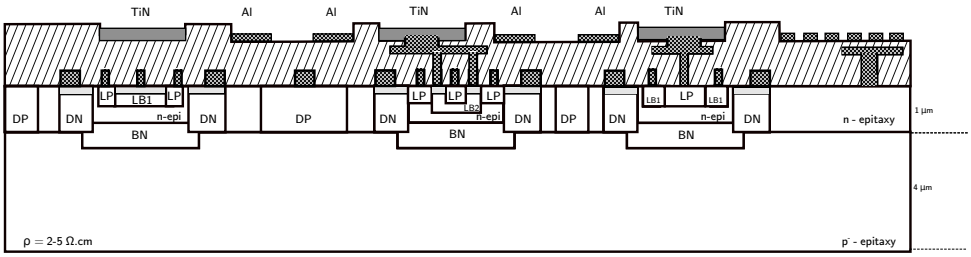


Figure 5.54: A sidewall passivation ensures the sidewalls of aluminum are not in contact with the neural tissue.

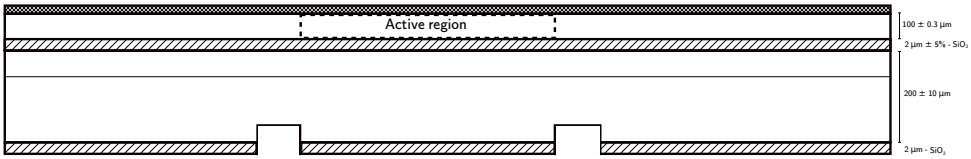


Figure 5.55: Trenches are initially created to prepare the optrodes to be released from the wafers. The mask RIE is used and the trenches etched with BHF and DRIE steps.

5

A plasma etcher removes 2 µm of SiO_2 to open windows on the backside of the wafer. Next, the process utilizes a DRIE step to etch approximately 20–40 µm of silicon, creating trenches that shape the optrodes.

After completing an RCA cleaning, the process proceeds with a lithographic step by spraying a 12 µm-thick of negative photoresist on the backside of the wafer. After the abovementioned step, the photoresist is subjected to a cross-linking process at a temperature of 115 °C for 90 s and exposed to light through a mask RIE2, creating openings on the wafer where the optrodes will be released. The photoresist can then undergo a photoreaction process for an appropriate period before manual development (Fig. 5.56).

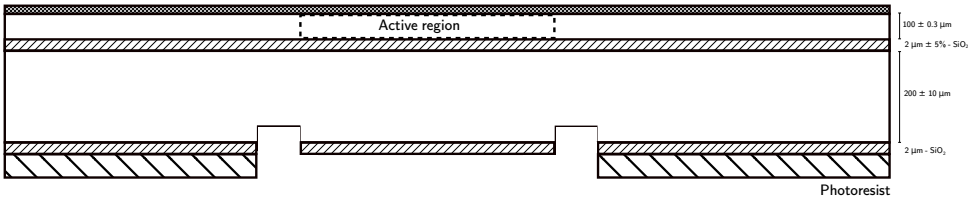


Figure 5.56: An RIE2 mask is used to pattern the regions where the backside oxide must be removed.

The manual development process must continue until no residual photoresist materials are observed inside the trenches. Inspection using a scanning electron microscope (SEM) is recommended. Upon successful removal of residues, the wafers proceed to a BHF solution bath to etch a 2 µm thick layer of SiO_2 (Fig. 5.57). After removing the oxide layer, the wafers are ready for the second DRIE step.

The second DRIE step etches approximately 200 µm of silicon until the trenches reach a 2 µm-thick BOX layer (Fig. 5.58). Upon completing this step, the regions beneath each optrode, i.e., the active regions, are protected with a 20–40 µm-thick of

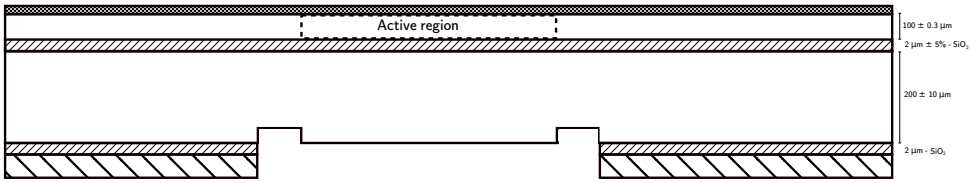


Figure 5.57: A BHF bath removes the 2 µm of SiO_2 on the backside, and it prepares the wafer for the next DRIE step.

monocrystalline silicon layer.

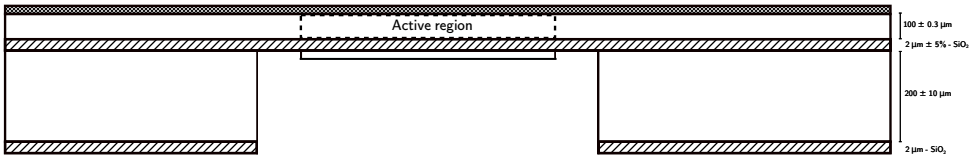


Figure 5.58: A DRIE step etches approximately 200 µm of silicon until it lands on the BOX.

The next step involves immersing the wafer in a BHF bath to remove the 2 µm layer of SiO_2 covering the BOX, which exposes the device layer (Fig. 5.59). The process follows with an RCA cleaning and a carrier wafer subsequently bonded to the front side of the wafer for the final DRIE step[23]. Because the temperature of the chuck can increase during the DRIE process, it is crucial to ascertain that this temperature increase does not affect the bond between the carrier and the processing wafers.

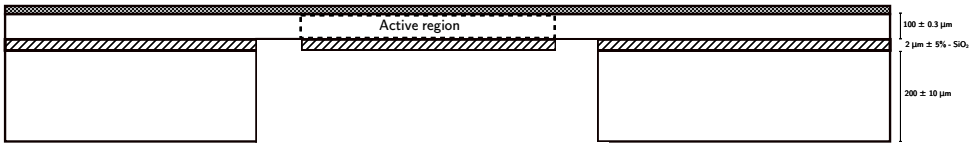


Figure 5.59: A BHF bath removes the 2 µm of SiO_2 from the BOX and the device layer is exposed.

The last DRIE step etches 100 µm of silicon (Fig. 5.60) until it lands on the carrier wafer. At this stage, the active region is still protected by the BOX layer due to the high $Si:SiO_2$ selectivity of the DRIE process.

An optional BHF bath removes the 2 µm of SiO_2 from the BOX, and the carrier wafer is removed from the processing wafer. The processing wafers proceed to a final RCA cleaning and are then stored in a carrier box for transportation.

Alas, the microfabrication could not be completed due to equipment malfunctioning in the cleanroom. Specifically, the second epitaxy film was not grown, and the implantations after the BN mask could not be performed.

[23] A carrier wafer may be bonded to a processing wafer using polyimide adhesive tapes or photoresist.

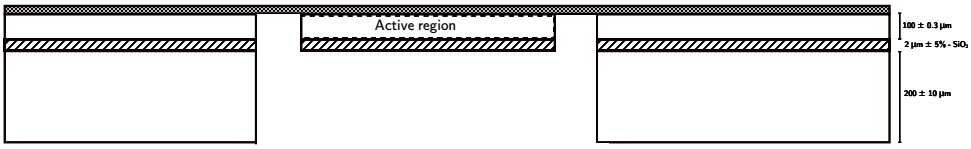


Figure 5.60: The last DRIE step etches 100 µm of silicon until it lands on the carrier wafer.

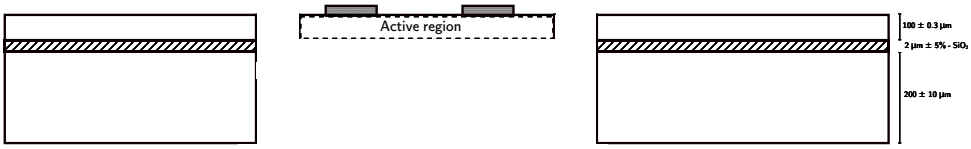


Figure 5.61: The carrier wafer is removed; the processing wafers, cleaned; and the wafers stored on a carrier box for transportation.

Nevertheless, the following section presents the lithographic results achieved prior to the second epitaxy and the steps that start the backside processing. The latter was tested with bulk silicon wafers to verify the steps involved in the backside processing.

5.9.4. RESULTS AND DISCUSSION

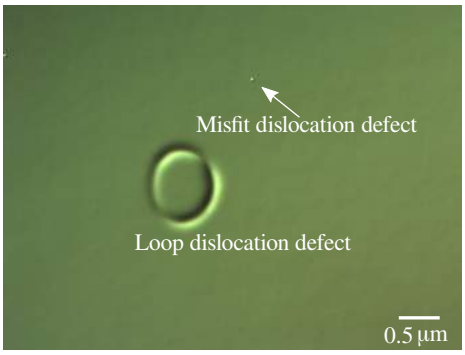
SOI wafers are often manufactured by bonding two silicon wafers together such that there is a buried oxide layer between them. Subsequent thinning of one of the wafers produces a monocrystalline film of desirable thickness separated from the substrate by the insulator.

Because the bonding occurs at annealing temperatures, it is often accompanied by elastic wafer deformation that may contribute to an increase in the number of morphological defects at the Si–SiO_2 interface that propagates during the epitaxy: the so-called 'misfit dislocation'. As a result, wafer inspection plays a crucial role to ensure device performance and the overall process reliability.

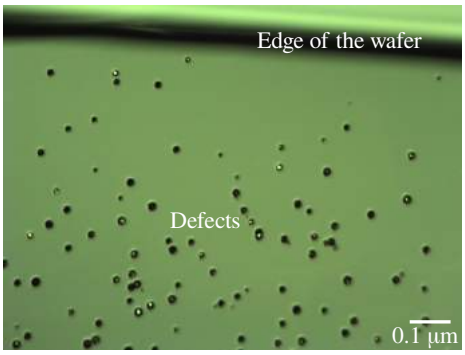
Figures 5.62a and 5.62b show examples of such defects found during wafer inspection under an optical microscope. The ocurrance of misfit dislocations was mostly noticed on the edge of the wafers (Fig. 5.62b), which are processing-free regions. Other minor defects were identified on the processing regions (Fig. 5.62a), but much scarcer in density. Hence, their impact on the device performance is expected to be very limited or null.

Following the epitaxy, the definition of the BN regions takes place. Fig. 5.63 shows the lithographic result after exposure of the BN mask and photoresist development.

Next, the screen oxide used for implantation of the BN mask was measured using an optical spectrometer through the oxide windows. Fig. 5.64 shows the reflectance measurements on a 50 µm wide window. The measured oxide thickness based on the reflectance was 18 nm, which is in accordance with the expected 20 nm. Various windows were measured, in different wafers, and the results were consistent. Accordingly,



(a)



(b)

Figure 5.62: Defects noticed under an optical microscope during inspection after the epitaxy: a) defects noticed on the processing regions. The cause of the loop defect is uncertain, but possibly also associated to misfit dislocation during the epitaxy growth, and b) defects noticed on the wafer edge. Its impact on the device performance is limited because such regions are not processed.

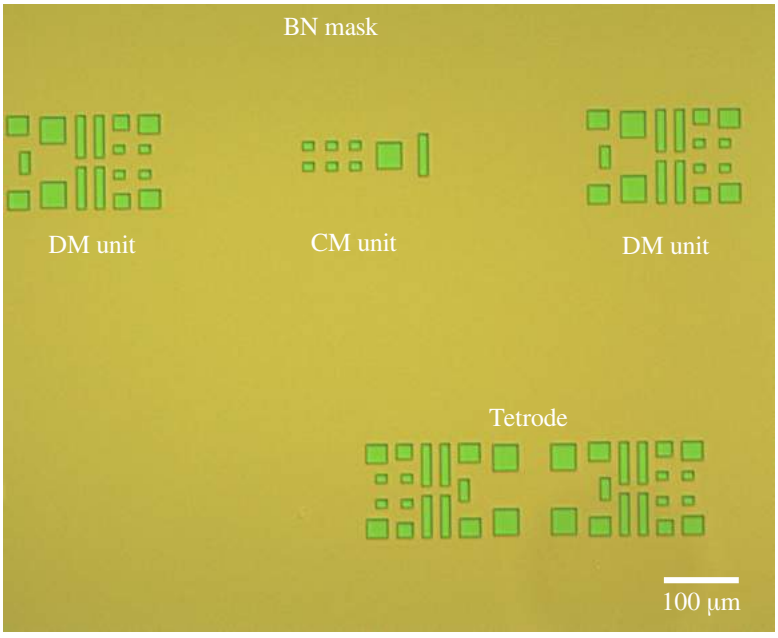


Figure 5.63: Lithographic result under optical microscope showing the regions where the BN mask was exposed and developed. Notice that the regions denote two different optrodes: the upper one using the DM and CM units; the lower, using the tetrode.

the wafers were sent for implantation to IBS in France.

Meanwhile, bulk silicon wafers were used to test the backside processing. The spray coater was used to coat approximately 12 µm of photoresist and pattern the RIE mask. Because the rehydration and reaction times of 30 min were found to be insufficient in

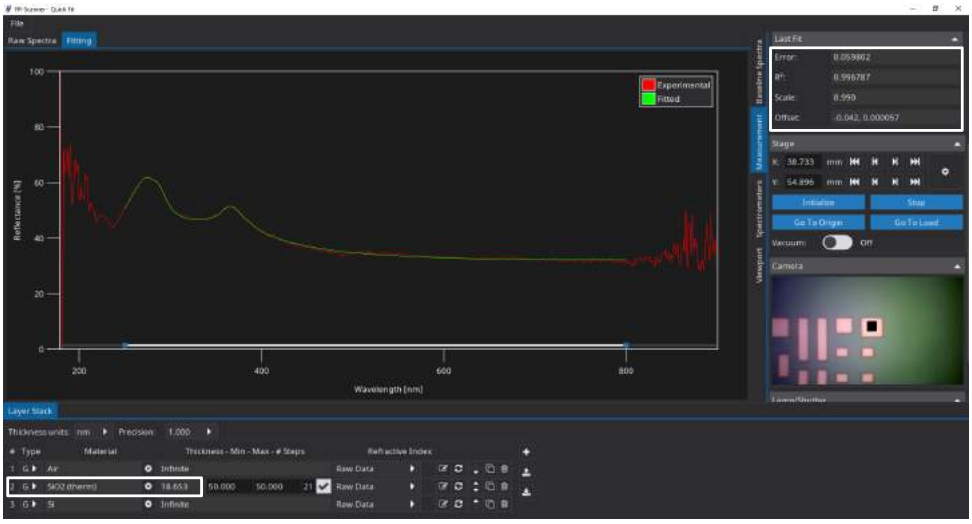


Figure 5.64: Reflectance measurements used to estimate the thickness of screen oxide grown during the thermal oxidation. The error between the experimental and theoretical curves is only 0.06. The estimated oxide thickness is 18 nm which is in good agreement with the expected value of 20 nm.

some wafers, two hours were used for each time. After the manual photoresist development, the 2 µm of SiO_2 was removed with plasma etching and the DRIE etched approximately 40 µm of silicon to create trenches that shapes the optrodes.

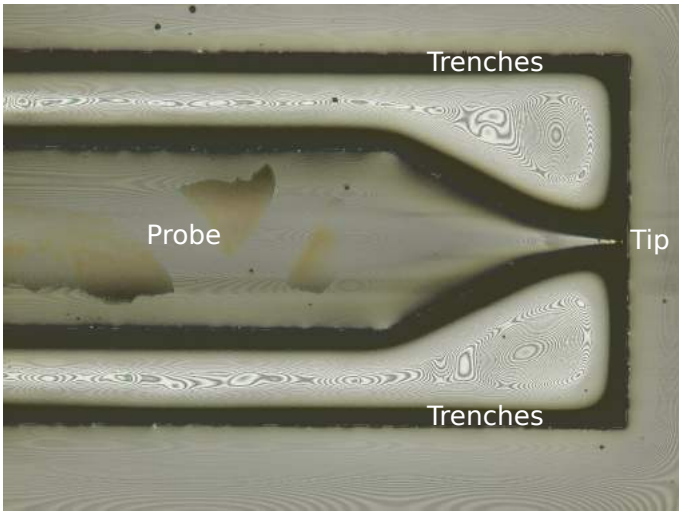


Figure 5.65: Top view of an optical image taken from a Keyence microscope detailing the trenches created on the silicon to shape the optrode.

Fig. 5.65 shows a top view of the test wafer ensuing the DRIE processing step, whereas

Fig. 5.66 details the same figure with a 3D perspective using a white light interferometer. Notice that the trenches are 40 µm deep with smooth sidewalls. The photograph was taken prior to cleaning, which explains the polymer residues on top of the probe. Such residues can be removed with an oxygen plasma followed by a RCA cleaning.

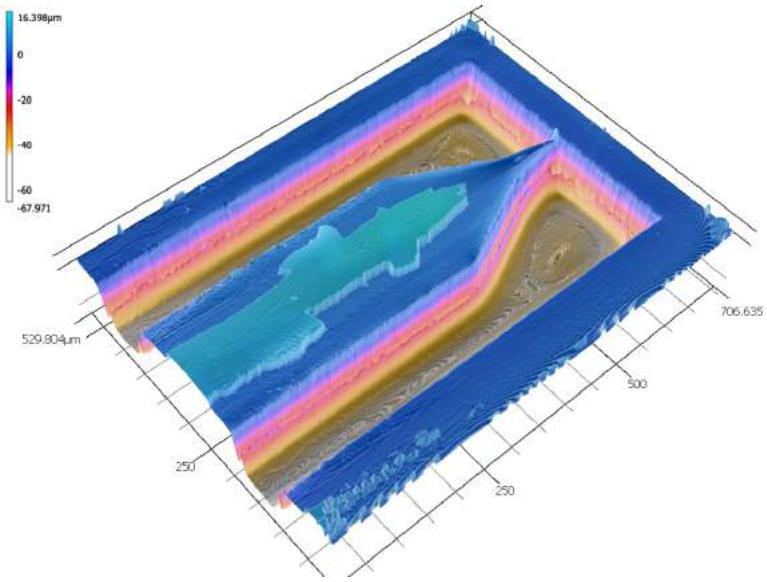


Figure 5.66: 3D image taken from a Keyence microscope using a white light interferometer to detail the roughness of different materials. Notice that the trenches are approximately 40 µm deep, and there are photoresist residues deposited on top of the probe.

After ten days, the processed SOI wafers returned from implantation but the fabrication was halted due to the absence of the Arsenic gas required for the next epitaxy growth.

5.9.5. CONCLUSION

This chapter described the methodology used to design artifact-resilient optrodes that enable the measurement of infraslow brain activity during optogenetics. The monolithic integration of ICs and MEMS enables the construction of miniaturized probes that incorporate electronic and mechanical functionalities. The former records infraslow electrical activity in the brain with optimized low-noise performance; the latter penetrates the laboratory mouse's delicate, soft, and small encephalon with minimal injury.

Challenges in the electrophysiological recordings include signal contamination by noise and interference. Furthermore, the so-called photo-induced artifacts are a kind of interference that often permeates optogenetic setups. Such interference contains the time-domain appearance and spectral features of genuine local field potentials [16]; therefore, its presence must be eliminated to discriminate false positives in the recordings.

The monolithic fabrication of in-situ low-noise recording units is a promising solution to control photo-induced artifacts because it relaxes the signal bandwidth and computational power compared to post-processing techniques. The circuit design of the low-noise recording units benefits from a p-channel JFET optimized for low-noise operation in the infraslow frequency range, and a common-mode feedback unit that dramatically reduces the common-mode interference in-situ; thus, it enhances the signal quality during the recordings. Simulations using a SPICE-like program revealed that the circuit behaves as expected with good performance and robustness against electrical instability. Moreover, real LFP signals were used for the transient simulations, whereas Monte Carlo and worst-case scenarios were evaluated to account for the process spread during fabrication.

The methodology also benefited from a holistic iterative co-design thinking process. The specifications fed the co-design phase such that the parameters in various design domains were accommodated after some iteration. The functional decomposition that preceded the fabrication process anticipated the mismatch between the electrical characteristics of the SOI wafers and the ones required by the DIMES-03 protocol. Process simulations using the finite element software TSUPREM-4 revealed the minimum epilayer thickness required to change the dopant concentration on the device layer of the SOI wafers. The fabrication protocol accounted for such specifications.

Alas, the fabrication process was halted prior to the second epitaxy growth due to the unavailability of Arsenic during the remainder of the project. Nevertheless, some fabrication results were presented. Misfit defects were noticed after the first epitaxy growth, but the majority is located in processing-free regions. Therefore, their presence most likely does not interfere with the device's performance. The buried n^+ layer was implanted through a 18 nm of thermal SiO_2, and the backside processing using test wafers reveals the accuracy and the sidewall smoothness created with the DRIE. Such smoothness is particularly crucial for minimizing injuries of the mouse's small encephalons.

Lastly, the use of μLEDs directly mounted on a custom micromachined silicon-based probe allows for a more compact approach compared to bulky laser-based setups. Integrating the optrodes with a PCB that includes an LDO powered by a 6.5-V-coin battery and an Arduino board with Bluetooth interface is expected to enable the construction of wireless closed-loop optrodes required in the behavioral experimentation of untethered animal subjects. Such setups are especially crucial when social behaviour with other subjects plays a major role during the optogenetic experimentation.

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6

Conclusions and Recommendations

When it is dark enough, you can see the stars.

—Ralph Waldo Emerson

6.1. CONCLUSIONS

This doctoral thesis presented a comprehensive methodology for designing and co-fabricating integrated circuits (ICs) and microelectromechanical systems (MEMS) for emerging biomedical technologies. Specifically, this research project focused on designing and fabricating two biomedical devices, catering to both in-vitro and in-vivo applications. This thesis offers a detailed account of the different stages of the co-fabrication process, thereby enabling the development of innovative and effective biomedical devices that seamlessly integrate ICs and MEMS. It offers insights into the co-fabrication of ICs and MEMS, with potential implications for advancing biomedical technology and fostering breakthroughs in healthcare.

The primary motivation for the co-fabrication approach stems from acknowledging the detrimental effects caused by some microsystem integration techniques in specific biomedical applications, as discussed in Chapter 1. Specifically deserving attention is the increased footprint and the introduction of protrusions resulting from wire bonds, which may undermine the effectiveness of the interface between biomedical devices and biological systems. Therefore, it is essential to devise seamless interconnections between these microsystems to enhance robustness, optimize electrical performance, attain compactness, and ensure improved physical conformability to biological structures.

Using MEMS technology offers a promising means to construct essential functionalities in biomedical devices across diverse domains, such as mechanical, electrical, and optical. This technological capability has the potential to enable the precise regulation and observation of various biological systems at the microscale. Additionally, MEMS technology is compatible with IC technology, which is crucial for conditioning the signals of ubiquitous transducers in biomedical devices.

The co-fabrication of ICs and MEMS offers several advantages, especially when sensors can be positioned close to preamplifiers. This proximity ensures that information quality is maintained by effectively attenuating noise and sources of interference. Moreover, implementing local control loops incorporating sensors and actuators is feasible, potentially enhancing the system's time response. These benefits contribute to the increased functionality and performance of biomedical devices, which is essential in developing reliable and efficient diagnostic and therapeutic tools.

However, co-fabricating state-of-art complementary metal oxide semiconductor (CMOS) with MEMS technology poses several challenges. Specifically, the melting point of metals employed in the CMOS interconnects severely constrains the maximum thermal budget allowed by the MEMS process. This hindrance may compromise the integration with high-thermal-budget processing modules and the IC–MEMS co-design freedom. Moreover, the bottleneck in the photolithography pipeline dramatically increases the cost-per-unit area per function, which can prove especially onerous for emerging biomedical technology that interfaces with large-area transducers.

To overcome these difficulties, two proprietary IC technologies were employed to streamline the lithographic processing pipeline and enhance integration compatibility with supplementary MEMS-based processing modules, thereby enabling the cost-effective fabrication of monolithic ICs and MEMS for emerging biomedical technologies.

These advancements facilitate the creation of seamless microsystems that are expected to be integral components of the forthcoming generation of biomedical technology.

The first IC process technology, BiCMOS7, was employed to monolithically integrate a BiCMOS-based temperature sensor onto an organ-on-chip device that includes a polydimethylsiloxane (PDMS) membrane (Chapter 4). This integration was accomplished by interlacing the implantation doses of the CMOS and the vertical NPN bipolar devices, simplifying the lithography pipeline. The resulting process line was more versatile and robust than state-of-art CMOS technologies, enhancing integration compatibility with external micromachining processes.

Moreover, this IC technology facilitated the development of a novel IC-interlaced-MEMS fabrication technique, which streamlined the process by utilizing a single SiO_2 deposition for both the IC and the MEMS fabrication. This interlaced technique sacrifices process orthogonalization to favor fabrication simplicity, distinguishing it from existing interleaved techniques.

Generally, this co-fabrication accomplishment holds great promise for advancing organ-on-chip devices and related technologies, as it demonstrates the feasibility of integrating multiple functionalities and components into a single device. Furthermore, this development represents a stride toward creating smart and seamless biomedical devices that interface with biological structures with enhanced versatility cost-effectively. The findings of this study are expected to stimulate further research and innovation in this area and may potentially lead to groundbreaking discoveries in the realm of drug discovery.

The second IC process technology, DIMES03, was employed to construct silicon-based neural probes for recording low-noise infraslow activity (ISA) in the brain during optogenetic experimentation (Chapter 5). The optrodes devised in this thesis benefit from junction-gate field-effect transistors (JFET) readily available in the technology and already optimized for low-noise operation at low frequencies. This feature allows the construction of optrodes with in-situ DC low-noise amplifiers, for robust measurements of infraslow activity. This solution locally reduces interference, such as photo-induced artifacts, thereby relaxing the signal bandwidth and power, which is crucial for constructing wireless closed-loop systems without transmitting unnecessary information. Such wireless systems are crucial in the behavioral experimentation of untethered animal subjects.

Additionally, various optrode designs were created to accommodate various optogenetic experiments. These designs considered the number of μLEDs mounted on the shaft, electrode quantity and size, electrode spacing, common-mode feedback loops, ground and reference electrode position, the number of shafts, and the length of the probe. All in all, optogenetics has emerged as a potent neuroscientific tool that can provide an improved understanding of brain connectivity, as well as the diagnosis and treatment of various pathologies and disorders that impact the brain. These advancements in optogenetics research provide promising possibilities for developing future neuroscientific research tools.

6.2. SCIENTIFIC CONTRIBUTIONS

CHAPTER 2: DISCLOSURE, ELUCIDATION, AND NEW INTERPRETATION OF THE "INTERLEAVED TECHNIQUE".

Chapter 2 introduced a novel classification scheme for IC–MEMS monolithic fabrication techniques. The classification framework addressed inconsistencies in prior works and provided a more coherent and understandable organization of the diverse techniques. The proposed scheme employs the "thermal budget" as a benchmark to establish the process sequence and identify the type of technique employed.

Besides improving the classification of existing techniques, the novel scheme also incorporates a new fabrication approach, IC-interlaced-MEMS, further explored in Chapter 4. This technique is similar to its "sibling version" IC-interleaved-MEMS. However, it differs because specific process steps are shared or interlaced between the IC and MEMS fabrication domains, resulting in a non-orthogonal process. Consequently, the IC-interlaced-MEMS scheme can lead to a performance contradiction, necessitating the reassessment or fine-tuning of specific design parameters or specifications. Conversely, the IC-interlaced-MEMS approach offers various advantages, such as a reduced cost-per-area per unit function and improved photolithography pipeline workflow. These advantages result primarily from the interlaced process steps across different design domains. These benefits are especially relevant for integrating large-area transducers, ubiquitous in biomedical applications. In summary, Chapter 2 of this thesis provides a comprehensive and systematic framework for co-fabricating ICs with MEMS.

CHAPTER 3: CREATION OF A METHODOLOGY NAMED "IC–MEMS HOLISTIC ITERATIVE CO-DESIGN THINKING" FOR THE MONOLITHIC FABRICATION OF IC–MEMS MICROSYSTEMS.

Motivated by the interaction between design and fabrication, a co-design approach for the monolithic fabrication of ICs and MEMS was developed. This approach, named IC–MEMS holistic iterative co-design thinking, is described in detail in Chapter 3. The IC–MEMS holistic iterative co-design thinking approach involves splitting, combining, adding, or removing process steps and integrating this information into the co-design step. This approach allows for the revision, adjustment, and proper accommodation of different device attributes over the design domain. The iterative process continues until the designer finds a solution that meets the performance specifications.

Moreover, this approach includes a functional decomposition method to segregate the complex multidimensional problems associated with IC–MEMS monolithic fabrication into one-dimensional subproblems that are easier to solve. Eight functional groups were proposed to identify the main challenges involved during the IC–MEMS monolithic fabrication.

Each functional group requires posing specific and more general questions during the co-design phase to anticipate and clarify specific microfabrication challenges. This functional decomposition step is expected to give the designer tools for a better holistic understanding of the process. Benefits of using this approach include the capacity to an-

ticipate and proactively overcome microfabrication hurdles, devise innovative solutions or protocols, adjust parameters or variables in the co-design phase, and organize process steps orthogonally. This approach is mainly intended to provide a more structured and systematic view of the design and fabrication of microsystems.

Overall, the IC–MEMS holistic iterative co-design thinking enhances our understanding of the complex interactions between ICs and MEMS and fosters the development of advanced, multifunctional biomedical devices. Additionally, the proposed approach and methods may find applications that extend the bioelectronics field, including nanotechnology, automotive, aerospace engineering, photonics, and quantum computing. Essentially, "the IC–MEMS holistic iterative co-design thinking" catalyzes future research in related fields that benefits from the monolithic integration of ICs with MEMS.

CHAPTER 4: USING A NOVEL IC-INTERLACED-MEMS TECHNIQUE TO ENABLE THE CO-FABRICATION OF A BICMOS-BASED TEMPERATURE SENSOR ON A MEMS-BASED ORGAN-ON-CHIP DEVICE.

Chapter 4 applied the "IC–MEMS holistic iterative co-design thinking" methodology to design and fabricate a BiCMOS-based temperature sensor on a silicon-based organ-on-chip device that includes a stretchable PDMS membrane. A novel IC-interlaced-MEMS fabrication technique was investigated to enable the monolithic fabrication of circuits with micromachining processes. This IC-interlaced-MEMS technique contributed to a better photolithography pipeline workflow, leading to a more efficient and streamlined process for co-fabrication.

Organ-on-chip technology as a research tool allows for the conduct of customized experiments using induced pluripotent stem cells (iPSC), which can provide insights into how pathophysiological responses at the sub-cellular level impact different scales, such as tissues, organs, and systems.

Integrating in-situ transducers that can accurately monitor physical quantities, such as temperature, is essential for cell experimentation involving incubators. Integrating a BiCMOS-based temperature sensor on an organ-on-chip device enabled continuous in-situ temperature monitoring of cells for the first time, which is particularly important during optical inspection outside the incubator. Additionally, the results of this chapter provide practitioners with valuable information about how long cells can be outside the incubator for optical inspection at room temperature.

Overall, Chapter 4 represents a contribution to the field of IC–MEMS co-fabrication for biomedical applications, as it showcases the successful integration of complex circuits with MEMS-based structures, thereby paving the way for future developments in organ-on-chip devices and related technologies.

CHAPTER 5: ENABLING ARTIFACT-RESILIENT INFRASLOW ACTIVITY RECORDINGS BY CO-FABRICATING IN-SITU DC LOW-NOISE AMPLIFIERS WITH SILICON-BASED NEURAL PROBES.

Chapter 5 applied the "IC–MEMS holistic iterative co-design thinking" methodology to design artifact-resilient optrodes with in-situ DC low-noise amplifiers for infraslow activity recordings in optogenetic experimentation. These optrodes incorporate in-situ DC low-noise amplifiers and commercially available in-situ μLEDs mounted on the shaft, emitting light at a wavelength of 460 nm. By utilizing low-noise p-channel JFETs in a fully-differential mode and implementing common-mode feedback, these optrodes enable high-quality measurements of infraslow activity under 100 mHz. The photomasks were designed to accommodate six different designs for multiple studies. However, the microfabrication progress was halted after the BN implantation due to the inactivation of the epitaxy machine and the ion-beam implanter. Despite this setback, Chapter 5 represents a contribution to optogenetic experimentation. It demonstrates the successful application of the IC–MEMS co-design methodology to design artifact-resilient optrodes with in-situ DC low-noise amplifiers. Moreover, the multiple design options provided by the photomasks highlight the potential for this technology to facilitate a wide range of future studies including, but not limited to, epilepsy, Parkinson's, and migraine.

6

6.3. RECOMMENDATIONS FOR FUTURE WORK

INVESTIGATING CHIPS FAILURE

In light of the chips failure described in Chapter 4, it is recommended to investigate a more refined RCA cleaning procedure involving an additional photoresist stripping step with an oxygen plasma to improve the wire-bonding adhesion during system-level integration. Likewise, it is advised to investigate alternative approaches to integrating chips into the PCB, such as flip-chip bonding. Alternatively, one could investigate the integration of chips that have not undergone wafer-level measurement to minimize the adverse effects of scratches on the bond pads caused by microprobes. The scratches caused by the microprobes on the pads can compromise the quality of the wire bond adhesion and negatively affect the overall performance and reliability of the device.

Accordingly, it is recommended to investigate additional metrology methods to identify the root cause of the chip failures. Inspection with an optical microscope has proven insufficient due to limited resolution after the system-level integration, which includes the integration of wells, glue, and other components. Alternative metrology methods, such as scanning electron microscopy (SEM) and X-ray, could be explored to detect potential circuitry issues. These advanced techniques have the potential to provide higher-resolution imaging of the integrated circuits and help identify any possible defects.

INCORPORATING ADDITIONAL FEATURES IN ORGAN-ON-CHIP TECHNOLOGY

In the context of next-generation organ-on-chip technology, it is critical to integrate transducers to achieve a more controlled cellular environment. One of the essential pa-

rameters to monitor in addition to temperature is pH, given that cells grow within a constantly changing microenvironment. In this regard, ion-sensitive field-effect transistor (ISFET) technology is a promising candidate for pH sensing in organ-on-chip applications. ISFETs are solid-state devices that have the potential to be integrated with MEMS-based structures to form microsystems. They operate by measuring the potential difference created by the charge of ions at the surface of the gate insulator. Combining ISFETs with MEMS-based structures makes achieving accurate and reliable pH measurements in a microfluidic environment possible. Such measures can provide important insights into the metabolic activity of cells and the response of cells to various stimuli, which can have implications for drug development and disease modeling. Therefore, integrating ISFET technology with MEMS-based structures represents an useful step toward developing advanced organ-on-chip technology with enhanced sensing capabilities. As an example, the current BiCMOS flowchart can be modified to incorporate an LPCVD silicon nitride surface as the sensitive gate for the ISFET devices, as demonstrated in [1].

The BiCMOS-based temperature sensor can provide a temperature input to compensate for the pH readout since the ISFET is a temperature-dependent device. ISFETs have been successfully used as biosensors for various analytes and biological processes, such as nucleic acid hybridization, protein-protein interaction, and enzyme-substrate reactions involving glucose and GABA, when suitably functionalized [2, 3].

Besides incorporating transducers, microfluidics is a crucial feature of organ-on-chip technology, as the removal of toxins and waste products necessitates the use of microchannels. Therefore, integrating microfluidics is necessary for the successful development of organ-on-chip technology.

Likewise, incorporating actuators in a closed-loop manner could enable more autonomous solutions. For instance, in-situ heaters could be fabricated to achieve better temperature control. At the same time, MEMS-based drug delivery systems could allow accurate drug delivery and the precise delivery of optogenetic constructs through microfluidic channels and reservoirs. However, the fabrication of in-situ heaters requires identifying a stable material that can maintain its thin film form across a broad temperature range and is compatible with IC process fabrication lines.

INVESTIGATING HEAT CONDUCTION PATHWAYS INTO THE BRAIN TISSUE

Considering the system-level operation of the optrodes described in Chapter 5, the author acknowledges the limited efficiency of the μLEDs, which currently stands at approximately 10 %, thus resulting in heat losses that are ultimately transferred to the brain tissue. Given this fact, further research is necessary to ascertain the extent to which the heat produced by the μLEDs affects optogenetic experimentation. Nevertheless, implementing a light control scheme utilizing pulse width modulation (PWM) may be a viable solution to mitigate excessive heat generated by the μLEDs, as the light is not maintained at full power for extended periods.

INCORPORATING ADDITIONAL FEATURES IN OPTOGENETICS TECHNOLOGY

Incorporating photometry is also a valuable feature to integrate into the next generation of optrode technology. Optogenetic labeling is a powerful strategy to confirm the genetic expression of opsins in neurons through fluorescent markers. In-situ image sensors to detect fluorescent responses could be an excellent technological tool for rapidly validating optogenetic expression in neurons. However, constructing high-resolution image sensors necessitates access to modern CMOS technology. An in-depth study of their monolithic fabrication and foundry compatibility is necessary, as demonstrated in this Chapters 2 and 3 of this doctoral thesis.

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A

Appendix A: process flow for BiCMOS-based temperature sensor on Cytostretch

A

BICMOS-BASED SMART TEMPERATURE SENSOR WITH ORGAN-ON-CHIP USING THE **IC-INTERLACED-MEMS** TECHNIQUE

Fabrication Protocol (Class ISO-7)—frontside wafer treatment

- *Substrate:* double-side polished, <100>-oriented crystalline silicon, p-type, boron, 2–5 $\Omega \cdot$ cm, 400 µm thick, 100 mm of diameter.
- *Fiducial markers definition:* lithography by coating of 1.4 µm thick of Shipley SPR3012 positive photoresist, exposure at 150 mJ/cm^2, focus of 0, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s. creation of 120 nm deep structures into the silicon with plasma etching using CF_4/O_2 and Cl_2/HBr.
- *Cleaning line:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for 10 min and HNO_3 65 % at 110 °C for 10 min, rinse with DI water, drying).
- *Marangoni:* native oxide removal using HF (0.55 %), rinsing with DI water, and drying using IPA for marangoni effect.
- *Epitaxy:* growing 2 µm of boron-doped epitaxial film, with concentration of 1.0E16 atoms/cm^3 at 1050 °C and 60 torr.
- *Dry oxidation:* oxidation at 950 °C for 35 min using O_2 at 3.0 L/min
- *N-well definition:* lithography by coating of 3.1 µm thick of Shipley SPR3012 positive photoresist, exposure at 420 mJ/cm^2, focus of −1, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *Phosphorus implantation:* implantation of P^- with dose of 5.0E12 ions/cm^2 at 150 keV, with implantation angle of 7° and flat side turned 22° north east.
- *Cleaning line:* photoresist removal using O_2 plasma, and RCA cleaning.
- *Annealing:* drive-in at 1150 °C for 240 min using N_2 at 3.0 L/min and O_2 at 0.3 L/min
- *Oxide stripping:* HF with 1:7 of selectivity and etch rate of 1.3±0.2 nm/s
- *Cleaning line:* photoresist removal using O_2 plasma, and RCA cleaning.
- *Dry oxidation:* oxidation at 950 °C for 35 min using O_2 at 3.0 L/min
- *Shallow-N definition:* lithography by coating of 1.4 µm thick of Shipley SPR3012 positive photoresist, exposure at 140 mJ/cm^2, focus of 0, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.

Fabrication Protocol (Class ISO-7)—frontside wafer treatment

- *Arsenic implantation:* implantation of As^- with dose of 5.0E15 ions/cm^2 at 40 keV, with implantation angle of 7° and flat side turned 22° north east.
- *Cleaning line:* photoresist removal using O_2 plasma, and RCA cleaning.
- *Shallow-P definition:*lithography by coating of 1.4 µm thick of Shipley SPR3012 positive photoresist, exposure at 140 mJ/cm^2, focus of 0, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *Boron implantation:* implantation of B^+ with dose of 4.0E14 ions/cm^2 at 20 keV, with implantation angle of 7° and flat side turned 22° north east.
- *Cleaning line:* photoresist removal using O_2 plasma, and RCA cleaning.
- *Threshold voltage adjustment - bottom half:* lithography by coating of 1.4 µm thick of Shipley SPR3012 positive photoresist, exposure at 140 mJ/cm^2, focus of 0, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s. After development, only the bottom half of the wafer remains free from photoresist.
- *Boron implantation:* implantation of B^+ with dose of 15E11 ions/cm^2 at 25 keV, with implantation angle of 7° and flat side turned 22° north east.
- *Cleaning line:* photoresist removal using O_2 plasma, and RCA cleaning.
- *Threshold voltage adjustment - right half:* lithography by coating of 1.4 µm thick of Shipley SPR3012 positive photoresist, exposure at 140 mJ/cm^2, focus of 0, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s. After development, only the right half of the wafer remains free from photoresist.
- *Boron implantation:* implantation of B^+ with dose of 5E11 ions/cm^2 at 25 keV, with implantation angle of 7° and flat side turned 22° north east.
- *Cleaning line:* photoresist removal using O_2 plasma, and RCA cleaning.
- *Oxide stripping:* HF with 1:7 of selectivity and etch rate of 1.3±0.2 nm/s
- *RCA cleaning*
- *Marangoni:* native oxide removal using HF (0.55 %), rinsing with DI water, and drying using IPA for marangoni effect.
- *Annealing and oxidation:* dopant activation at 600 °C for 15 min using N_2 at 6.0 L/min and oxidation at 1000 °C for 10 min using O_2 at 2.25 L/min and H_2 at 3.85 L/min. The field oxide must be 100 nm thick on undoped regions and 220 nm in shallow-N-doped areas

A

Fabrication Protocol (Class ISO-7)—frontside wafer treatment

- *Cleaning line:* photoresist removal using O_2 plasma, and RCA cleaning.
- *Contact opening definition:* lithography by coating of 1.4 µm thick of Shipley SPR3012 positive photoresist, exposure at 150 mJ/cm^2, focus of 0, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *Oxide stripping:* BHF with 1:7 of selectivity and etch rate of 1.3±0.2 nm/s. **Very important:** the oxide in the SN regions is approximately 200 nm thick, whereas outside the SN regions is approximately 100 nm. Therefore, the required etching time for the CO-SN combination is about twice the time to obtain a hydrophobic backside of the wafer. Etching untill the CO windows in the SN areas are open.
- *Cleaning line:* photoresist removal using O_2 plasma, and RCA cleaning.
- *Marangoni:* native oxide removal using HF (0.55 %), rinsing with DI water, and drying using IPA for marangoni effect. **Note:** Immediately after marangoni, metallization must be performed.
- *1st metal:* sputtering 99 % Al and 1 % Si at 300 °C with 100 sccm of Ar flow to deposit 200 nm thick layer.
- *M1 definition:* lithography by coating of 1.4 µm thick of Shipley SPR3012 positive photoresist, exposure at 140 mJ/cm^2, focus of 0, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *Plasma etch aluminum:* plasma etching using HBr/Cl_2 at 25 °C to etch 200 nm of aluminum.
- *Aluminum fence removal*: Etching for 30 s using H_3PO_4 at 85 %, HNO_3 at 65 %, CH_3COOH at 100 %, and DI water.
- *Cleaning line:* photoresist removal using O_2 plasma, and RCA cleaning.
- *PECVD oxide:* deposition of 2000 nm of SiO_2.
- *M1 definition:* lithography by coating of 2.1 µm thick of Shipley SPR3012 positive photoresist, exposure at 230 mJ/cm^2, focus of 0, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *Plasma etch oxide:* plasma etching using C_2F_6/CHF_3, with soft landing on aluminum, to etch 2000 nm of SiO_2. Initial power of 300 W, then reduced to 100 W. Test wafers must be used to calculate etch rate.
- *Cleaning line:* photoresist removal using O_2 plasma, and RCA cleaning.
- *2nd metal:* sputtering 99 % Al and 1 % Si at 300 °C with 100 sccm of Ar flow to deposit 2075 nm thick layer.

Fabrication Protocol (Class ISO-7)—frontside wafer treatment

- *M2 definition:* lithography by coating of 3.1 µm thick of Shipley SPR3012 positive photoresist, exposure at 230 mJ/cm^2, focus of −1, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *Plasma etch aluminum:* plasma etching using HBr/Cl_2 at 25 °C to etch 2075 nm of aluminum.
- *Aluminum fence removal*: Etching for 30 s using H_3PO_4 at 85 %, HNO_3 at 65 %, CH_3COOH at 100 %, and DI water.
- *Cleaning line:* photoresist removal using O_2 plasma, and RCA cleaning.
- *Alloying:* alloying for 400 °C for 20 min using N_2 at 3.0 L/min and H_2 at 0.3 L/min.

Fabrication Protocol (Class ISO-7 and SAL)—backside wafer treatment

- *PECVD oxide:* deposition of SiO_2 on the backside of the wafer. The time is approximately 75 s. This step is the hardmask for the DRIE and the definition of the dogbone shapes of the organ-on-chip device.
- *Dogbone definition - oxide:* lithography by coating on the backside of the wafer 4.0 µm thick of Shipley SPR3027 positive photoresist, exposure at 600 mJ/cm^2, focus of −1, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s. The box is Cyto CM1 IMG3, the mask name is 2x2, the alignment on stepper is Backside_4 with number of alignments equals 2.
- *Plasma etch oxide:* plasma etching using C_2F_6/CHF_3. Use the StdOx for 6 min plus another 6 min to avoid burning the photoresist.
- *PDMS preparation:* 10:1 of monometer of PDMS and curing agent. Note: 6–7 g per wafer. Weight first the monomer then the curing agent. Then weight both together with the case to calibrate the machine. The recipe used was xpdms15um. Hence, 15 µm of thin-film PDMS is spin coated on top of the wafer.

A

Fabrication Protocol (Class ISO-7 and SAL)—backside wafer treatment

- *Extra resist bake:* 1 h in the oven at 90 °C for extra resist bake.
- *Aluminum sputtering:* sputtering 300 nm of aluminum silicide on top of the PDMS membrane. The recipe used was AlSi-300nm-25C-PDMS.
- *Spray coating:* coating 3 µm of thick photoresist on frontside of the wafer for protection purposes.
- *Dogbone definition - PDMS:*lithography by coating on the backside of the wafer 1.5 µm thick of negative photoresist, curing for 30 min at 90 °C on the oven, exposure at 110 mJ/cm^2, focus of 0, cross-link bake for 90 s at 115 °C, manual development with Shipley MF322 for 60 s. The box is EC2289, the mask name is 2x2, CYTOCM4 - IM4 - WO/EDGE, CYTOCM4 - IM4 - EDGE, the alignment on stepper is Backside_4.
- *PDMS etching:* plasma etching for 10 min to etch 7.5 µm of PDMS. The etch rate is 0.75 µm/min. Use dummy wafers for testing the etch rate.
- *DRIE:* deep reactive ion etching to create the cavities. Number of loops equals 350. The recipe used was UEKL_Speed_20C_XXX
- *Spray coater:* coating 3 µm of photoresist on top of frontside wafer with the vaccuum chuck on the edges.
- *Curing:* 30 min
- *Triton X 100 metals special etching line (SAL):* 10–15 min to remove the 2 µm of oxide.
- *Oxide removal:* BHF 1:7 to remove SiO_2 on the back.
- *Rinsing with DI water + acetone for* 1 min
- *Rinsing with DI water for* 5 min
- *PES:* removal of aluminum. Note: the PDMS must be transparent. Time must be checked with dummy wafers.
- *Rinsing with DI water for* 5 min
- *Drying wafers*

B

Appendix B: process flow for BiFET-based artifact-resilient optrodes

BIFET-BASED ARTIFACT-RESILIENT OPTRODES FOR INFRASLOW BRAIN ACTIVITY MEASUREMENTS IN OPTOGENETICS

Fabrication Protocol (Class ISO-7)—frontside wafer treatment

- *Substrate:* single-side polished, <100>-oriented crystalline silicon, p-type, boron, 0.01–0.02 $\Omega \cdot$ cm, 100±0.3 µm of device thickness, 350±10 µm of device thickness, 2 µm±5 % of BOX thickness, 2 µm of thick oxide on the backside, 100 mm of diameter.
- *Epitaxy:* growing 4.5 µm of boron-doped epitaxial film on the frontside, with concentration of 1.0E16 atoms/cm^3 at 1050 °C and 60 torr.
- *Marker oxidation:* oxidation at 1100 °C for 38.5 min using O_2 at 2.25 L/min and H_2 at 3.85 L/min to grow 500 nm of thick oxide.
- *Fiducial markers definition:* lithography by coating of 1.4 µm thick of Shipley SPR3012 positive photoresist, exposure at 150 mJ/cm^2, focus of 0, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *Window etching:* BHF 1:7 to create fiducials on the SiO_2. Etching time is approximately 6.5 min.
- *Cleaning procedure:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for 10 min and HNO_3 65 % at 110 °C for 10 min, rinse with DI water, drying).
- *Marker oxidation:* oxidation at 1100 °C for 38.5 min using O_2 at 2.25 L/min and H_2 at 3.85 L/min to grow 750 nm of thick oxide.
- *BN definition:* lithography by coating of 1.4 µm thick of Shipley SPR3012 positive photoresist, exposure of mask BN at 150 mJ/cm^2, focus of 0, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *Window etching:* BHF 1:7 to create fiducials on the SiO_2. Etching time is approximately 10.5 min.
- *Cleaning procedure:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for 10 min and HNO_3 65 % at 110 °C for 10 min, rinse with DI water, drying).
- *Marangoni:* native oxide removal using HF (0.55 %), rinsing with DI water, and drying using IPA for marangoni effect.
- *Dry oxidation:* oxidation at 950 °C for 35 min using O_2 at 3.0 L/min

Fabrication Protocol (Class ISO-7)—frontside wafer treatment

- *Arsenic implantation:* implantation of As^- with dose of 5.0E15 ions/cm^2 at 180 keV, with implantation angle of 7° and flat side turned 22° north east.
- *Implanted oxide stripping:* HF (0.55 %) for 4 min.
- *Cleaning procedure:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for 10 min and HNO_3 65 % at 110 °C for 10 min, rinse with DI water, drying).
- *Oxidation & annealing:* dopant activation at 600 °C for 20 min using N_2 at 3.0 L/min and oxidation at 1000 °C for 30 min using O_2 at 2.25 L/min. Oxide thickness is 65 nm above the BN area.
- *Oxide stripping:* BHF (1:7) with etch rate of 1.3±0.2 nm/s. Etching until surface is hydrophobic.
- *Cleaning procedure:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for 10 min and HNO_3 65 % at 110 °C for 10 min, rinse with DI water, drying).
- *Marangoni:* native oxide removal using HF (0.55 %), rinsing with DI water, and drying using IPA for marangoni effect.
- *Epitaxy:* growing 300 nm of intrinsic silicon and 700 nm of arsenic-doped epitaxial film on the frontside, with concentration of 1.0E16 atoms/cm^3 at 1050 °C and 60 torr.
- *Wet oxidation:* oxidation at 850 °C for 20 min using O_2 at 2.25 L/min and H_2 at 3.85 L/min to grow 300 Å of thick oxide.
- *DP (deep plug) definition:* lithography by coating of 2.3 µm thick of Shipley SPR3012 positive photoresist, exposure the mask DP at 250 mJ/cm^2, focus of 0, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *Extra resist bake:* baking the wafers at 110 °C for 30 min, and then increase the temperature to 130 °C for the next 30 min.
- *Boron implantation:* implantation of B^+ with dose of 5.0E15 ions/cm^2 at 180 keV, with implantation angle of 7° and flat side turned 22° north east.
- *Cleaning procedure:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for 10 min and HNO_3 65 % at 110 °C for 10 min, rinse with DI water, drying).

B

Fabrication Protocol (Class ISO-7)—frontside wafer treatment

- *DN (deep Nplug) definition:* lithography by coating of 2.3 µm thick of Shipley SPR3012 positive photoresist, exposure the mask DN at 250 mJ/cm^2, focus of 0, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *Extra resist bake:* baking the wafers at 110 °C for 30 min, and then increase the temperature to 130 °C for the next 30 min.
- *Phosphorus implantation:* implantation of P^- with dose of 5.0E15 ions/cm^2 at 180 keV, with implantation angle of 7° and flat side turned 22° north east.
- *Cleaning procedure:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for 10 min and HNO_3 65 % at 110 °C for 10 min, rinse with DI water, drying).
- *LP (low ohmic extrinsic base) definition:* lithography by coating of 1.4 µm thick of Shipley SPR3012 positive photoresist, exposure the mask LP at 150 mJ/cm^2, focus of 0, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *Boron implantation:* implantation of B^+ with dose of 3.0E15 ions/cm^2 at 15 keV, with implantation angle of 7° and flat side turned 22° north east.
- *Cleaning procedure:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for 10 min and HNO_3 65 % at 110 °C for 10 min, rinse with DI water, drying).
- *LB1 (base-link) definition:* lithography by coating of 1.4 µm thick of Shipley SPR3012 positive photoresist, exposure the mask LB1 at 150 mJ/cm^2, focus of 0, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *Boron implantation:* use six processing wafers to implant B^+ with dose of 1.1E14 ions/cm^2 at 11 keV, and other six processing wafers to implant B^+ with dose of 8.0E13 ions/cm^2 at 15 keV with implantation angle of 7° and flat side turned 22° north east.
- *Cleaning procedure:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for 10 min and HNO_3 65 % at 110 °C for 10 min, rinse with DI water, drying).
- *LB2 (p-channel) definition:* lithography by coating of 1.4 µm thick of Shipley SPR3012 positive photoresist, exposure the mask LB2 at 150 mJ/cm^2, focus of 0, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.

Fabrication Protocol (Class ISO-7)—frontside wafer treatment

- *Boron implantation:* implanting B^+ with dose of 4.5E12 ions/cm^2 at 40 keV with implantation angle of 7° and flat side turned 22° north east.
- *Cleaning procedure:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for 10 min and HNO_3 65 % at 110 °C for 10 min, rinse with DI water, drying).
- *Low-stress oxide deposition:* LPCVD using SiH_2Cl_2/NH_3 at 169.5/30.5 sccm to deposit 300 nm of thick silicon nitride. If LPCVD is not available, then deposit TEOS.
- *CO (contact opening) definition:* lithography by coating of 1.4 µm thick of Shipley SPR3012 positive photoresist, exposure the mask CO at 150 mJ/cm^2, focus of 0, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *RIE etching nitride + oxide (contact windows):* etching the nitride using C_2F_6 at 65 sccm, pressure of 130 mtorr, and RF power of 250 W. Etching the oxide using C_2F_6/CHF_3 at 36/144 sccm, pressure of 180 mtorr, and RF power of 300 W. Use dummy wafers to measure the etch rate. The nitride etch rate must be 6.5 nm/s.
- *Cleaning procedure:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for 10 min and HNO_3 65 % at 110 °C for 10 min, rinse with DI water, drying).
- *WN (emitter and collector plug) definition:* lithography by coating of 1.4 µm thick of Shipley SPR3012 positive photoresist, exposure the mask WN at 150 mJ/cm^2, focus of 0, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *Oxide dip etch:* HF (0.55 %) for 4 min.
- *Arsenic implantation:* implantation of As^- with dose of 7.5E15 ions/cm^2 at 40 keV, with implantation angle of 7° and flat side turned 22° north east.
- *Cleaning procedure:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for 10 min and HNO_3 65 % at 110 °C for 10 min, rinse with DI water, drying).
- *NWN (intrinsic base) definition:* lithography by coating of 1.4 µm thick of Shipley SPR3012 positive photoresist, exposure the mask NWN at 150 mJ/cm^2, focus of 0, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.

Fabrication Protocol (Class ISO-7)—frontside wafer treatment

- *Boron implantation:* implanting B^+ with dose of 1.4E14 ions/cm^2 at 20 keV with implantation angle of 7° and flat side turned 22° north east.
- *Cleaning procedure:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for 10 min and HNO_3 65 % at 110 °C for 10 min, rinse with DI water, drying).
- *Annealing in argon gas:* annealing at 950 °C for 20 min using argon at 3.0 L/min. Note: do not use dummy wafers between the process wafers because they are heavily doped.
- *Oxide dip etch:* HF (0.55 %) for 4 min.
- *1st metal:* sputtering of aluminum silicide with 99 % Al and 1 % Si, at 350 °C with 100 sccm of Ar flow to deposit 675 nm of thick layer. The chuck temperature is at 350 °C.
- *IC definition:*lithography by coating of 1.4 µm thick of Shipley SPR3012 positive photoresist, exposure mask IC at 140 mJ/cm^2, focus of 0, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *Plasma etch aluminum:* plasma etching using HBr/Cl_2 at 25 °C to etch 600–1000 nm of aluminum.
- *Cleaning procedure:* photoresist removal using O_2 plasma
- *Aluminum fence removal*: Etching for 30 s using H_3PO_4 at 85 %, HNO_3 at 65 %, CH_3COOH at 100 %, and DI water.
- *Cleaning procedure:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for metal for 10 min, rinse with DI water, drying).
- *PECVD oxide:* deposition of 800 nm of SiO_2.
- *Back etch plasma (spacer formation):* etching the oxide using C_2F_6/CHF_3 at 36/144 sccm, pressure of 180 mtorr, and RF power of 300 W. Use dummy wafers to measure the etch rate.
- *PECVD oxide:* deposition of 600 nm of SiO_2.
- *CT definition:*lithography by coating of 2.1 µm thick of Shipley SPR3012 positive photoresist, exposure mask IC at 230 mJ/cm^2, check the focus, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.

Fabrication Protocol (Class ISO-7)—frontside wafer treatment

- *PECVD oxide window etching:* etching the bulk oxide using C_2F_6/CHF_3 at 36/144 sccm, pressure of 180 mtorr, and RF power of 300 W, and then reduce the power to 100 W. Use dummy wafers to measure the etch rate.
- *Cleaning procedure:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for metal for 10 min, rinse with DI water, drying).
- *2^{nd} metal:* sputtering of aluminum silicide with 99 % Al and 1 % Si, at 350 °C with 100 sccm of Ar flow to deposit 1475 nm of thick layer. The chuck temperature is at 350 °C.
- *IN definition:*lithography by coating of 2.1 µm thick of Shipley SPR3012 positive photoresist, exposure mask IN at 300 mJ/cm^2, focus of −1, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *Plasma etch aluminum:* plasma etching using HBr/Cl_2 at 25 °C to etch 1400–1700 nm of aluminum.
- *Cleaning procedure:* photoresist removal using O_2 plasma.
- *Aluminum fence removal*: Etching for 30 s using H_3PO_4 at 85 %, HNO_3 at 65 %, CH_3COOH at 100 %, and DI water.
- *Cleaning procedure:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for metal for 10 min, rinse with DI water, drying).
- *PECVD silicon nitride:* deposition of 800 nm of silicon nitride using $N_2/SiH_4/NH_3$ at 1000/280/1800 sccm.
- *VIA definition:*lithography by coating of 2.1 µm thick of Shipley SPR3012 positive photoresist, exposure mask VIA at 230 mJ/cm^2, check the focus, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *PECVD-nitride window etching:* etching the nitride for 90 s using C_2F_6 at 65 sccm, pressure of 130 mtorr, and RF power of 250 W, then reduce the power to 100 W and etch for more 60 s. Use dummy wafers to measure the etch rate.
- *Cleaning procedure:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for metal for 10 min, rinse with DI water, drying).
- *3^{rd} metal:* sputtering of aluminum at 350 °C with 100 sccm of Ar flow to deposit 1475 nm of thick layer and titanium nitride to deposit 375 nm of thick layer. The chuck temperature is at 350 °C.

Fabrication Protocol (Class ISO-7)—frontside wafer treatment

- *TIN definition:* lithography by coating of 2.1 µm thick of Shipley SPR3012 positive photoresist, exposure mask TIN at 230 mJ/cm^2, check the focus, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *Plasma etch titanium nitride:* plasma etching titanium nitride.
- *Cleaning procedure:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for metal for 10 min, rinse with DI water, drying).
- *AL definition:* lithography by coating of 2.1 µm thick of Shipley SPR3012 positive photoresist, exposure mask AL at 230 mJ/cm^2, check the focus, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *Plasma etch aluminum:* plasma etching using HBr/Cl_2 at 25 °C to etch the aluminum.
- *PECVD silicon nitride:* deposition of 800 nm of silicon nitride using $N_2/SiH_4/NH_3$ at 1000/280/1800 sccm.
- *CT2 definition:* lithography by coating of 2.1 µm thick of Shipley SPR3012 positive photoresist, exposure mask CT2 at 230 mJ/cm^2, check the focus, development with Shipley MF322 with a single puddle process, and hard bake at 100 °C for 90 s.
- *PECVD-nitride window etching:* etching the nitride for 90 s using C_2F_6 at 65 sccm, pressure of 130 mtorr, and RF power of 250 W, then reduce the power to 100 W and etch for more 60 s. Use dummy wafers to measure the etch rate.
- *Alloying:* alloying at 400 °C for 20 min using N_2 at 3.0 L/min and H_2 at 0.3 L/min.

Fabrication Protocol (Class ISO-7)—backside wafer treatment

- *RIE definition:* lithography by coating of 12 µm thick of positive photoresist, wait 1 h for rehydration of the photoresist, exposure mask RIE at correct exposure dose (approximately 1200 mJ^2/cm), check the focus, wait 1 h for the reaction time, post-exposure baking for 90 s at 115 °C on the hotplate, manual development with Shipley MF322 for approximately 180 s, and hard bake at 100 °C for 90 s.
- *PECVD oxide window etching:* etching the bulk oxide using C_2F_6/CHF_3 at 36/144 sccm, pressure of 180 mtorr to etch 2000 nm of thick oxide on the backside of the wafer. Use dummy wafers to measure the etch rate.
- *DRIE:* deep reactive ion etching to etch 20–40 µm of silicon to create the trenches for the optrodes' shapes. The recipe used was EKL Smooth @ 20C.
- *Cleaning procedure:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for metal for 10 min, rinse with DI water, drying).
- *RIE2 definition:* lithography by spray coating 12 µm of thick **negative photoresist** using the AZ Nlof 2070, cross-link baking at 115 °C for 90 s, wait 1 h for rehydration of the photoresist, exposure mask RIE2 at correct exposure dose (approximately 1200 mJ^2/cm), check the focus, wait 1 h for the reaction time, post-exposure baking for 90 s at 115 °C on the hotplate, manual development with Shipley MF322 for approximately 180 s, and hard bake at 100 °C for 90 s.
- *DRIE:* deep reactive ion etching to etch the silicon until it lands on the BOX. The recipe used was EKL Smooth @ 20C.
- *Frontside passivation:* lithography by coating 2 µm of thick **negative photoresist**, cross-link baking at 115 °C for 90 s.
- *BOX window etching:* BHF (1:7) with etch rate of 1.3 ± 0.2 nm/s. Etching until the BOX is removed and the device layer is exposed. A SEM inspection must be performed.
- *DRIE:* last deep reactive ion etching to release the optrodes. The recipe used was EKL Smooth @ 20C. Note 1: use carrier wafer with polymide tapes on the sides for landing. Note 2: Take care of the temperature of the chuck. Note 3: Use dummy wafers always.
- *Cleaning procedure:* photoresist removal using O_2 plasma, and RCA cleaning (HNO_3 100 % for metal for 10 min, rinse with DI water, drying).
- *Boxing:* transport the wafers outside the cleanroom for sysmte-level integration.

C

APPENDIX C: OPTRODES' DESIGNS FOR MULTIPLE NEUROSCIENTIFIC STUDIES

This appendix overviews the various layouts developed for optogenetic studies. Next in line are some general remarks regarding these layouts.

First, the width of all optrode shafts measures 190 µm. Second, the common-mode biasing uses the ground electrode. On the other hand, the reference electrode offers an optional feature for referential measurements, i.e., a measurement between a DM unit and the reference electrode. Third, some designs incorporate a ground electrode extending to the tip of each shank, which allows for a better study of how the common-mode feedback biasing manifests itself: locally or globally. Finally, all designs include in-situ bond pads for the hybrid integration of at least one µLED.

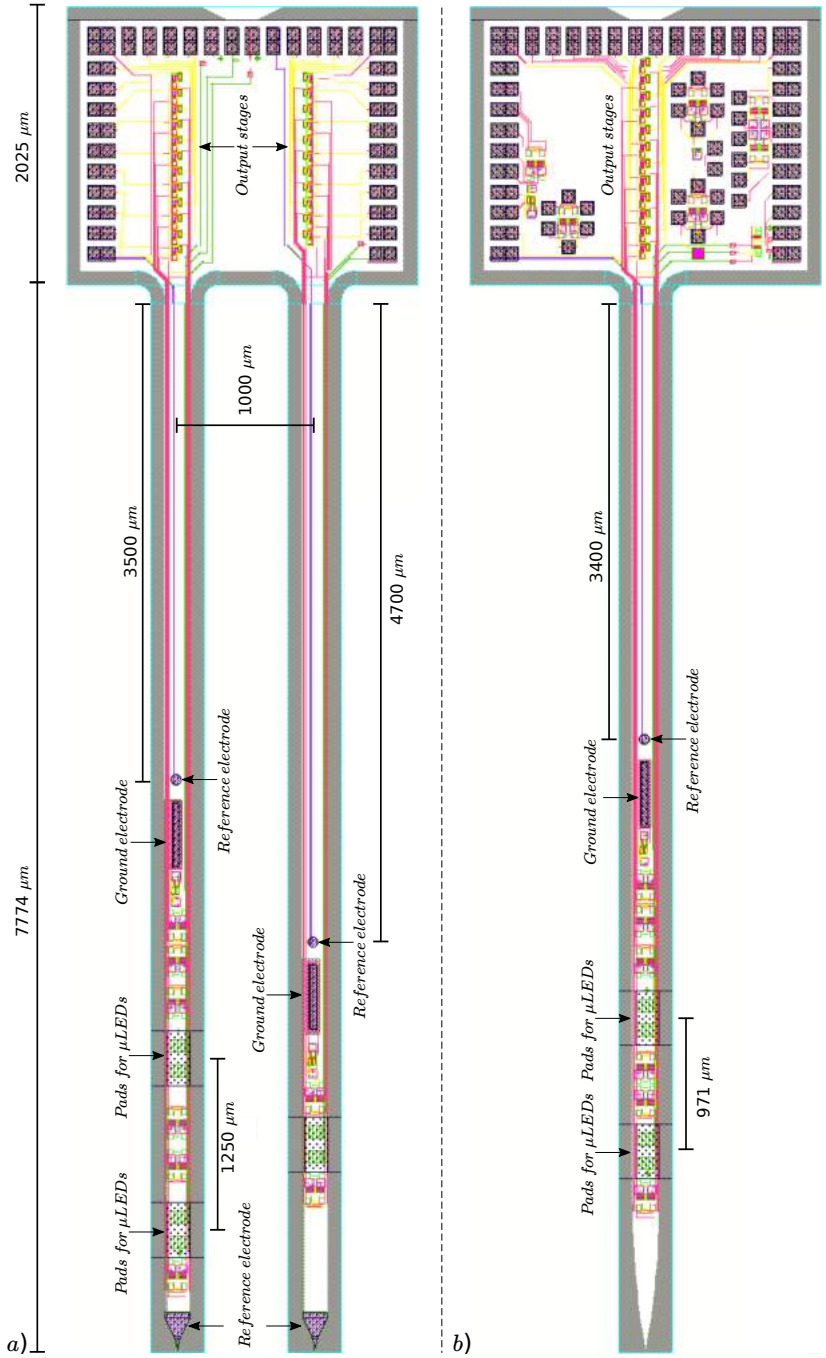

Figure C.1: The optrode shown in a) comprises two shanks: the left shank includes six DM units, one CM unit, and bond pads for two µLEDs; the right shank includes two DM units, one CM unit, and bond pads for one µLED. The optrode shown in b) includes six DM units, one CM unit, and bond pads for two µLEDs. Important to notice the different physical designs of the optrode's tip for better studies on tissue perforation and mechanical stability.

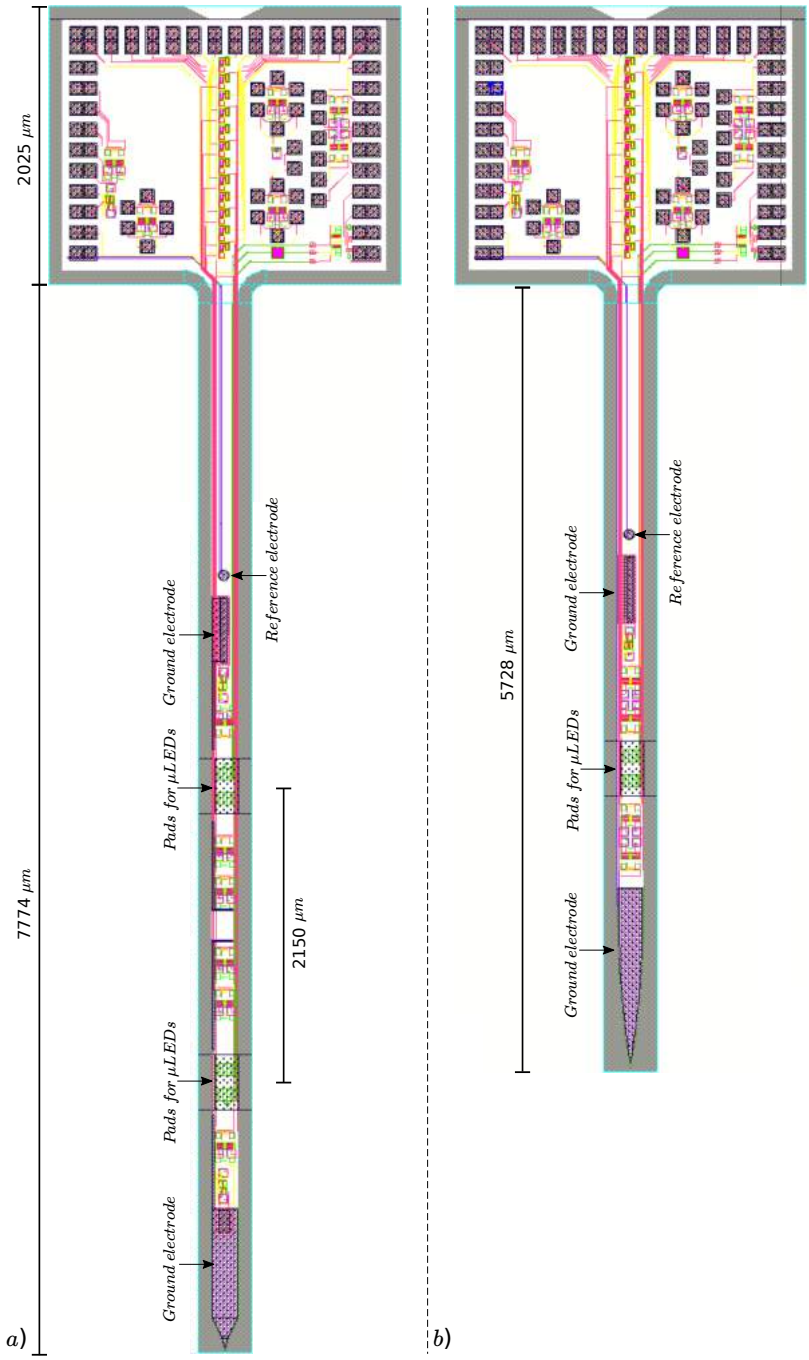

Figure C.2: The optrode shown in a) includes six DM units, two CM units, and bond pads for two µLEDs. The optrode shown in b) includes two DM units in tetrode configuration, one CM unit, and bond pads for one µLED. Important to notice the different physical designs of the optrode's tip for better studies on tissue perforation and mechanical stability.

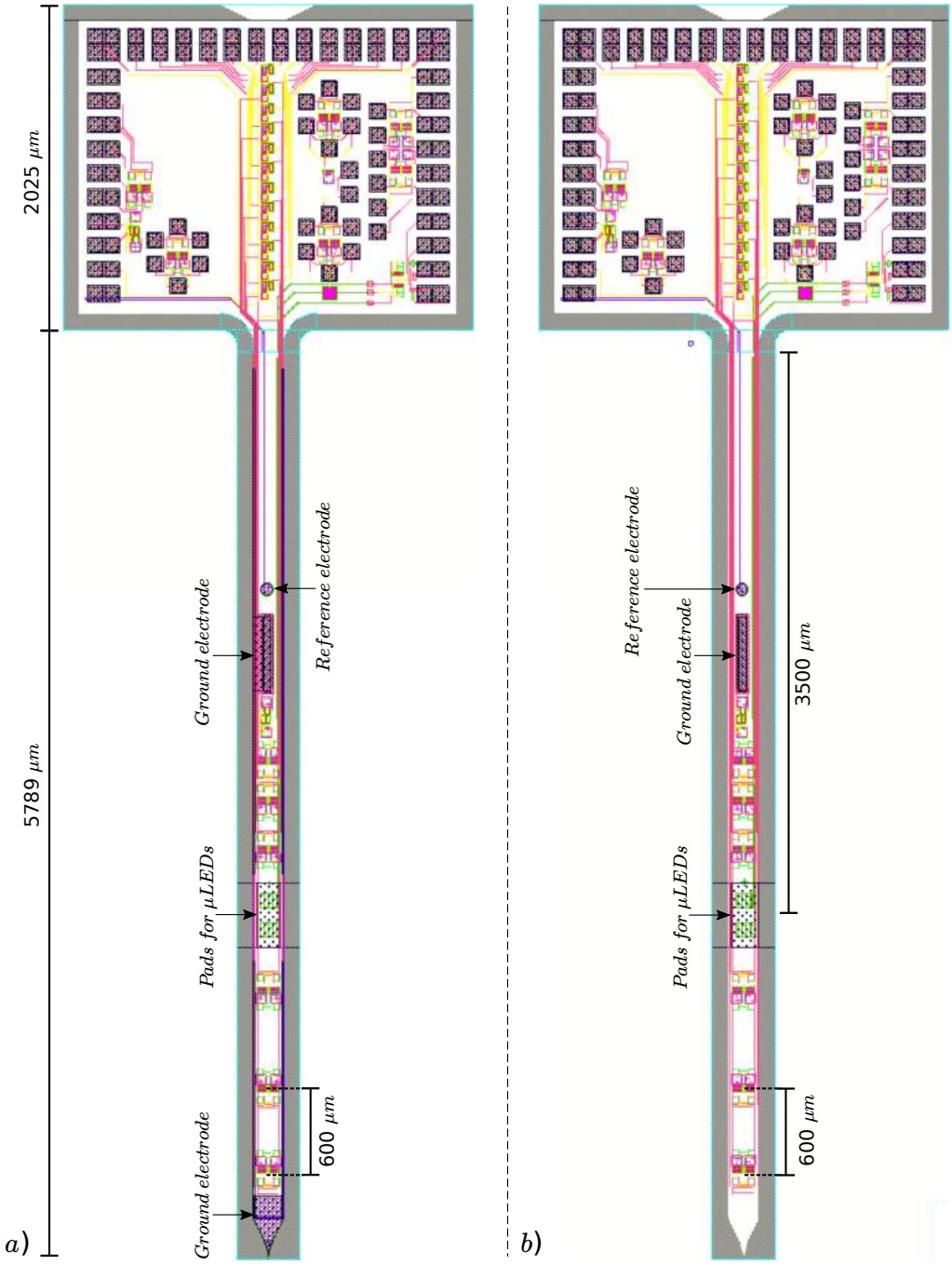

Figure C.3: The optrode shown in a) includes six DM units, one CM unit, and bond pads for one µLEDs. The optrode shown in b) includes six DM units, one CM unit, and bond pads for one µLED.

D

APPENDIX D: SPICE MODELS

This appendix presents a list of the SPICE models derived from the BiCMOS7 and the DIMES03 process utilized during the circuit analysis and simulation.

BICMOS7 SPICE MODELS

NPN

```
*************************************************************
*  Level-3 Model for BJT NW 3um
*************************************************************
.model DIMES6NW3um NPN (IS=9E-16 NF=0.9919 BF=200 IKF=0.003 VAF=12
+  ISE=3.03E-15 NE=2.5 NR=1.0 BR=50 IKR=3.9E-3 VAR=3
+  ISC=1.6E-17 NC=1.46 RB=17 RE=9 RC=6
+  CJC=988E-15 CJE=1E-12 MJC=0.306 MJE=0.552
+  VJC=0.554 VJE=0.931 TF=600E-12 TR=3E-9 Vceo=15 Icrating=5)
*Reverse knee current (IKR) is IKR=3.9E-11
```

NMOS

```
.model  delftnmos  nmos  level = 49
*************************************************************
*               MODEL FLAG PARAMETERS
*************************************************************
+lmin    = 2e-006          lmax    = 20e-005         wmin    = 5e-006
+wmax    = 60e-005         nqsmod  = 0               binflag = 0
+version = 3.2             mobmod  = 1               capmod  = 0
+binunit = 1               stimod  = 0               paramchk= 0
+vfbflag = 0               hspver  = 2000.2          lref    = 1e+020
+wref    = 1e+020
*************************************************************
*               GENERAL MODEL PARAMETERS
*************************************************************
+tref    = 25              xl      = 0               xw      = 0
+wmlt    = 1               ld      = 0               llc     = 0
+lwlc    = 0               wlc     = 0               wwc     = 0
+tox     = 1e-007          toxm    = 1e-007          wl      = 0
+hdif    = 0               ldif    = 0               ll      = 0
+lln     = 1               wln     = 1               lw      = 0
+lwn     = 1               wwn     = 1               lwl     = 0
+cgbo    = 0               xpart   = 1               lmlt    = 1
+lwc     = 0               wwlc    = 0               wwl     = 0
+ww      = 0               wint    = -1.3000878e-006
+lint    = 3.9931632e-007
*************************************************************
*               EXPERT PARAMETERS
*************************************************************
+vth0    = 1.96            k1      = 1.5961015       k2      = -0.06
+k3b     = -7.113511       nlx     = 0               vbm     = -3
+dvt1    = 0.66823344      dvt2    = -0.031099273    elm     = 5
+dvt2w   = 0               nch     = 2.0064e+016     delta   = 0.01
```

```
+cdsc     = 0               cdscb    = -0.00029430785  cdscd    = 0
+u0       = 0.059608        ua       = 2.1677e-009     prwg     = 0
+ngate    = 0               xj       = 1.5e-007        w0       = 0
+prwb     = 0               wr       = 1               rdsw     = 0
+ags      = 0.1             a1       = 0.01            a2       = 1
+b1       = 5.9928421e-005  vsat     = 122774.2        pscbe2   = 8e-006
+dwb      = -3.6919843e-007 alpha0   = 0               beta0    = 30
+pdiblc1  = 0.16938795      pdiblc2  = 0               pdiblcb  = 1
+pvag     = 0.70000716      pscbe1   = 4.24e+008
+eta0     = 0               etab     = -0.010129428
+alpha1   = 0               k3       = 15.919406
+dvt0     = 2.4481878       dwg      = -4.3070327e-007
+dvt1w    = 45899.231       pclm     = 15.252
+nfactor  = 4.9835838       drout    = 0.49848551
+cit      = 0.0003107754    a0       = 0.6105386
+uc       = -2.9295e-011    ub       = 4.4958e-019
+b0       = 3.6195968e-006  dvt0w    = 0.88173932
+voff     = -7.8096268      keta     = 0.068470003
+dsub     = 0.016400197     dvt0     = 2.4481878

*****************************************************************
*               CAPACITANCE PARAMETERS
*****************************************************************
+clc      = 1e-007          cle      = 0.6             ckappa   = 0.6
+cgsl     = 0               vfbcv    = -1              acde     = 1
+noff     = 1               voffcv   = 0               cgdl     = 0
+moin     = 15
*****************************************************************
*               TEMPERATURE PARAMETERS
*****************************************************************
+kt1      = -0.11           kt1l     = 0               kt2      = 0.022
+ua1      = 4.31e-009       ub1      = -7.61e-018
+at       = 33000           ute      = -1.5
+uc1      = -5.6e-011       prt      = 0
*****************************************************************
*               NOISE PARAMETERS
*****************************************************************
+noimod   = 1               noia     = 1e+020          noib     = 50000
+em       = 41000000        af       = 1               ef       = 1
+gdsnoi   = 1               noic     = -1.4e-012       kf       = 0
*****************************************************************
*               DIODE PARAMETERS
*****************************************************************
+rsh      = 20              js       = 0.0001          jsw      = 0
+mj       = 0.5             cjsw     = 5e-010          mjsw     = 0.33
```

```
+rd      = 52              rdc     = 2.3             rs      = 52
+xti     = 3               acm     = 0               calcacm = 0
+pbsw    = 1               tt      = 0               ijth    = 0.1
+tcj     = 0               tcjsw   = 0               tcjswg  = 0
+tpbsw   = 0               tpbswg  = 0               tpb     = 0
+nrd     = 1               nrs     = 1               cj      = 0.0005
+pb      = 1               rsc     = 2.3             nj      = 1
*************************************************************
*               STRESS PARAMETERS
*************************************************************
+sa0     = 1e-006          sb0     = 1e-006          wlod    = 0
+lkvth0  = 0               wkvth0  = 0               pkvth0  = 0
+wlodvth = 0               stk2    = 0               lodk2   = 1
+ku0     = 0               lku0    = 0               wku0    = 0
+llodku0 = 0               wlodku0 = 0               kvsat   = 0
+tku0    = 0               llodvth = 0               lodeta0 = 1
+kvth0   = 0               pku0    = 0               steta0  = 0
```

D

PMOS

```
.model  delftpmos  pmos  level = 49
*************************************************************
*               MODEL FLAG PARAMETERS
*************************************************************
+lmin    = 2e-006          lmax    = 20e-005         wmin    = 5e-006
+version = 3.2             mobmod  = 1               capmod  = 0
+binunit = 1               stimod  = 0               paramchk= 0
+vfbflag = 0               hspver  = 2000.2          lref    = 1e+020
+wmax    = 60e-005         nqsmod  = 0               binflag = 0
+wref    = 1e+020
*************************************************************
*               GENERAL MODEL PARAMETERS
*************************************************************
+tref    = 25              xl      = 0               xw      = 0
+wmlt    = 1               ld      = 0               llc     = 0
+lwlc    = 0               wlc     = 0               wwc     = 0
+tox     = 1e-007          toxm    = 1e-007          wwl     = 0
+hdif    = 0               ldif    = 0               lw      = 0
+lln     = 2.5             wln     = 1               lmlt    = 1
+lwn     = 1               wwn     = 1               ww      = 0
+cgbo    = 0               xpart   = 1               wwlc    = 0
+lwc     = 0               ll      = 1.6449227e-020
+wl      = 1e-015          lint    = 3.2459148e-007
+wint    = -1.3583817e-006 lwl     = -4.335301e-025
```

```
**************************************************************
*               EXPERT PARAMETERS
**************************************************************
+vth0     = -2.54           k1       = 2               k2       = 0.1
+k3b      = 1.5463811       nlx      = 0               vbm      = -3
+dvt1     = 0.536           dvt2     = -0.032          elm      = 5
+dvt2w    = -0.2            nch      = 8e+016          pclm     = 3.195
+cdsc     = 0.01597564      cdscb    = -0.1            cdscd    = 0
+u0       = 0.017846        ua       = 1.8415e-009     a0       = 0.5
+ngate    = 0               xj       = 4.6e-007        w0       = 0
+prwb     = -0.028211283    wr       = 0.7             delta    = 0.01
+ags      = 0.1             a1       = 0.01            a2       = 0.02
+b1       = 1.2504217e-006  vsat     = 52679.704       keta     = 0.1
+dwb      = -4.1366432e-007 alpha0   = 0               beta0    = 30
+pdiblc1  = 0.68160706      pdiblc2  = 0               pdiblcb  = 1
+pvag     = -1.9536318      pscbe1   = 4.24e+008       pscbe2   = 8e-006
+eta0     = 0.08            etab     = -0.07           dsub     = 0.56
+alpha1   = 0               k3       = -13.253466      dvt0     = 0
+dvt1w    = 18770           nfactor  = 3.642875
+uc       = -2.4756e-011    prwg     = -0.049069067
+b0       = 0               dwg      = 1.0392951e-007
+drout    = 0.12940028      cit      = 0.0003107754
+dvt0w    = 0.43812687      voff     = -0.36055378
+ub       = -5.2209e-018    rdsw     = 7038.7379

**************************************************************
*               CAPACITANCE PARAMETERS
**************************************************************
+clc      = 1e-007          cle      = 0.6             ckappa   = 0.6
+cgsl     = 0               vfbcv    = -1              acde     = 1
+noff     = 1               voffcv   = 0               cgdl     = 0
+moin     = 15
**************************************************************
*               TEMPERATURE PARAMETERS
**************************************************************
+kt1      = -0.11           kt1l     = 0               kt2      = 0.022
+ua1      = 4.31e-009       ub1      = -7.61e-018      uc1      = -5.6e-011
+at       = 33000           prt      = 0               ute      = -1.5
**************************************************************
*               NOISE PARAMETERS
**************************************************************
+noimod   = 1               noia     = 1e+020          noib     = 50000
+em       = 41000000        af       = 1               ef       = 1
+gdsnoi   = 1               noic     = -1.4e-012       kf       = 0
**************************************************************
```

```
*                DIODE PARAMETERS
************************************************************
+rsh      = 500              js       = 0.0001          jsw      = 0
+mj       = 0.5              cjsw     = 5e-010          mjsw     = 0.33
+rd       = 0                rdc      = 17              rs       = 0
+xti      = 3                acm      = 10              calcacm  = 0
+pbsw     = 1                tt       = 0               ijth     = 0.1
+tcj      = 0                tcjsw    = 0               tcjswg   = 0
+tpbsw    = 0                tpbswg   = 0               pb       = 1
+nrd      = 1                nrs      = 1               cj       = 0.0005
+rsc      = 17               nj       = 1               tpb      = 0
************************************************************
*                STRESS PARAMETERS
************************************************************
+sa0      = 1e-006           sb0      = 1e-006          wlod     = 0
+lkvth0   = 0                wkvth0   = 0               pkvth0   = 0
+wlodvth  = 0                stk2     = 0               lodk2    = 1
+ku0      = 0                lku0     = 0               wku0     = 0
+llodku0  = 0                wlodku0  = 0               kvsat    = 0
+tku0     = 0                kvth0    = 0               llodvth  = 0
+lodeta0  = 1                pku0     = 0               steta0   = 0
```

DIMES03 SPICE MODELS

NPN —EMITTER AREA: 2×1 μm^2

```
.model npn2x1 npn
IS=6.1E-18 NC=1.6000 VJC=.4
BF=195 MJC=.2
NF=1.0080 RE=60 CJS=123E-15
VAF=45 RB=600 VJS=.5
IKF=10.000E-3 RC=250 MJS=.1
ISE=1.300E-18 RBM=100 TF=10E-12
NE=1.9000 IRB=8E-6 XTF=25
BR=9 CJE=11.0000E-15 VTF=2
VAR=1.6000 VJE=1 ITF=8.0000E-3
IKR=10.000E-3 MJE=.6 PTF=60
ISC=2.100E-18 CJC=16.0000E-15 TR=1.0000E-9

FOR PSPICE: NK=.57063
```

NPN —EMITTER AREA: 4×1 μm^2

```
.model npn4x1 npn
IS=12.200E-18    RE=30          CJS=138E-15
BF=195           RB=300         VJS=.5
NF=1.0080        RC=125         MJS=.1
VAF=45           RBM=50
IKF=16.000E-3    IRB=16E-6      XTF=25
ISE=2.6000E-18   CJE=20.000E-15 VTF=2
BR=9             VJE=1          ITF=16.00E-3
VAR=1.6000       MJE=.6         PTF=60
IKR=200.00E-6    CJC=22.000E-15 TR=1.0000E-9
ISC=4.2000E-18   VJC=.4
NC=1.6000        MJC=.2

FOR PSPICE: TP=9.0000E-12
```

NPN —EMITTER AREA: 8×1 μm^2

```
.model npn8x1 npn
IS=24.400E-18    RE=15          CJS=157E-15
BF=195           RB=150         VJS=0.5
NF=1.0080        RC=62          MJS=0.1
VAF=45           RBM=25         TF=8.0000E-12
IKF=32.000E-3    IRB=32E-6      XTF=50
ISE=5.2000E-18   CJE=38.000E-15 VTF=0.9
```

```
BR=9              VJE=1             ITF=32.000E-3
VAR=1.6000        MJE=0.6           PTF=60
IKR=400.00E-6     CJC=34.000E-15    TR=1.0000E-9
ISC=8.4000E-18    NC=1.6000         VJC=.4
MJC=0.2
```

NPN —EMITTER AREA: $16\times1\,\mu m^2$

```
.model npn16x1 npn
IS=48.800E-18     RE=8              CJS=196E-15
BF=195            RB=75             VJS=0.5
NF=1.0080         RC=31             MJS=0.1
VAF=45            RBM=12.5          TF=8.0000E-12
IKF=64.000E-3     IRB=64E-6         XTF=50
ISE=10.400E-18    CJE=72.000E-15    VTF=0.9
BR=9              VJE=1             ITF=64.000E-3
VAR=1.6000        MJE=.6            PTF=60
IKR=800.00E-6     CJC=56.000E-15    TR=1.0000E-9
ISC=16.800E-18    NC=1.6000         VJC=0.4MJC=0.2
MJC=0.2
```

NPN —EMITTER AREA: $32\times1\,\mu m^2$

```
.model npn32x1 npn
IS=97.600E-18     RE=4              CJS=235E-15
BF=195            RB=35             VJS=0.5
NF=1.0080         RC=15             MJS=0.1
VAF=45            RBM=6.25          TF=8.0000E-12
IKF=0.128         IRB=128E-6        XTF=50
ISE=20.800E-18    CJE=144.00E-15    VTF=0.9
BR=9              VJE=1             ITF=0.128
VAR=1.6000        MJE=0.6           PTF=60
IKR=1.6000E-3     CJC=96.000E-15    TR=1.0000E-9
ISC=33.600E-18    NC=1.6000         VJC=0.4
MJC=0.2
```

LATERAL PNP —EMITTER AREA: $30\times2\,\mu m^2$

```
.model lpnp30x2 pnp
IS=50.000E-18     VJS=0.5
BF=55             RE=25             MJS=0.1
NF=1.2000         RB=80             TF=2.0000E-9
VAF=20            RC=150            XTF=25
IKF=10.000E-6     CJE=65.000E-15    VTF=2
ISE=500.00E-18    VJE=0.67          ITF=6E-3
NE=2              MJE=0.34          PTF=60
```

```
BR=17              CJC=160.00E-15  TR=10.000E-9
VAR=10             VJC=0.7         EG=1.2000
IKR=10.000E-3      MJC=0.4         XTB=1.5000
ISC=1.4000E-15     CJS=350E-15     XTI=2.5000
* FOR PSPICE:  NK=0.3
```

SUBSTRATE PNP —EMITTER AREA: 2×6 µm^2

```
.model spnp2x6 pnp
IS=250.00E-18      CJE=25.000E-15
BF=220             CJC=55.000E-15
VAF=25             TF=300.00E-12
IKF=100.00E-6      XTF=4
ISE=50.000E-8      VTF=2
BR=10              ITF=4.0000E-3
VAR=5              TR=3.0000E-9
IKR=5.0000E-3      RE=20
RB=100             RC=2000
```

SUBSTRATE PNP —EMITTER AREA: 2×15 µm^2

```
.model spnp2x15 pnp
IS=500.00E-18      RC=1.0000E3
BF=220             CJE=50.000E-15
VAF=25             CJC=110.00E-15
IKF=200.00E-6      TF=300.00E-12
ISE=50.000E-18     XTF=4
BR=10              VTF=2
VAR=5              ITF=8.0000E-3
IKR=10.000E-3      TR=3.0000E-9
RE=10              RB=50

FOR PSPICE: NK=0.3
```

SUBSTRATE PNP —EMITTER AREA: 2×30 µm^2

```
.model spnp2x30 pnp
IS=125.00E-18      CJE=13.000E-15
BF=220             CJC=30.000E-15
VAF=25             TF=300.00E-12
IKF=50.00E-6       XTF=4
ISE=25.000E-18     VTF=2
BR=10              ITF=2.0000E-3
VAR=5              TR=3.0000E-9
IKR=2.50000E-3     RE=40
RB=200             RC=4000
```

P-CHANNEL JOINED-GATE JFET —W=2 µm, L=1 µm

```
.model pjfw2l1 pjf
BETA=12.000E-6      VTO=-1.9
LAMBDA=60.000E-3    RD=2000
RS=2000             CGD=11.000E-15
CGS=11.000E-15      KF=1.0000E-18
*FOR PSPICE:
* BETATCE=-.5       VTOTC=-2.5000E-3
* ALPHA=1.0000E-6   VK=0.1
```

P-CHANNEL JOINED-GATE JFET —W=4 µm, L=1 µm

```
.model pjfw4l1 pjf
BETA=25.000E-6      VTO=-1.9
LAMBDA=60.000E-3    IS=20.000E-15
RD=1000             RS=1000
CGD=20.000E-15      CGS=20.000E-15
KF=1.0000E-18
* FOR PSPICE:
* BETATCE=-.5        VTOTC=-2.5000E-30
* ALPHA=1.0000E-6    VK=1
```

P-CHANNEL JOINED-GATE JFET —W=20 µm, L=1 µm

```
.model pjfw20l1 pjf
BETA=125.000E-6    IS=100.000E-15
LAMBDA=60.000E-3   VTO=-1.9
RD=200             RS=200
CGD=100.000E-15    CGS=100.000E-15
KF=1.0000E-18
* FOR PSPICE:
* BETATCE=-.5        VTOTC=-2.5000E-3
* ALPHA=1.0000E-6    VK=1
```

LOW-NOISE SEPARATED-GATE P-CHANNEL JFET —W=2 µm, L=1 µm

```
.model jfet02 pjf
BETA=626E-6       VTO=-2.33
LAMBDA=45E-3      IS=500.000E-15
RD=25             RS=25
CGD=500.000E-15   CGS=500.000E-15
KF=5.3E-17        AF=1
* FOR PSPICE:
* BETATCE=-.5       VTOTC=-2.5000E-3
* ALPHA=1.0000E-6   VK=1
```

LIST OF FIGURES

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LIST OF TABLES

Curriculum Vitæ

Ronaldo Martins da Ponte

Education

2003–2007	Bachelor's degree in Electrical Engineering Universidade Federal do Rio Grande do Norte, Brazil
2007–2011	Instrumentation & Control engineer Chemtech—a Siemens Company
2012–2015	Master's degree in Electrical Engineering Field of study: Integrated circuits & systems Universidade Federal de Santa Catarina, Brazil
2016–2023	Ph.D. degree in Microelectronics Delft University of Technology, The Netherlands
2022–Now	Principal Analog Circuit Designer, The Netherlands Nowi, Nexperia—Energy Harvesting solutions

Short Bio

Ronaldo Martins da Ponte, born in Brazil in 1985, works for Nexperia since 2022. He is involved in the design of analog circuits for energy harvesting and power management integrated circuits. He obtained his Ph.D. degree in Microelectronics from Delft University of Technology, the Netherlands in 2023. His doctoral research topic was dedicated to the monolithic integration of integrated circuits with micro-electromechanical systems for biomedical applications. Throughout his doctoral studies, Ronaldo developed a deep understanding and expertise in microfabrication of semiconductor technologies, including BiCMOS, BiFET, and MEMS. Ronaldo obtained his M.Sc. degree from the Federal University of Santa Catarina in 2015 and a B.Eng. in Electrical Engineering from the Federal University of Rio Grande do Norte in 2007. During his master's studies, Ronaldo developed a strong proficiency in the design of analog, mixed-signal, and radio-frequency circuits, with a primary emphasis on transistor-level CMOS design employing inversion-based CMOS models such as the ACM and the EKV. From 2008 to 2011 he worked in Siemens providing industrial solutions and services for petrochemical plants. He actively participated in the front-end engineering design of the instrumentation field for the Rio de Janeiro Petrochemical Complex (Comperj). Ronaldo was also pivotal for the Abreu and Lima Refinery (RNEST) project's closure during the instrumentation detailing phase of offsite. His main research interests include Analog IC design, energy harversting, power management, CMOS and MEMS microfabrication, semiconductor physics and modeling.

List of Publications

Journal papers

1. Y. Liu; A. Urso; **Martins da Ponte, Ronaldo**; T. Costa; V. Valente; V. Giagka; W.A. Serdijn; T.G. Constandinou; T. Denison, *Bidirectional Bioelectronic Interfaces: System Design and Circuit Implications*, IEEE Solid-State Circuits Magazine, Volume 12, Issue 2, pp. 30-46, 23 June 2020.

2. **Martins da Ponte, Ronaldo**; Nikolas Gaio; Henk van Zeijl; Sten Vollebregt; Paul Dijkstra; Ronald Dekker; Wouter A. Serdijn; Vasiliki Giagka, *Monolithic Integration of a Smart Temperature Sensor on a Modular Silicon-based Organ-on-a-Chip Device*, Sensors and Actuators A: Physical, Nov. 21 2020. ISSN 0924-4247.

Conference papers

1. **Martins da Ponte, Ronaldo**; Vasiliki Giagka; Wouter A. Serdijn; *Design and Custom Fabrication of a Smart Temperature Sensor for an Organ-on-a-chip Platform*, In proc. IEEE Biomedical Circuits and Systems Conference (BioCAS 2018), IEEE, Oct. 17–19 2018.

Posters and Presentations

1. Asli Yelkenci; **Martins da Ponte, Ronaldo**; Virgilio Valente, *Co-integration of flip-tip patch-clamp and microelectrode arrays for in-vitro recording of electrical activity of heart cells*, In Book of Abstracts, 7th Dutch Biomedical Engineering Conf. (BME) 2019, Jan. 24–25 2019.

2. Asli Yelkenci; **Martins da Ponte, Ronaldo**; Virgilio Valente, *Co-integration of flip-tip patch-clamp and microelectrode arrays for in-vitro recording of electrical activity of cardiac cells*, In Book of Abstracts, 2019 International Winterschool on Bioelectronics Conference (BioEl 2019), Kirchberg, Tirol, Austria, 16–23 March 2019

3. **Martins da Ponte, Ronaldo**; Vasiliki Giagka; Wouter A. Serdijn; *Design and custom fabrication of a smart temperature sensor for an organ-on-a-chip platform*, In Book of Abstracts, 7th Dutch Biomedical Engineering Conf. (BME) 2019, Jan. 24–25 2019.

4. **Martins da Ponte, Ronaldo**; Vasiliki Giagka; Wouter A. Serdijn; *Design of a multi-functional smart optrode for electrophysiology and optogenetics*, In Book of Abstracts, 7th Dutch Biomedical Engineering Conf. (BME) 2019, Jan. 24–25 2019.

5. **Martins da Ponte, Ronaldo**; Vasiliki Giagka; Wouter A. Serdijn; *MEMS–Electronics Integration: A Smart Temperature Sensor for an Organ-on-a-chip Platform*, In Proc. ProRISC, Enschede, the Netherlands, June 7–8 2018.

6. **Martins da Ponte, Ronaldo**; Vasiliki Giagka; Wouter A. Serdijn; *Towards a Flexible Implant with Distributed Electronics, Wireless Communication and Energy Transfer*, In Book of Abstracts, 6th Dutch Bio-Medical Engineering Conference, 26 and 27 January 2017, Egmond aan Zee, The Netherlands, 2017.

7. **Martins da Ponte, Ronaldo**; Vasiliki Giagka; Wouter A. Serdijn; *MEMS–electronics integration: a smart temperature sensor for an organ-on-a-chip platform*, In Proc. Design of Medical Devices Conf. (DMD) 2017 Microfabrication for Medical Devices, Eindhoven, 14 – 15 Nov 2017.

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This Ph.D. thesis has not been a solo act. Therefore, I would like to thank those who helped shape my research. Naturally, my first warmhearted gratitude goes to my "scientific parents," Prof. Wouter Serdijn and Prof. Vassiliki (Vasso) Giagka.

Dear Wouter, I am deeply grateful for your tireless support and guidance throughout my thesis research. While reflecting on my academic journey and the guidance I've received, I can't help but draw parallels between you and the character of John Keating from the film "Dead Poets Society." Just as Keating inspired his students to think independently, appreciate the beauty of art, and embrace life to the fullest, you have consistently encouraged me to do the same. You are fearless in going against some of the dubious traditions of the academic system; you do what you believe in. Your mentorship has been transformative—it helped me look at the world from different perspectives and achieve my full potential on my own terms. Thank you for always finding positivity even when things do not go in the most beneficial direction. I also cherish fond recollections of our countless *borrel* gatherings fueled by IPAs and *bitterballen* at the */pub*, also the BioCAS conference in the US, and the many editions of our great Belca festival. Being part of your group and the Belca Band has been an honor. Thank you for bringing music to us!

Along with Wouter, I had the opportunity to be supervised by Vasso. During my research, Vasso introduced me to the hurdles and subtleties associated with system integration. These subtleties became apparent as I delved into problems that initially appeared straightforward but were far more complex than I could see from the surface. Thank you for these new insights, Vasso. I also extend my appreciation for your caring character with people. Vasso (and Wouter) always found the time to listen to me, especially during the most challenging moments; they supported me consistently throughout my journey.

Changing the figures now, I thank the committee members for accepting the invitation, dedicating their time to reading my thesis, and sharing valuable feedback. Discussing ideas and standpoints with highly knowledgeable independent members is always beneficial and a great pleasure.

Inevitably, I must acknowledge the CNPq (Conselho Nacional de Desenvolvimento Científico e Tecnológico) for my scholarship (yet a remarkably modest one) and its financial support. This research would not be possible if not for CNPq.

Getting back to people again, throughout my Ph.D. research journey, I was privileged to engage in enriching discussions with many knowledgeable colleagues. I want to thank Sten V. for the discussions on wafer-level measurements; Henk van Zeijl for back-and-forths on lithography, device physics, microfabrication, and packaging; Tom Scholtes for the chemistry lessons (and adopting me in the cleanroom); Johannes for the dielectrics background support; and Silvana for discussions on the device physics simulation and her incredible support during very challenging times. From the circuit design domain, I

want to thank Antoon Montagne for his invaluable support with SliCAP and our productive discussions on structured electronic design methodology. Discussing Middlebrook's General Feedback Theorem with Frank Wiedmann was of great help for conducting stability and loop-gain analysis of differential circuits using LTSpice.

I am deeply grateful to the many cleanroom researchers and practitioners who helped my academic research journey, including Mario, Violeta, Jia Wei, Aleksander, Nikolas, Juan, Joost Romijn, and others whose names have regrettably slipped my mind—special thanks to Paolo and Bruno. Paolo, you make the energy of the cleanroom vibrant. Bruno, I'll never forget your advice when I saw you, let's say, not in your best shape, dressing up just moments before entering the cleanroom: "Ronaldo, think seriously before getting married." "Why?" I asked. "For instance, you can sleep." I must admit I've been rigorously following your advice, although I am unsure if it is by personal choice.

Thanks to the technical team, including Lukas Pakula for the incredible help with the instrumentation, Antoon Frehe for the Linux support, Wim for the TSUPREM support, and Atef for the great help setting up the DIMES03 library in Cadence. Speaking of the DIMES03 reminds me now that I must thank whoever had the brilliant idea to create the Wayback machine. This tool was the only way to resurrect the DIMES03 models of an internet archive in the mid-90s that (almost) faded away from existence. Chapter 5, for instance, would not be possible without it.

Changing from the technical team to the administration team, my appreciation goes to the adorable Marion and the secretary team for their exceptional support throughout this journey.

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That's all, folks! And remember, in the end, we are all stardust. Cheers!