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DOI
10.1109/JSSC.2023.3271270

Publication date
2023

Document Version
Final published version

Published in
IEEE Journal of Solid-State Circuits

A 1.2-mW/Channel Pitch-Matched Transceiver ASIC Employing a Boxcar-Integration-Based RX Micro-Beamformer for High-Resolution 3-D Ultrasound Imaging

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***Abstract*— This article presents a low-power and small-area transceiver application-specific integrated circuit (ASIC) for 3-D trans-fontanelle ultrasonography. A novel micro-beamforming receiver architecture that employs current-mode summation and boxcar integration is used to realize delay-and-sum on an N-element sub-array using $N\times$ fewer capacitive memory elements than conventional micro-beamforming implementations, thus reducing the hardware overhead associated with the memory elements. The boxcar integration also obviates the need for explicit anti-aliasing filtering in the analog front end, thus further reducing die area. These features facilitate the use of micro-beamforming in smaller pitch applications, as demonstrated by a prototype transceiver ASIC employing micro-beamforming on sub-arrays of $N = 4$ elements, targeting a wearable ultrasound device that monitors brain perfusion in preterm infants via the fontanel. To meet its strict spatial resolution requirements, a 10-MHz 100-μm-pitch piezoelectric transducer array is employed, leading to a per-element die area $>2\times$ smaller than prior designs employing micro-beamforming.**

***Index Terms*— Application-specific integrated circuit (ASIC), micro-beamformer (μBF), pitch-matched analog front end (AFE), sub-array beamforming, ultrasound imaging.**

I. Introduction

TRANS-FONTANELLE ultrasonography (TFUS) is a favorable approach for monitoring brain perfusion in neonates. In contrast with other imaging techniques such as positron emission tomography (PET) and magnetic resonance imaging (MRI), it allows for bedside monitoring of the neonatal brain and avoids exposure to ionizing radiation and the need for sedation [1]. Moreover, it offers better spatial resolution than near-infrared spectroscopy (NIRS) [2].

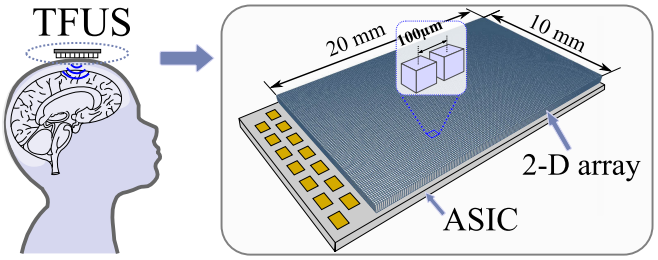

Fig. 1. Wearable neuro-monitoring device for TFUS with inset showing the envisioned pitch-matched ASIC with the transducer array built on top.

Preterm infants regularly show inadequate brain perfusion during and after the delivery, resulting in brain injuries and neuro-developmental problems [3]. A wearable neuro-monitoring device that can continuously assess brain perfusion and brain development of preterm infants would enable timely treatment of brain perfusion abnormalities [4]. Fig. 1 shows the device envisioned in this work, which uses pulse-echo ultrasound through the fontanel to generate high-resolution images of the brain and Doppler techniques to image blood flow in the brain. To be able to assess the relevant part of the brain, a 2-D transducer array is required, which allows for beamforming in 3-D space. To visualize sub-millimeter brain vessels, a small wavelength is required, resulting in a high ultrasound frequency and small array pitch. A higher ultrasound frequency leads to faster attenuation in brain tissue [5] and thus shortens the penetration depth. As a tradeoff, a 2-D transducer array with 10-MHz central frequency and 100-μm pitch was chosen in our application to ensure sufficient resolution and penetration depth. As shown in Fig. 1, an aperture size of 20×10 mm^2 is suitable according to studies of anterior fontanel size in preterm infants [6], [7], resulting in a vast 2-D transducer array of 20 000 elements for the selected 100-μm pitch size in such a wearable device.

Manuscript received 3 February 2023; revised 30 March 2023; accepted 25 April 2023. Date of publication 11 May 2023; date of current version 25 August 2023. This article was approved by Associate Editor Nick van Helleputte. This work was supported by the Dutch Research Council (NWO) through the MIFFY Project of the Open Technology Programme under Grant 15293. *(Corresponding author: Peng Guo.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2023.3271270.

Digital Object Identifier 10.1109/JSSC.2023.3271270

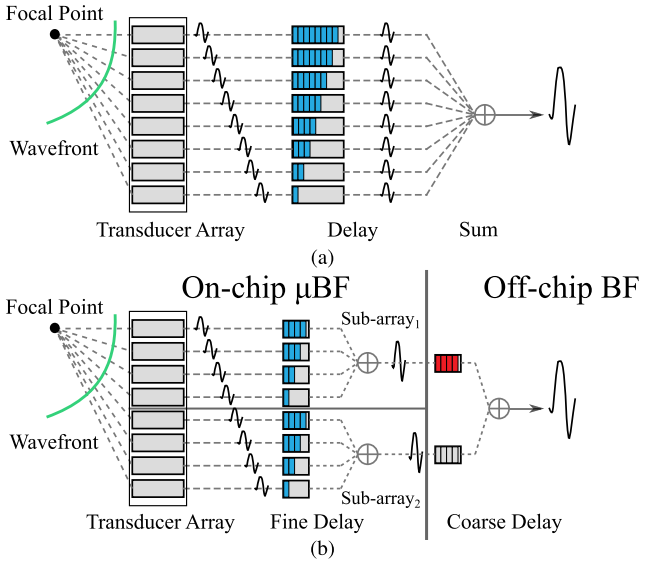

Fig. 2. (a) Beamforming process employing DAS. (b) Micro-beamforming process employing two-step DAS.

This high number of elements and small array pitch make pulse transmission (TX) and echo reception very challenging, and beamforming plays a central role in this. The most common receive (RX) beamforming approach is the delay-and-sum (DAS) algorithm, as shown in Fig. 2(a). After pulse TX, the echoes from a focal point arrive at the elements of the transducer array at slightly different times and are converted into electrical signals with the corresponding time shifts by the transducer array. These signals can be coherently detected by applying correct delays to each channel and summing the resulting signals. Due to modern integrated circuit technology, DAS can be performed by high-speed processors such as graphics processing units (GPUs) [8]. Nevertheless, this requires element-level digitization beforehand. Direct RF digitization was realized in [9], where an element-level $\Delta\Sigma$ modulator directly digitizes the ultrasound RF signal from each transducer element, followed by an on-chip digital beamformer to post-process the digitized data in the chip's periphery. Noting that each RX channel in the reported work occupies nearly all element-level area of 250 $\times$ 250 μm^2, the element-level digitization poses fundamental challenges to our circuit design when taking the array pitch of 100 μm and the need to include element-level high-voltage (HV) pulsers into account.

An alternative is to divide the transducer array into sub-arrays of N elements each and to combine the signals in each sub-array locally by means of an analog DAS operation, also referred to as micro-beamforming [10], [11], as shown in Fig. 2(b). Further beamforming of the micro-beamformer (μBF) outputs can be done either off chip or on the periphery of the chip. The channel count is thus reduced by a factor of N allowing for a pitch-matched layout at the sub-array level and much less signal routing compared to the element-level digitization scheme. However, prior μBF implementations employ per-element capacitive memory to realize the delay [12], [13], making it cumbersome and unfavorable for the desired 100-μm-pitch array.

In this article, we present a compact, pitch-matched prototype application-specific integrated circuit (ASIC) employing a boxcar-integration-based RX μBF. In contrast to conventional RX micro-beamformers, which perform delay before the summation [12], the boxcar-integration-based beamformer sums the signals from different elements in the current domain before the delay operation takes place, leading to a reduction in the number of required memory cells, the associated dynamic switches, and signal routing. In addition, the boxcar integration provides built-in anti-aliasing filtering, obviating the need for an explicit anti-aliasing filter (AAF) in-between the analog front end (AFE) and the digitizer and relaxing the design requirements for the AFE. In the ASIC's TX circuitry, a novel row-level beamforming scheme is deployed that moves the bulky HV MOS transistors to the chip's periphery, in contrast with a conventional push–pull structure [13], and only uses one HV isolation diode per element. All these result in a compact transceiver ASIC meeting stringent restrictions on die area.

This article is organized as follows. Section II reviews the prior art and compares voltage- and current-mode beamformers. Section III describes the architecture design of the boxcar-integration-based μBF and provides the system overview. Section IV presents the detailed circuit implementation. Section V describes the fabricated prototype, as well as the electrical and acoustic measurement results. This article ends with conclusions.

II. Prior Art

Various RX beamformer topologies have been used to realize the DAS process. Direct RF digitization with subsequent beamforming in the digital domain [9], [14], as mentioned, requires a relatively large die area and power consumption and will not be discussed in more detail. Other beamformer topologies can be broadly classified into three categories: beamformers based on phase rotation applied to I/Q demodulated RF signals [15], beamformers based on continuous-time delay lines in which the delays are tuned continuously [16], [17], and beamformers based on discrete-time delay lines in which the delays are discretized conforming to a clock signal [11], [12], [18], [19], [20].

The phase-rotation-based beamformer as shown in Fig. 3(a) applies direct I/Q demodulation to the bandpass-filtered RX signals followed by digitization. The digitized I/Q signals are fed to a series of phase rotators in the digital domain to approximate time delays before the summation takes place. In [15], a direct sampling I/Q demodulation is employed, and analog-to-digital conversion is required for each I/Q channel. The solution is attractive for narrow-band ultrasound signals, for which phase shifting is a good approximation for delay, and which can be multiplexed on a high-speed analog-to-digital converter (ADC), thus saving area. However, echo signals in ultrasound imaging generally have a very wide bandwidth, e.g., 80% bandwidth around a 10-MHz central frequency in our application, leading to too many high-speed ADCs in the system, therefore making the solution unattractive for our application.

As shown in Fig. 3(b), a continuous-time delay cell employs current-mirror-based circuits to construct an all-pass filter, which is a first-order approximation of an ideal delay tuned by the bias currents of the current mirror network. A delay line can be constructed by cascading multiple of such delay

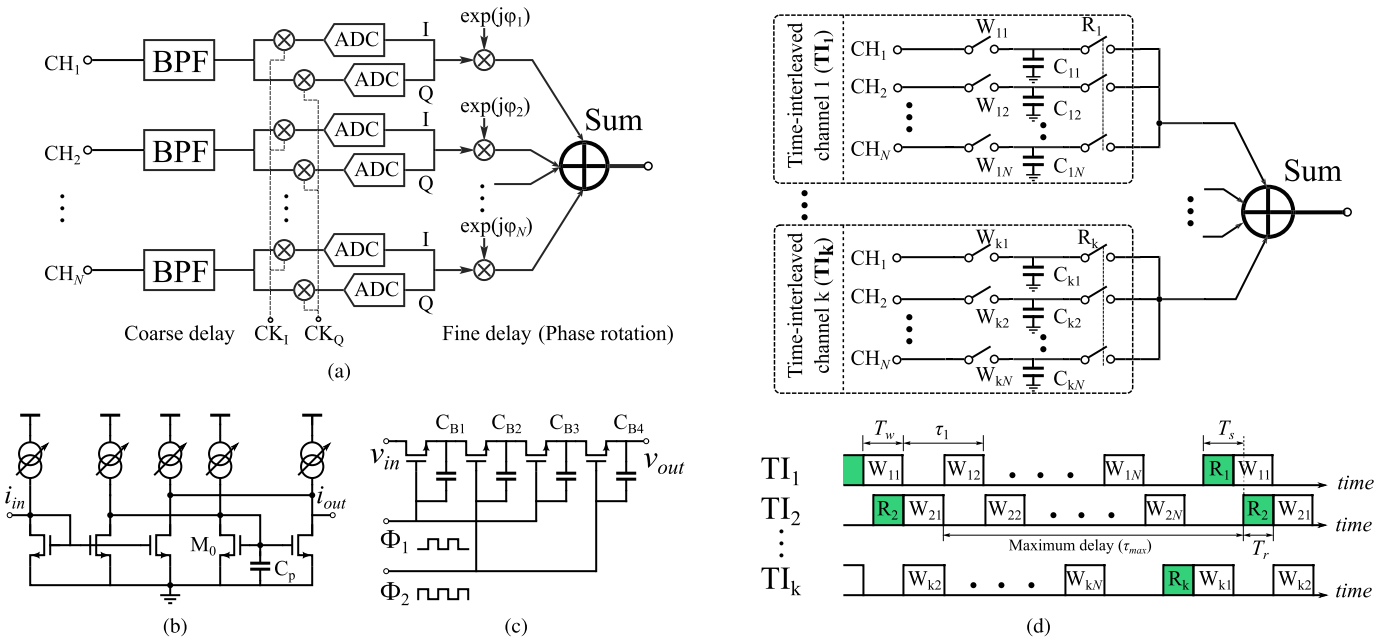

Fig. 3. Circuits to implement RX beamforming: (a) direct I/Q demodulation in conjunction with digital phase rotation [15], (b) continuous-time delay cell [16], (c) BBD-based delay line [18], and (d) switched-capacitor/-current-based delay line [12], [19], [20].

cells [16]. The implementation has no passive devices and is potentially small. However, it suffers from non-linear phase response, resulting in different delays for different frequency components in a wideband ultrasound signal and high sensitivity to temperature and process drift.

A discrete-time delay line using bucket-brigade devices (BBDs) [18] is shown in Fig. 3(c). A series of bucket capacitors $C_{\mathrm{B1–4}}$ stores the information as charge packets transported by means of MOS transistors [21]. The speed of the charge transportation is controlled by two complementary clock signals, making the delay step equal to the clock period. Although the BBDs delay line uses a minimum number of transistors and occupies a small area, it suffers from poor charge-transfer linearity [22].

Other types of discrete-time beamformers are based on switched-capacitor [12], [19] or switched-current delay lines [20] as shown in Fig. 3(d), in which the capacitor array (e.g., $C_{11–1N}$) samples the voltage/current signals of all channels ($\mathrm{CH}_{1–N}$), controlled by a series of write clock signals (e.g., $W_{11–1N}$), and stores the information for a certain amount of time until the read/summation (assuming that they happen simultaneously) takes place controlled by a read clock signal (R_1). Thus, the delays between adjacent channels (e.g., τ_1) are accurately defined by the falling edges of the write clock signals (e.g., W_{11} and W_{12}). Multiple time-interleaved (TI) channels ($\mathrm{TI}_{1–k}$) are needed to prevent information loss during DAS since the required maximum delay ($\tau_{\max}$) is generally much longer than the sampling period (T_s). The total required number of TI channels k can be expressed as [19]

$$k = \frac{T_w + T_r + \tau_{\max}}{T_s} \tag{1}$$

and the total required number of memory cells N_{mem}, as well as the number of switches N_{sw}, can be expressed as

$$\begin{aligned} N_{\mathrm{mem}} &= k \cdot N \\ N_{\mathrm{sw}} &= 2 \cdot k \cdot N \end{aligned} \tag{2}$$

where T_w, T_r, and $\tau_{\max}$ are the write, read cycle time, and the maximum RX beamforming delay, respectively, and N is the total number of ultrasound channels. The information can be delayed and summed in different forms, such as the voltage domain [19], the current domain [20], and the charge domain [12]. However, a large number of memory cells, the associated switches, and interconnections are required in all cases, making these solutions less favorable for our application.

III. Architecture Design

A. Boxcar-Integration-Based Micro-Beamformer

As shown in Fig. 3(d), each TI channel contains N memory cells, and these memory cells cannot be shared with other TI channels during the delay process of the DAS since the stored information can only be flushed once the following read/summation cycle completes. An effective way to reduce the number of memory cells is reversing the DAS process and using "sum and delay" instead, as shown in Fig. 4(a). The proposed μBF operates on current-mode input signals $I_{1–N}$ and successively integrates these currents on the memory cells, e.g., C_1 of the first TI channel TI_1. These input currents are generated by AFEs that have high-impedance output stages, as will be elaborated in Section IV, allowing summation to take place in the current domain before delays are applied. A similar clock scheme is used, which accurately sets the delay between two adjacent channels by the delay (e.g., τ_1) between the falling edges of two write cycles (e.g., W_{11} and W_{12}). The total number of TI channels is the same as given by (1), but there is only one memory cell in every TI channel, thus reducing the total number of memory cells by a factor of N compared to the aforementioned beamformers. The required total number of switches is reduced by about 2×.

The integration of input currents on the memory capacitors is an implementation of boxcar integration [23], which is an

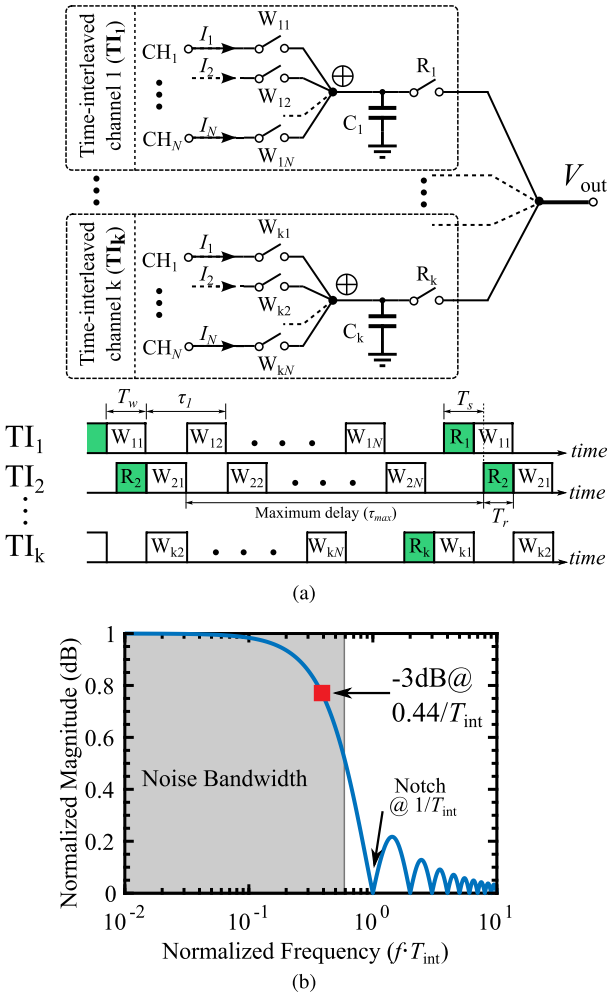

Fig. 4. (a) Box-integration-based μBF. (b) Frequency response of the boxcar integration.

effective technique to suppress out-of-band noise from the preceding AFE and acts as an implicit AAF for sampling in the beamformer. The normalized magnitude response of boxcar integration can be expressed as [24]

$$|H(f)| = \left| \frac{\sin(\pi f T_{\text{int}})}{\pi f T_{\text{int}}} \right| \tag{3}$$

where T_{int} is the integration time. Fig. 4(b) shows the normalized magnitude response, and the notch frequency of the boxcar integration is inversely proportional to the integration time. Therefore, an integration time equal to the sampling period T_s is selected in our design to maximize the filtering effect and minimize aliasing, as shown in Fig. 4(a). In contrast to the continuous-time delay line employing the all-pass filter, boxcar integration has a linear phase response and does not cause a frequency-dependent delay for the wideband ultrasound signal. The -3-dB corner of the boxcar integration filter is about $0.44 \cdot f_s$ in our design, which is higher than the required signal bandwidth with insignificant in-band attenuation, as a sampling frequency of $4\times$ of the transducer resonance frequency is selected in our design.

As derived in the Appendix, the theoretical total capacitance required to achieve a given output signal-to-noise ratio (SNR) is similar for the conventional switched capacitor and the proposed boxcar-integration-based beamformer. However, in practice, the latter still significantly reduces chip area considering that the conventional beamformer requires $N\times$ more distributed memory capacitors, two times more switches, and the associated interconnections. In addition, the boxcar-integration-based beamformer obviates the need for an explicit AAF that also saves area. All these factors result in very compact beamformer implementation.

A similar current-mode beamformer was introduced in [25]. In contrast with our proposal, this design employs a voltage-mode AFE with element-level sampling capacitors and explicit voltage-to-current converters at the input of the beamformer, resulting in large die area and additional power consumption. Moreover, either an explicit AAF or an AFE with limited bandwidth is needed to avoid thermal noise folding. Finally, a clocking scheme was used in which a half-cycle for sampling and a half-cycle for integrating, leading to weaker anti-aliasing filtering compared to our proposed full-cycle integration. These issues are mitigated in our design by the boxcar-integration-based μBF, leading not only to a compact circuit topology but also significantly relaxing the design requirements of the AFE, as will be further elaborated in Section IV-B.

B. System Overview

As shown in Fig. 5, the prototype ASIC interfaces with an 8×8 transducer array and can be divided into two regions: the element-level region in which the pitch-matched layout is strictly limited by the pitch of the transducer and a peripheral region in which the area is less constrained. HV pulsers consisting of peripheral pulsers and element-level diode isolators drive all elements to generate ultrasound pressure, with the ability to define time delays at the row or column level to steer the resulting TX beam to different angles. As a proof of concept, only the row-level TX beamforming is implemented in our design. During the TX phase, unipolar square-wave pulses are generated for each transducer element in the prototype, with an amplitude up to 36 V, 50-ns duration, and a minimum 12.5-ns delay step. In contrast to a push–pull transmitter [13] where a pair of bulky HV PMOS/NMOS transistors generate the needed square wave, the element-level isolator only consists of an area-efficient HV diode and thus significantly reduces the required element-level die area. This also allows us to accommodate an RX circuit with more complicated functions in the pitch-matched layout area, such as an AFE with continuous time-gain compensation (TGC).

For echo reception, the 8×8 array is divided into sub-arrays of 2×2 elements. After the TX, HV transmit/receive (T/R) switches and multiplexers connect two of these sub-arrays to the receive circuitry inside the element-level region. The signal currents from the four elements of the selected sub-array are amplified by four AFEs and then fed to the RX μBF consisting of profile multiplexers that set the element delays, write switches, and boxcar memory cells that store the summed-and-delayed current signals. Four TI memory cells, each of which comprises an active integrator, are followed by a sample-and-hold (S/H) stage that joins TI signals together. An output buffer drives the S/H output off the chip.

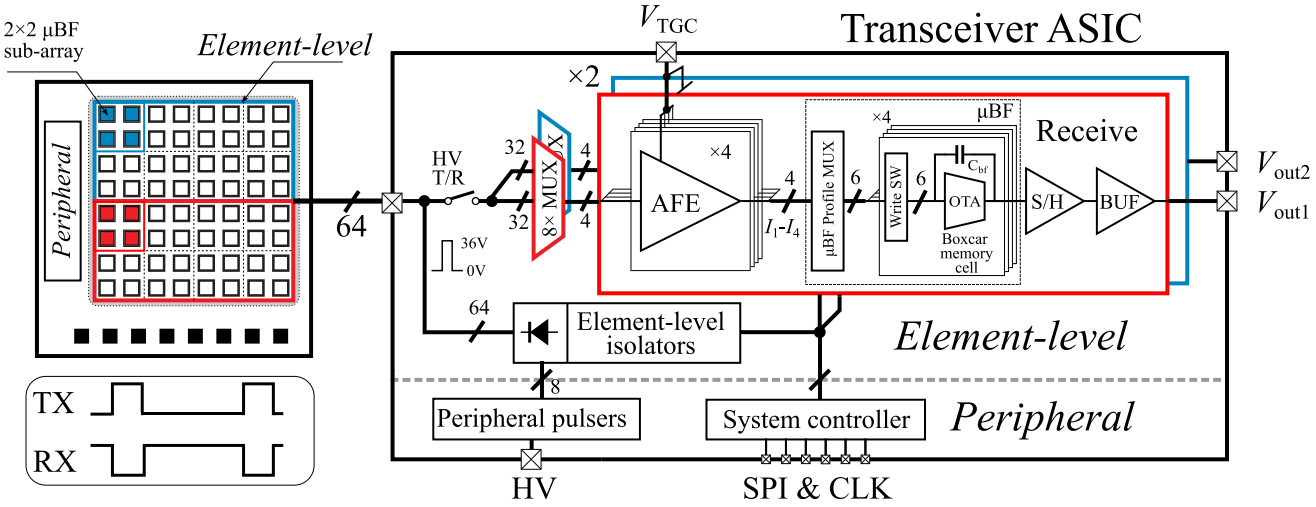

Fig. 5. Block diagram of the transceiver ASIC.

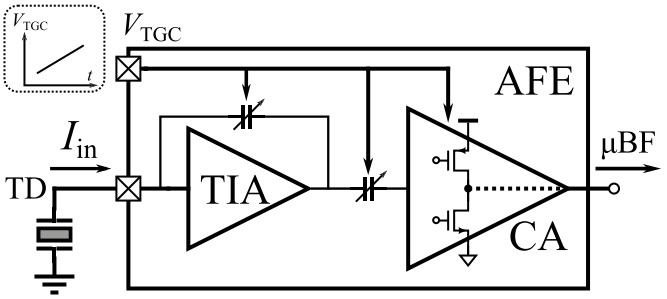

Fig. 6. Circuit diagram of the AFE consisting of a TIA, a CA, and a coupling capacitor in between.

IV. Circuit Design

A. Analog Front End

The AFEs are based on the design presented in [26]. As shown in Fig. 6, each AFE channel consists of a capacitive-feedback trans-impedance amplifier (TIA), the output of which is capacitively coupled to the input of a current amplifier (CA). The CA provides a high-impedance output to drive the boxcar integrator in the μBF with an amplified version of the transducer's signal current. The AFE's gain can be continuously tuned in a range of 36 dB by an external voltage V_{TGC} to provide TGC, i.e., to compensate for the stronger attenuation of echoes that arrive later. The AFE provides less than $\pm$0.4-dB gain error and has a 1.31-pA/$\sqrt{\text{Hz}}$ input-referred noise density within 6–14-MHz bandwidth at its maximum gain ($V_{TGC} = 1.1$ V).

B. Micro-Beamformer

Fig. 7(a) shows the detailed implementation of the boxcar-integration-based μBF. As mentioned, it has $N = 4$ input channels and four TI channels (TI$_{1-4}$). In contrast with the concept shown earlier in Fig. 4, the inputs are not connected directly to the boxcar integrators, but through two layers of switches, i.e., the μBF profile multiplexer and the write switches $W_{1-6}\langle 1{:}4\rangle$. First, to set the delay profile, a μBF profile multiplexer connects each of the input current I_{1-4} to one of the six summation nodes, which correspond to six possible delay values. These six summation nodes are cyclically connected to the four boxcar integrators via the write switches ($W_{1-6}\langle 1{:}4\rangle$), orchestrated by an 80-MHz clock CLK$_D$, which is twice the output sampling rate of 40 MHz and gives a delay step of 12.5 ns. Active boxcar integrators are implemented instead of passive integrators to improve the linearity in the write cycles ($\bar{R}_{1-4}$). These are reconfigured to voltage buffers driving the following S/H stage in the read cycle (R_{1-4}). Fig. 7(a) also shows an example output waveform (V_{BF1}) of the first TI channel (TI$_1$) receiving four sinusoidal current inputs (I_{1-4}) with a uniform delay of 12.5 ns between each. These current inputs are connected to the first four summing nodes (nodes 1–4), corresponding to an equally spaced delay profile of 12.5 ns, and sequentially integrated on the feedback capacitor C_{BF1} via switches $W_{1-4}\langle 1\rangle$.

An important advantage of the two layers of switches is that the μBF profile multiplexer switches remain static during the RX period, while the switches connecting to the boxcar integrators can be driven by a simple profile-independent clock generator, providing accurate timing with low clock skew, which is important for generating accurate steering angles during RX beamforming [27]. The clock control signals of the 24 write switches only have eight different phases, e.g., write switches $W_2\langle 4\rangle$, $W_4\langle 3\rangle$, and $W_6\langle 2\rangle$ can share the same control signal Φ_8, as shown in Fig. 7(a). Therefore, an eight-phase digital clock generator is implemented using a 1-bit shift register (SR) and generates eight clock signals (Φ_{1-8}), each of which drives identical loads (i.e., three write switches). Compared to the single-layer switching scheme [28], in which a multi-bit SR and the following μBF delay profile multiplexers are both implemented in the digital domain to generate clock signals for every switch, resulting in a large number of clock signals that need to be routed across the digital and analog domain and difficulty to match the routing length, this clocking scheme both reduces the number of logical gates in the clock signal path and the number of clock signal connections to the write switches, making it less demanding to equalize the propagation delay, thus effectively minimizing the clock skew. Due to the current-mode operation, the associated switches can be made small with an insignificant area overhead.

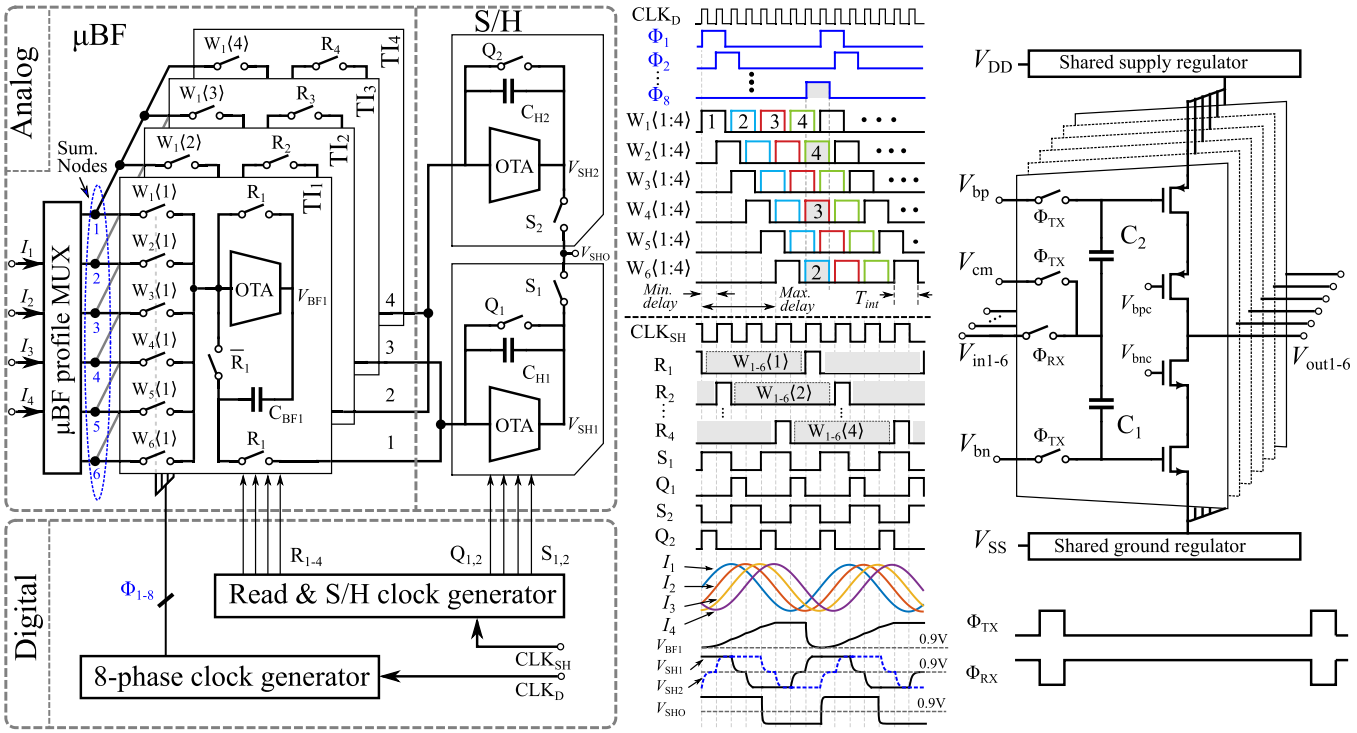

Fig. 7. (a) Circuit diagram of the boxcar-integration-based μBF, the ping-pong S/H stage, and the related timing details. (b) Circuit diagram of the inverter-based amplifiers used in the μBF and the S/H stage.

The active boxcar integrators alternate between integration ($R_i = 0$) and readout ($R_i = 1$) phases. During the latter, the accumulated charge is transferred to one of two S/H stages, which operate in a ping-pong fashion and alternately drive the output controlled by a 40-MHz clock CLK_{SH}, as shown by example waveforms in Fig. 7(a). In these S/H stages, the accumulated charge of $C_{\text{BF1,3}}$ and $C_{\text{BF2,4}}$ is transferred to hold capacitors C_{H1} and C_{H2} during read phases $R_{1,3}$ and $R_{2,4}$, respectively. During phases S_1 and S_2, they serve as intermediate buffer stages and alternately drive the output V_{SHO}, which is loaded by the following output buffer. During phases Q_1 and Q_2, the hold capacitors are reset in preparation of the next cycle.

The clock signal CLK_D sets the minimum delay step to 12.5 ns and the delay range to 62.5 ns, allowing for steering the 2×2 sub-array to an angle within the range of $-74°$ to $74°$, while CLK_{SH}, independently, sets the output sampling period to 25 ns. The boxcar integration time (T_{int}) is 25 ns, which provides effective anti-aliasing filtering for the AFE. In this work, the delay profile is predefined and can only be updated every pulse-echo cycle, while the proposed μBF architecture can be extended to other beamforming schemes (e.g., dynamic RX focusing) by adding additional digital control.

The operational transimpedance amplifiers (OTAs) in the boxcar integrators and S/H stages are implemented using inverter-based amplifiers [Fig. 7(b)] with current-reuse supply and ground regulators [26] that suppress interference and are shared at the sub-array level to save area. Two capacitive level shifters (C_1/C_2) are used to enlarge the dynamic range (DR) of the OTAs. These are reset to the associated common-mode voltages (V_{bp}, V_{bn}, and V_{cm}) during the TX period (Φ_{TX}) and hold the dc bias points during the RX period (Φ_{RX}).

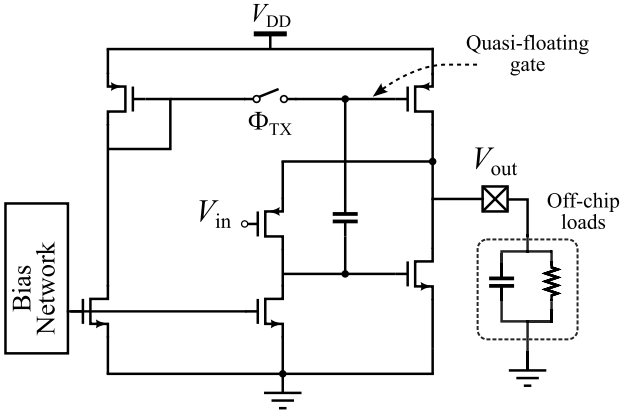

Fig. 8. Circuit diagram of the class-AB output stage with the quasi-floating biasing scheme.

C. Output Buffer

A class-AB output buffer as shown in Fig. 8 is adopted to provide sufficient drive capability for off-chip loads, such as parasitic interconnect capacitance [29]. A dynamic biasing scheme is used instead of the pseudo-resistor used in [29] to dynamically bias the static current of the class-AB output stage, i.e., dynamically resetting the quasi-floating gate during the TX phase (Φ_{TX}) and keeping it floating during the RX phase, thus improving the noise performance of the output buffer by isolating the noise originating from the bias network. The bandwidth, noise, and harmonic distortion of the output buffer were designed to be negligible compared to those of the preceding stages and therefore have an unnoticeable impact on the measurements.

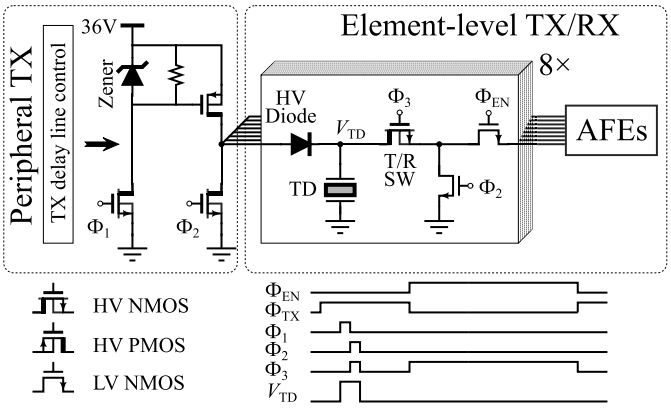

Fig. 9. Circuit diagram of the proposed transmitter employing HV diodes as isolation.

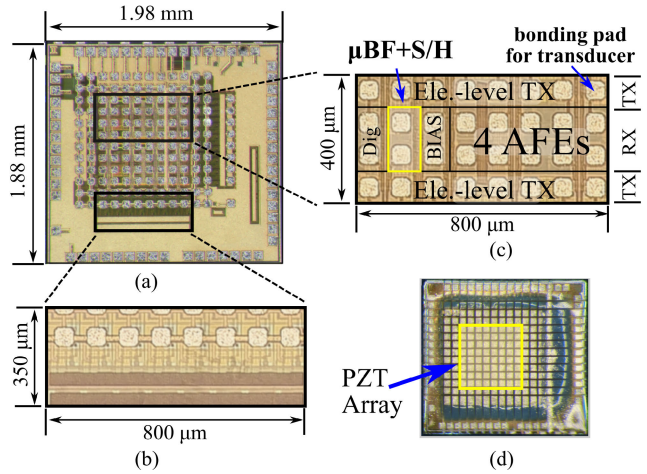

Fig. 10. (a) Micrograph of the transceiver ASIC. (b) Inset showing the peripheral TX circuitry. (c) Inset showing the element-level TX/RX circuitry. (d) Prototype of the transceiver ASIC with PZT array on top.

D. Transmitter

A row-level TX scheme is adopted in our design as a proof of concept, which employs row-level push–pull pulsers in the periphery and element-level HV diodes to provide necessary isolation between transducer elements, as shown in Fig. 9. The scheme allows for row-level TX beamforming controlled by the digital delay line also located in the periphery. During TX, HV pulses are generated by charging the transducer elements of a row via peripheral HV PMOS and element-level HV diodes. The PMOS is turned on via a level shifter controlled by clock signal Φ_1. The elements are then discharged via a peripheral HV NMOS, an element-level HV NMOS that also serves a T/R switch, and a low-voltage NMOS ($\Phi_{2,3} = 1$). The metal interconnect between the peripheral circuitry and the elements is dimensioned to ensure that the associated propagation delay is negligible. During reception, the transducer elements, isolated from each other by reverse biasing the HV diodes, connect to the AFEs via the T/R switch and a low-voltage multiplexer switch controlled by Φ_{EN}. The passive HV diode is generally smaller than HV MOS transistors as widely adopted in other designs [13], [30], [31], due to the lack of active structure, thus making the transmitter very compact and reserving more room for the RX electronics.

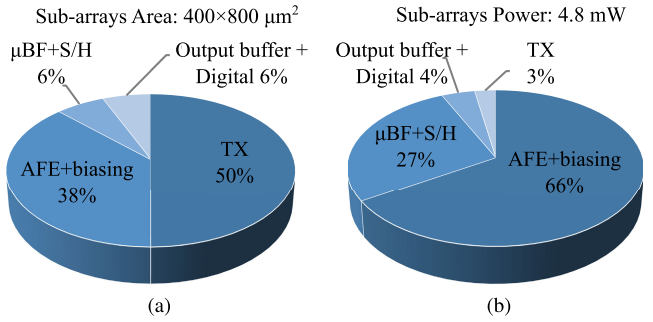

Fig. 11. (a) Area breakdown and (b) power breakdown of eight sub-arrays of 2 × 2 elements.

V. Experimental Results

A. ASIC Prototype

The ASIC has been fabricated in a 180-nm HV BCD process. The chip size of the prototype is 1.98 × 1.88 mm^2 [see Fig. 10(a)], in which the peripheral TX circuitry occupies 0.8 × 0.35 mm^2 as shown in Fig. 10(b). The top-half floor plan of the element-level TX/RX circuitry is shown in Fig. 10(c), which includes four RX channels interfacing eight sub-arrays of 2 × 2 elements via the multiplexer and has the area breakdown shown in Fig. 11(a). Per channel, the RX circuitry occupies 0.04 mm^2 of which the μBF plus the S/H occupies only 0.005 mm^2 when not taking the 8× multiplexing factor into account, i.e., dividing the area by a factor of 4. The power breakdown is shown in Fig. 11(b). The power consumption was measured on a chip with the transducer array built on top, and the measured total power consumption is 4.8 mW, i.e., 1.2 mW/channel, of which 0.8 mW is consumed by the AFE and biasing, 0.33 mW by the μBF and the S/H, and 0.06 mW by the output buffer and digital, while the TX consumes only 32 μW/channel at a pulse repetition frequency of 10 kHz, i.e., transmitting one 50-ns 30-V pulse in every 100 μs.

Fig. 10(d) shows a prototype with an 8 × 8 central PZT transducer array built on top, connected to the ASIC via the transducer bonding pads [see Fig. 10(c)] and surrounded by an outer ring of dummy transducer elements. The array was built using a fabrication scheme similar to that described in [32]. The prototype was wire-bonded to a daughter PCB, which was then mounted on a mother PCB, for the following measurements. The mother PCB contains a field-programmable gate array (FPGA), which controls the TX and RX functionality via the ASIC's SPI interface (see Fig. 5) and also synchronizes the data acquisition between the ASIC and an oscilloscope.

B. Electrical Characterization

Test currents can be injected into the inputs of a sub-array by applying voltage signals to four 1-pF capacitors on the chip, which emulate 2 × 2 transducer elements. By measuring the output voltage of the output buffer, the transfer function was extracted at different TGC control voltages (V_{TGC}) as shown in Fig. 12(a), From this, the gain at 10 MHz was extracted as shown Fig. 12(b), which reveals that the measured RX gain in decibels is a linear function of V_{TGC} from 0.5 to 1.1 V, leading to a total gain range of 36 dB. A −3-dB bandwidth curve across the overall gain range was also derived from

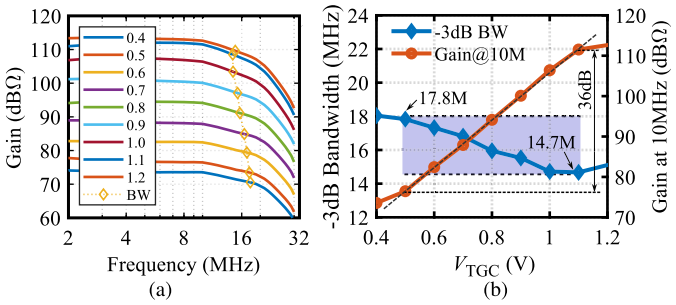

Fig. 12. (a) Measured gain transfer function. (b) Extracted −3-dB bandwidth and gain at 10 MHz as a function of TGC control voltage V_{TGC}.

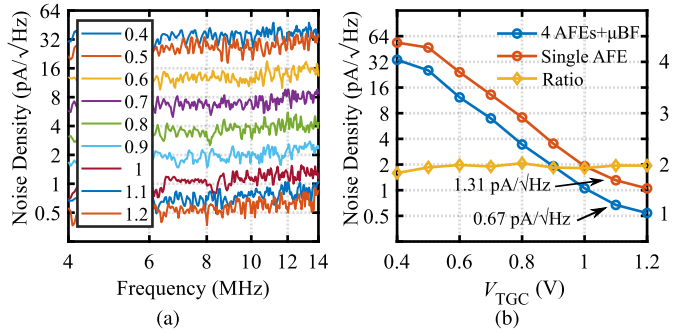

Fig. 13. (a) Measured input referred noise spectra. (b) Input-referred in-band noise density measured at AFE's and μBF's output as well as the ratio between them as a function of TGC control voltage V_{TGC}.

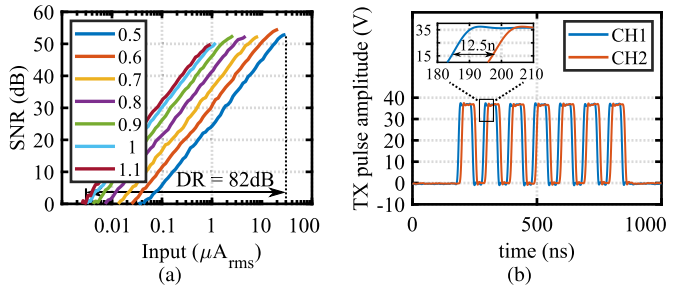

Fig. 14. (a) Measured SNR as a function of the input current in different TGC control voltages. (b) Measured outputs of two TX pulsers with inset showing a minimum delay of 12.5 ns and 36-V amplitude.

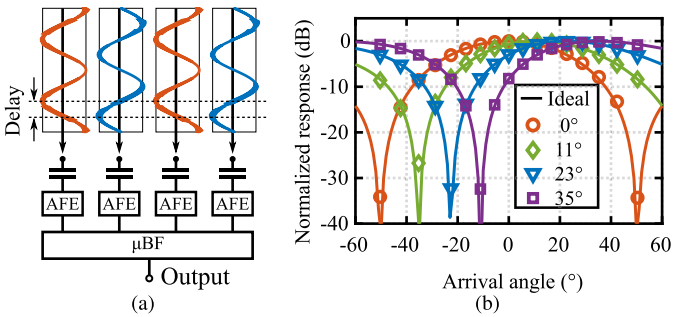

Fig. 15. (a) Spatial directivity measurement emulating acoustic waves arriving at different angles by means of four time-shifted sinusoidal inputs. (b) Normalized measured μBF response as a function of emulated arrival angles, for μBF steering angles.

the transfer function, indicating the bandwidth variation at different AFE gains. The overall bandwidth at different gains is a bit smaller than that of the AFE alone [26], due to the additional filtering effect of the boxcar integration, but the minimum measured bandwidth, i.e., 14.7 MHz, still meets the requirement of our application. The measured bandwidth variation is less than ±10% around 16.3 MHz across the gain range, which is also smaller than the variation measured at the AFE's output [26], due to the fact that the −3-dB corner of the boxcar integration filter is accurately controlled by the clock regardless of different AFE gains.

Fig. 13(a) shows the input-referred noise spectra for a set of TGC control voltages covering the full gain range. The output noise density was first measured at the output of the μBF via the output buffer by connecting the on-chip 1-pF capacitors at the inputs of the AFEs to ground, and the input-referred noise is then calculated by dividing the measured output noise density by the measured gains, as shown in Fig. 12(a). The noise contribution of the output buffer was designed to be negligible. The input-referred noise of a single AFE channel was measured in the same way by internally bypassing the μBF. In Fig. 13(b), the noise density averaged from 6 to 14 MHz is plotted as a function of the TGC control voltage both for the complete signal path (i.e., four AFEs + μBF) and for the AFE only. The figure also shows the ratio between them. An averaged input-referred noise of 0.67 pA/$\sqrt{\text{Hz}}$ is measured at the μBF's output when $V_{TGC} = 1.1$ V, which is close to half of the input-referred noise (1.31 pA/$\sqrt{\text{Hz}}$) measured at a single-channel AFE's output. This factor well meets the theoretical noise reduction of 2 expected from the μBF of four elements without noticeable noise-folding effects and is stably maintained across the full gain range [see Fig. 13(b)].

Fig. 14(a) shows the SNR as a function of the input current for different TGC control voltages, which was also measured via the final output buffer. It demonstrates a measured DR of 82 dB, which is the ratio of the maximum input signal level at the 1-dB compression point and the minimum detectable input signal level at which the input power is equal to the noise power, allowing for measuring an acoustic pressure within the range of about 3.4 Pa–42 kPa.

For characterization of the TX circuitry, two of the transducer bonding pads were wire-bonded to the daughter board and were connected to two off-chip 1-pF capacitive loads emulating two transducer elements. The HV pulsers successfully produce unipolar seven-cycle pulses with up to a 36-V amplitude and a minimum delay resolution of 12.5 ns, as shown in Fig. 14(b).

The RX beamforming performs spatial filtering of incoming acoustic wave, resulting in spatial directivity for different beamformer steering angles. As shown in Fig. 15(a), this spatial directivity was first evaluated through an electrical test by applying four time-shifted 10-MHz sinusoidal inputs via the on-chip capacitors to the AFEs, thus emulating acoustic waves arriving at different angles, and comparing the μBF response with the theoretical spatial directivity for different μBF steering angles. A 6.25-ns time shift step was applied to the four sinusoidal inputs during the measurement, which emulates an angle of incidence of an incoming acoustic wave that changes by 5°–7° in each step, assuming that the ultrasound speed is 1540 m/s. The μBF was configured to four different steering angles from 0° to 35°. As shown in Fig. 15(b), the μBF response is in very good agreement with the theoretical directivity curve.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE PRIOR ART

	This work	[12]	[13]	[33]	[9]
μBF type	**Boxcar integration**	Voltage S/H	Voltage S/H	Voltage S/H	Digital
Process	**180-nm BCD**	180-nm BCD	180-nm SOI	130-nm CMOS	28-nm CMOS
Sub-array size	**2 × 2**	3 × 3	4 × 6	8	4 × 4
Transducer type	**PZT**	PZT	PZT	CMUT	CMUT
Pitch	**100 μm**	150 μm	300 μm	—	250 μm
Center frequency	**10 MHz**	5 MHZ	<5 MHz	3 MHz	5 MHz
Sampling rate	**40 MS/s**	30 MS/s	40 MS/s	40 MHz	20 MS/s
μBF delay resolution	**12.5 ns**	33.3 ns	25 ns	6.25 ns	8.33 ns
μBF maximum delay	**62.5 ns**	233.3 ns	750 ns	1000 ns	940 ns
μBF area/channel	**0.005 mm^2 (*)**	0.011 mm^2 (§)	0.03 mm^2	0.03 mm^2	0.041 mm^2 (†)
μBF power/channel	**0.33 mW (*)**	0.17 mW (§)	0.19 mW	12.4 mW	17.5 mW (†)
AFE type	**LNA + TGC**	LNA + PGA	LNA + PGA	LNA + PGA	LNA + PGA
RX area/channel	**0.04 mm^2**	0.026 mm^2	0.09 mm^2	0.132 mm^2	0.088 mm^2
RX power/channel	**1.2 mW**	0.91 mW	0.43 mW	18 mW	33 mW
Peak SNR	**54 dB**	52 dB	—	—	60 dB
Input DR	**82 dB**	85 dB	85 dB	—	—
Element-level TX	**Y**	N	Y	N	N
TX voltage	**36 V**	—	138 V	—	—

* Including S/H stage. § Including sub-array ADC. † Including element-level ADC.

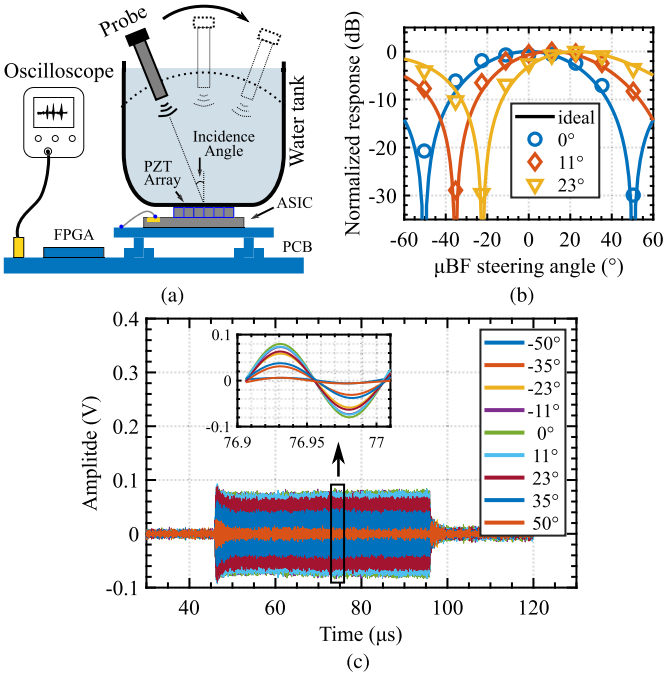

Fig. 16. (a) Acoustic measurement setup for μBF directivity test. (b) Measured μBF directivity at different probe incidence angles of 0°, 11°, and 23° as a function of μBF steering angles, as well as the theoretical directivity. (c) Measured μBF outputs at different μBF steering angles with a probe incidence angle of 0°, and inset showing the details of the amplitude change.

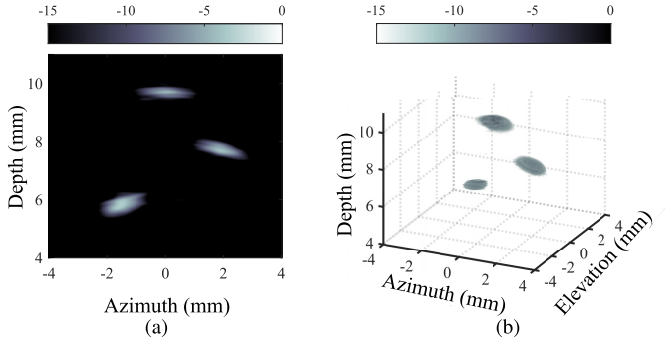

Fig. 17. (a) B-mode image in elevation plane. (b) Rendered 3-D image.

C. Acoustical Characterization

The μBF directivity was also evaluated through an acoustic test by using the measurement setup shown in Fig. 16(a). A small water tank was mounted on top of the chip. An unfocused single-element probe was immersed in the water and was driven by a continuous 10-MHz sinusoidal wave to transmit acoustic waves to the chip at different incidence angles of 0°, 11°, and 23°, aligned with the azimuth direction of the chip. The single-element probe was accurately positioned on a circular trajectory centered at the location of the PZT transducer array, by using a 3-D printed rotating holder (not shown). The μBF of a 2 × 2 sub-array was configured to different steering angles ranging from −50° to 50°, while its output amplitude was recorded and normalized, as shown in Fig. 16(b). The theoretical ideal directivity curves are also plotted, which show a good alignment with the measured data. As shown in Fig. 16(c), at a specific incidence angle of 0°, the change in output amplitude for different μBF steering angles clearly shows the expected μBF directivity and the consequential spatial filtering effect.

The same test bench was also used for an imaging experiment, by replacing the single-element probe with three needle reflectors positioned at about 8 mm above the chip [34]. The ASIC was used to generate three-cycle 30-V pulses for pulse TX and to capture the returning echo signals. An image was generated using DAS beamforming with coherence factor weighting [35]. The resulting B-mode image in an azimuthal plane is shown in Fig. 17(a), which clearly shows the positions of the needles, while a rendered 3-D image based on the same recording is shown in Fig. 17(b), where the needle heads are clearly distinguishable from the background even with the small aperture size of 0.8 × 0.8 mm^2.

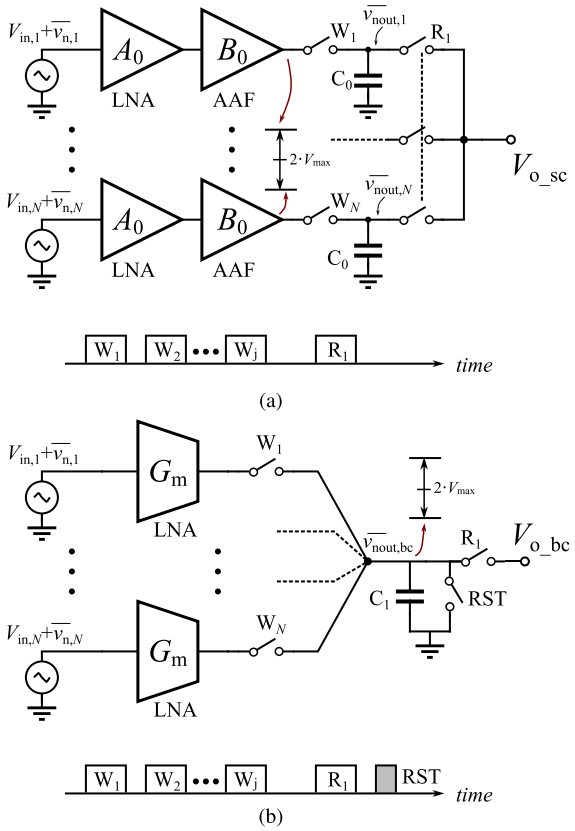

Fig. 18. (a) Simplified switched-capacitor-based μBF for noise calculation. (b) Simplified boxcar-integration-based μBF for noise calculation.

The performance and characteristics of our work and the prior have been summarized in Table I. Compared to prior μBF designs, this work achieves the smallest array pitch, the highest center frequency, and the smallest μBF area per channel.

VI. Conclusion

This article has presented a 100-μm-pitch-matched transceiver ASIC with a boxcar-integration-based RX μBF and an element-level TX. For N input channels, the presented μBF reduces the total number of memory cells by a factor of N compared to a conventional μBF employing discrete-time delay lines, thus saving area, and combines boxcar integration with built-in anti-aliasing filtering, thus relaxing the design requirements of the AFE and further reducing the area. Active boxcar integration has been implemented to make the μBF less sensitive to parasitic capacitance, followed by a ping-pong S/H and a high-efficiency output buffer. A novel TX scheme has been implemented allowing area-hungry devices, such as the HV PMOS/NMOS, to be moved to the periphery of the chip, and only using a small-sized HV diode as the element-level isolation plus an HV NMOS as the T/R switch. All these features make the design very compact and allow us to integrate more complicated functions, such as an AFE with continuous TGC, on the chip in a pitch-matched fashion.

Appendix

In this appendix, we derive the total capacitance required to obtain a given output SNR, for both a μBF based on switched-capacitor delay lines [as in Fig. 3(d)] and for the proposed boxcar-based μBF [as in Fig. 4(a)]. Fig. 18(a) shows a simplified switched-capacitor μBF for noise calculation, which consists of N voltage-mode LNAs with a gain of A_0, N AAFs with a bandwidth of B_0, sampling switches controlled by clock signals W_{1-N} and R_1, and sampling capacitors C_0. $V_{\text{in},1-N}$ and $\bar{v}_{\text{n},1-N}$ represent the input voltage and the equivalent input-referred noise of the LNAs and AAFs, respectively. All noise sources are independent white noise with power spectral density (PSD) of S_0. We assume that the maximum peak output swing at all AAFs' outputs is V_{max}. During a write phase, delays are applied to each channel and accurately controlled by the write clock W_{1-N}, followed by the summation in the following read phase. At the end of the write phase, the amplified and band-limited noise of each LNA and AAF, as well as the noise of the sampling switch W_i, is sampled on the capacitor C_0, and the associated output noise power $\overline{v^2}_{\text{nout},i}$ can be expressed as

$$\overline{v^2}_{\text{nout},i} = {A_0}^2 \cdot S_0 \cdot B_0 + \frac{k \cdot T}{C_0}, \quad (1 \le i \le N). \tag{4}$$

The noise of the N channels is averaged in the following read phase, leading to a maximum SNR_{sc} expressed as

$$\begin{aligned}\text{SNR}_{\text{sc}} &= \frac{V_{\text{max}}^2 \cdot N}{2 \cdot \overline{v^2}_{\text{nout},i}} \\ &= \frac{V_{\text{max}}^2 \cdot N}{2 \cdot \left({A_0}^2 \cdot S_0 \cdot B_0 + \frac{k \cdot T}{C_0}\right)}.\end{aligned} \tag{5}$$

A similar analysis can be applied to the μBF based on boxcar integration, as shown in Fig. 18(b). The voltage-mode LNAs are replaced by transconductance amplifiers with a transconductance of G_{m}, and a short reset phase is required to clear the memory capacitor C_1 after each read phase R_1, giving rise to kT/C noise. At the end of the write phase, the output noise power $\overline{v^2}_{\text{nout,bc}}$ can be expressed as

$$\begin{aligned}\overline{v^2}_{\text{nout,bc}} &= N \cdot {A_1}^2 \cdot S_0 \cdot B_1 + \frac{k \cdot T}{C_1} \\ A_1 &= \frac{G_m}{C_1} \cdot T_0 \\ B_1 &= \frac{1}{2 \cdot T_0}\end{aligned} \tag{6}$$

where A_1 and B_1 are the dc gain and the equivalent noise bandwidth of the boxcar integration, respectively; T_0 is the integration time; and S_0 is the input-referred PSD, which is identical to the input-referred noise PSD of the switched-capacitor μBF. In the following read phase, the maximum SNR_{bc} can be expressed as

$$\begin{aligned}\text{SNR}_{\text{bc}} &= \frac{V_{\text{max}}^2}{2 \cdot \overline{v^2}_{\text{nout,bc}}} \\ &= \frac{V_{\text{max}}^2}{2 \cdot \left(N \cdot {A_1}^2 \cdot S_0 \cdot B_1 + \frac{k \cdot T}{C_1}\right)}.\end{aligned} \tag{7}$$

Note that A_1 should comply with

$$A_1 = \frac{A_0}{N} \tag{8}$$

to achieve the same maximum output swing V_{max}. Substituting (8) into (6) and (7) and letting $C_1 = N \cdot C_0$, $B_1 = B_0$ results in

the same SNR for both μBF structures. We can conclude that the μBF based on boxcar integration requires the same total capacitance as the conventional μBF to achieve a given output SNR, while the proposed μBF architecture still occupies less area in practice factoring in the area needed for AAF, the required space between memory capacitors, the number of switches, and the associated interconnections.

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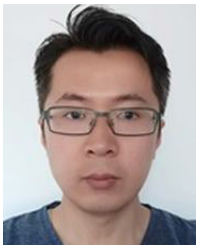

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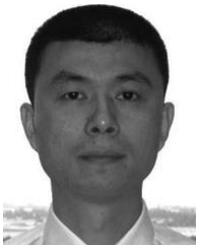

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