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Design and Characterization of a Data Converter in a SiC CMOS Technology for Harsh Environment Sensing Applications

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***Abstract*—This work presents the design and characterization of an analog-to-digital converter (ADC) with silicon carbide (SiC) for sensing applications in harsh environments. The SiC-based ADC is implemented with the state-of-the-art low-voltage SiC complementary-metal-oxide-semiconductor (CMOS) technology developed by Fraunhofer IISB. Two types of ADCs, i.e., a 4-bit flash ADC and a 6-bit successive-approximation (SAR) ADC, are designed and simulated up to 300 degrees Celsius. The measurement results show that the 4-bit SiC flash ADC can operate reliably up to at least 200 degrees Celsius, which outperforms the Si counterpart regarding the maximum operating temperature.**

***Index Terms*—silicon carbide, analog-to-digital converter, harsh-environment**

I. Introduction

In a smart sensing system, the on-chip data conversion from the analog signal to the digital signal is crucial because the digital signal is less vulnerable to interference and noise along the signal path [1]. Thanks to the mature silicon (Si) technology, most data converters are implemented with standard Si integrated circuit (IC) technologies provided by the foundry [2]–[4]. Undeniably, ADCs fabricated with the Si platform have many advantages, such as small area, high yield, and high performance. However, increasing applications, such as space exploration, geological drilling and aviation engine manufacturing, require smart sensors to be placed in harsh environments where the ambient temperature can easily exceed 200°C [5], [6]. At such temperatures, Si electrical components will suffer from significantly higher leakage current and increased intrinsic carrier concentration, which leads to compromised circuit performance [6]–[8].

Silicon carbide (SiC), a well-known wide bandgap semiconductor, has great potential to be the platform for electronics in high-temperature environments. In previous publications, we have demonstrated various sensors and analog/digital circuits, including a 2-bit flash ADC, in an emerging SiC CMOS technology developed by Fraunhofer Institute for Integrated Systems and Device Technology IISB [7], [9]–[11]. The reported flash ADC operated from room temperature to 200°C [9]. However, an ADC with only 2-bit is insufficient in practical use. In addition, the flash ADC is unsuitable for a higher number of bits as it will consume an exponential amount of area with the increasing number of bits.

In this work, we have expanded the flash ADC from 2-bit to 4-bit for better resolution in practical use. The total number of transistors in the circuit increases from 68 to 266 (from 1400 × 2300 μm^2 to 8809 × 1907 μm^2). The 4-bit ADC showed stable operation up to 200°C. To implement ADC with more bits, a 6-bit successive-approximation (SAR) ADC is also designed. The simulation result suggests that the SAR ADC can work up to 300°C. The total area of the SAR ADC is 4850 × 4850 μm^2, consisting of 821 transistors.

II. SiC CMOS Technology

A cross-sectional view of the SiC CMOS is shown in Fig. 1. The process starts with the 4H-SiC wafer with an n-type epitaxial layer. This technology is a double-well process (n-well and p-well) and contains heavily doped n- and p-type regions (sn and sp). Dedicated ohmic contact processes are developed for the sn and sp regions. Thanks to the thick gate oxide (approximately 55 nm), the gate voltage can be up to 25 V. The minimum channel length is 2 μm, which is limited by the lithography tool. Two metal layers and a poly-Si layer are available for interconnection.

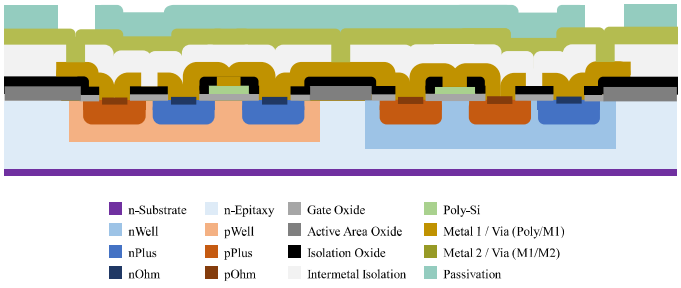

Fig. 1. The cross-sectional view of the SiC CMOS technology.

Financial support by the iRel40 Project is acknowledged gratefully. iRel40 is a European co-founded innovation project that has been granted by the ECSEL Joint Undertaking (JU) under grant agreement NO876659. The funding of the project comes from the Horizon 2020 research program and participating countries.

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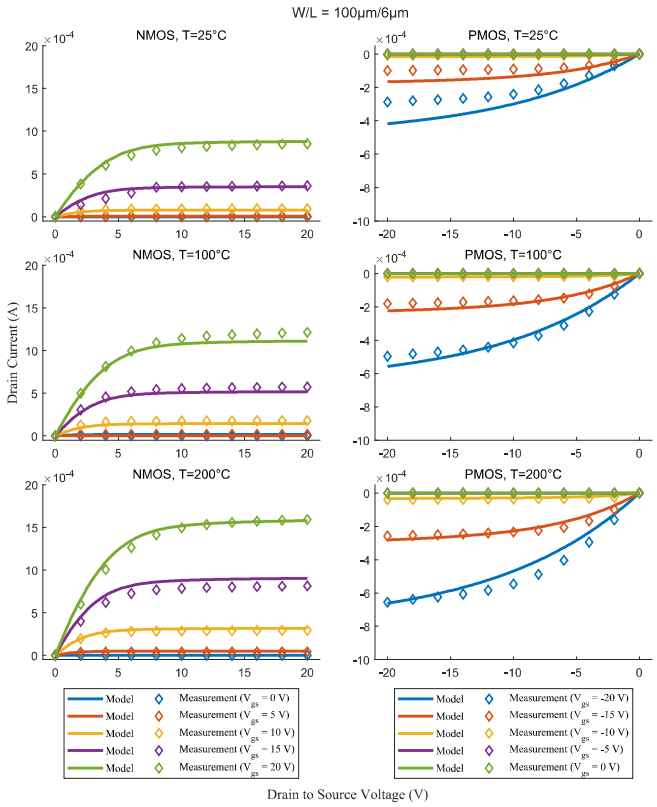

Fig. 2. NMOS and PMOS characteristics under different temperatures (Solid curves and dotted curves indicate simulation result and experimental result, respectively). The measured devices have a size of 100 μm width and 6 μm length

Along with the process, a process design kit (PDK) is also developed by Fraunhofer IISB, which allows users to carry out circuit simulation and layout, layout versus schematic, and design rule checks on commercial EDA software. However, the current version of PDK does not support components other than MOSFETs. Passives like capacitors and resistors will be available in the next Europractice run in 2024.

III. Device Level Evaluation

In this section, the I-V characteristic of the discrete SiC MOSFET was measured to verify the correctness of the model. To compare the difference between NMOS and PMOS, both types of devices with same dimension (W/L = 100 μm / 6 μm) were measured. The measurement was done with a probe station equipped with B1500A Semiconductor Device Parameter Analyzer. The device under test was heated by the chuck to 25°C, 100°C, and 200°C.

The drain current (I_d) as a function of the drain-source voltage (V_{ds}) under different gate-source voltages (V_{gs}) is plotted in Figure 2. From the experimental results, SiC-based MOSFET exhibits a notable advantage by operating reliably at 200°C, where typical Si devices would already fail. As also can be seen, the actual measurement exhibits a good degree of alignment compared to the simulation, as indicated by solid curves in Fig. 2.

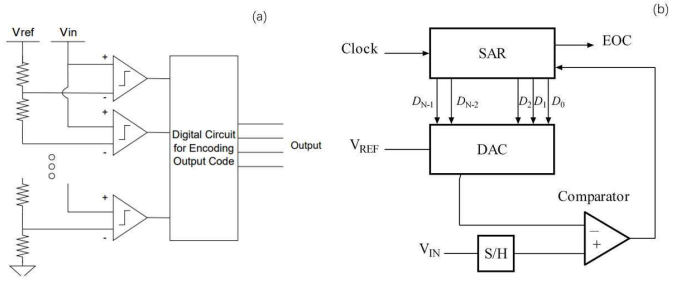

Fig. 3. (a) Overall Structure of the 4-Bit Flash ADC. (b) Overall Structure of the SAR ADC

Fig. 2 also shows that the NMOS has a larger drain current, primarily due to the electron having higher mobility than that of holes. At the same time, the drain current of the NMOS is more significantly affected by temperature variations compared to the PMOS. Therefore, when designing circuits operating over a wider temperature range, it is advisable to consider this effect during device size selection for better performance and stability.

IV. Circuit Design and Measurement

A. 4-Bit flash ADC

The basic structure of the flash ADC used in this paper is shown in Fig. 3(a). It mainly consists of a resistor ladder, comparators, and digital encoding circuitry. The flash ADC employs a linear voltage ladder with comparators placed at each step to compare the input voltage with a series of successive reference voltages. The resistors in the ladder are implemented using the sn region, with a nominal resistance of 20 kΩ at room temperature. Although the resistance of the ladder resistors depends on temperature and the manufacturing

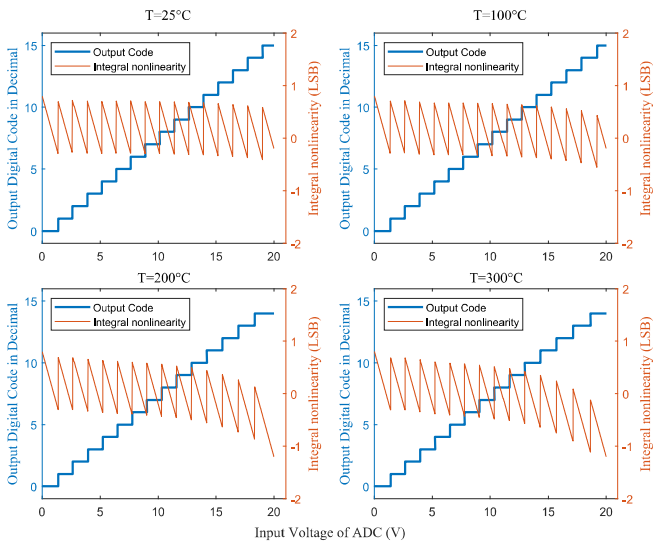

Fig. 4. The simulation result of the 4-bit flash ADC at room temperature, 100, 200, and 300°C.

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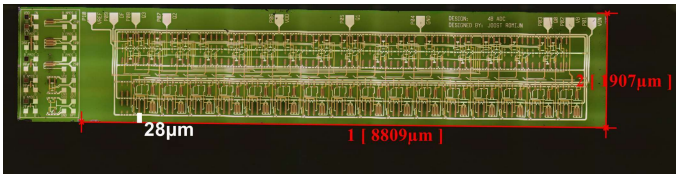

Fig. 5. An optical image of SiC flash-ADC in the SiC CMOS technology.

process, the absolute resistance value is not the key factor in ensuring the precise output of the ADC.

1) Simulation: Fig. 4 shows the Flash ADC design simulation result at 25, 100, 200, and 300 °C. From the simulation results, it can be observed that the SiC-based ADC maintains relatively good linearity up to 300°C. However, when the input voltage approaches the circuit's power supply voltage, the output of the ADC fails to reach the expected maximum value, resulting in a missing code. This is caused by the relatively high threshold voltage of the MOSFETs used in the adopted process. Therefore, the allowable input voltage range of the ADC will be smaller than the circuit's supply voltage unless an additional compensation design is implemented.

2) Measurement: The fabricated flash-ADC is illustrated in Fig. 5. The input/output characteristic was measured with the same setup described in the previous section. Due to the limited temperature of the hotplate, the ADC was only measured up to 200°C instead of 300°C. Figure 6 illustrates the measurement results of the device at various temperatures. The flash ADC shows good stability and linearity over a wide range of temperatures. It can be observed that there are abnormal spikes at specific voltages. During the sweeping of input voltages, only one bit of the flash ADC output can be measured each time (due to the limited number of probe needles), and the data obtained from multiple scans are combined to obtain the complete output of the ADC at each voltage. When the input voltage approaches the critical value of output voltage

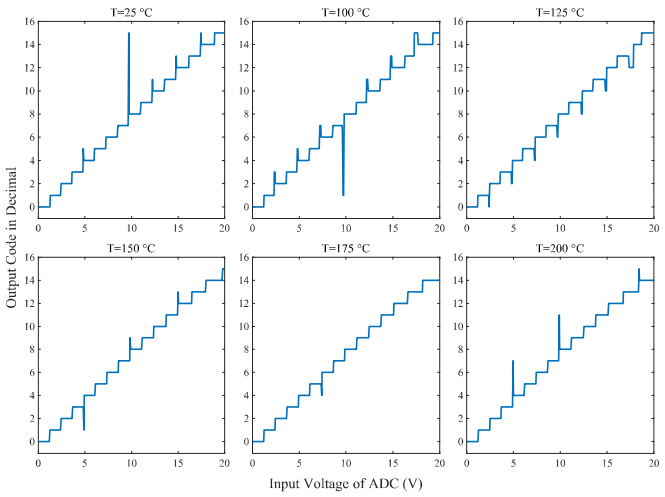

Fig. 6. The measurement result of the 4-bit flash ADC at six temperature points (25, 100, 125, 150, 175, and 200°C).

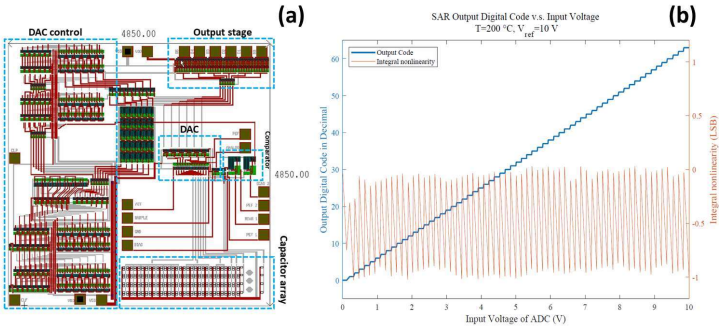

Fig. 7. (a) The layout of 6-bit SiC SAR ADC (4850 × 4850 μm^2 with 821 transistors); (b) The simulation result of the 6-Bit SAR ADC under 300°C.

variation, inconsistencies in the output of a particular bit may occur in multiple sweeps. Therefore, it is inferred that this is not due to significant errors in the ADC output but rather a limitation of the measuring instruments used.

B. 6-Bit Successive Approximation Register (SAR) ADC

Compared to flash ADCs, SAR ADCs require more complex control circuits and have timing requirements. For the current technology, due to the significant variation in the characteristics of individual devices over a wide operating temperature range, the exploration of SAR ADCs will not only verify the feasibility of this ADC implementation but also to some extent, validate whether the technology can be used to implement more complex circuits or even general-purpose processing chips.

Fig. 3(a) represents the basic structure of the Successive Approximation Register (SAR) ADC. Figure 7 displays our SAR ADC design's layout and simulation results, which exhibit good linearity across the entire measurement range. The SAR ADC is currently in fabrication, and its measurement will be in future work.

V. Conclusions

In this work, the 4H-SiC CMOS technology is introduced and regarded as a promising platform for on-chip data conversion in high-temperature environments. The single MOSFET transistor was measured and was proved to function as predicted by the PDK. Two types of ADCs, i.e., 4-bit flash ADC and 6-bit SAR ADC, are designed and simulated up to 300°C. The SiC flash ADC was measured up to 200°C and showed good stability and linearity over a wide range of temperatures. The testing at higher temperatures will be reported in the future to further validate the potential of SIC CMOS platform devices for operation in high-temperature and high-radiation environments. These results enable that multiple sensors and readout circuits can be integrated to address more challenging application scenarios and reduce system costs.

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REFERENCES

[1] K.A.A. Makinwa, "Smart temperature sensors in standard CMOS," Procedia Eng., vol. 5, pp. 930—939, 2010.

[2] X. Tang, X. Yang, J. Liu, Z. Wang, W. Shi, D.Z. Pan, and N. Sun, "A Bandwidth-Adaptive Pipelined SAR ADC With Three-Stage Cascoded Floating Inverter Amplifier," IEEE J. Solid-State Circuits, Early access, pp. 1–11, May 2023.

[3] E. Eland, S. Karmakar, B. Gönen, R. van Veldhoven, and K. A. A. Makinwa, "A 440-μW, 109.8-dB DR, 106.5-dB SNDR Discrete-Time Zoom ADC With a 20-kHz BW," IEEE J. Solid-State Circuits, vol. 56, pp. 1207–1215, Jan. 2021.

[4] Y. Shen, H. Li, H. Xin, E. Cantatore, and P. Harpe, "A 103-dB SFDR Calibration-Free Oversampled SAR ADC With Mismatch Error Shaping and Pre-Comparison Techniques," IEEE J. Solid-State Circuits, vol. 57, pp. 734–744, Mar. 2022.

[5] R. Ramesham, N. Kumar, J. Mao, D. Keymeulen, R.S. Zebulum, and A. Stoica, "Data converters performance at extreme temperatures," 2006 IEEE Aerospace Conf., USA, Mar. 2006.

[6] P. French, G. Krijnen, and F. Roozeboom, "Precision in harsh environments," Microsyst. Nanoeng., vol. 2, pp. 1–12, Oct. 2016.

[7] J. Mo, J. Li, Y. Zhang, J. Romijn, A. May, T. Erlbacher, G. Zhang, and S. Vollebregt, "A Highly Linear Temperature Sensor Operating up to 600°C in a 4H-SiC CMOS Technology," IEEE Electron Device Lett., vol. 44, pp. 995–998, Apr. 2023.

[8] A. Rahman, L. Caley, S. Roy, N. Kuhns, A. Mantooth, J. Di, A. M. Francis, and J. Holmes, "High Temperature Data Converters in Silicon Carbide CMOS," IEEE Trans. Electron Devices, vol. 64, pp.1426–1432, Feb. 2017.

[9] J. Romijn, S. Vollebregt, L.M. Middelburg, B.E. Mansouri, H.W.van Zeijl, A. May, T. Erlbacher, G. Zhang, and P.M. Sarro, "Integrated Digital and Analog Circuit Blocks in a Scalable Silicon Carbide CMOS Technology," IEEE Trans. Electron Devices, vol. 69, pp.4–10, Jan. 2022.

[10] J. Romijn, S. Vollebregt, L.M. Middelburg, B.E. Mansouri, H.W. van Zeijl, A. May, T. Erlbacher, J. Leijtens, G. Zhang, and P.M. Sarro, "Integrated 64 pixel UV image sensor and readout in a silicon carbide CMOS technology," Microsyst. Nanoeng., vol. 8, pp. 114, Oct. 2022.

[11] J. Romijn, L.M. Middelburg, S. Vollebregt, B.E. Mansouri, H.W. van Zeijl, A. May, T. Erlbacher, G. Zhang, and P.M. Sarro, "Resistive and CTAT Temperature Sensors in a Silicon Carbide CMOS Technology," 2021 IEEE Sensors, Australia, Dec. 2021.

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