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# Design of High-Frequency Fast-Rise Pulse Modulators for Lifetime Testing of Dielectrics

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and Peter Vaessen, Member, IEEE

**Abstract**—Penetration of power electronics in the grid has produced a new species of stresses, characterized by fast-rising pulsed waveforms with microsecond rise times repeating at several tens of kilohertz. Analyzing their impact on existing and future insulation systems requires pulse modulators, most often with pulse transformers (PTs), to perform aging and breakdown tests. PT design for klystron loads has been studied extensively albeit for either low repetition rates or short pulse durations. However, capacitive dielectric loads impose additional complex constraints on optimizing leakage ( $L_g$ ) and parasitic capacitance ( $C_d$ ) in order to minimize rise time ( $T_r$ ) and overshoot ( $V_{pk}$ ). Ensuring consistent output pulse shape is crucial since breakdown is sensitive to voltage magnitude. This article discusses these challenges through the design procedure of a modulator prototype capable of producing bipolar pulses up to 14 kV with rise times  $< 2 \mu s$  at frequencies between 10 and 50 kHz. Major challenges, especially core selection, winding design, PT parasitic optimization, breakdown detection, and failure modes, are highlighted. A new PQR equation is derived to model modulators with capacitive loads. Finally, the output pulses are applied across oil-impregnated paper samples to generate statistics on insulation breakdown strength and lifetime at 10 and 50 kHz. Results illustrate a reduction in lifetime and breakdown strength at 50 kHz. This is possibly due to the nonhomogenous distribution of dielectric losses within the oil-paper leading to local hotspots and eventual thermal breakdown. Furthermore, a critical field  $F_c = 21 \text{ kV/mm}$  is found below which the slope of the lifeline decreases dramatically, thereby indicating a shift in the aging mechanism. Potential reasons for this phenomenon are also discussed.

**Index Terms**—Dielectric aging, distributed capacitance, high power, leakage flux, mixed-frequency, oil-paper, pulse modulator, pulsed power, pulse transformer (PT), solid-state transformer (SST), transformer parasitics.

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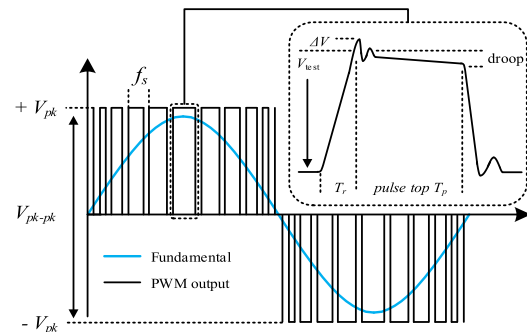


Fig. 1. Typical pulsewidth modulated output of a two-level inverter.

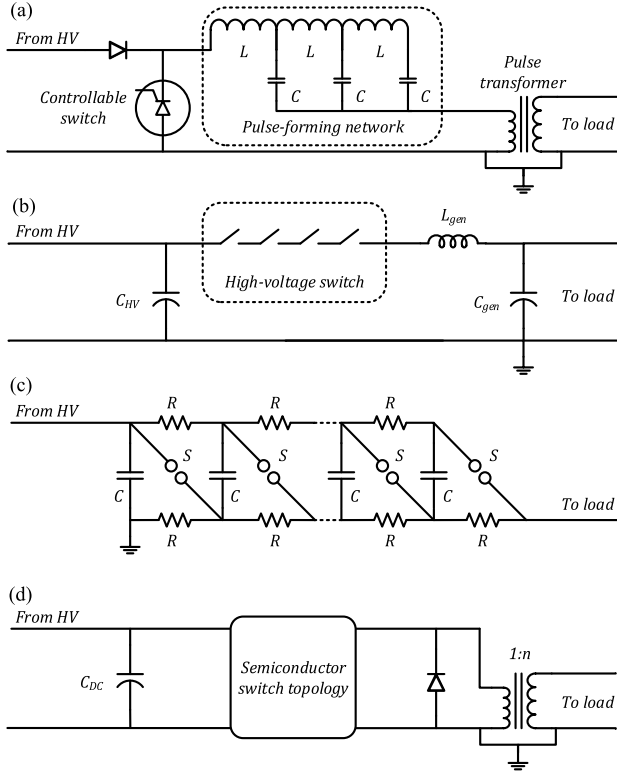
## I. INTRODUCTION

THE ongoing energy transition toward a greener future is facilitated by widespread application of power electronics in the grid. Increased expertise in high power and the introduction of silicon carbide has catalyzed key technologies such as solid-state transformers (SSTs). SSTs are expected to play a vital role in future power systems by offering large energy densities and flexible power flow [1] although at the cost of severe mixed frequency pulsed stresses experienced by the dielectric insulation of their inverter-fed medium frequency transformers (MFTs) [2]. These stresses are characterized by fast-rising pulsed waveforms, as shown in Fig. 1.

In contrast to pure sinusoids, the aging of dielectrics under pulsed stresses is still under investigation. The influence of such waveforms was first observed in an increase of stator winding failures during the widespread application of variable speed drives for motors in the 1980s [3], [4], [5], [6], [7], [8]. Kaufhold et al. [5] showed that time-to-failure can be predicted by an  $n_b$  number of partial discharges (PDs). Yin [6] attributed insulation failure to a combinatory effect of PD, dielectric heating, and space charge formation. Her work demonstrated that the frequency dependence of insulation lifetime differs under either pulsed or sinuous stress [7]. Montanari et al. [8] separated aging mechanisms above and below the PD inception voltage (PDIV). Cavallini et al. [9] identified pulse magnitude as the dominating aging factor apart from frequency, rise time, polarity, and duty cycle. More recent works by Wang et al. [10] studied PD characteristics under square waveforms and assessed the impact of rise time [11], frequency [12], and duty cycle [13] on aging. Koltunowicz et al. [14], [15] also studied the impact of frequency on oil-impregnated paper insulation (OIP).

**TABLE I**  
TYPICAL PARAMETER RANGES OF INVERTER WAVEFORMS

Parameter	Symbol	Typical range
Peak-to-peak voltage	$V_{pk-pk}$	500 V – 20 kV
Switching frequency	$f_s$	5 Hz – 50 kHz
Pulse rise time	$T_r$	100 ns – 4 $\mu$ s



**Fig. 2.** Popular modulator topologies. (a) Line-type modulator. (b) Series HV-switch. (c) Marx generator. (d) LV-switch with PT.

However, despite extensive literature, lifetime statistics under pulsed waveforms are not available above a few kilohertz. Since MFT insulations experience pulses up to 50 kHz, filling this research gap forms the first core motivation of this article.

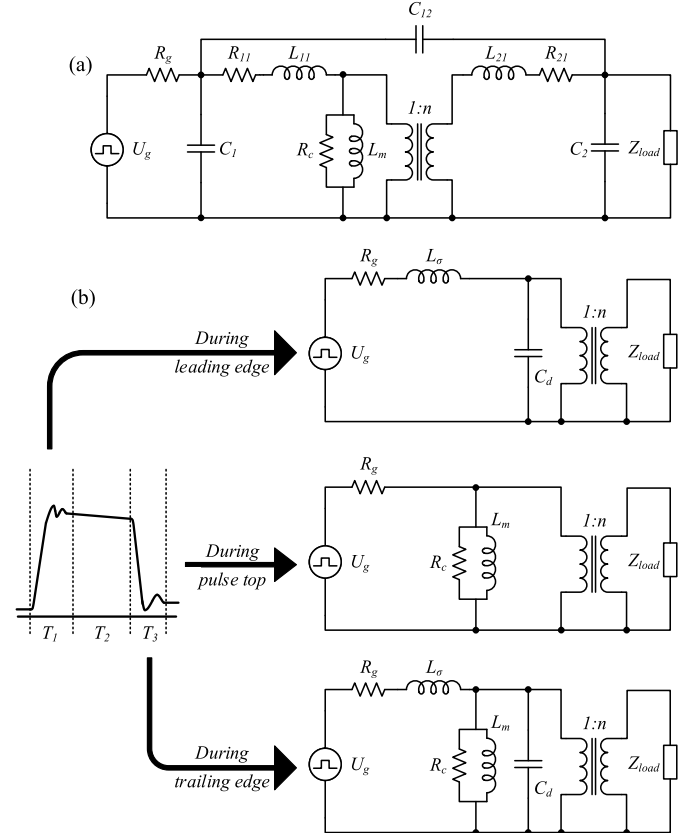
Analyzing the impact of pulsed waveforms requires pulse modulators to produce quick quasi-rectangular voltages across dielectric samples. An important modulator component is the pulse transformer (PT), the design of which has been studied in-depth such as in klystrons [16], [17], [18], treating air pollution [19], and cancer radiation therapy [20], [21]. However, the capacitive nature of dielectrics needs significantly more complex PT design criteria for lifetime tests. The derivation and description of these criteria form the second core motivation of this article.

Typical values of pulse waveform parameters for two-level SST inverters compiled from [22] and [23] are summarized in Table I. Four popular modulator choices are shown in Fig. 2. Line type is not picked due to limited pulse shaping [24]. The Marx generator is limited in repetition rate and requires many stages decreasing reliability [25], [26]. Series HV switches are suitable and have been used extensively for dielectric tests in the literature [27], [28]. However this topology requires:

- 1) a high-voltage dc source which can be quite expensive;
- 2) high-voltage switches that can be expensive to procure;

**TABLE II**  
COMPARISON OF MODULATOR TOPOLOGIES

Topology	Advantage	Disadvantage
Line-type	Relatively compact	Limited shape control
Series HV-switch	Simple design	$\uparrow$ Cost (source, switch)
Marx generator	Sourced at LV	$\uparrow N_{stages} = \downarrow$ reliability
LV-switch + PT	Flexible control	Transformer parasitics



**Fig. 3.** (a) IEEE 390 equivalent PT circuit and (b) splitting into three separate circuits for modeling characteristics during each pulse duration.

- 3) series inductance to limit current after dielectric breakdown.

Considering the points mentioned in Table II, the LV-switch with PT topology was finally selected. This setup can be sourced at 230 V, implemented with inexpensive switches, produces both unipolar/bipolar pulses, and also has a short-circuit limitation from the inductance of the PT.

## II. MODULATOR MODEL

Due to their diverse application set, pulse modulators have been modeled extensively to predict the output waveform at a certain operating point. The standard IEEE 390 model [29] is shown in Fig. 3(a) with the following elements:

- 1) ideal transformer of ratio  $n$ ;
- 2) ideal pulse generator  $U_g$ ;
- 3) output load impedance  $Z_{load}$ ;
- 4) winding resistances  $R_{11}$ – $R_{21}$ ;
- 5) leakage inductances  $L_{11}$ – $L_{21}$ ;

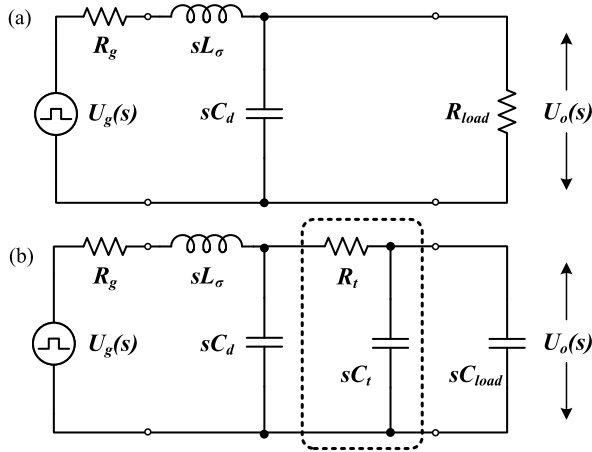


Fig. 4. Equivalent PT circuit with (a) resistive and (b) capacitive loads.

- 6) distributed winding self-capacitances  $C_1$ – $C_2$ ;
- 7) interwinding capacitance  $C_{12}$ ;
- 8) core-loss resistance  $R_c$  and magnetizing inductance  $L_m$ .

In the time domain, a pulse can be divided into three unique portions, i.e., leading edge T1, pulse top T2, and trailing edge T3. The dynamics during these durations can be studied separately as shown in Fig. 3(b) (remains applicable to the nanosecond scale [16]). In T1, shunt  $R_c$  and  $L_m$  are removed due to negligible core excitation in short rise times. In T2, series  $L_\sigma$  and shunt  $C_d$  is neglected since only low-frequency components are present. Parameters of interest are rise time ( $T_r$ ) and overshoot ( $\Delta V$ ) in T1 and pulse droop in T2. Since tests will be performed with bipolar pulses, T3 parameters, such as settling time will have no impact on the output. In Section II-A, a relation from  $T_r$  and  $\Delta V$  to PT parameters  $L_\sigma$  and  $C_d$  is derived for resistive and capacitive loads.

#### A. For Resistive Loads

The equations for resistive-load PTs, as shown in Fig. 4(a), were first derived by Glasoe and Bostick [30] of the MIT Radiation Laboratory in 1948. This combined with [16] linked the transformer leakage flux  $L_\sigma$  and parasitic capacitance  $C_d$  with the parameters rise time  $T_r$  and peak overshoot  $\Delta V$  as

$$2R_{load} \cdot \sigma = \sqrt{\frac{L_\sigma}{C_d}} \quad (1)$$

$$T_r = 2\pi \cdot T_{10\%-90\%} \sqrt{L_\sigma C_d} \quad (2)$$

where  $\sigma$  is the damping coefficient and  $T_{10\%-90\%}$  is the time taken for voltage magnitude to rise from 10% to 90%. The key observation was that rise time reduction requires minimizing parasitic product  $L_\sigma C_d$  while peak overshoot reduction requires minimizing parasitic ratio ( $L_\sigma/C_d$ ) causing a resulting in an inherent trade-off requiring compromise. Bortis et al. [16] showed the product depends on physical design, while the ratio depends on the choice of transformer interconnections.

#### B. For Capacitive Loads

Unlike the above equations, pulse modulators for dielectric testing will instead see a load insulation sample modeled as a

capacitance. However, this  $C_{load}$  would be added to parasitic  $C_d$  causing zero damping (high overshoots) and longer rise times

$$\sigma \propto \frac{1}{R_{load}} \sqrt{\frac{L_\sigma}{(C_d + C_{load})}} \xrightarrow{R=0} 0 \quad (3)$$

$$T_r \propto \sqrt{L_\sigma (C_d + C_{load})}. \quad (4)$$

A possible solution is to add in this article is to add test elements  $R_t$  and  $C_t$ , as shown in Fig. 4(b). The inclusion of  $R_t$  decouples transformer-load dynamics, while the  $R_t C_t$  combination filters the output pulse waveform with a cutoff frequency:

$$F_c = \frac{1}{2\pi \cdot R_t C_t}. \quad (5)$$

Since  $C_{load}$  depends on both electrode arrangement and insulation sample thickness and permittivity, this pulse tuning capability is necessary in order to ensure consistent waveform shape throughout all tests, considering that breakdown is most sensitive to peak voltage. Furthermore,  $R_t$  limits steady-state short-circuit current through the modulator after dielectric breakdown occurs, while the transformer inductance slows down the dynamic current-rise providing a sufficient time window to disconnect the modulator from the load. The addition of  $R_t$  and  $C_t$  thus results in a third-order circuit. After simplifications, the output voltage can be expressed as

$$U_o(s) = \frac{U_g}{s L_\sigma C_d R_t C_{eq}} \times \frac{1 + s R_t C_{eq}}{s^3 + s^2 \left( \frac{1}{R_t C_{eq}} + \frac{1}{R_t C_d} \right) + s \left( \frac{1}{L_\sigma C_d} \right) + \left( \frac{1}{L_\sigma C_d R_t C_{eq}} \right)}. \quad (6)$$

Setting  $C_{eq} = C_t + C_{load}$  and  $R_g \approx 0$ , the equation becomes:

$$U_o(s) = \frac{U_g}{s} \times P Q \times \frac{1}{s^3 + s^2 R + s P + P Q} \quad (7)$$

$$P = \frac{1}{L_\sigma C_d} \quad Q = \frac{1}{R_t C_{eq}} \quad R = \frac{1}{R_t} \left( \frac{1}{C_{eq}} + \frac{1}{C_d} \right) \quad (8)$$

where parasitics parameter ( $P$ ) represents transformer dynamics, quality parameter ( $Q$ ) represents the dynamics of the  $R_t C_{eq}$  filter, and relational parameter ( $R$ ) represents the coupling between  $P$  and  $Q$ .

This PQR (7) can be solved for  $u_o(t)$  with varied values of  $L_\sigma C_d R_t C_t$  from a default  $L_\sigma = 250 \mu\text{H}$ ,  $C_d = 200 \text{ pF}$ ,  $R_t = 10 \text{ k}\Omega$ ,  $C_t = 60 \text{ pF}$ , and  $C_{load} = 50 \text{ pF}$  to illustrate the impact of each element.

From Fig. 5(a), achieving faster rise times and lower overshoots clearly requires minimization in transformer parasitics. However, it also shows that even unrealistically low values of  $L_\sigma C_d$  produce an almost critically damped response, further demonstrating the limitations when designing transformers for capacitive loads.

On the other hand, the advantageous effect of  $R_t C_t$  is shown in Fig. 5(b) where an increase of either results in lower cutoff frequency and lower overshoot. It is thus vital to have these test elements for tuning output pulse shape for dielectric tests with different electrode arrangements and insulation permittivities.

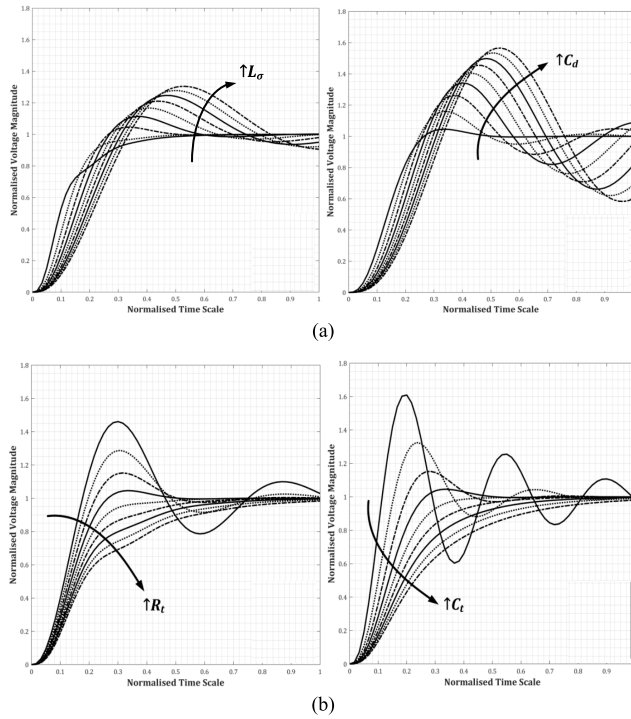


Fig. 5. Effect of (a) parasitics and (b) test elements on output.

 TABLE III  
 DESIRED PULSE MODULATOR SPECIFICATIONS (SEE FIG. 7)

Parameter	Symbol	Usual range
DC link voltage	$V_{in}$	230 V
Maximum test voltage	$V_{test}$	14 kV <sub>pk-pk</sub>
Transformer turns ratio	$n$	1:50
Pulse repetition rate	$f_s$	10 – 50 kHz
Pulse overshoot	$\Delta V$	< 1 % $V_{test}$
Pulse rise (0-100%)	$T_r$	< 20 % $(2f_s)^{-1}$
Load capacitance	$C_{load}$	30 pF

### III. MODULATOR PROTOTYPE

This section describes the design of a modulator with desired specifications in Table III. Input is 230 V fed from ac mains. An output of 14 kV<sub>pk-pk</sub> is required for testing samples. Load capacitance  $C_{load} = 30$  pF is calculated for a single-layer OIP sample of thickness 150  $\mu$ m and an electrode diameter of 2.54 mm. The turns ratio of  $n = 50$  was chosen to reduce primary turns. Pulse frequency should be variable from 10 to 50 kHz for studying the impact of frequency on dielectric lifetime. Minimal overshoot is imperative since sample breakdown is mostly sensitive to peak voltage magnitude. The modulator should be capable of producing sustained pulses over several hours for lifetime tests without any waveform change. There should exist a reliable method for applying a 1 kV/s ramp rise during breakdown tests. Finally, the modulator should disconnect within a short time frame to reduce electrode breakdown marks.

Unlike sine-wave transformers, PTs transmit a bandwidth of frequencies [ $f_{lower}$ ,  $f_{upper}$ ]. The frequency spectrum of a sample 50 kHz pulse is analyzed in Fig. 6. The  $f_{lower}$  is limited

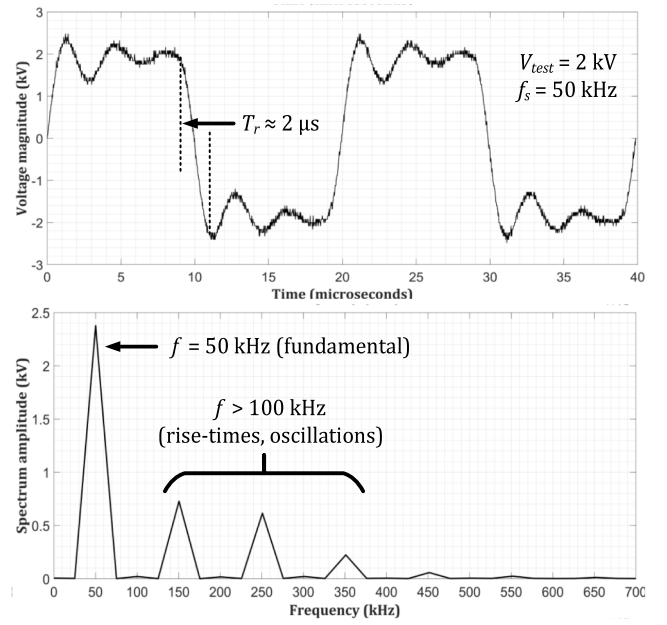


Fig. 6. Fourier analysis of sample 2-kV 50-kHz pulse.

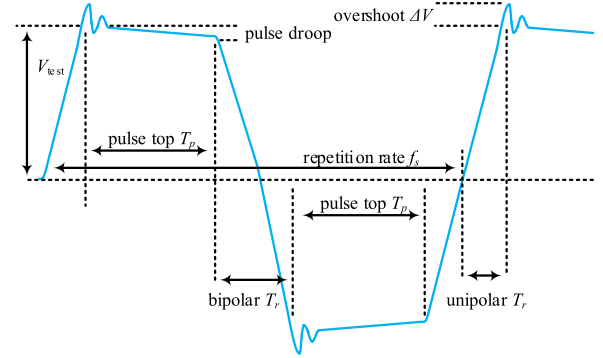


Fig. 7. Definitions of bipolar pulse waveform parameters.

 TABLE IV  
 N87 MNZN TDK MAGNETIC CORE PARAMETERS

Parameter	Symbol	Usual range
Saturation flux at 25°C	$B_{sat}$	500 mT
Cross-sectional area	$A_e$	840 mm <sup>2</sup>

by the core saturation criteria, while  $f_{upper}$  limited by  $L_\sigma$  and  $C_d$  winding parasitics. The fundamental dominates, but there also exists a significantly higher frequency content in the range of several hundreds of kilohertz corresponding to rise times. The pulse waveform parameters are defined, as shown in Fig. 7.

#### A. Magnetic Core

The magnetic core tightly bundles the flux lines within itself, increases magnetic field density, and improves linking between the windings. Commonly used materials include iron-based alloys (high  $B_{sat}$  but high losses) and soft ferrites (low  $B_{sat}$  but low losses). The unipolar PT in [6] used an amorphous iron-based magnetic alloy from Metglas USA with a  $B_{sat} = 1.6$  T. However, such cores are expensive and highly lossy for faster sustained repetition rates. Instead, an N87 MnZn ferrite



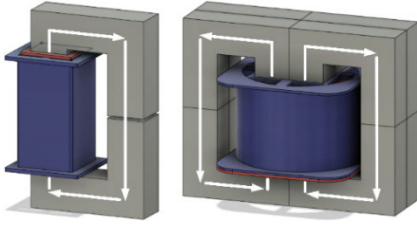


Fig. 8. Comparison of two-core (left) and eight-core (right) geometries.

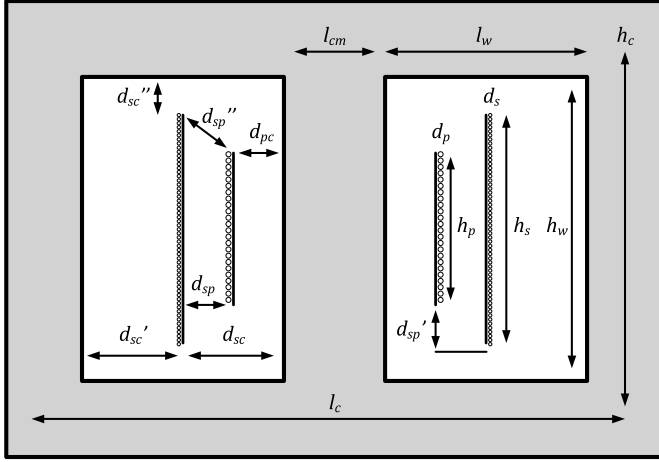


Fig. 9. Geometrical parameters of PT design (not to scale).

U-core from TDK was selected with specifications detailed in Table IV. This selection of a ferrite core now imposes limitations on the saturation prevention criteria. The maximum flux swing ( $\Delta B = 2B_{\max}$ ) under a bipolar excitation depends on the volt-per-turn ( $V_{\max}/n_1$ ), and the pulse duration  $T_p$  and core cross section are expressed as

$$B_{\max} = \frac{V_{\max} \cdot T_p}{2 \cdot n_1 \cdot A_e}. \quad (9)$$

An operating  $B_{\max} = 400$  mT was selected considering the increase in temperature (decrease in  $B_{\text{sat}}$ ) due to core losses. The required primary to prevent core saturation at 10 kHz is

$$\Rightarrow n_1^{\min} = \frac{230 \text{ V} \cdot 50 \mu\text{s}}{2 \cdot 400 \text{ mT} \cdot 840 \text{ mm}^2} \approx 17 \text{ turns}.$$

However, this would lead to drastically high  $L_\sigma$  values, high overshoots, and slow rise times. To reduce the  $L_\sigma$  Klystron modulators commonly have a single turn primary ( $n_p = 1$ ) to reduce the leakage flux, but this is only possible when producing pulses of short duration  $\approx 5 \mu\text{s}$  [16] or at low repetition rates [31], [32]. An eight-core structure (Fig. 8) is used instead for a fourfold increase in cross section, thereby reducing the criteria to  $n_p = 4$ . This design also reduces the effective reluctance improving magnetic linkage.

### B. Winding Design

Designing an optimal winding involves balancing sufficient clearances (which cause flashovers) and transformer parasitics (which affect pulse performance). These tradeoffs are further strained due to the limited window size of the chosen N87 core. The geometrical parameters of the PT design are shown in Fig. 9.

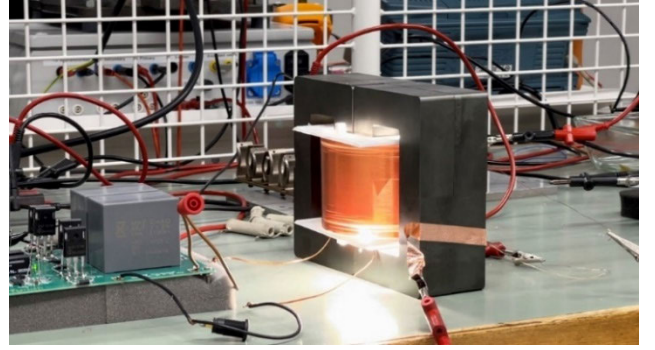


Fig. 10. Flashover at  $V_{\text{test}} = 17 \text{ kV}_{\text{pk-pk}}$  between the highest potential of HV to LV winding due to an insufficient  $d_{\text{sp}}''$  isolation distance.

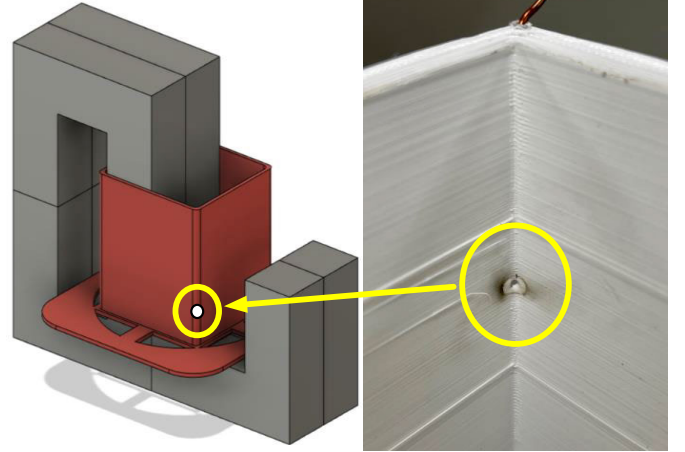


Fig. 11. Structure damage due to repeated LV-core discharges.

1) **Primary Winding Parameters:** Foil windings are ideal for reducing leakage ( $h_p = h_s$ ), but their construction can be quite difficult for  $n_p > 1$ . Enamelled wire can be used instead despite a relatively larger leakage. This  $L_\sigma$  can then be reduced by spreading the turns across  $h_p$ , but this also reduces  $d_{\text{sp}}''$  isolation leading to severe HV-LV flashovers, as shown in Fig. 10. As a tradeoff, silicon insulated (thickness 3 mm) wire was selected.

Winding currents of the PT can be calculated as:

$$I_s = 4 \cdot \frac{C_{\text{load}} \cdot V_{\text{test}}}{T_r} = 4 \cdot \frac{30 \text{ pF} \cdot 7 \text{ kV}_{\text{pk}}}{4 \mu\text{s}} \approx 210 \text{ mA} \quad (10)$$

$$I_p = n \cdot I_s = 50 \cdot 210 \text{ mA} \approx 10.5 \text{ A} \quad (11)$$

hence,  $d_p = 2$  mm is selected for a  $3\text{-A/mm}^2$  current density. The final measured height of the primary winding is  $h_p = 35$  mm and  $d_{\text{pc}} = 3$  mm is now the thickness of the wire silicon insulation. Secondary energization induces a potential onto the core causing LV-core discharges leading to damages on the LV structure, as shown in Fig. 11. This potential was estimated with finite element analysis (FEA) and measured with an electrostatic voltmeter to be 0.3 times the  $V_{\text{test}}$  magnitude. The core is thus grounded and  $d_{\text{pc}}$  is kept as short as possible to provide flexibility for other tradeoffs.

Improper grounding can cause discharges between core pieces, only diagnosed with auditory feedback. Each core interface was then coated with a 1:1 (catalyst:base) paste mixture of TFC Silicone Rubber Type 3 and conductive carbon

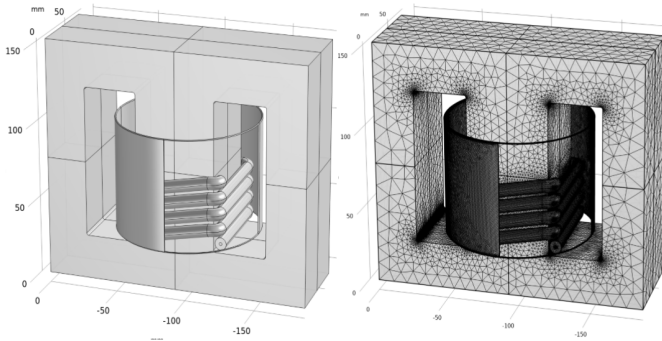


Fig. 12. Three-dimensional FEA model and mesh of prototype PT.

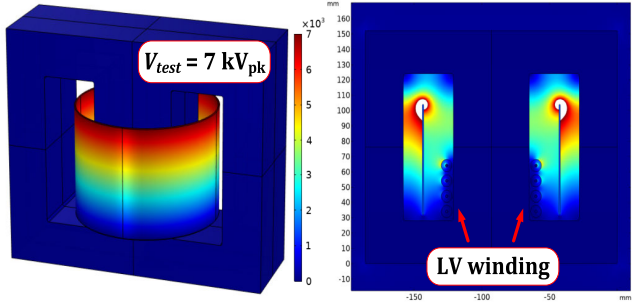


Fig. 13. HV potential distribution (left: 0–7 kV<sub>pk</sub>) and E-field magnitudes inside PT window from FEA (right: 0–0.5 kV/mm).

black. Larger paste volumes can decrease inductance and cause pulse droop.

2) *Secondary Winding Parameters*: An enameled wire of  $d_s = 0.35$  mm is selected to construct a 200-turn secondary HV winding of height  $h_s = 70$  mm. This is made in a single layer so as to reduce  $C_d$  parasitic. The transformer is 3-D modeled for FEA, as shown in Fig. 12. Secondary voltage  $V_{test}$  is implemented as a gradient along the HV winding length.

The vertical position of the primary winding ( $d'_{sp}$ ) influences the HV–LV field stresses and is hence set to 0 mm to limit the average field strength to 500 V/mm, as shown in Fig. 13. The largest possible vertical clearance between the highest potential of the HV winding to the grounded core is  $d''_{sc} = 20$  mm for this core. It can be seen in Fig. 13 that the highest field stresses occur at the top of the HV winding. This can be studied with an  $xy$  2-D cut plane slicing the transformer model, as shown in Fig. 14. The curvature of the secondary results in two critical points, i.e., at  $d'_{sc}$  inside the transformer and at an external distance  $d'''_{sc}$  (Fig. 14). Since an increase in either of these clearances reduces the other, an optimal balance is found at  $d'_{sc} = 12.5$  mm and  $d'''_{sc} = 11.5$  mm through FEA. The average field strength in this area also satisfies the 500-V/mm limit. The peak stresses here are improved by applying insulating grease on the winding. It should also be noted that liquids are unsuitable as an alternative medium due to nonunity permittivities ( $\epsilon_r \neq 1$ ) multiplying with  $C_d$  parasitic. SF<sub>6</sub> can offer desirable properties but is not considered due to negative environmental impact, and high-pressure gases will require expensive gas-tight enclosures.

3) *Parasitic Evaluation*: The final prototype is shown in Fig. 15 and summarised in Table V. The silicon-insulated LV is contained inside the HV, both of which were designed in CAD and 3-D printed in polylactic acid (PLA). The core is

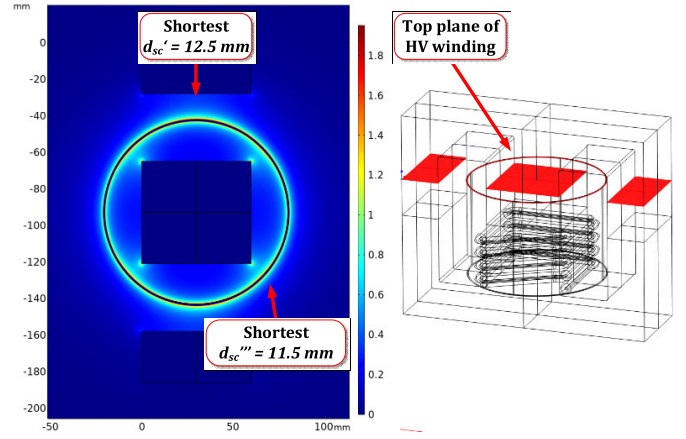


Fig. 14. Obtained E-field magnitudes (left: 0–1.9 kV/mm) and studied 2-D  $xy$  cut plane at the top of HV winding (right: red).

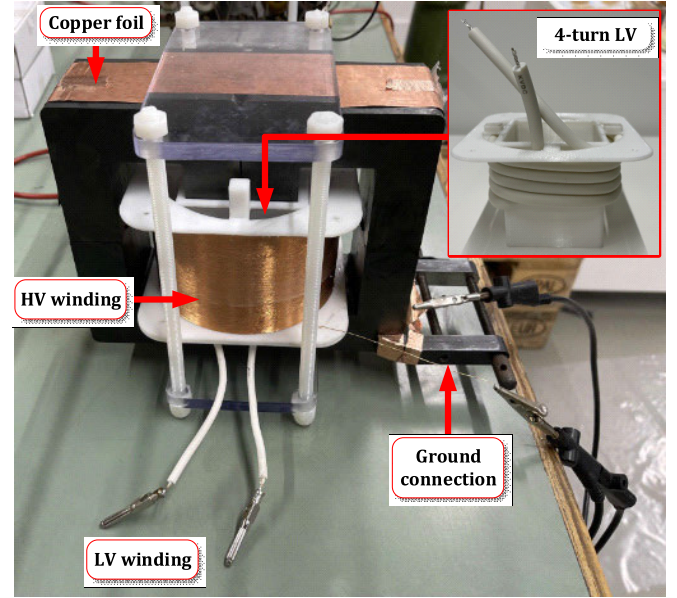


Fig. 15. Final PT prototype (note that LV is shown inverted here).

TABLE V  
SUMMARY OF FINAL PT GEOMETRY VALUES (REFER FIG. 9)

Primary LV	Secondary HV	Core
$n_p = 4$ turns	$n_s = 200$ turns	$N_c = 8$ core pieces
$d_p = 2$ mm stranded	$d_s = 0.35$ mm solid	$h_c = 152$ mm
$h_p = 35$ mm	$h_s = 70$ mm	$l_c = 186$ mm
$d_{pc} = 3$ mm	$d_{sc} = 22.5$ mm	$l_{cm} = 20$ mm
$d_{sp} = 10$ mm	$d'_{sc} = 12.5$ mm	$h_w = 96$ mm
$d_{sp}' = 0$ mm	$d_{sc}'' = 20$ mm	$l_w = 37$ mm
$d_{sp}'' = 45$ mm	$d_{sc}''' = 11.5$ mm	$A_e = 3360$ mm <sup>2</sup>

uniformly grounded and held together in a plexiglass frame. Measured PT parasitics are  $L_\sigma = 730$   $\mu$ H and  $C_d = 25$  pF.

### C. Variable Test Elements

Test elements include a series  $R_t$  and a parallel  $C_t$ , which can tune output pulse shape and ensure consistency across tests.

$R_t$  is implemented as a bank of three series sets of five parallel high-power resistors, as shown in Fig. 16. Since



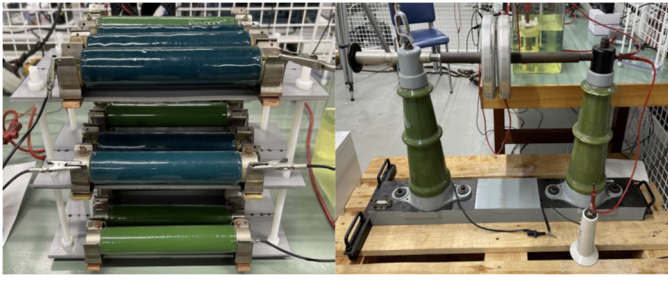


Fig. 16. Left: resistance bank ( $R_t$ ) Right: HV disk capacitor ( $C_t$ ).

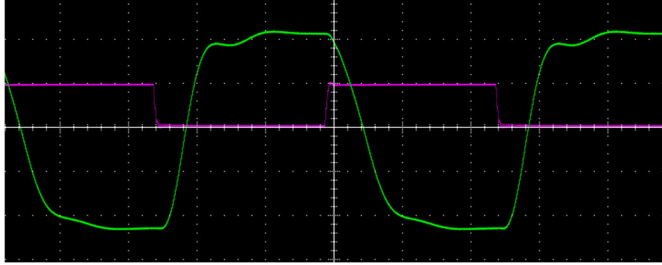


Fig. 17. Pulse shape (green) deformation above  $R_{t\_max} = 20 \text{ k}\Omega$ .

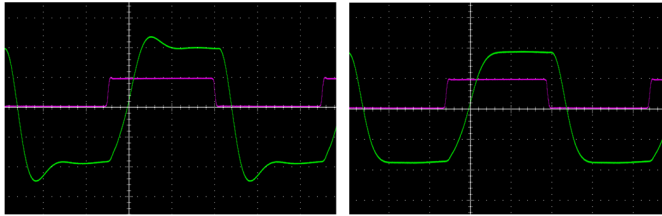


Fig. 18. Pulse shape without (left) and with (right)  $R_t C_t$  elements.

values above  $R_{t\_max} = 20 \text{ k}\Omega$  overdamp the output pulse as shown in Fig. 17, hence,  $R_t = 17.75 \text{ k}\Omega$  is implemented with combinations of 20 and 50  $\text{k}\Omega$ . This reduces the power dissipation per resistor ensuring stable temperatures (and resistance) during long aging tests.

$C_t$  is implemented as a high-voltage capacitor connected in parallel to the test sample, as shown in Fig. 16. The disk diameter is 20 cm and the distance between disks ( $d$ ) can be altered with a rotational handle. Smaller  $d$  increases  $C_t$  and, thereby, the pulse damping, which is important since  $R_t$  alone cannot be used to tune output wave shape ( $R_{t\_max}$  criterion). Typical  $C_t$  magnitudes between tests at 10–50 kHz ranged between 50 and 150 pF.

The impact of tuning  $R_t C_t$  on the pulse shape is shown in Fig. 18.

#### D. Breakdown Detection

In the event of insulation breakdown, the modulator must automatically disconnect the supply in a few milliseconds. In the absence of this function, a conducting arc will gradually burn the oil-paper sample and cause electrode deformation (Fig. 19). To prevent this, an analog circuit was designed in the ESE Laboratory, TU Delft, to detect dielectric breakdown. Since  $(dV/dt)$  of output waveform is high, it cannot be used as a trigger parameter. Instead, the detector is connected in series to and measures overcurrent through the test sample. Furthermore, the current flowing through the capacitive sample increases for higher frequencies, requiring adjustment of overcurrent threshold for breakdown detection.

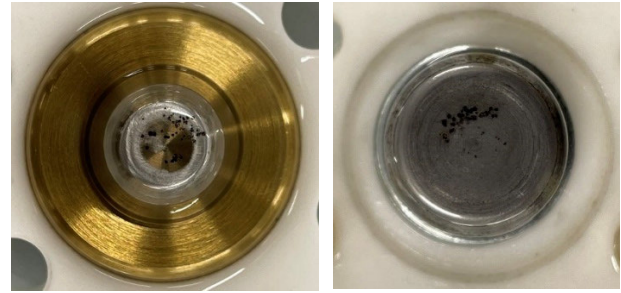


Fig. 19. Electrode breakdown marks requiring sand polishing.

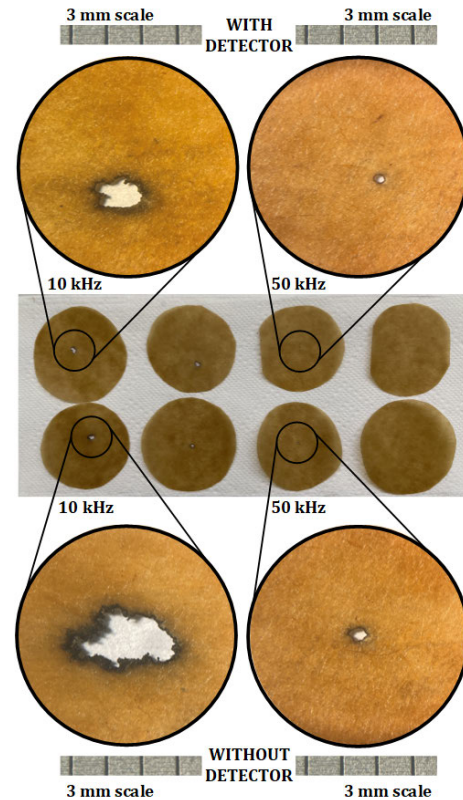


Fig. 20. Effect of sensitivity frequency on breakdown mark.

If the detector is made oversensitive, it would disconnect before dielectric breakdown, statistically neglecting healthy samples. If undersensitive, breakdown arcs are longer leading to carbonization and electrode deformation. Few reference test samples were checked after breakdown under an Olympus SZH-ILLD microscope. The effect of pulse frequency and detection sensitivity is shown in Fig. 20. The burn mark was observed to be sharper at 50 kHz than at 10 kHz.

#### E. Prototype Summary

An overview of the built prototype pulse modulator is shown in Fig. 21. The system operates in the following three stages.

- 1) The source 230-V<sub>AC</sub> mains is isolated through a transformer and rectified to a smooth dc with a thyristor bridge.
- 2) The bridge powers an H-bridge pulse generator PCB, which produces 650-V<sub>pk-pk</sub> bipolar pulses controlled by an Arduino.
- 3) The low voltage pulses are stepped up through the designed 1:50 PT and tuned by test elements  $R_t$  and



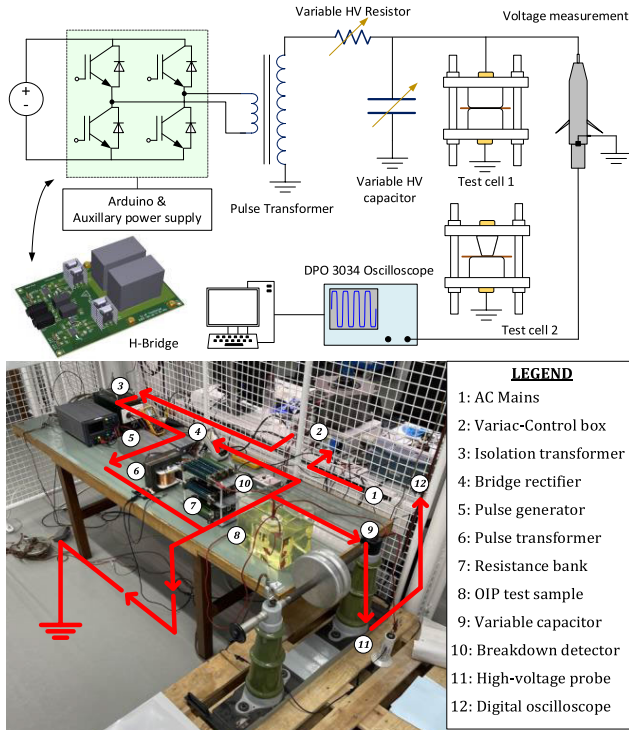


Fig. 21. Overview of modulator prototype for dielectric testing.

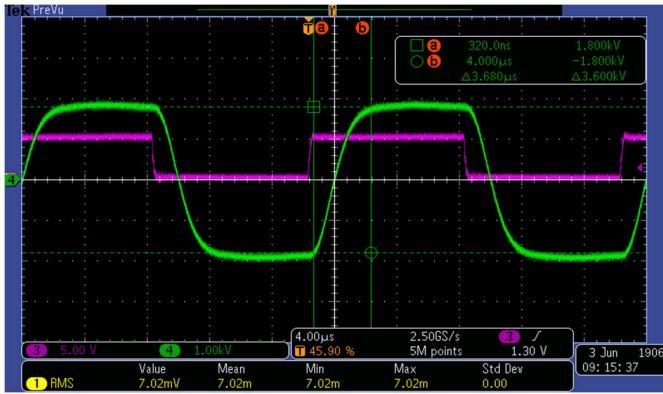


Fig. 22. Measurement of pulse parameters at 50 kHz.

$C_t$  before being applied across the oil-immersed test sample.

The output pulse waveform is analyzed in Fig. 22. The measured rise time  $T_r = 1.84 \mu s$  (Fig. 22) satisfies the  $T_r < 0.2T_p$  criteria in Table III. Measured pulse tops were  $T_p = 6.32 \mu s$  at 50 kHz and  $T_p = 46.32 \mu s$  at 10 kHz. Pulse overshoot was critically damped ( $\Delta V \approx 0$ ) for all tests to study the impact of pulse frequency. The duty cycle was set to 50%. In the next section, these pulses will be applied in tests.

#### IV. DIELECTRIC TESTING

This section applies the modulator prototype to perform dielectric tests. OIP samples with average thickness of  $150 \mu m$  are cut and impregnated inside a vacuum oven as shown in Fig. 23. Samples are kept under oil, transferred to the test setup, and stored later for breakdown pattern analysis [33].

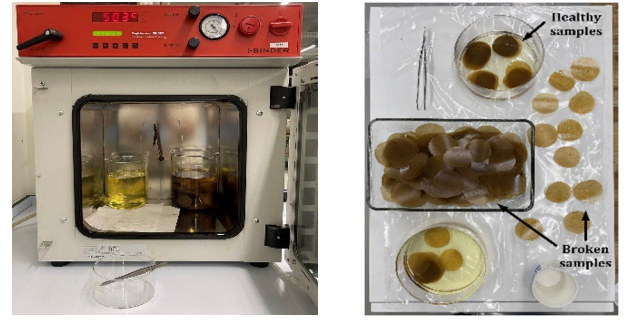


Fig. 23. Preparation workflow of OIP samples for pulsed tests.

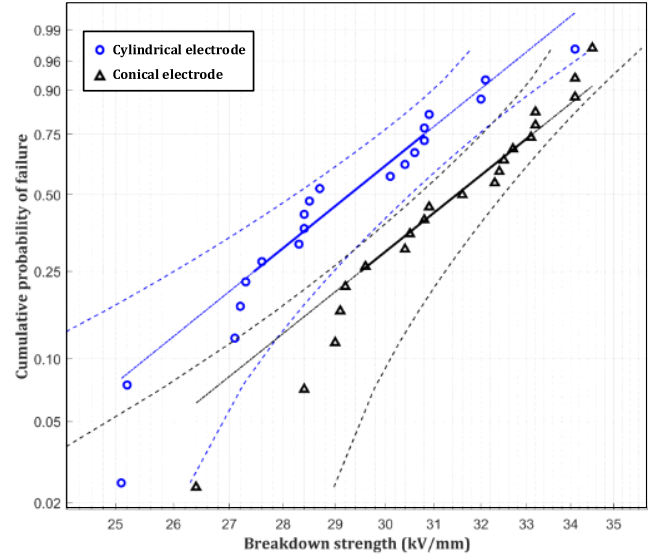


Fig. 24. Breakdown distribution for cylindrical/conical electrodes.

#### A. Breakdown Strength

To determine the breakdown strength of insulation samples with cylindrical and conical electrodes, pulsed waveforms at 50-kHz ramping at  $1 \text{ kV}_{pk}/s$  were applied. The cumulative failure probability  $F(E)$  is linearized across field magnitudes. This is expressed according to the Weibull probability model

$$F(E) = 1 - e^{-\left(\frac{E_{break}}{\alpha}\right)^\beta} \quad (12)$$

Shape parameter  $\beta$  in Table VII is the slope of the resultant line, and scale parameter  $\alpha$  represents  $E_{break}$  at  $F(E) = 63.2\%$ . Plotting  $F(E)$  against breakdown strengths produces Fig. 24. The cylindrical electrode shown in Fig. 19 applies field uniformly across a larger area, thereby lowering breakdown strength (shifted left), and was hence selected for lifetime tests.

#### B. Accelerated Aging

To perform lifetime tests, six  $E$ -field values were chosen with the highest value lower than the lowest breakdown strength  $E_{break} \approx 25 \text{ kV/mm}$  (Fig. 25). A total of 292 tests were performed with 20–41 tests at each field.  $R_t$  temperature was kept  $< 50^\circ \text{C}$  with a fan and measured at intervals. Electrodes were polished after breakdowns. Failure time is plotted logarithmically in Fig. 25. Median lifetimes (blue points) are connected with a best-fit line to obtain lifelines at

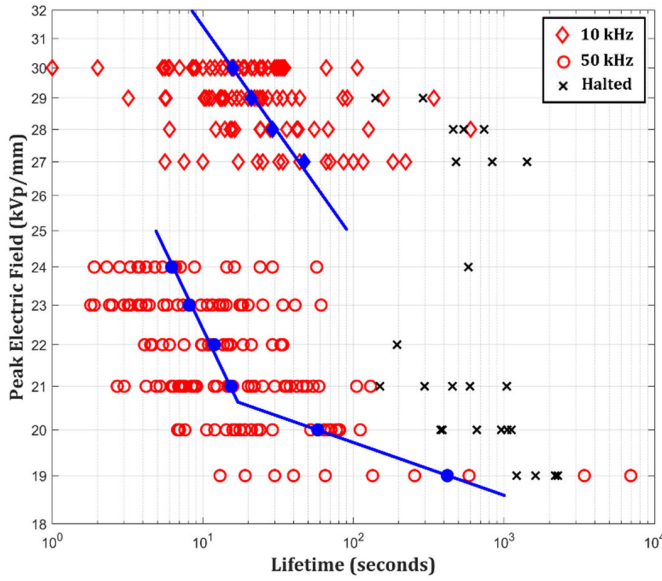


Fig. 25. Obtained lifelines at 10 kHz (red diamonds) and 50 kHz (red circles) by connecting median points (blue points). Halted experiments (black crosses) are included in the median calculation.

TABLE VI

OBTAINED WEIBULL DISTRIBUTION PARAMETERS

Parameter	$\beta$	$\alpha$
Conical electrode	32.3	18.1 kV/mm
Cylindrical electrode	31.3	17.8 kV/mm

10 and 50 kHz. The remaining lifetime can then be expressed as an inverse power law model

$$T_{\text{life}} = k \left( \frac{E}{E_0} \right)^{-n} \quad (13)$$

Constant  $k$  has a unit of time (seconds), while  $E_0$  has a unit of field strength (V/mm). Slope  $n$  indicates the sensitivity of lifetime to field variation. The obtained values are summarized in Table VI.

### C. Analysis of Aging Results

Trends from Fig. 25 can be divided into two aspects.

1) **Frequency Impact:** Dielectric lifetime and breakdown strength at 50 kHz is reduced when compared to 10 kHz. This aligns well with previous observations in the literature between 50 and 1500 Hz [33]. One potential cause is the increased dielectric losses leading to excessive heating in the insulation when stressed with higher frequency components [34]. However, the OIP sample is immersed in oil, an effective thermal conductor with low loss tangent. Hence, it is unlikely that the temperature of the test object would increase. The failure could then be due to the nonhomogenous nature of the oil-paper itself. This would result in an irregular temperature gradient with local hotspots, which eventually cause local (and over time, global) failure of the insulation. Tests at higher frequency produce larger capacitive losses, bring about earlier thermal breakdowns, and hence have shorter failure times.

2) **Electric Field Impact:** Dielectric lifeline at 50 kHz seems to “slow down” below a certain critical field  $F_c \approx 21$  kV/mm. A similar bend has been observed in literature by:

First, Yin et al. [7] indicated that the dielectric losses in magnet wire dramatically increase above the PDIV. These

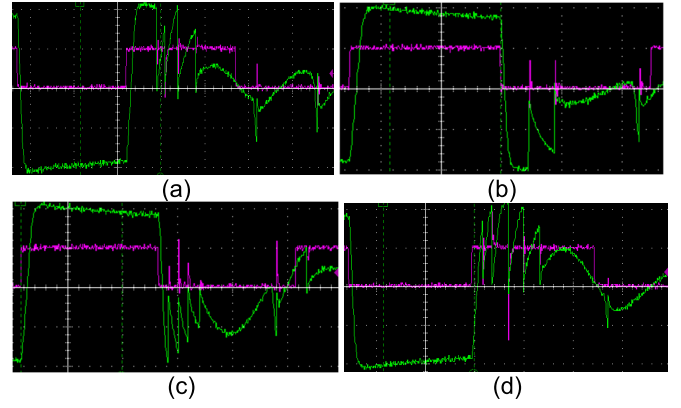


Fig. 26. Observed breakdown instants during. (a) During positive pulse top. (b) During negative pulse top. (c) During pulse fall time. (d) During pulse rise time.

TABLE VII

OBTAINED LIFETIME CURVE PARAMETERS

Parameter	$n$	$k$
10 kHz (above transition)	9.5	$1.7 \times 10^{15}$ s
50 kHz (above transition)	6.9	$2.1 \times 10^{10}$ s
50 kHz (below transition)	37.5	$3.6 \times 10^{50}$ s

TABLE VIII

STATISTICS OF BREAKDOWN INSTANTS OF 20 TESTS AT 10 KHZ

Breakdown instant	Breakdowns	Percentage
Pulse tops	14	70 %
Pulse rise or fall	6	30 %

discharges produce heat within the dielectric leading to higher leakage currents and losses. This PD inception level has been shown to depend on specific pulse parameters [35].

Second, Crine [36] linked space charge injection in polyethylene above a critical field to an accelerated dielectric aging [37]. His work predicted a transition at  $F_c = 18$ –20 kV/mm at which any injected charges that have energies greater than the polymer cohesion energy can break weaker van der Waals bonds and speed up the insulation aging process [38].

Two alternate hypotheses for this bend are also explored.

- 1) Field enhancement in oil-filled voids between individual paper fibers can exceed local PDIV and accelerate aging.
- 2) Field enhancement at electrode edges exceeding local oil PDIV can accelerate aging due to discharges. However the breakdown burn marks from tests were always seen to be at the center, ruling out this explanation.

Although the above correlations sound promising, they must be explored further with extensive statistics specifically with oil-paper insulations. The modulator design presented in this article provides confidence in performing future research to fill this gap. It should also be noted that this phenomenon could not be observed at lower frequencies since the field strengths required for breakdown are far larger than the observed  $F_c$  value. High frequencies allow us to study low-field dielectric dynamics.

Finally, breakdown instants are analyzed in Fig. 26. Statistics from 20 tests given (Table VIII) show that most failures occur at the pulse top. It was seen that failures during pulse rise or fall usually occur at the end of the transition near maximum voltage.

## V. CONCLUSION

This article illustrates the complexities involved in developing pulse modulators for dielectric testing. A new PQR equation is derived to model such systems since existing literature cannot be applied to capacitor loads. The design procedure for a prototype modulator is described: navigating challenges such as tight core saturation criteria, optimization of transformer parasitics, and failure modes. Test elements  $R_t$ ,  $C_t$  allow pulse shaping for consistent testing. Future work is aimed at applying the PQR equation to different modulator prototypes toward building a single comprehensive design optimization model. Breakdown and aging tests are performed on OIP samples at 10 and 50 kHz with pulses of  $T_r = 1.84 \mu\text{s}$ . A significant reduction is seen in lifetimes at 50 kHz. This is potentially due to the nonhomogenous distribution of dielectric losses leading to local hotspots in the insulation which eventually cause thermal breakdown. Increased losses at higher frequencies hence lead to shorter lifetimes. A critical field level  $F_c = 21 \text{ kV/mm}$  is found below which aging is slowed, possibly the transition into the non-PD regime of oil-filled cavities between paper fibers. Future research is aimed at generating a lifeline at 30 kHz and identifies  $F_c$  to understand if its value is an inherent property of the material itself or instead depends on pulse frequency.

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